CSI-2/DSI D-PHY Rx IP

IP Version: 2.1.0

User Guide

FPGA-IPUG-02081-2.5

December 2025

Disclaimers

Lattice makes no warranty, representation, or guarantee regarding the accuracy of information contained in this document or the suitability of its products for any particular purpose. All information herein is provided AS IS, with all faults, and all associated risk is the responsibility entirely of the Buyer. The information provided herein is for informational purposes only and may contain technical inaccuracies or omissions, and may be otherwise rendered inaccurate for many reasons, and Lattice assumes no obligation to update or otherwise correct or revise this information. Products sold by Lattice have been subject to limited testing and it is the Buyer's responsibility to independently determine the suitability of any products and to test and verify the same. LATTICE PRODUCTS AND SERVICES ARE NOT DESIGNED, MANUFACTURED, OR TESTED FOR USE IN LIFE OR SAFETY CRITICAL SYSTEMS, HAZARDOUS ENVIRONMENTS, OR ANY OTHER ENVIRONMENTS REQUIRING FAIL-SAFE PERFORMANCE, INCLUDING ANY APPLICATION IN WHICH THE FAILURE OF THE PRODUCT OR SERVICE COULD LEAD TO DEATH, PERSONAL INJURY, SEVERE PROPERTY DAMAGE OR ENVIRONMENTAL HARM (COLLECTIVELY, "HIGH-RISK USES"). FURTHER, BUYER MUST TAKE PRUDENT STEPS TO PROTECT AGAINST PRODUCT AND SERVICE FAILURES, INCLUDING PROVIDING APPROPRIATE REDUNDANCIES, FAIL-SAFE FEATURES, AND/OR SHUT-DOWN MECHANISMS. LATTICE EXPRESSLY DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY OF FITNESS OF THE PRODUCTS OR SERVICES FOR HIGH-RISK USES. The information provided in this document is proprietary to Lattice Semiconductor, and Lattice reserves the right to make any changes to the information in this document or to any products at any time without notice.

Inclusive Language

This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

Contents

Figures

Tables

Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
ADW	AXI4-Stream Data Width
AXI	Advance eXtensible Interface
CIL	Control and Interface Logic
CRC	Cyclic Redundancy Check
CSI-2	Camera Serial Interface-2
CSR	Control and Status Register
DDRDLL	Double Data Rate Delay-Locked Loop
DPHY	Digital PHY (Physical Layer)
DSI	Display Serial Interface
DW	Data Width
ECC	Error Correction Code
EoTp	End of Transmission Packet
FIFO	First In First Out
FPGA	Field-Programmable Gate Array
GUI	Graphical User Interface
HDL	Hardware Description Language
HS	High-Speed
IDDRX4	Input Double Data Rate Register x4
IP	Intellectual Property
LMMI	Lattice Memory Mapped Interface
LP	Low Power
LSE	Lattice Synthesis Engine
LUT	Look-up Table
MIPI	Mobile Industry Processor Interface
PDC	Physical Design Constraint
PLL	Phase-Locked Loop
RX	Receiver
SoT	Start of Transmission
SoTp	Start-of-Transmission Pattern
TX	Transmitter
ULPS	Ultra Low Power State
UVM	Universal Verification Methodology
VC	Virtual Channel
VCX	Virtual Channel Extension

1. Introduction

1.1. Overview of the IP

The Lattice Semiconductor CSI-2/DSI D-PHY Receiver IP Core converts DSI or CSI-2 data to 8-bit, 16-bit, 32-bit, or 64-bit data for Lattice FPGA devices built on the Lattice Avant™, Nexus™, and Nexus 2 platforms as indicated in the dark gray boxes in Figure 1.1.

The CSI-2/DSI D-PHY Receiver IP Core is intended for use in applications that require a D-PHY receiver in the FPGA logic. D-PHY Rx IP includes in both the high-speed and low power modules. The payload data (image data) uses the high-speed mode whereas the control and status information are sent through low power mode. The number of D-PHY data lanes for data transmission is configurable and supported 1, 2, 3, or 4 data lanes.

The IP design is implemented in Verilog HDL language.

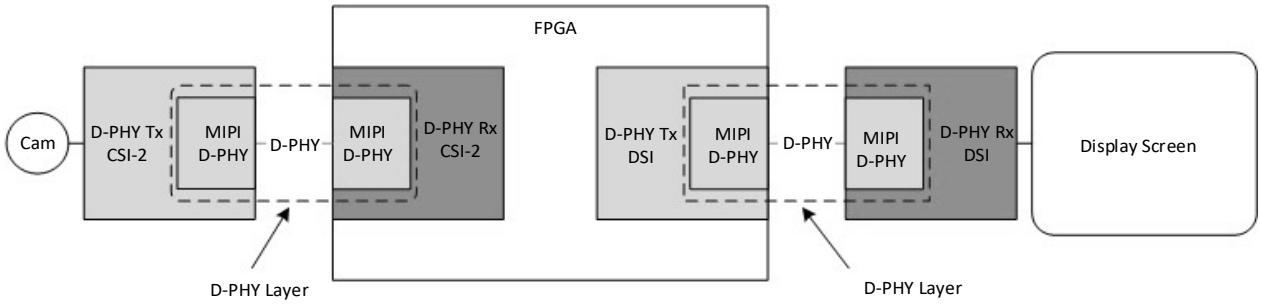

Figure 1.1. D-PHY Rx IP

1.2. Quick Facts

Table 1.1 presents a summary of the CSI-2/DSI D-PHY Rx IP Core.

Table 1.1. CSI-2/DSI D-PHY Rx IP Core Quick Facts

IP Requirements	Supported Devices	CrossLink™-NX, Certus™-NX, CertusPro™-NX, MachXO5™-NX, Lattice Avant, Certus-N2
	IP Changes[1]	Refer to the CSI-2/DSI D-PHY Rx IP Release Notes (FPGA-RN-02040).
Resource Utilization	Supported User Interfaces	LMMI/AXI4-Stream Interface
	Resources	See the Resource Utilization section
Design Tool Support	Lattice Implementation	IP Core v2.1.0 – Lattice Radiant software 2025.2
	Synthesis	Lattice Synthesis Engine (LSE)
		Synopsys® Synplify Pro® for Lattice
	Simulation	Refer to the Lattice Radiant software user guide for the list of supported simulators.

Note:

1. In some instances, the IP may be updated without changes to the user guide. This user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.

1.3. IP Support Summary

The table below shows the IP configurations that are hardware validated. Refer to the Features section for the full list of supported features.

Table 1.2. CSI-2/DSI D-PHY Rx IP Support Readiness

Device Family	Rx Interface Type	Packet Parser	LMMI Interface	D-PHY Clock Mode	Number of RX Lanes	RX Line Rate (Mbps)	Radiant Timing Model	Hardware Validated
Lattice Avant	CSI-2	Enabled	Disabled	Continuous, Non-continuous	1, 4	800, 1000, 1500, 1800	Preliminary	Yes
		Disabled	Disabled	Continuous	2	800	Preliminary	Yes
				Non-Continuous	3	1500	Preliminary	Yes
					4	1200, 1500	Preliminary	Yes
	DSI	Enabled	Disabled	Continuous	1, 4	800, 1200, 1500, 1800	Preliminary	Yes
				Non-Continuous	4	1500, 1800	Preliminary	Yes
		Disabled	Disabled	Continuous	1	1200, 1500	Preliminary	Yes
				Non-Continuous	1	800	Preliminary	Yes
CertusPro-NX	CSI-2	Enabled	Disabled	Continuous, Non-continuous	1, 4	800, 1000, 1500	Final	Yes
				Continuous	2	1400, 1500	Final	Yes
		Disabled	Disabled	Continuous	2	800	Final	Yes
				Non-Continuous	3	1500	Final	Yes
					4	1200, 1500	Final	Yes
	DSI	Enabled	Disabled	Continuous	1, 4	800, 1200, 1500	Final	Yes
					2	900	Final	Yes
				Non-Continuous	4	1500	Final	Yes
		Disabled	Disabled	Non-Continuous	1	800	Final	Yes
			Disabled	Continuous	1	1200, 1500	Final	Yes
CrossLink-NX	CSI-2	Enabled	Disabled	Continuous	1	800[3], 1500[2,3]	Final	Yes
					2	2400[1], 2500[1,2]	Final	Yes
					4	1500[3, 4]	Final	Yes
		Disabled	Disabled	Continuous	2	1500[3]	Final	Yes
				Non-Continuous	4	2500[2]	Final	Yes
	DSI	Enabled	Disabled	Continuous	4	2400[1], 1500[4,]	Final	Yes
				Non-Continuous	1	1500[3]	Final	Yes
		Disabled	Disabled	Continuous	2	2500[2]	Final	Yes
				Non-Continuous	1	2500[1], 1500[3]	Final	Yes

Notes:

1. This covers only the hard D-PHY with *CIL Bypass == checked* and *Rx Gear == 16.*
2. This covers only the hard D-PHY with *CIL Bypass == unchecked* and *Rx Gear == 16.*
3. This covers only the hard D-PHY with *CIL Bypass == checked* and *Rx Gear == 8.*
4. This covers only the hard D-PHY with *CIL Bypass == unchecked* and *Rx Gear == 8.*

1.4. Features

- Compliant with MIPI D-PHY v1.2, MIPI DSI v1.1, and MIPI CSI-2 v1.2 specifications.
- Selection between Hard Rx D-PHY or Soft Rx D-PHY implementation. Hard Rx D-PHY is only available for CrossLink-NX devices.

- Supports MIPI DSI and MIPI CSI-2 interfaces up to 6 Gb/s for Soft D-PHY and up to 10 Gb/s for Hard D-PHY.
- Supports 1, 2, 3, or 4 data lanes and one clock lane.
- Supports continuous and non-continuous MIPI D-PHY clock.
- Supports all MIPI DSI Video Mode of operations.
  - Non-Burst Mode with Sync Pulses
  - Non-Burst Mode with Sync Events
  - Burst Mode
- Optional packet parsing or parallel data translation only.
- Supports optional periodic deskew detection.
- Supports all MIPI DSI compatible video formats.
- Supports all MIPI CSI-2 compatible video formats.

1.4.1. Hard CSI-2/DSI D-PHY Rx IP Core Features

- Maximum rate is up to 2500 Mbps per lane.
- Supports 8x or 16x gearing.
- Option to use internal or external clock source.
- Option to use hardened Control and Interface Logic (CIL) or Fabric Logic.
- Supports dynamic lane and rate reconfiguration during run time. Refer to the Dynamic Reconfiguration section for details.
- Hard D-PHY is supported only on CrossLink-NX devices.

1.4.2. Soft CSI-2/DSI D-PHY Rx IP Core Features

- Maximum rate of up to 1500 Mbps per lane for CrossLink-NX, Certus-NX, and CertusPro-NX devices.
- Maximum rate of up to 1800 Mbps per lane for Lattice Avant devices.
- For Lattice Avant devices, dynamic clock-to-data calibration is automatically enabled for rate ≥ 1000 Mbps per lane.
- Supports 8x gearing only.
- External clock source.
- Supports dynamic lane and rate reconfiguration during run time. Refer to the Dynamic Reconfiguration section for details.

1.5. Licensing and Ordering Information

The CSI-2/DSI D-PHY Receiver IP Core is provided at no additional cost with the Lattice Radiant software.

1.6. Hardware Support

Refer to the Example Design section for more information on the boards used.

1.7. Minimum Device Requirements

Refer to the Resource Utilization section for the minimum required resource to instantiate this IP.

1.8. Naming Conventions

1.8.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.8.2. Signal Names

- *_n* are active low (asserted when value is logic 0)
- *_i* are input signals

- _*o* are output signals
- _*io* are bidirectional signals

2. Functional Description

2.1. IP Architecture Overview

Figure 2.1 and Figure 2.2 show the architecture blocks and data flow in the CSI-2/DSI D-PHY Receiver IP.

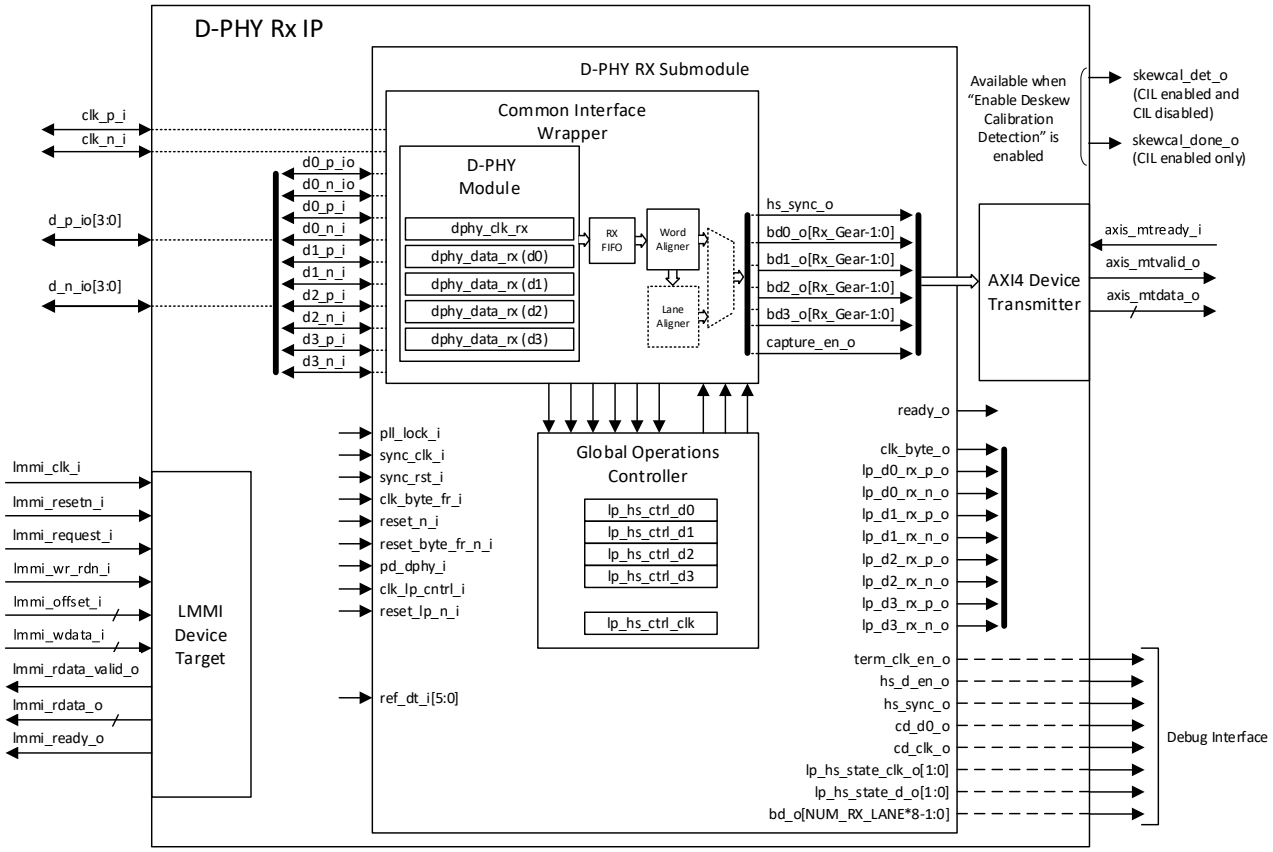

Figure 2.1. D-PHY Rx IP Block Diagram with AXI4-Stream Enabled, LMMI Enabled, and Packet Parser OFF

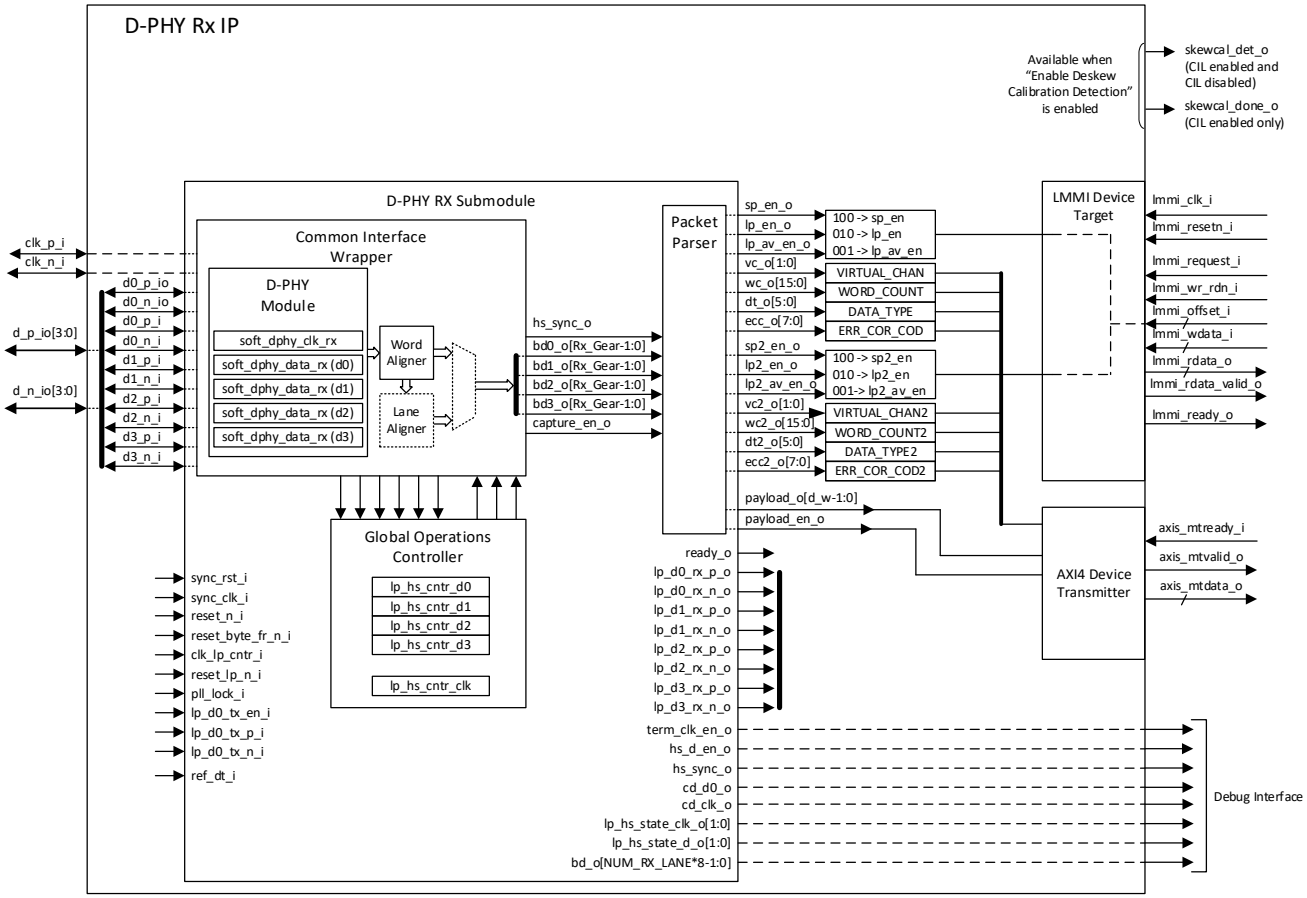

Figure 2.2. D-PHY Rx IP Block Diagram with AXI4-Stream Enabled, and LMMI Disabled

The CSI-2/DSI D-PHY Receiver IP includes the following layers:

- Common Interface Wrapper
- Global Operations Controller
- Packet Parser (optional)
- AXI4 Device Transmitter (optional)
- LMMI Device Target (optional)

The D-PHY Rx IP block diagram configured with the AXI4-Stream OFF and the Packet Parser OFF is shown in Figure 2.11.

The D-PHY Rx IP block diagram configured with the AXI4-Stream ON and the Packet Parser OFF is shown in Figure 2.12.

The D-PHY Rx IP block diagram configured with the AXI4-Stream OFF and the Packet Parser ON is shown in Figure 2.14.

The D-PHY Rx IP block diagram configured with the AXI4-Stream ON and the Packet Parser ON is shown in Figure 2.15.

2.2. Clocking

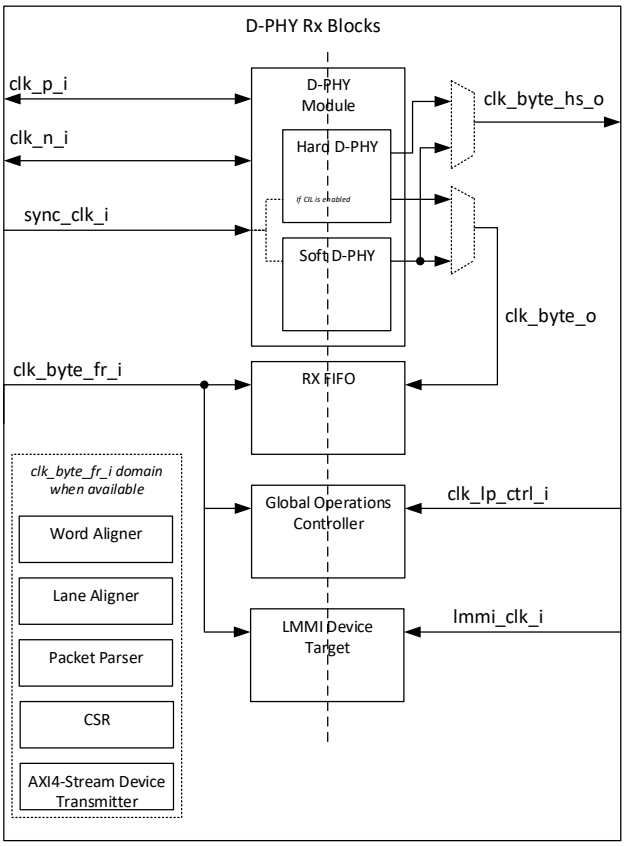

Figure 2.3. Clock Domain and Clocking Overview

The blocks and clocks are available based on the selected configuration. Refer to Table 4.2 for more details about these clock signals.

2.3. User Interfaces

Table 2.1 lists the available user interface and protocols used on the CSI-2/DSI D-PHY Receiver IP.

Table 2.1. User Interfaces and Supported Protocols

User Interface	Supported Protocols	Description
Control	LMMI	Configures the control registers of the D-PHY Rx IP.
Device Transmitter	AXI4-Stream	Transmits the payload data (byte data or packet data with virtual channel, data type, and word count).

2.3.1. LMMI Device Target Interface

The LMMI Device Target module (Lattice Memory Mapped Interface) is used for configuring the control registers of the D-PHY Rx IP.

For more information on LMMI, refer to Lattice Memory Mapped Interface and Lattice Interrupt Interface User Guide (FPGA-UG-02039).

2.3.2. AXI4-Stream Device Transmitter Interface

AXI4-Stream Device Transmitter provides an interface for transmitting payload data (byte data or packet data with virtual channel, data type, and word count). Figure 2.4 shows data format when AXI4-Stream is enabled.

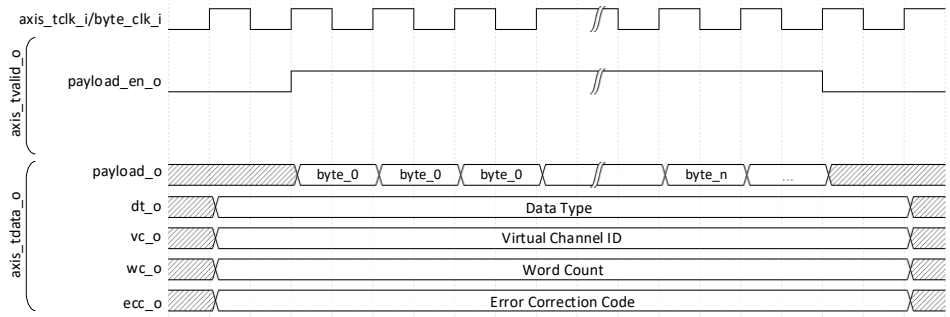

Figure 2.4. AXI4-Stream is ON and Packet Parser is ON Data Format (Active Payload)

If the AXI4-Stream device is not enabled and the D-PHY Rx IP is configured with Packet Parser (see Figure 2.14 and Figure 2.15), the following internal signals turn to top-level input signals as shown in Figure 2.16:

- payload_en_o
- payload_o[*Number of RX Lanes* × *RX Gear* -1:0]
- dt_o[5:0]
- vc_o[1:0]
- wc_o[15:0]
- ecc_o[5:0]
- vcx_o[1:0]
- dt2_o[5:0]
- vc2_o[1:0]
- wc2_o[15:0]
- ecc2_o[5:0]

If the AXI4-Stream device is not enabled and the D-PHY Rx IP is configured without Packet Parser (see Figure 2.12 and Figure 2.13), the following internal signals turn to top-level input signals:

- capture_en_o
- bd0_o[*RX Gear* -1:0]
- bd1_o[*RX Gear* -1:0]
- bd2_o[*RX Gear* -1:0]
- bd3_o[*RX Gear* -1:0]

2.4. D-PHY Rx Common Interface Wrapper

The Common Interface Wrapper module instantiates either the hard or the soft D-PHY module to receive MIPI D-PHY data from all enabled data lanes.

When soft D-PHY is used, this module also includes the Word Aligner module and optionally a Lane Aligner to ensure the correct alignment of bytes among the D-PHY data lanes. See the Word Aligner and Optional Lane Aligner section for more details regarding these modules.

2.5. D-PHY Module

The D-PHY module instantiates either the hardened D-PHY module or a soft logic equivalent using the FPGA fabric and generic blocks.

2.5.1. Hard D-PHY

Hardened D-PHYs are available in CrossLink-NX devices. Each of these hard blocks contains a Control Interface Logic (CIL) that detects the lane transitions.

The skew calibration detection feature is available for Hard D-PHY configuration. The skew_cal_det_o asserts if it detects the all 1's sync pattern and clears when DP/DN lines are back to LP11 state. An additional signal skew_cal_done_o is available when CIL is enabled. You can optionally enable this feature for data rates of 1.5 Gbps and below.

The hardened PHY module divides the high-speed D-PHY clock to create the output byte clocks clk_byte_o and clk_byte_hs_o. The clk_byte_hs_o toggles when the D-PHY clock lane is active, and can be used as the input clock clk_byte_fr_i when the source D-PHY clock is continuously running. The clk_byte_o, is active only after the deserializer within the hard PHY block detects the Start-of-Transmission pattern (SoTp) and stops when the data lanes go out of high-speed mode. This clock is used as strobe to latch the parallel byte data from the hardened D-PHY block. Because of the dependence on the SoTp detection, the clk_byte_o is out of phase with the clk_byte_hs_o.

The hardened D-PHY also makes use of the input sync_clk_i to clock various control logic. The hardened D-PHY requires a certain period between high-speed transactions to be able to properly handle the internal signals crossing these clock domains. This period is described by the following equations:

For continuous clock mode:

$$T_{HS-EXIT} + T_{LPX} \geq 8T_{clk\_byte} + 3T_{sync\_clk}$$

For non-continuous clock mode:

$$T_{CLK-POST} + T_{LPX} \geq 8T_{clk\_byte} + 3T_{sync\_clk}$$

Where $T_{CLK-POST}$ is at least six byte clock cycles.

2.5.2. Soft D-PHY

When the soft PHY is used, the clk_byte_o is the same as the clk_byte_hs_o. Both are the outputs of a clock divider with the D-PHY clock as its input. Refer to the High-Speed I/O Interface document of each device for the Soft MIPI D-PHY architecture implementation details.

For Lattice Avant devices, dynamic clock-to-data calibration of soft D-PHY is automatically performed for *RX Line Rate per Lane ≥ 1,000 Mbps*. During this time, the IP uses the incoming short and long high-speed packets to perform internal clock-to-data alignment. Because of the dynamic nature of the calibration, lock is achieved after a few video frames. The IP guarantees valid output data only after the edgemon_done_o signal is asserted when calibration is enabled. All output data of the IP can be ignored prior to edgemon_done_o assertion.

2.6. RX_FIFO

As mentioned in the D-PHY Module section, the data words from the D-PHY module are synchronous with the output clock clk_byte_hs_o. The rest of the data path, including the soft aligner modules, are clocked by the input clk_byte_fr_i. An rx_fifo module is used to cross the data between these two clock domains. When the hardened Control Interface Logic (CIL) is enabled, the RX_FIFO Module is not used. Instead, a single 1024-deep dual-clock FIFO is used.

In the case of the soft PHY implementation, the RX_FIFO is instantiated before the D-PHY module and the Word Aligner module. Data being buffered includes the hs-zero bytes before the SoTp, the actual packets, the trail bits, and the data lane value right before the D-PHY lanes transition to LP-11.

The following subsections describe the various implementation types.

2.6.1. RX_FIFO OFF

If the clk_byte_fr_i has the same frequency and is synchronous with the clock strobe clk_byte_o, the RX_FIFO can be removed. In the actual generated design, there is still a fixed 4-deep single clock FIFO implemented as LUTs.

This setting is recommended when the D-PHY module is using Soft D-PHY implementation with the D-PHY clock running continuously in high-speed mode and the clk_byte_fr_i is driven by the clk_byte_hs_o.

2.6.2. RX_FIFO_TYPE = SINGLE

The RX_FIFO Single type is primarily intended as an elastic FIFO to buffer the frequency or phase difference between the stoppable byte clock domain (clk_byte_o) and the continuous byte clock domain (clk_byte_fr_i).

The MIPI D-PHY protocol does not allow data throttling when high-speed transfer is already on-going. Full or empty FIFO condition does not halt the data stream. Configure the depth of the FIFO and the packet delay to ensure it does not overflow or underflow.

When the two byte clocks have slightly different frequency (such as using two different oscillators with ppm tolerance), it is recommended to increase the buffered data before reading out from the FIFO using the packet delay parameter. If the continuous clock is slightly slower than the strobe clk_byte_o and the low power period between high-speed transfers is enough to absorb the time difference, the delay value can be set to 1; the depth depends on the amount of possible accumulated data because of the clock difference.

If the two byteclocks are asynchronous with each other, set Clock Mode to DC.

When the frequency of both clocks are exactly the same but are out-of-phase, when the input clock clk_byte_fr_i is driven by the clk_byte_hs_o from the Hard D-PHY module in continuous clock mode, set the delay value to 1 and depth to 16, which is the minimum depth for the FIFO control signals crossing clock boundaries.

In all cases of the Single Type RX_FIFO, the read from the FIFO continues until the empty flag asserts. The interval between high-speed transactions (low power blanking) must be long enough to ensure the FIFO is already empty before the next one is written, otherwise, the FIFO assumes it is still part of the previous data stream. This causes the word aligner to miss the SoTp of the second data stream and interpret the packets erroneously.

Figure 2.5 illustrates the contents of the FIFO when a high-speed blanking DSI stream is being buffered using the RX_FIFO SINGLE.

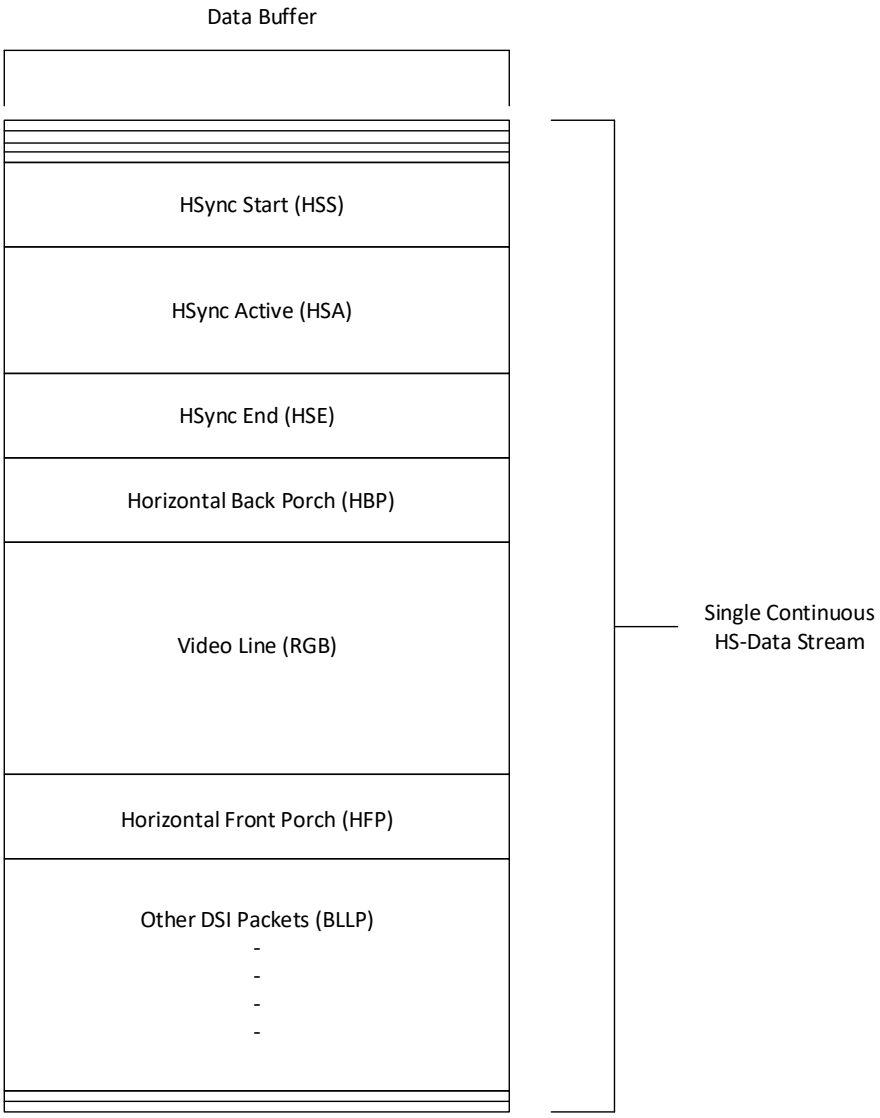

Figure 2.5. RX_FIFO SINGLE

2.6.3. RX_FIFO_TYPE = PINGPONG

This FIFO instantiates two dual_clock FIFOs that alternately stores data of every high-speed transaction. Each data buffer can hold the largest data within a high-speed transaction, including the hs-zero, SoTp, and trail bits.

Similar with the single type, this implementation also has a parameterized delay before reading out from the buffer to maintain intervals between packets. If packet delay = 0, read starts once the empty signal deasserts and the other one is not busy with read. If packet delay is non-zero, read from that buffer starts once the delay value is met and the other one is not busy with read. This implementation does not track the number of entries within the buffers; read stops once the empty flag asserts. Each buffer is reset after the read operation.

This type is more suitable for high-speed transfers with short intervals because data is written alternately between the two buffers. This is recommended for DSI with low power blanking.

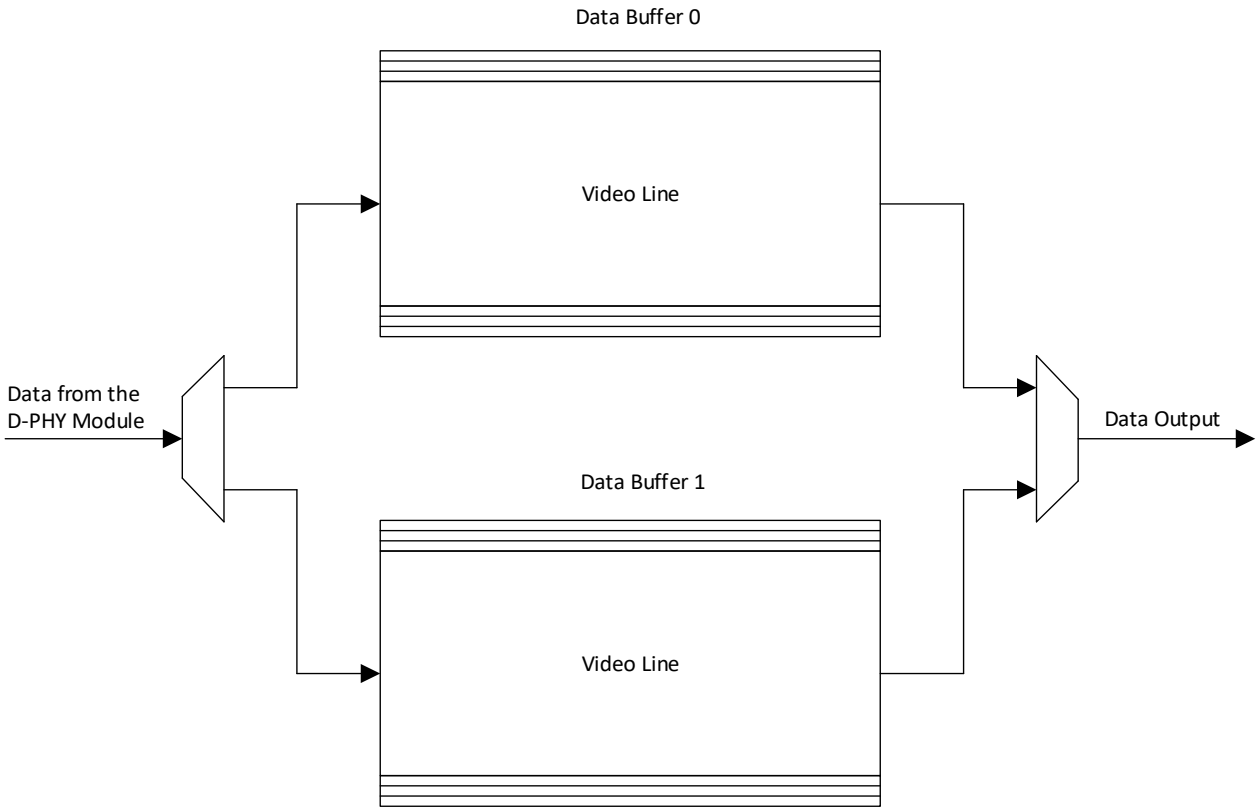

Figure 2.6. RX_FIFO PINGPONG

2.6.4. RX_FIFO_TYPE = Queue

This FIFO instantiates one dual-clock FIFO. This FIFO also acts as a circular buffer that holds data from multiple high-speed transactions.

Unlike the other two types, this FIFO does not have a delay counter. Instead, HS data is buffered completely and a counter tracks the number of rows written during the high-speed transaction. This count is stored in an entry queue.

When there is a valid entry in the entry queue, read from the data buffer is triggered. The number of read cycles from the data buffer corresponds to the entry read from the entry queue. This enables the FIFO controller to distinguish the boundaries between successive HS transactions. This setting introduces significant latency on the first video line, but also enables the IP to support short intervals between HS transactions.

This implementation is suitable for CSI-2, where the packet intervals are not critical, but the intervals between successive high-speed transactions are short.

Figure 2.7 illustrates a sample entry within a 4-deep entry queue for a CSI-2 sequence.

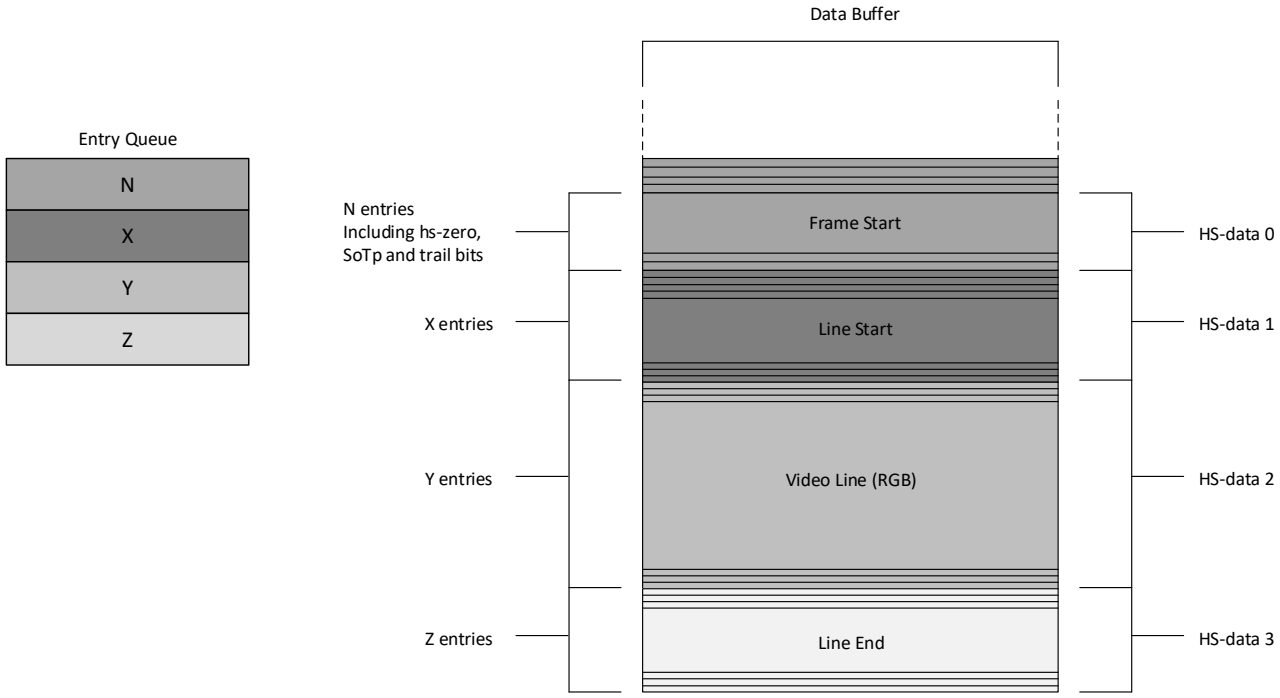

Figure 2.7. RX_FIFO QUEUE

2.7. Global Operations Controller

This block detects the low power state transitions of the clock and data lanes. This controller also controls the resistor termination when switching between low power and high-speed states. The Global Operations Controller only supports low power to high-speed sequence (LP-11 -> LP-01 -> LP-00 -> HS0 -> HS0/1 -> LP11). Figure 2.8 shows the LP-to-HS transition flow diagram for data lanes.

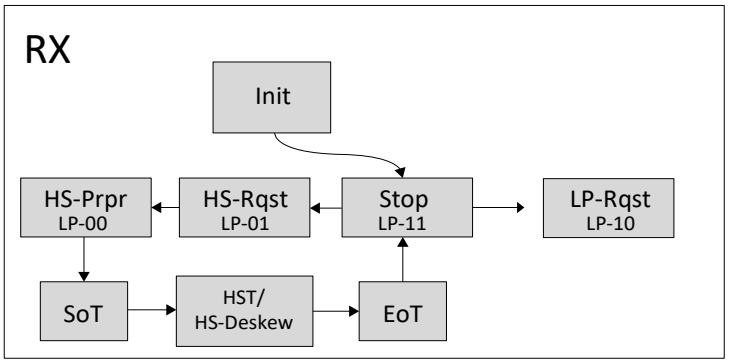

Figure 2.8. MIPI D-PHY Rx LP to HS Transition Flow Diagram on Data Lanes

When the MIPI D-PHY clock is continuous, the HS termination enable of clock lane is tied to VCC. When the MIPI D-PHY clock is non-continuous, the HS termination enable of clock lane becomes active right after proper LP to HS transition is observed. This function requires a reference clock input. Figure 2.9 shows the required LP to HS transition on clock lane per MIPI D-PHY Specification version 2.1.

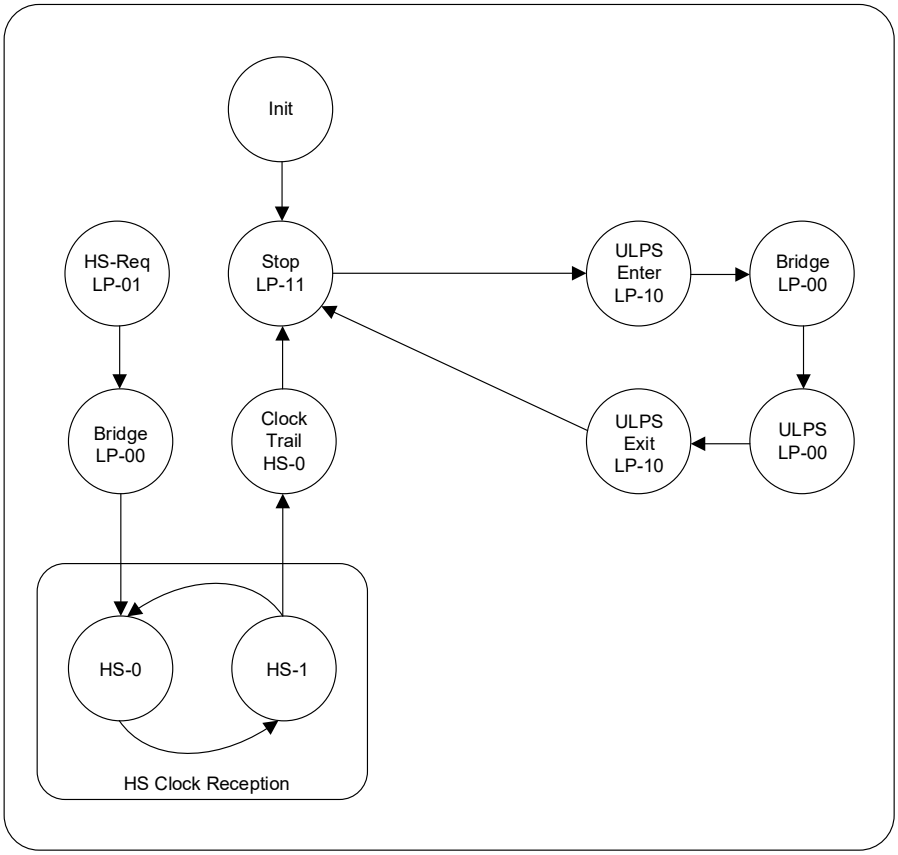

Figure 2.9. MIPI D-PHY Rx LP to HS transition on Clock Lane

During normal operation, a data lane is either in control or in high-speed (HS) mode.

In low power (control) mode, the D-PHY transmitter performs the high-speed entry sequence which consists of driving LP11 -> LP01 -> LP00 on the data lanes as shown in Figure 2.10. Upon successful detection of this sequence, the Global Operations Controller enables the differential resistor termination to receive the high-speed data. A free-running byte clock is used during HS mode.

Once enabled, HS receiver termination continues to receive the data until it encounters the LP11 state on the lanes, which is also known as the Stop State. The Stop State brings back the data lane from high-speed mode to low power mode.

To handle the transition effects in the data lanes when going from low power to high-speed mode, the D-PHY protocol requires the receiver to neglect the data lanes for a certain time interval, tHS_SETTLE. In the IP, you can set this time interval through the Data Settle Cycle attribute in the GUI. If LMMI interface is available, you can configure this interval by writing to the NOCIL_DSETTLE register. Alternatively, if LMMI is disabled but the Configurable Data Settle Count is checked, an input port rxcsr_datsettlecyc_i is available for the same function.

For Hard D-PHY with CIL bypassed, the counter for the data settle, and the FSM that detects the low power to high-speed transition of the data lanes, are in the clk_byte_fr_i domain.

For Soft D-PHY, the FSM is also in the clk_byte_fr_i domain, but the tHS_SETTLE timer is in the clk_byte_o domain.

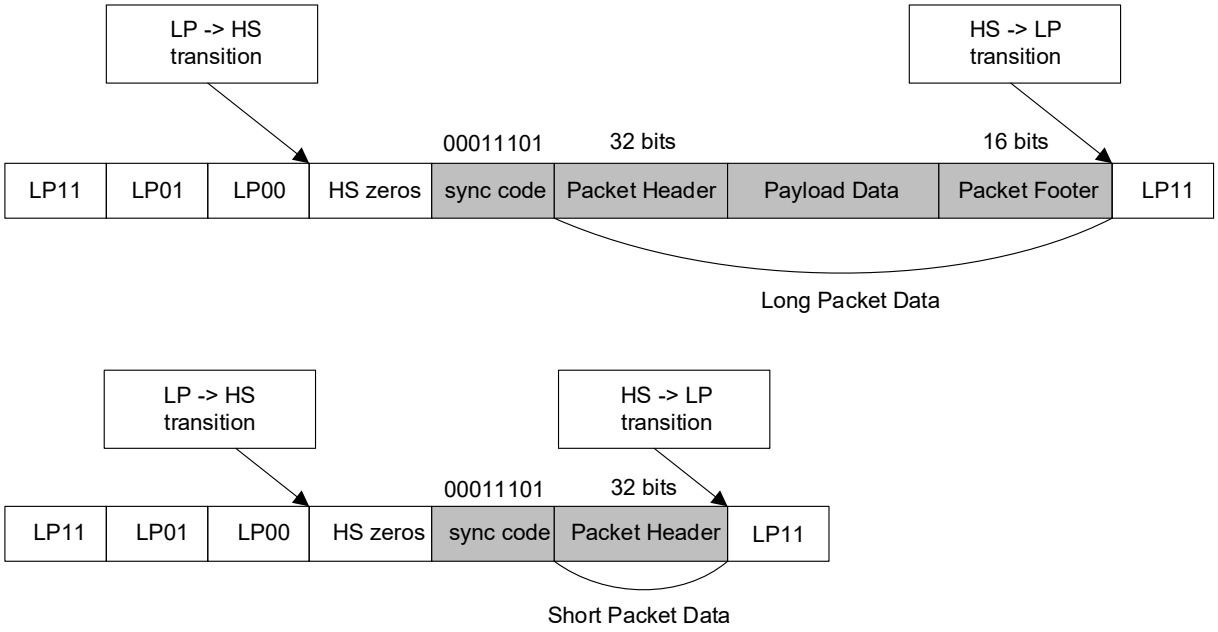

Figure 2.10. High-Speed Entry Sequence and Payload Data Transmission Cycle on Data Lanes

2.8. D-PHY Rx IP without Packet Parser

When D-PHY Rx IP is configured without the packet parser, as shown in Figure 2.11 and Figure 2.12, the output is the received bytes from the D-PHY Rx IP starting from the reception of the Start of Transmit (SoT) code in all the active data lanes until the detection of LP-11, signifying the end of high-speed transmission. The interfacing logic obtains and decodes the valid data packets from the trail. This configuration is useful for bridging D-PHY packets without going to the protocol level.

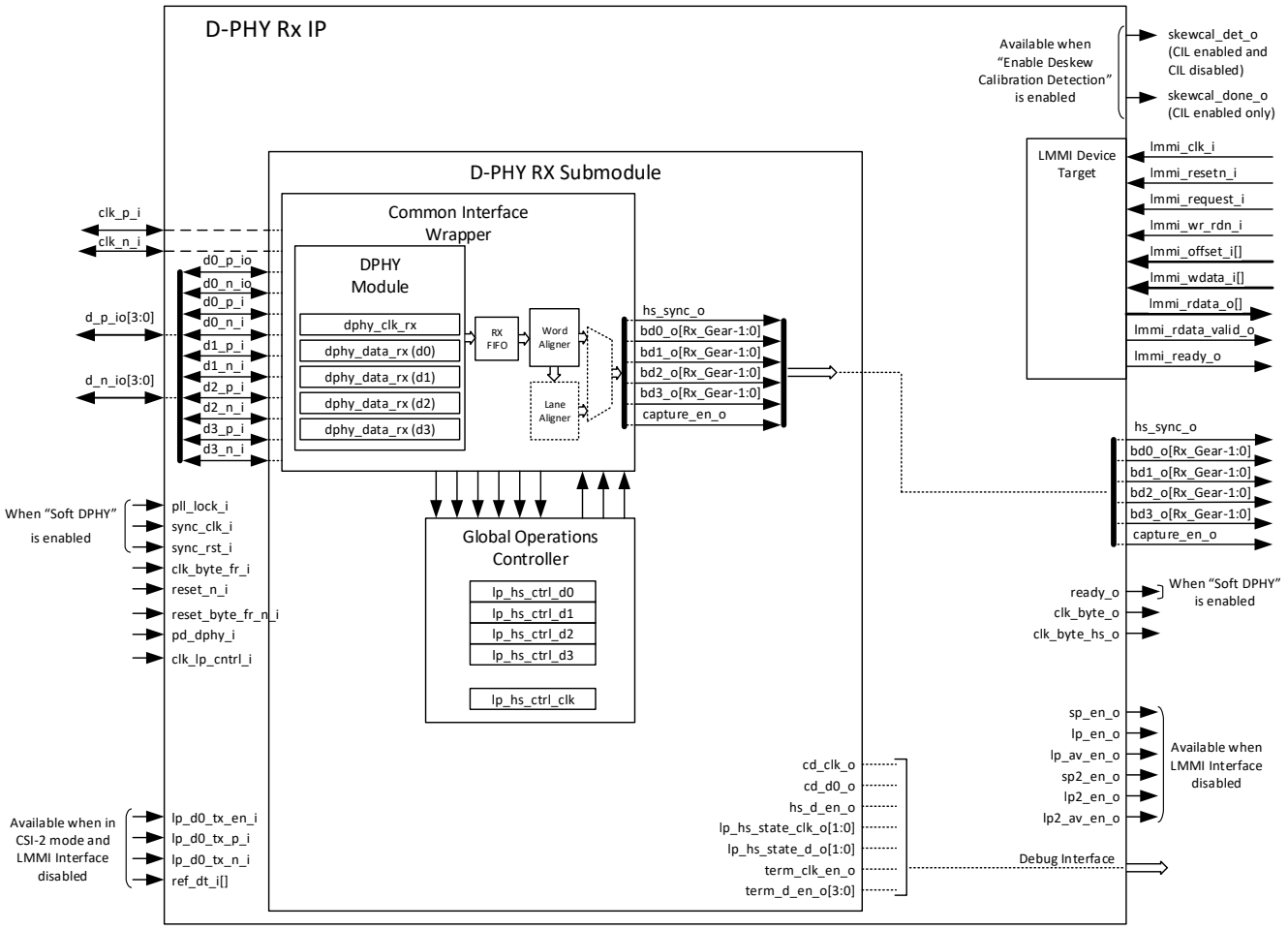

Figure 2.11. D-PHY Rx IP Configuration with AXI4-Stream Disabled and Packet Parser Disabled

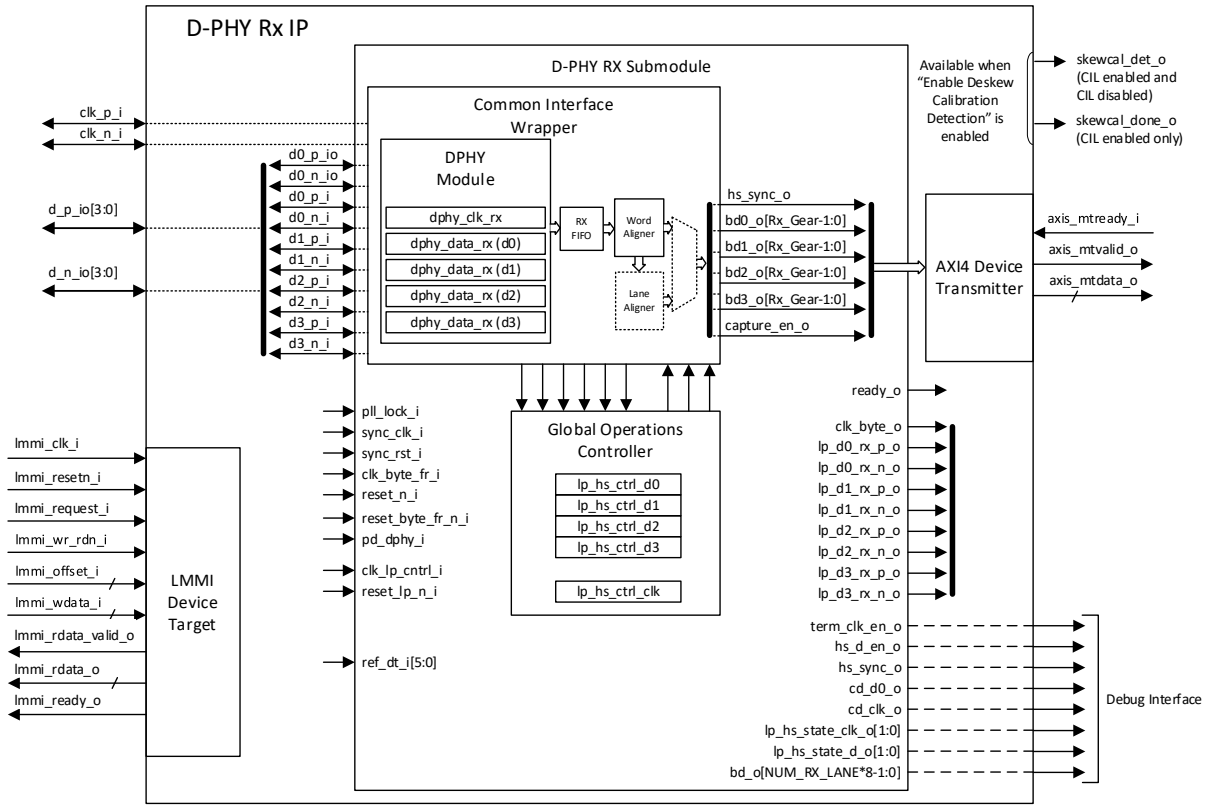

Figure 2.12. D-PHY Rx IP Configuration with AXI4-Stream Enabled and Packet Parser Disabled

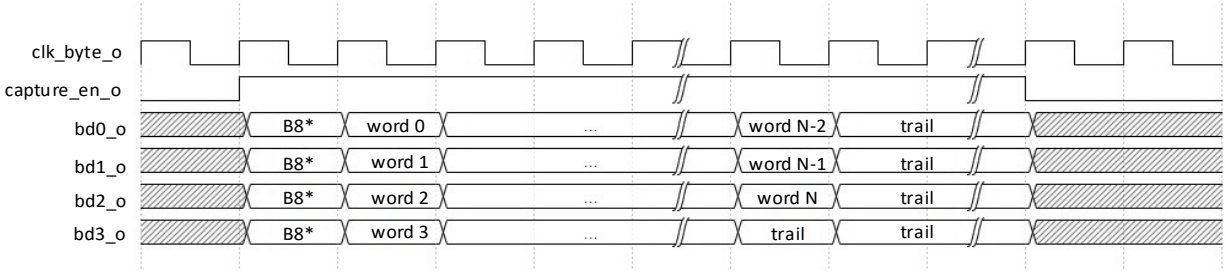

Figure 2.13. D-PHY Rx IP Output Timing Diagram without Packet Parser

2.9. D-PHY Rx IP with Packet Parser

When D-PHY Rx IP is configured with the DSI/CSI-2 packet parser included, as shown in Figure 2.14 and Figure 2.15, the parser checks the incoming data for a valid data type and the corresponding packet fields.

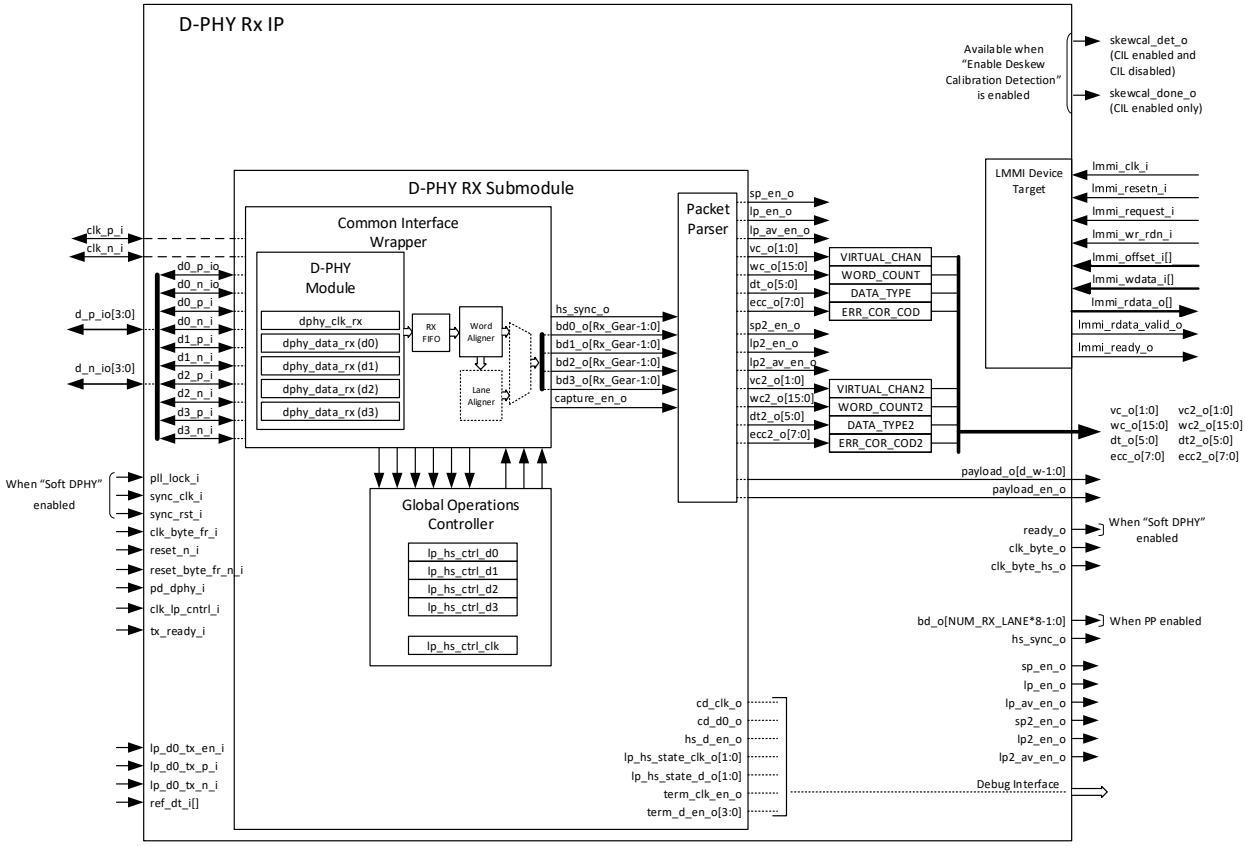

Figure 2.14. D-PHY Rx IP Configuration with AXI4-Stream Disabled and Packet Parser Enabled

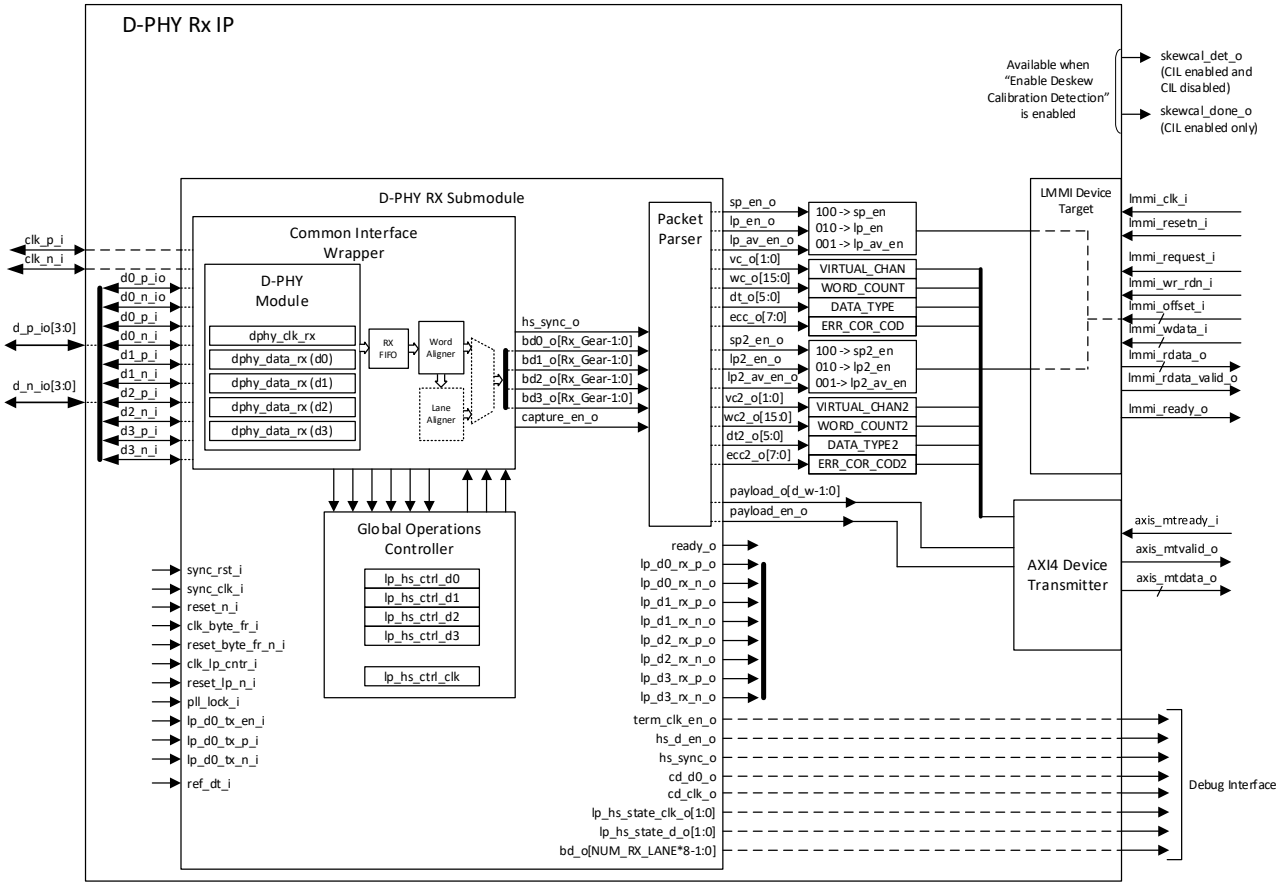

Figure 2.15. D-PHY Rx IP Configuration with AXI4-Stream Enabled and Packet Parser Enabled

2.10. Packet Parser

The Packet Parser module parses the data bytes from D-PHY Common Interface Wrapper, and detects short and long packets defined by MIPI DSI or MIPI CSI-2. This block extracts video data and other control parameters from the packets. There are no signals from the external logic to this block to control the flow of output data. The interfacing logic must provide ample buffering to ensure the continuous flow of data from this submodule is transferred correctly. The output-timing diagram of D-PHY Rx IP interface with the packet parser enabled is shown in Figure 2.16.

The lp_en_o or sp_en_o signal asserts when a valid data type is received. These signals also indicate the valid data type, virtual channel ID, wordcount, and ECC fields. The lp_av_en_o only asserts with the lp_en_o, if the long packet received is the same as the input reference data type ref_dt_i. This is to differentiate active video packets from other long packets, such as null or blanking. Consequently, this signal does not assert on any video data type other than the defined ref_dt_i value. The payload_en_o signal indicates that the data in the payload_o bus contain the valid payload bytes. The width of the payload, data_width, is the number of gear bits multiplied by the number of data lanes. Upper data bytes for the last payload data must be ignored if the wordcount is not a multiple of data_width/8. The interfacing module extracts the correct payload bytes based on the valid output wordcount wc_o.

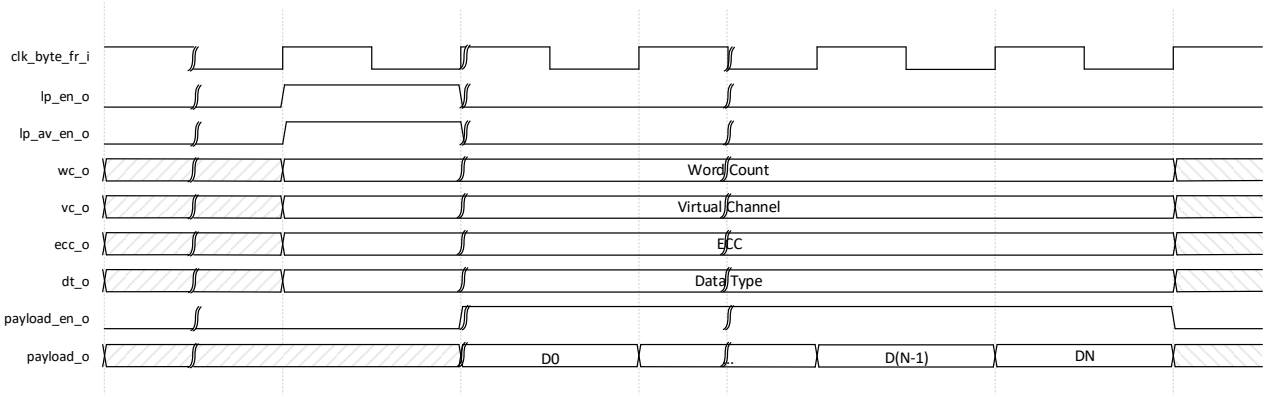

Figure 2.16. D-PHY Rx IP Output Timing Diagram with Packet Parser

Example timing diagram for a consecutive short and long packet transactions is shown in Figure 2.17.

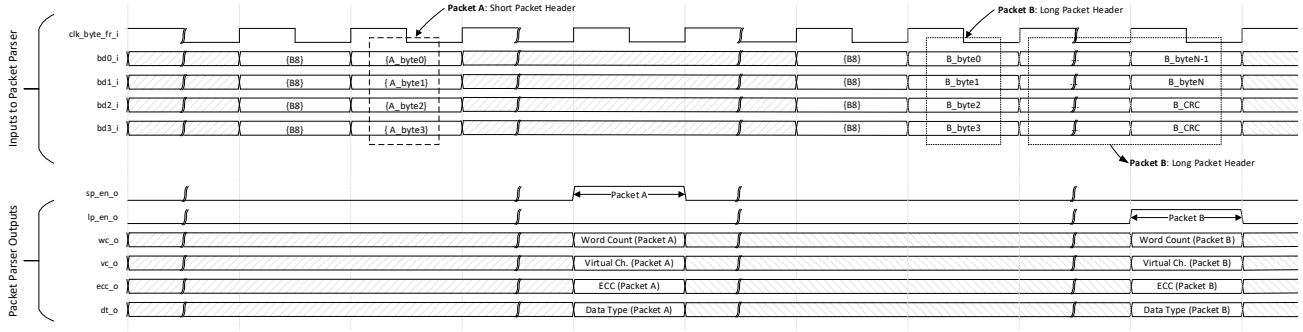

Figure 2.17. Output Timing Diagram of a RX Gear == 8 Configuration

When the input data bus going to the packet parser is greater than 32, the Second Set of Packet is valid. In this configuration, two packet headers may simultaneously be decoded within the same byte clock cycle.

The packet parser input and output timing diagram with valid Second Set of Packet information is shown in Figure 2.18.

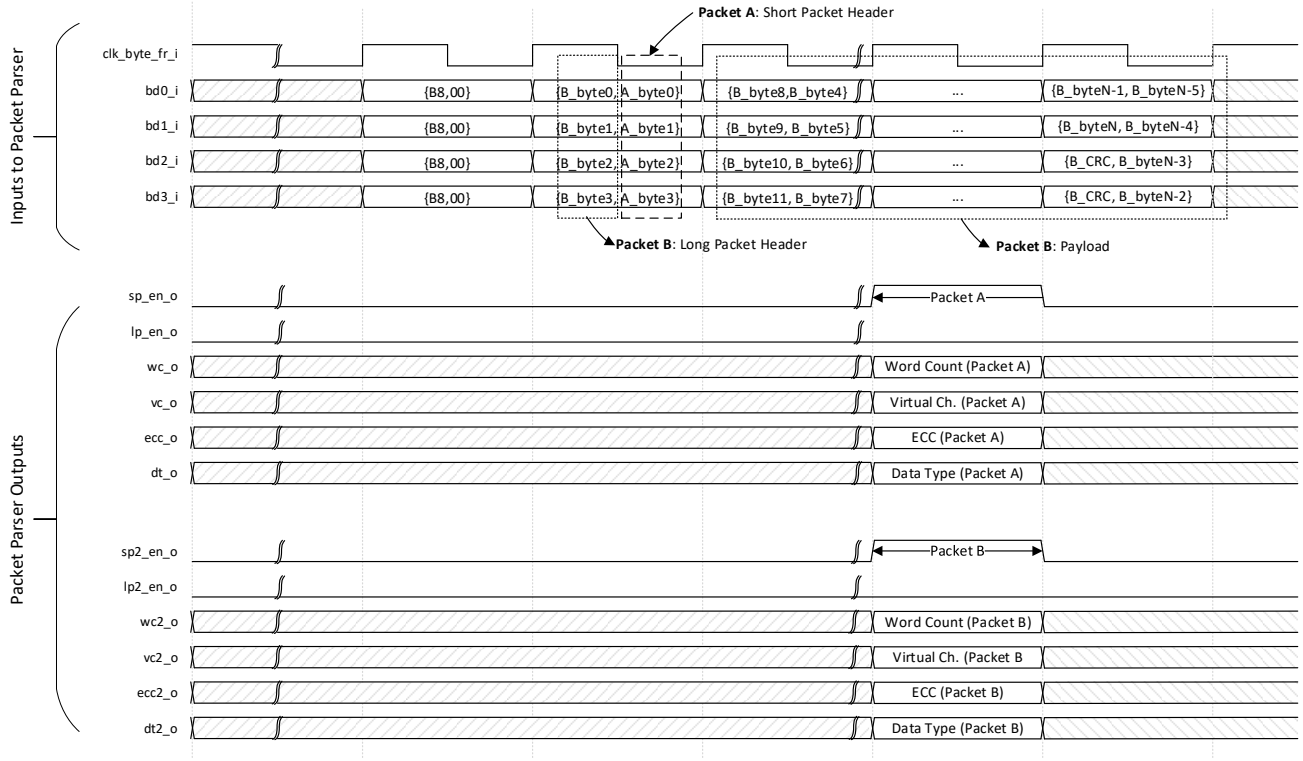

Figure 2.18. Output Timing Diagram with Valid Second Set of Packet Information

2.11. Word Aligner and Optional Lane Aligner

Before the payload data of every HS burst on each lane, the transmitting D-PHY inserts a sync sequence Start-of-Transmit (SoT) pattern. For hardened PHY, the hard deserializer checks for the sync pattern on each lane. For soft PHY, a Word Aligner module detects the pattern in the deserialized data and establishes the correct byte boundary on the high-speed payload data.

The Word Aligner logic detects the SoT pattern from each lane and ensures the parallel data are word (byte) aligned. The design assumes that input data lanes are driven at the same time, and skew between data lanes are less than 1 UI. However, because of deserialization, data buffering, and handling of clock domain crossing signals, the detection of the aligned data from all the lanes may not happen at the same cycle. An optional lane aligner module may be instantiated to rectify this issue, see Figure 2.19.

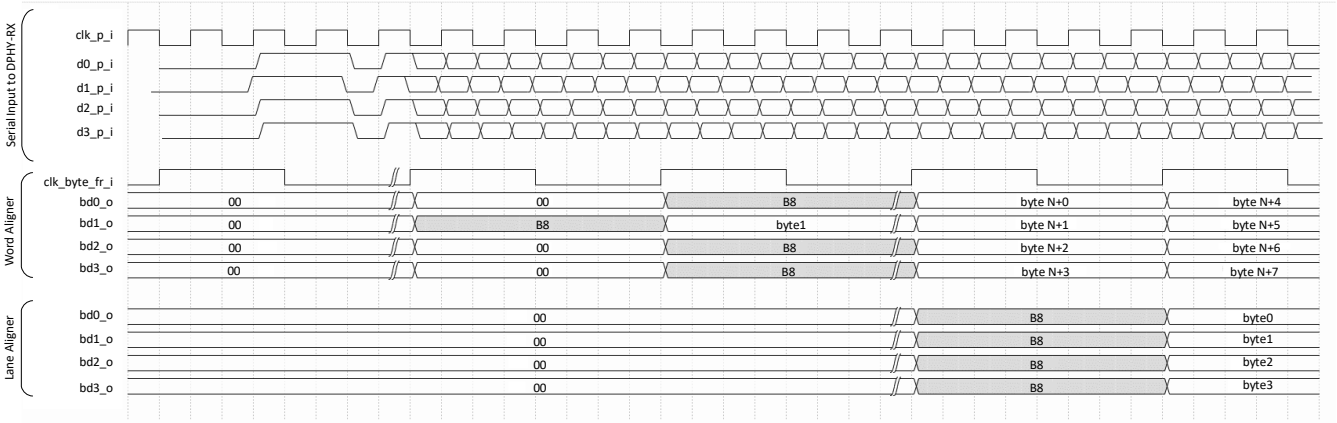

Figure 2.19. Lane Data Alignment

2.12. Dynamic Reconfiguration

Starting from IP v1.6.0, the IP can be reconfigured during run time to support dynamic lane and rate reconfiguration for the modes in the table below.

Table 2.2. D-PHY Rx Settings that Support Dynamic Reconfiguration

IP Version[1]	Family	D-PHY RX IP	CIL Bypass	Enable Packet Parser
IP v1.6.0	Nexus	Hard D-PHY	unchecked	checked
IP v2.0.0	Nexus	Hard D-PHY	unchecked	unchecked
	Nexus	Soft D-PHY	—	unchecked, checked
IP v2.1.0[2]	Avant	Soft D-PHY	—	unchecked, checked

Notes:

1. All features available in previous versions of the IP remain fully supported in newer versions unless otherwise specified in the IP Release Notes. Each row highlights only the additional dynamic reconfiguration features introduced in each release.
2. For Avant, only dynamic lane reconfiguration is supported in IP v2.1.0.

To enable these functions, configure the IP based on the supported IP attributes in Table 2.2. Check the additional IP attributes in the Module/IP Block Wizard in the Lattice Radiant software as follows:

- *Enable LMMI Interface* is checked. This is required as registers are accessible only through LMMI.
- Set the parameters of *RX Line Rate, Number of RX Lanes*, and *RX Gear* to the maximum desired value at compile time to enable dynamic reconfiguration of all possible combinations.
- To enable CRC checking function for the dynamically configured lane and gear, check the following attributes:
  - Enable Packet Parser is checked.
  - Enable CRC Check is checked.
  - *CRC Check Mode* == *Dynamic*. Setting the *CRC Check Mode* attribute to Static with *Enable CRC Check* == checked causes the CRC checking function to operate only based on compile-time IP configuration.
- For soft D-PHY in Nexus devices, if you plan to change the data rate, it is recommended to begin with the default static delay settings first by unchecking the *Enable Dynamic Delay Control* attribute. This approach simplifies the design and may be sufficient for stable operation. In the case that the pre-defined static delay does not work for the new data rates, and issues such as corrupted data or missing Start of Transmission Pattern (SoTp) are observed, you can enable the *Enable Dynamic Delay Control* attribute. This activates additional IP ports that allow dynamic adjustment of both coarse and fine delay settings in the soft IP. Refer to Table 3.3 for details.

To reconfigure the dynamic registers, follow these steps:

1. Stop the D-PHY Transmitter from sending packets.
2. Configure the IP registers.

- Write to register 0x27[5:0] to update the reference data type.
- For Hard D-PHY with hard CIL enabled:
  - Write to register 0x09[2:1] to change between Gear 8 and Gear 16.
  - Write to register 0x0A[2:1] to change the number of active lanes.
  - If you plan to change the data rate, update the following timing parameters registers to adjust the protocol timing parameters:
    - Write to register 0x0A[3], 0x0B[3:0], and 0x0C[0] to change the tCLK-SETTLE counter value.
    - Write to register 0x0F and 0x10 to change the tHS-SETTLE counter value.
  - If you plan to change the data rate to ≤ 1.5 Gbps and the compile time IP configuration selected is >1.5 Gbps, write 0x2 to register 0x1B and 0x8 to register 0x1D.
- For Soft D-PHY:
  - Write to register 0x0A[2:1] to change the number of active lanes.
  - If you plan to change the data rate, update the following timing parameters registers to adjust the protocol timing parameters:
    - Write to register 0x36[7:0] to change the tHS-SETTLE counter value.

3. Configure the D-PHY Transmitter.

4. Assert all the resets and clock control ports of the IP (whichever are available in the selected configuration) except the LMMI reset:

- reset_byte_fr_n_i
- reset_n_i
- pd_dphy_i
- sync_rst_i
- pll_lock_i

Note: After resetting the D-PHY Receiver IP—especially when the IP has been placed in power-down mode—you must also reset the D-PHY transmitter. This ensures proper synchronization and prevents any unexpected clock behavior.

5. Trigger the D-PHY transmitter to send normal transactions based on the new configuration. To prevent any packet loss, ensure that the D-PHY receiver is already out of reset and operating in active mode before valid packet transmission starts.

If you only need dynamic reconfiguration of the lane and gear without the CRC check function, do not check the *Enable CRC Check* attribute. Instead, you can simply enable the LMMI interface and dynamically write to the corresponding IP registers.

3. IP Parameter Description

The configurable attributes of the D-PHY Rx IP are shown in the following tables. You can configure the IP by setting the attributes accordingly in the IP Catalog Module/IP Block Wizard of the Lattice Radiant software.

Wherever applicable, default values are in bold.

3.1. General

Table 3.1. General Attributes

Attribute	Selectable Values	Description
Receiver		
RX Interface Type	DSI, **CSI-2**	D-PHY Rx interface type.
D-PHY RX IP	**Hard D-PHY**, Soft D-PHY	Implementation of the PHY layer of the D-PHY Rx. Only the CrossLink-NX device supports Hard D-PHY.
Number of RX Lanes	1, 2, 3, **4**	Number of D-PHY Rx high-speed ports. 3-lane configuration is only available when the Packet Parser is disabled.
RX Gear	**8**, 16	This is the width of the deserialized data stream per data lane. *RX Gear == 16* is available only on *D-PHY RX IP = Hard D-PHY* and when selected, it is recommended to operate the IP at data rates of 1000 Mbps or higher to ensure optimal performance.
Enable Deskew Calibration Detection	checked, **unchecked**	This entry is available when data rate is less than 1.5 Gbps. This is automatically set to enabled (and grayed out) at data rate over 1.5 Gbps as this feature is required for data rates over 1.5 Gbps.
Clock		
RX Line Rate per Lane (Mbps)[1]	160–2500, **800**	Maximum bandwidth for *RX Gear = 16*,
	80–1500, 80–1800, **800**	Maximum bandwidth for *RX Gear = 8*. Maximum line rate is 1800 Mbps for Lattice Avant devices and 1500 Mbps for other devices.
D-PHY Clock Frequency (MHz)	40–1250, **400**	Operating frequency of the PHY layer. The value is *RX Line Rate per Lane (Mbps)* / 2. Not editable. For information only.
Byte Clock Frequency (MHz)	10–187.5, **100**	Operating byte clock frequency of the IP. The value is *RX Line Rate per Lane (Mbps)* / *RX Gear*. Not editable. For information only.
D-PHY Clock Mode	**Continuous**, Non-continuous	Determines the clock mode of the PHY layer. The D-PHY protocol has an option for the clock lane to go to low power in between high-speed transfers to reduce power consumption. If the mode selected is *Non-continuous*, the control logic that detects the LP-to-HS and HS-to-LP sequences of the clock lane is enabled. Otherwise, the IP assumes the D-PHY clock lane is always in high-speed mode.
Sync Clock Frequency (MHz)	**60**–200	Operating frequency of the components interfaced with the fabric.
Module Architecture		
CIL Bypass	checked, **unchecked**	When using *D-PHY RX IP = Hard D-PHY*, this option bypasses the built-in Control Interface Logic (CIL) of the Hard D-PHY. CIL is the hardened block that controls the clock and data lane state transitions. If the CIL is bypassed, soft logic is used. When using *D-PHY RX IP = Soft D-PHY*, this option is automatically checked.
Enable Lane Aligner Module	checked, **unchecked**	Enables the lane alignment feature for multi-lane configuration. This feature is available when *D-PHY RX IP = Soft D-PHY*. This attribute is

Attribute	Selectable Values	Description
		automatically enabled if *Enable LMMI Interface* == checked, and always enabled for Lattice Avant devices with *RX Line Rate per Lane ≥ 1,000 Mbps*.
Enable Packet Parser	**checked**, unchecked	Enables or disables the packet parser function. When the packet parser is enabled, the IP reads through the contents of the packet header and converts them into CSI-2 or DSI related bus/signal outputs. When this is disabled, the deserialized data are sent out without analyzing the contents.
Enable AXI4-Stream Interface[3]	checked, **unchecked**	Enables the AXI4-Stream bus.
Enable LMMI Interface	checked, **unchecked**	Enables the LMMI bus used for accessing IP registers. When *D-PHY RX IP = Hard D-PHY*, the lmmi_clk_i signal is limited to a maximum operating frequency of 60 MHz.
Enable Miscellaneous Status Signals	checked, **unchecked**	Enables or disables the miscellaneous status signals. When enabled, select internal signals such as high-speed termination enables are available to the top-level IP wrapper. This may be used for debugging purposes. Not available when *CIL Bypass* is unchecked.
Enable CRC Check	checked, **unchecked**	Available for selection when *Enable Packet Parser* is checked, *Enable AXI4-Stream Interface* is unchecked, and *DSI Back-to-Back HS Packets== OFF*. When this option is checked, CRC checking function is enabled based on the *CRC Check Mode* attribute. The IP core computes the CRC for the payload and checks against the packet footer CRC. CRC error flag with valid is provided as output status signals. If CRC checking is not required, you do not need to select this option.
CRC Check Mode[2]	**Static**, Dynamic	Editable when *Enable CRC Check* and *Enable LMMI Interface* are checked for both *D-PHY RX IP = Soft D-PHY* and *D-PHY RX IP = Hard D-PHY* with *CIL Bypass* unchecked. This option is unavailable for *D-PHY RX IP = Hard D-PHY* with *CIL Bypass* checked. Select **Static** if you want the CRC checking function to operate only based on the compile-time IP configuration. This setting is suitable for cases where you want to enable CRC checking function but do not plan to dynamically reconfigure the lane and/or gear of the IP. Select **Dynamic** if you want the CRC checking function to operate based on the dynamically configured lane and/or gear. This setting is suitable for cases where you want to enable CRC checking for dynamically reconfigured lane and/or gear of the IP. Refer to the Dynamic Reconfiguration section for details.
Parser Configuration		
DSI Back-to-Back HS Packets	ON, **OFF**	Available for Rx Interface Type = *DSI* with *Enable Packet Parser* checked. Select OFF when there are low power states between packet transfers. Select ON if two or more DSI packets, including EoTp, Null and Blanking, are transmitted within a single HS transmission. When back-to-back packets are received, no ECC or CRC check is done and dynamic reconfiguration is not supported.
Timing Parameter		
Customize Data Settle Cycle	checked, **unchecked**	Enables customization of the data settle parameter, when *CIL Bypass* is checked. Check this option and re-calculate the Data Settle Cycle value based on the guidance.
Data Settle Cycle	1–255, **14**	Value of the data settle parameter when *CIL Bypass* is checked. This parameter corresponds to the THS-SETTLE timing parameter as defined in the MIPI D-PHY specification. When this *Customize Data*

Attribute	Selectable Values	Description
		Settle Cycle parameter is checked, you can determine the value of Data Settle Cycle (in the unit of byte clock cycle) based on the equation of ceil((85 ns+6 × UI) / TCLK_BYTE) , where 1 UI is equal to half of the period of D-PHY clock and TCLK_BYTE is equal to the period of byte clock (clk_byte_o for Soft D-PHY, clk_byte_fr_i for Hard D-PHY with CIL bypassed). For Soft D-PHY mode, the calculated value has to be offset down by 3 clk_byte_o cycles for clock domain crossing, except when using *RX_FIFO Type ==QUEUE* with the corresponding byte clock of 30 MHz and below. Example: D-PHY Rx IP = Soft D-PHY D-PHY Clock Frequency (MHz) = 220 MHz Frequency of clk_byte_o = 220/4 = 55 MHz TCLK_BYTE = 1/55 = 18182 ps 1 UI = (1/220)/2 = 2272.5 ps 85 ns+6 × UI = 85000 + 6 × (2272.5) = 85000 + 13635 = 98635 ps In this example, Data Settle Cycle = ceil(98635/18182) = 6. Taking the 3 clock cycles internal delay into account, the selected value must be set to 6 – 3 = 3.
Customize CIL Data Settle	checked, **unchecked**	Enables customization of the data settle parameter, when *CIL Bypass* is unchecked.
CIL Data Settle Cycle	1–63, **6**	Value of the data settle parameter when *CIL Bypass* is unchecked. Default value is computed in sync clock cycles based on THS-SETTLE timing with margin: ceil(100ns+8UI), where 1 UI is based on floor(*Byte Clock Frequency*). Example: RX Line Rate per Lane = 1500 Mbps Rx Gear = 8 Byte Clock (internal) = floor(RX Line Rate per Lane/RX Gear) = floor(1500/8) = floor(187.5) = 187 MHz 1 UI = (1000/(187 x 8) = 668.45 ps ceil(100 ns+8 × UI = ceil(100000 + 8 × (668.45)) = ceil(100000 + 5347.6) = 106000 ps Sync Clock Frequency = 60 MHz In this example, CIL Data Settle Cycle = int(106000/(1000000/60)) = 6.
Customize CIL Clock Settle	checked, **unchecked**	Enables customization of the clock settle parameter, when *CIL Bypass* is unchecked.
CIL Clock Settle Cycle	1–63, **9**	Value of the clock settle parameter when *CIL Bypass* is unchecked. Default value is computed in sync clock cycles based on TCLK-SETTLE == 150 ns timing. Example: Sync Clock Frequency = 60 MHz In this example, CIL Clock Settle Cycle = int(150000/(1000000/60)) = 9.

Attribute	Selectable Values	Description
Configurable Data Settle Count	checked, **unchecked**	When checked, an input bus rxcsr_datsettlecyc_i is available when D-PHY RX IP = *Soft D-PHY* or *CIL Bypass* is checked. You can adjust the tHS-SETTLE timer value without generating a new bitstream. This attribute is available starting from IP version 1.6.0.

Notes:

1. The maximum data rate depends on the gear, family, package, and speed grade of the device. Check the device data sheet for more information.
2. The *Enable Lane/Gear Dynamic Reconfiguration* attribute is available in IP versions prior to IP v2.0.0. Starting from IP v2.0.0, the *CRC Check Mode* attribute replaces the *Enable Lane/Gear Dynamic Reconfiguration* attribute. Setting the *CRC Check Mode* attribute to **Dynamic** is equivalent to having *Enable Lane/Gear Dynamic Reconfiguration* == checked in earlier versions of the IP.
3. As part of the ongoing efforts to enhance and streamline user experience, support for AXI4-Stream is gradually phased out. To ensure continuity and a smooth transition, discontinue the use of this feature and begin migration to the available alternative.

3.2. RX_FIFO Settings

Table 3.2. RX FIFO Settings Attributes

Attribute	Selectable Values	Description
RX_FIFO[1]		
RX_FIFO Enable	**checked**, unchecked	Enables or disables the RX FIFO function. When enabled, the FIFO after the PHY may be customized. Otherwise, a 4-register deep buffer is used. When using *D-PHY RX IP = Hard-D-PHY*, this option cannot be disabled. This FIFO buffers all high-speed transactions on the D-PHY data lanes, including the trail bits. For Soft D-PHY, this also includes the hs-zero bits.
Type	**PINGPONG**, QUEUE, SINGLE	Type of the FIFO implemented. This feature is available when *RX_FIFO Enable* is checked.
Implementation	**EBR**, LUT	Selects the memory implementation of the FIFO. This feature is available when *RX_FIFO Enable* is checked.
Depth	2, 4, 8, 16, 32, 64, 128, **256**, 512, 1024, 2048, 4096, 8192, 16384	Selects the memory depth of the FIFO. This feature is available when *RX_FIFO Enable* is checked.
Number of Queue Entries	2, **4**, 8	Determines the amount of Queue Entries available for the RX_FIFO. This option is editable when *Type = QUEUE* and *RX_FIFO* is checked.
Default FIFO Read Delay	0–16384, **8**	Determines the amount of delay of the RX_FIFO. This value is valid when *Type = PINGPONG or Type = SINGLE*, and *RX_FIFO* is checked. When this parameter is set to 0, the entire hs-transaction is buffered before FIFO is read, including the trail bits. For Soft D-PHY, this includes the hs-zero bits. For non-zero values, this sets the number of cycles of clk_byte_fr_i before reading from the RX_FIFO, starting from the deassertion of the fifo_empty signal. When *RX_FIFO Enable* is unchecked, the default value is 1.
Configurable FIFO Read Delay	checked, **unchecked**	When this is checked, an input bus rxcsr_rxfifo_pktdly_i is available to adjust the delay before the contents of the RX_FIFO is read.
Counter Width	1–14, **4**	When *Type = QUEUE*, this sets the width of the counter that tracks the number of write cycles per high-speed transaction, including trail bits (for Hard D-PHY) and hs-zero bits (for Soft D-PHY). For *Type = PINGPONG* or *SINGLE*, this is the width of the packet delay counter. This value is editable when *Type = QUEUE* and *RX_FIFO* is checked. If the Type = *Queue*, set to minimum of the ceiling value of log2(TOTAL_HS_BITS/(*Number of RX Lanes* × *RX Gear*)).

Attribute	Selectable Values	Description
		For example: Number of RX lane = 4 RX Gear = 8 Total HS bits including HS-ZERO and HS-TRAIL = 24000 The ceiling value is ceil(log2(24000/(4 × 8))) = 10
Clock Mode	SC, **DC**	Determines if the FIFO is implemented in Single Clock and Dual Clock. This value is editable when *Type = SINGLE* and *RX_FIFO* is checked. The clock mode is always *DC* when *D-PHY RX IP = Hard D-PHY*.
Misc Signals	checked, **unchecked**	When checked, this shows the fifo_empty and fifo_full status signals, and other miscellaneous debug ports at the top-level module.

Note:

1. RX FIFO attributes are unavailable when *D-PHY RX IP = Hard D-PHY* and *CIL Bypass* is unchecked.

3.3. Soft PHY Settings

Table 3.3. Soft PHY Settings Attributes

Attribute	Selectable Values	Description
Soft PHY[1]		
Delay Mode	**Edge Clock Centered**, User Defined	*Edge Clock Centered* uses a predetermined static delay value of the delay cells. The value is used to center align the D-PHY data with respect to the D-PHY clock edges. *User Defined* allows for customization of the delay cell settings.
Coarse Delay	**0 ns** 0.8 ns 1.6 ns	This attribute is applicable and editable only when the Delay Mode is *User Defined*. Selects between 0, 0.8, or 1.6 ns coarse delay.
Fine Delay	0-127	This attribute is applicable and editable only when the Delay Mode is *User Defined*. Each step value adds 12.5 ps delay on the data lanes.
Enable Dynamic Delay Control	checked, **unchecked**	When selected, a delay cell with dynamic adjustment capabilities is used instead of a static delay cell. Ports for dynamically controlling the fine and coarse delay are available in the soft IP. This feature is primarily used to adjust the delay dynamically when operating at different line rates.

Note:

1. In IP v1.6.0 onwards, a GUI tab for modifying the delay cell within the soft PHY is available. The attributes in this table are applicable only for Nexus devices.

4. Signal Description

This section describes the D-PHY Rx IP ports.

4.1. Clock and Reset Interface

Table 4.1. Clock and Reset Ports Description

Port Name	Direction	Mode/Configuration	Description
D-PHY Rx			
reset_n_i	Input	Not available when D-PHY RX IP == *Hard D-PHY* and *CIL Bypass* is unchecked	Active low asynchronous system reset of D-PHY core blocks.
reset_lp_n_i	Input	Not available when D-PHY Clock Mode == *Continuous* or (D-PHY RX IP == *Hard D-PHY* and *CIL Bypass* is unchecked)	Low asserted reset for the nets in the clk_lp_ctrl_i clock domain. The signal driving this port must be synchronized to the clk_lp_ctrl_i.
reset_byte_fr_n_i	Input	—	Low asserted reset for the nets in the clk_byte_fr_i clock domain.
sync_rst_i	Input	Not available when D-PHY RX IP == *Hard D-PHY* and *CIL Bypass* is checked	Active high reset. The signal driving this port must be synchronized to the sync_clk_i.
clk_lp_ctrl_i	Input	Not available when D-PHY Clock Mode == *Continuous* or (D-PHY RX IP == *Hard D-PHY* and *CIL Bypass* is unchecked)	Clocks the logic that detects the Rx D-PHY clock lane LP <-> HS transitions. The minimum frequency for clk_lp_ctrl_i is 40 MHz, as the minimum TLPX is 50 ns (1/25 ns = 40 MHz). Drives the term_clk_en_o and lp_hs_state_clk_o output ports.
clk_byte_fr_i	Input	—	Continuously running byte clock. This is div8 (in Gear 16) or div4 (in Gear 8) of the input D-PHY clock and follows the frequency set in the *Byte Clock Frequency (MHz)* attribute. This also clocks the logic that detects the Rx D-PHY data lane transitions (lp_hs_ctrl_d0-3 modules). This is used by the word_align, lane_align, and capture_control modules. Payload output is also in this clock domain. Drives the following output ports: • payload_en_o, payload_o, payload_bytevld_o, payload_crc_o, payload_crcvld_o, hs_sync_o, capture_en_o, bd_o, bd0_o, bd1_o, bd2_o, bd3_o, lp_en_o, sp_en_o, lp_av_en_o, lp2_en_o, sp2_en_o, lp2_av_en_o, vcx_o, dt_o, vc_o, wc_o, ecc_o, dt2_o, vc2_o, wc2_o, ecc2_o, crc_check_o, crc_error_o, ecc_check_o, ecc_1bit_error_o, ecc_2bit_error_o, ecc_byte_error_o • axis_tvalid_o, axis_tdata_o • rxdatsyncfr_state_o, rxemptyfr0_o, rxemptyfr1_o, rxque_curstate_o, rxque_empty_o, rxque_full_o, fifo_dly_err_o, fifo_undflw_err_o, fifo_ovflw_err_o • hs_d_en_o, term_d_en_o, lp_hs_state_d_o • skewcal_det_o when *D-PHY RX IP* == Soft D-PHY

Port Name	Direction	Mode/Configuration	Description
sync_clk_i	Input	Not available when D-PHY RX IP == *Hard D-PHY* and *CIL Bypass* is checked	Low speed or oscillator clock. This clock follows the frequency set in the *Sync Clock Frequency (MHz)* attribute. Drives the ready_o output port.
clk_byte_o	Output	—	Byte clock generated from the D-PHY module based on the input D-PHY clock lane. This clock latches the internal parallel byte data from dphy_rx_wrap. This is div4 or div8 of the *D-PHY Clock Frequency (MHz)* and follows the frequency set in the *Byte Clock Frequency (MHz)* attribute. This is only active when the data lanes are in high-speed mode. Default is 1'd0. Drives the rxfullfr0_o and rxfullfr1_o output ports.
clk_byte_hs_o	Output	—	Generated byte clock from the D-PHY module based on the input D-PHY clock lane, active only when the clock lanes are in high-speed mode. This clock is the same as the clk_byte_o when the D-PHY implementation is Soft D-PHY. Default is 1'd0. Drives the edgemon_done_o output port.
LMMI Device Target Interface			
lmmi_resetn_i	Input	Available when *Enable LMMI Interface* is checked	Active low signal to reset the configuration registers. Because of implementation constraints, this does not apply to hard D-PHY registers. To restore hard D-PHY registers to the default values, you must manually reprogram each register.
lmmi_clk_i	Input	Available when *Enable LMMI Interface* is checked	LMMI interface clock. When *D-PHY RX IP = Hard D-PHY*, the lmmi_clk_i signal is limited to a maximum operating frequency of 60 MHz. Drives the following output ports: • dphy_cfg_num_lanes_o, dphy_rxdatawidth_hs_o • lmmi_ready_o, lmmi_rdata_o, lmmi_rdata_valid_o

4.2. D-PHY Rx Interface

Table 4.2. D-PHY Rx Port Description

Port Name	Direction	Mode/Configuration	Description
D-PHY Rx			
clk_p_io, clk_n_io	Input/Output	—	MIPI D-PHY clock lane (positive and negative signals).
d_p_io[BUS_WIDTH[1] – 1:0], d_n_io[BUS_WIDTH[1] – 1:0]	Input/Output	—	MIPI D-PHY data lanes.
lp_d_rx_p_o[BUS_WIDTH[1] – 1:0], lp_d_rx_n_o[BUS_WIDTH[1] – 1:0]	Output	Not available when D-PHY RX IP == *Hard D-PHY* and *CIL Bypass* is unchecked	Low power data lanes. Default is {BUS_WIDTH[1]{1'b1}}.
pd_dphy_i	Input	Not available when D-PHY RX IP == *soft D-PHY*	Powers down the hardened D-PHY block. This can be used as an asynchronous high asserted hard reset of the hardened D-PHY block. This signal must not be tied to 1'b0. Assert this signal in the beginning, and then de-assert after the VCC is stabilized. Alternatively, drive this signal with the AND of the global reset with the PLL lock signal.

Port Name	Direction	Mode/Configuration	Description
tx_rdy_i	Input	Not available when D-PHY RX IP == *Hard D-PHY* and *CIL Bypass* is unchecked	Indicates that the module at the receiving end is ready to receive data from the CSI-2/DSI D-PHY Rx IP module. When asserted, the IP transmits data from RX FIFO or internal buffer as the data becomes available.
pll_lock_i	Input	Not available when D-PHY RX IP == *Hard D-PHY*	PLL lock indicator indicating if a PLL is used to generate a free-running byte clock. Set this to 1 if a PLL is not used. This is also used to reset rx_fifo and is connected to the start_i pin of gddr_sync.
ref_dt_i[5:0]	Input	Available when LMMI is disabled and Enable Packet Parser is enabled	Reference data type.
rxcsr_datsettlecyc_i [7:0]	Input	Available when *Configurable Data Settle Count* is checked and LMMI is disabled	Controls the tHS-SETTLE protocol timing parameter. Check the t-HSZERO parameter of the D-PHY transmitter to ensure the tHS-SETTLE setting can properly detect the Start-of-Transmit pattern.
rxcsr_rxfifo_pktdly_i[15:0]	Input	Available when *Configurable RX_FIFO Read Delay* is checked and LMMI is disabled	Controls the delay before the contents of the RX_FIFO is read out. This is applicable for pingpong or single RX_FIFO types.
rxcsr_dropnull_i	Input	Available when LMMI is disabled and Enable Packet Parser is enabled	This signal is tied to 0 when it is not exposed. Drive this signal when it is exposed: • 1'b0 – Null and Blanking packets trigger an assertion of lp_en. Payload is also transmitted out. The output signal lp_av_en stays low. • 1'b1 – Null and Blanking packets are ignored by the IP.
rxcsr_vcx_on_i	Input	Available when LMMI is disabled, and Enable Packet Parser is enabled	This signal is tied to 0 when it is not exposed. Drive this signal when it is exposed: • 1'b0 – No extended virtual channel ID; uses 24-bit Hamming code. • 1'b1 – Packet header ECC byte[7:6] is used as extended virtual channel ID; uses 26-bit Hamming code.
lp_d0_tx_en_i	Input	Available in DSI Mode and *CIL Bypass* is checked	Active high. Enables low power transmit back to the DSI host. Data lane 0 goes out of differential mode and switches to low power signaling.
lp_d0_tx_p_i	Input	Available in DSI Mode and *CIL Bypass* is checked	This is the transmit value for the low power data lane 0 p-channel.
lp_d0_tx_n_i	Input	Available in DSI Mode and *CIL Bypass* is checked	This is the transmit value for the low power data lane 0 n-channel.
ready_o	Output	Not available when D-PHY RX IP == *Hard D-PHY*	Indicates the state of gddr_sync. Default is 1'd0.

Port Name	Direction	Mode/Configuration	Description
edgemon_done_o	Output	Available in Lattice Avant devices	Indicates that dynamic clock-to-data centering of the soft D-PHY is complete. This is only applicable when *RX Line Rate per Lane ≥ 1,000 Mbps*. This is tied to 1'd0 for other data rates. For *RX Line Rate per Lane ≥ 1,000 Mbps,* because of the dynamic nature of the clock-to-data centering, lock is achieved after a few frames. The IP guarantees valid output data only after this signal is asserted. Default is 1'd0.
payload_en_o	Output	Available when *Enable Packet Parser* is checked and AXI4-Stream is disabled	Signifies the arrival of valid payload data without the CRC. Default is 1'd0.
payload_o[DW[3]-1:0]	Output	Available when *Enable Packet Parser* is checked and AXI4-Stream is disabled	This is the payload of a long packet, excluding the CRC bits, arranged the way it is received in the data lanes. Default is {DW[3]{1'd0}}.
payload_bytevld_o[7:0]	Output	Available when *Enable Packet Parser* is checked and AXI4-Stream is disabled	Each bit corresponds to a valid byte in the payload_o. [0] – payload_o [7:0] is valid [1] – payload_o [15:8] is valid [2] – payload_o [23:16] is valid [3] – payload_o [31:24] is valid [4] – payload_o [39:32] is valid [5] – payload_o [47:40] is valid [6] – payload_o [55:48] is valid [7] – payload_o [63:56] is valid All bits are tied to low when *DSI Back-to-Back HS Packet == ON*. Default is 8'd0.
payload_crc_o[15:0]	Output	Available when *Enable Packet Parser* is checked and AXI4-Stream is disabled	Long packet footer CRC bytes. Default is 16'd0.
payload_crcvld_o	Output	Available when *Enable Packet Parser* is checked and AXI4-Stream is disabled	Indicates the payload_crc_o is valid when asserted. Default is 1'd0.
hs_sync_o	Output	Not available if *CIL_Bypass* is unchecked	Indicates the successful detection of the synchronization code 'B8 in the data lanes. This signal asserts from the start of synchronization pattern 'B8 up to the last data captured before detecting LP-11 state of any lane (for Soft D-PHY) or data lane 0 (for Hard D-PHY). Default is 1'd0.

Port Name	Direction	Mode/Configuration	Description
capture_en_o	Output	Available when *Enable Packet Parser* is unchecked and AXI4-Stream is disabled	Functions as a valid signal for bd0_o to bd3_o. This is enabled from the start of synchronization pattern 'B8 up to the last data captured before detecting LP-11 state of any lane (for Soft D-PHY) or data lane 0 (for Hard D-PHY). When *CIL Bypass* is unchecked, hard-DPHY does not output the synchronization pattern 'B8 and first byte is replaced with a dummy byte and must be ignored. If last bit of the valid HS data is 0, there may be a dummy byte after the trail bytes as D-PHY includes the tHS-EXIT detection of all lanes before deasserting capture_en_o. This is the same as hs_sync_o. Default is 1'd0.
bd_o[DW[3]-1:0]	Output	Available when *Enable Packet Parser* is checked	Valid only for Rx gear 8. This is the D-PHY byte data. Default is {DW[3]{1'd0}}.
bd0_o[*RX Gear*-1:0]	Output	Available when *Enable Packet Parser* is unchecked and AXI4-Stream is disabled	Parallel data from lane 0. This is 8-bit wide if the design is configured as Gear 8, or 16-bit wide if gearing is 16. Default is {*RX Gear*{1'b0}}.
bd1_o[*RX Gear*-1:0]	Output	Available when *Enable Packet Parser* is unchecked and AXI4-Stream is disabled	Parallel data from lane 1. This is 8-bit wide if the design is configured as Gear 8, or 16-bit wide if gearing is 16. Default is {*RX Gear*{1'b0}}.
bd2_o[*RX Gear*-1:0]	Output	Available when *Enable Packet Parser* is unchecked and AXI4-Stream is disabled	Parallel data from lane 2. This is 8-bit wide if the design is configured as Gear 8, or 16-bit wide if gearing is 16. Default is {*RX Gear*{1'b0}}.
bd3_o[*RX Gear*-1:0]	Output	Available when *Enable Packet Parser* is unchecked and AXI4-Stream is disabled	Parallel data from lane 3. This is 8-bit wide if the design is configured as Gear 8, or 16-bit wide if gearing is 16. Default is {*RX Gear*{1'b0}}.
lp_en_o	Output	Available when *Enable Packet Parser* is checked	Signifies the arrival of long packet data. This asserts when a valid long packet data type is received. Default is 1'd0.
sp_en_o	Output	Available when *Enable Packet Parser* is checked	Signifies the arrival of short packet data. This asserts when a valid short packet data type is received. Default is 1'd0.
lp_av_en_o	Output	Available when *Enable Packet Parser* is checked	Asserts with lp_en_o if long packet received is the same as the input reference data type ref_dt_i. Default is 1'd0.
lp2_en_o[2]	Output	Available when *Enable Packet Parser* is checked	Same as lp_en_o only if *Number of RX Lanes* × *RX Gear* == 64. In 64-bit width configuration, the IP can sample 2 different valid packet headers in 1 byte clock cycle. Information for the second header is reflected in this port. Default is 1'd0.

Port Name	Direction	Mode/Configuration	Description
sp2_en_o[2]	Output	Available when *Enable Packet Parser* is checked	Same as sp_en_o only if *Number of RX Lanes* × *RX Gear* == 64. In 64-bit width configuration, the IP can sample 2 different valid packet headers in 1 byte clock cycle. Information for the second header is reflected in this port. Default is 1'd0.
lp2_av_en_o[2]	Output	Available when *Enable Packet Parser* is checked	Same as lp_av_en_o only if *Number of RX Lanes* × *RX Gear* == 64. In 64-bit width configuration, the IP can sample 2 different valid packet headers in 1 byte clock cycle. Information for the second header is reflected in this port. Default is 1'd0.
vcx_o	Output	Available when *Enable Packet Parser* is checked and AXI4-Stream is disabled	Virtual channel extension. Default is 2'd0.
dt_o[5:0]	Output	Available when *Enable Packet Parser* is checked and AXI4-Stream is disabled	CSI-2 or DSI 6-bit data type field. Default is 6'd0.
vc_o[1:0]	Output	Available when *Enable Packet Parser* is checked and AXI4-Stream is disabled	2-bit virtual channel ID of the packet. Default is 2'd0.
wc_o[15:0]	Output	Available when *Enable Packet Parser* is checked and AXI4-Stream is disabled	16-bit Word Count field. This denotes the number of bytes in the payload of a long packet. In a short packet, this contains a 2-byte data. Enabled when packet formatter is valid. Default is 16'd0.
ecc_o[5:0]	Output	Available when *Enable Packet Parser* is checked and AXI4-Stream is disabled	This is the received 6-bit error correction code (ECC). Default is 6'd0.
dt2_o[5:0][2]	Output	Available when *Enable Packet Parser* is checked and AXI4-Stream is disabled	Same as dt_o only if *Number of RX Lanes* × *RX Gear* == 64. In 64-bit width configuration, the IP can sample 2 different valid packet headers in 1 byte clock cycle. Information for the second header is reflected in this port. Default is 6'd0.
vc2_o[1:0][2]	Output	Available when *Enable Packet Parser* is checked and AXI4-Stream is disabled	Same as vc_o only if *Number of RX Lanes* × *RX Gear* == 64. In 64-bit width configuration, the IP can sample 2 different valid packet headers in 1 byte clock cycle. Information for the second header is reflected in this port. Default is 2'd0.
wc2_o[15:0][2]	Output	Available when *Enable Packet Parser* is checked and AXI4-Stream is disabled	Same as wc_o only if *Number of RX Lanes* × *RX Gear* == 64. In 64-bit width configuration, the IP can sample 2 different valid packet headers in 1 byte clock cycle. Information for the second header is reflected in this port. Default is 16'd0.

Port Name	Direction	Mode/Configuration	Description
ecc2_o[5:0][2]	Output	Available when *Enable Packet Parser* is checked and AXI4-Stream is disabled	Same as ecc_o only if *Number of RX Lanes* × *RX Gear* == 64. In 64-bit width configuration, the IP can sample 2 different valid packet headers in 1 byte clock cycle. Information for the second header is reflected in this port. Default is 6'd0.
crc_check_o	Output	Available when *Enable CRC Check* is checked and AXI4-Stream is disabled	Indicates the crc_error_o is valid when asserted. Default is 1'd0.
crc_error_o	Output	Available when *Enable CRC Check* is checked and AXI4-Stream is disabled	When asserted, it indicates the packet footer CRC bytes do not match the computed payload CRC bytes. Default is 1'd0.
ecc_check_o	Output	Available when *Enable Packet Parser* is checked and AXI4-Stream is disabled	Indicates that ecc_1bit_error_o, ecc_2bit_error_o, and ecc_byte_error_o signals are valid when asserted. Asserts 1 byte clock cycle before the corresponding sp_en_o or lp_en_o is asserted. Default is 1'd0.
ecc_1bit_error_o	Output	Available when *Enable Packet Parser* is checked and AXI4-Stream is disabled	Indicates that one bit error has been detected and corrected in the packet header when asserted. Default is 1'd0.
ecc_2bit_error_o	Output	Available when *Enable Packet Parser* is checked and AXI4-Stream is disabled	Indicates that two or more errors have been detected in the packet header when asserted. Long packet payload is dropped. Default is 1'd0.
ecc_byte_error_o	Output	Available when *Enable Packet Parser* is checked and AXI4-Stream is disabled	Indicates that a flipped bit has been detected in the packet header ECC byte when asserted. Long packet payload is propagated. Default is 1'd0.

skewcal_det_o[BUS_WIDTH[1] – 1:0]	Output	Available when *Enable Deskew Calibration Detection* is enabled	Indicates that skew calibration burst is detected. This is an asynchronous signal when *D-PHY RX IP* == Hard D-PHY and synchronous to clk_byte_fr_i when *D-PHY RX IP* == Soft D-PHY. The behavior of the signal depends on the following conditions:
			• When *D-PHY RX IP* == Soft D-PHY and either RX FIFO *Type* == *QUEUE* or FIFO Read Delay == 0:
			  • This signal is asserted for approximately four clock cycles after the entire deskew calibration sequence is received.
			• Else:
			  • This signal is asserted when high speed deskew burst is received and deasserted when data lanes transition back to LP-11 state.
			Default is {BUS_WIDTH[1]{1'd0}}.

Port Name	Direction	Mode/Configuration	Description
skewcal_done_o[BUS_WIDTH[1] – 1:0]	Output	Available when Enable Deskew Calibration Detection is enabled and *CIL Bypass* is unchecked	This is an asynchronous signal that indicates that skew calibration of RX is done. The signal toggles independently, and the assertion width is asynchronous and may vary, depending on the timing of the calibration process. Default is {BUS_WIDTH[1]{1'd0}}.
dphy_cfg_num_lanes_o[1:0]	Output	Available when *Enable Packet Parser* is checked	Number of active lanes that are configured for the IP: 2'b00: 1 lane 2'b01: 2 lanes 3'b10: 3 lanes 4'b11: 4 lanes Default is the number of active lanes configured during generation.
dphy_rxdatawidth_hs_o[1:0]	Output	Available when *Enable Packet Parser* is checked	Number of gears that are configured for the IP: 2'b00: Gear 8 2'b01: Gear 16 3'b10: Reserved 4'b11: Reserved Default is the number of gears configured during generation.
data_loadn_i[4]	Input	Available when *Enable Dynamic Delay Control* is checked	Dynamic delay cell control signal for Nexus devices. Set 0 on LOADN resets to default delay setting.
data_move_i[4]	Input	Available when *Enable Dynamic Delay Control* is checked	Dynamic delay cell control signal for Nexus devices. Pulse on MOVE changes delay setting. DIRECTION is sampled at the falling edge of MOVE.
data_dir_i[4]	Input	Available when *Enable Dynamic Delay Control* is checked	Dynamic delay cell control signal for Nexus devices. Set to 1 to decrease delay and 0 to increase delay.
data_coarsedly_i[1:0][4]	Input	Available when *Enable Dynamic Delay Control* is checked	Dynamic delay cell control signal for Nexus devices. Dynamic coarse delay control (2 bits). 00: No coarse delay 01: 800 ps delay 10: 1600 ps delay 11: Invalid
data_cflag_o[BUS_WIDTH[1] – 1:0][4]	Output	Available when *Enable Dynamic Delay Control* is checked	Dynamic delay cell status signal for Nexus devices. Asynchronous flag indicating the delay counter has reached the maximum (when moving up) or minimum (when moving down) value.

Notes:

1. BUS_WIDTH – Number of D-PHY Lanes that are available on the user interface (*Number of RX Lanes*).
2. When *Number of RX Lanes* × *RX Gear* == 64 and *DSI Back-to-Back HS Packets* == *ON*, the IP can sample 2 different valid packet headers in 1 byte clock cycle. For example, in a short packet to the HS blanking packet sequence, 4-byte header of short packet and 4-byte header of HS blanking packet are sampled in 1 byte clock cycle as the internal data sampling is 64-bit wide. The corresponding information for the second header is reflected in this port.
3. DW – Byte or Packet Data Width
   DW = *RX Gear* × *Number of RX Lanes*
4. Available only for Nexus devices. For more information, refer to the CrossLink-NX High-Speed I/O Interface User Guide (FPGA-TN-02097).

4.3. LMMI Device Target Interface

Table 4.3. LMMI Device Target Interface Signals Description

Port Name	Direction	Mode/Configuration	Description
LMMI Device Target Interface			
lmmi_wdata_i[7:0]	Input	Available when *Enable LMMI Interface* is checked	Start transaction.
lmmi_wr_rdn_i	Input	Available when *Enable LMMI Interface* is checked	Write = HIGH, Read = LOW.
lmmi_offset_i[7:0]	Input	Available when *Enable LMMI Interface* is checked	Register offset, starting at offset 0.
lmmi_request_i	Input	Available when *Enable LMMI Interface* is checked	Write data.
lmmi_ready_o	Output	Available when *Enable LMMI Interface* is checked	Read data. Default is 1'd0.
lmmi_rdata_o[7:0]	Output	Available when *Enable LMMI Interface* is checked	Read transaction is complete and lmmi_rdata_o[] contains valid data. When Soft D-PHY is enabled, default is 0x00. When Hard D-PHY is enabled, default is based on the corresponding register value when lmmi_offset_i == 0x00.
lmmi_rdata_valid_o	Output	Available when *Enable LMMI Interface* is checked	Indicates lmmi_rdata_o contains valid data. Default is 1'd0.

4.4. AXI4-Stream Device Transmitter Interface

Table 4.4. AXI4-Stream Device Transmitter Interface Signals Description

Port Name	Direction	Mode/Configuration	Description
AXI4-Stream Device Transmitter Interface			
axis_tready_i	Input	Available when *Enable AXI4-Stream Interface* is checked	Indicates that the module at the receiving end is ready to receive data from the CSI-2/DSI D-PHY RX IP module. Back-pressure is not yet supported and this is currently unused in the IP.
axis_tvalid_o	Output	Available when *Enable AXI4-Stream Interface* is checked	AXI4-Stream indicates that data to be transmitted is valid. Default is 1'd0.
axis_tdata_o[ADW[1]-1:0]	Output	Available when *Enable AXI4-Stream Interface* is checked	Payload data transmitting channel (byte data or packet data with virtual channel, data type, and word count). Default is {ADW{1'b0}}.

Note:

1. ADW – AXI4-Stream Data Width.
   - If *Enable Packet Parser* is unchecked, ADW = *Number of RX Lanes* × *RX Gear*.
   - If *Enable Packet Parser* is checked and *Number of RX Lanes* × *RX Gear* == 64, ADW = (*Number of RX Lanes* × *RX Gear*) + 64.
   - Otherwise, ADW = *Number of RX Lanes* × *RX Gear* + 32.

4.5. RX FIFO Status Interface

Table 4.5. RX FIFO Status Interface Signals Description

Port Name	Direction	Mode/Configuration	Description
RX FIFO Status Signals (available when Misc Signals of RX_FIFO is checked)			
rxdatsyncfr_state_o[1:0]	Output	—	State Machine for reading data from FIFO. SINGLE Mode: 2'b00 – IDLE state 2'b01 – Read data from buffer instance 0 QUEUE Mode: 2'b00 – IDLE state 2'b01 – Read data from buffer instance 0 2'b11 – Read data done PINGPONG Mode: 2'b00 – IDLE state 2'b01 – Read data from buffer instance 0 2'b10 – Read data from buffer instance 1 2'b11 – Read data done Default is 2'd0.
rxemptyfr0_o	Output	—	FIFO empty flag of instance 0. Default is 1'd1.
rxemptyfr1_o	Output	Only applicable in PINGPONG Mode	FIFO empty flag of instance 1. Default is 1'd1.
rxfullfr0_o	Output	—	FIFO full of instance 0. Default is 1'd0.
rxfullfr1_o	Output	Only applicable in PINGPONG Mode	FIFO full of instance 1. Default is 1'd0.
rxque_curstate_o[1:0]	Output	Only applicable in QUEUE Mode	State Machine of RX Queue: 2'b00 – IDLE state 2'b01 – Pop entry from queue 2'b10 – Wait for read data from buffer is done 2'b11 – One delay cycle before Idle Default is 2'd0.
rxque_empty_o	Output	Only applicable in QUEUE Mode	RX Queue empty flag. Default is 1'd1.
rxque_full_o	Output	Only applicable in QUEUE Mode	RX Queue full flag. Default is 1'd0.
fifo_dly_err_o	Output	Not applicable in QUEUE Mode	An error flag that indicates a write happened when there is still an outstanding transfer in the RX FIFO. This flag is cleared when a new HS transfer happens. Default is 1'd0.
fifo_undflw_err_o	Output	—	An error flag that indicates a read happened when the FIFO is empty. This happens if the TX clock is faster than RX clock and there is not enough data in the FIFO. This flag is cleared when a new HS transfer happens. Increase the FIFO delay setting to give time for data to accumulate in the buffer. Default is 1'd0.

Port Name	Direction	Mode/Configuration	Description
fifo_ovflw_err_o	Output	—	An error flag that indicates a write happens when the FIFO is full. This happens if the TX cannot flush out the FIFO fast enough. This flag is cleared when a new HS transfer happens. Decrease the delay setting, increase the FIFO depth, or both. Default is 1'd0.

4.6. Miscellaneous Status Interface

Table 4.6. Miscellaneous Status Interface Signals Description

Port Name	Direction	Mode/Configuration	Description
Miscellaneous Status Signals (available when Enable Miscellaneous Status is checked)			
term_clk_en_o	Output	Not available when D-PHY RX IP == *Hard D-PHY* and *CIL Bypass* is unchecked	Active-high enable signal for the line termination of the D-PHY clock lane. This is asserted on detection of transition from LP-11 to LP-01 of the clock lane, and de-asserted upon detection of LP-11 after a high-speed mode. Default is 1'd1 if *D-PHY Clock Mode* == *Continuous* and 1'd0 if *D-PHY Clock Mode* == *Non-Continuous*.
term_d_en_o[BUS_WIDTH[1]-1:0]	Output	Depends on *Number of RX Lanes* Not available when D-PHY RX IP == *Hard D-PHY* and *CIL Bypass* is unchecked	Active-high enable signal for the line termination of the D-PHY clock lane. This is asserted on detection of transition from LP-11 to LP-01 of the lanes, and de-asserted upon detection of LP-11 after a high-speed mode. Default is {BUS_WIDTH[1]{1'b0}}.
hs_d_en_o	Output	Not available when D-PHY RX IP == *Hard D-PHY* and *CIL Bypass* is unchecked	Active-high high-speed mode enable signal for data lane d0. For Hard D-PHY IP, this signal is also used for HS mode enable for other data lanes. Default is 1'd0.
cd_d0_o	Output	Not available when D-PHY RX IP == *Hard D-PHY* and *CIL Bypass* is unchecked	An asynchronouse signal used to indicate contention detection on lane 0. Default is 1'd1.
cd_clk_o	Output	Not available when D-PHY RX IP == *Hard D-PHY* and *CIL Bypass* is unchecked	An asynchronous signal used to indicate contention detection on the clock lane. Default is 1'd1.
lp_hs_state_clk_o[1:0]	Output	Not available when D-PHY RX IP == *Hard D-PHY* and *CIL Bypass* is unchecked	2-bit state encoding of the D-PHY clock controller: 2'b00 – Idle state 2'b01 – LP11 state 2'b10 – LP01 state 2'b11 – HS state Default is 2'd0.
lp_hs_state_d_o[1:0]	Output	Not available when D-PHY RX IP == *Hard D-PHY* and *CIL Bypass* is unchecked	2-bit state encoding of the D-PHY data lane 0 controller: 2'b00 – Idle state 2'b01 – LP11 state 2'b10 – LP01 state 2'b11 – HS state Default is 2'd0.

Note:

1. BUS_WIDTH – Number of D-PHY Lanes that are available on the user interface (*Number of RX Lanes*).

5. Register Description

All registers listed in Table 5.1, Table 5.2, and Table 5.3 are accessible through LMMI.

5.1. Register Address Map

Table 5.1. General Configuration Registers

Offset (6 bits)	Access Type	Register Name	Description
Available in Hard D-PHY			
0x00-0x1E[2,4]	R/W	Hard D-PHY Registers	LMMI accessible Hard D-PHY control registers
Packet Parser Registers[5]			
0x0A[2]	RW	LANE_SETTING_ADDR	Number of Lane Select
0x1F[3]	R	VC_DT_ADDR	Virtual channel and Data type register address
0x20[3]	R	WCL_ADDR	Word count low register address
0x21[3]	R	WCH_ADDR	Word count high register address
0x22[3]	R	ECC_ADDR	ECC register address. When extended virtual channel is enabled, packet header ECC byte[7:6] is used as extended virtual channel ID.
0x27	RW	REFDT_ADDR	Reference data type
0x35	RW	CONTROL_ADDR	Parser Controls
Available for *RX Gear == 16* with *Number of RX Lanes == 4* and *DSI Back-to-Back HS Packets == ON*[5]			
0x23[3]	R	VC_DT2_ADDR	Virtual channel 2 and Data type 2 register address
0x24[3]	R	WC2L_ADDR	Word count 2 low register address
0x25[3]	R	WC2H_ADDR	Word count 2 high register address
0x26[3]	R	ECC2_ADDR	ECC 2 register address
Error Control and Status Registers[5]			
0x28	W1C	ERROR_STATUS_ADDR	ECC and CRC error status address
0x29	RW	ERROR_STATUS_EN_ADDR	ECC and CRC error status enable address
0x30	R	CRC_BYTE_LOW_ADDR	Received payload CRC LSB address
0x31	R	CRC_BYTE_HIGH_ADDR	Received payload CRC MSB address
0x32	W1C	ERROR_CTRL_ADDR	Hard D-PHY control error address. This is only applicable when *CIL Bypass* is unchecked.
0x33	W1C	ERROR_HS_SOT_ADDR[1]	Hard D-PHY Start-of-Transmit error address. This is asserted when the high-speed SoT leader sequence is corrupted, but proper synchronization can still be achieved.
0x34	W1C	ERROR_HS_SOT_SYNC_ADDR[1]	Hard D-PHY Start-of-Transmit synchronization error address. This is asserted when the high-speed SoT leader sequence is corrupted, and synchronization cannot be achieved.
0x36	RW	NOCIL_DSETTLE_ADDR	Data Settle register for Soft D-PHY or CIL_bypassed Hard D-PHY
0x37	RW	NOCIL_RXFIFODEL_LSB_ADDR	RX_FIFO read delay LSB register for Soft D-PHY or CIL_bypassed Hard D-PHY
0x38	RW	NOCIL_RXFIFODEL_MSB_ADDR	RX_FIFO read delay MSB register for Soft D-PHY or CIL_bypassed Hard D-PHY
0x39	W1C	ERROR_SOT_SYNC_DET_ADDR	Soft D-PHY Start-of-Transmit synchronization detect error address

Notes:

1. When there is 2-bit error, the error may be the IP flags SOT error instead of SOT synchronization error depending on the bit location where the error is detected.
2. Offset 0x0A is also accessible for soft D-PHY mode but only 0x0A[2:1] has write permission. Dynamic lane reconfiguration feature is only supported in hard D-PHY with *CIL Bypass* unchecked and Nexus soft D-PHY configurations.
3. When *DSI Back-to-Back HS Packets == ON* and gap between packets is small, status reporting in this register is limited. It is recommended to refer to the corresponding IP top-level ports for real-time data.
4. Avoid accessing or modifying any addresses within the 0x00 – 0x1E range that are not specified in the table. Altering these addresses may lead to IP malfunctions.
5. For non-hard D-PHY registers (offset > 0x1E), status updates may be delayed by up to 8 lmmi_clk_i cycles after data becomes available on the native interface because of the internal IP processing latency.

5.2. General Configuration Registers

Table 5.2. Configuration Registers (MIPI Programmable Bits)

ADDR[5:0]	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
0x1F	Header Packet Virtual Channel ID [1:0] Default is 0x0.		Header Packet Data Type [5:0] Default is 0x00.					
0x20	Header Packet Byte 1 (Word Count LSB) [7:0] Default is 0x00.							
0x21	Header Packet Byte 2 (Word Count MSB) [7:0] Default is 0x00.							
0x22	Header Packet Byte 3 (ECC Byte) [7:0] Default is 0x00.							
0x23	Header Packet 2 Virtual Channel ID [1:0] Default is 0x0.		Header Packet 2 Data Type [5:0] Default is 0x00.					
0x24	Header Packet 2 Byte 1 (Word Count LSB) [7:0] Default is 0x00.							
0x25	Header Packet 2 Byte 2 (Word Count MSB) [7:0] Default is 0x00.							
0x26	Header Packet 2 Byte 3 (ECC Byte) [7:0] Default is 0x00.							
0x27	Unused Default is 0x0.		Reference data type. If the received packet data type is the same as the reference data type, the lp_av_en_i is asserted. Default is 0x00.					
0x28[1]	Unused Default is 0x0.				2-bit ECC error – more than 2 flipped bits encountered in the received packet header. Packet is dropped. Default is 1'b0.	1-bit ECC error – a flipped bit is encountered in the received packet header and is corrected. Packet transmission continues. Default is 1'b0.	ECC byte error – a flipped bit is encountered in the ECC byte. Packet transmission continues. Default is 1'b0.	CRC error – a CRC error is encountered in the payload bits. Default is 1'b0.

ADDR[5:0]	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
0x29[1]	Unused Default is 0x0.				2-bit ECC error enable – if this bit is 1, 2-bit ECC error is reported. Otherwise, bit[3] of the ERROR_STATUS register stays at 0. Default is 1'b1.	1-bit ECC error enable – if this bit is 1, 1-bit ECC error is reported. Otherwise, bit[2] of the ERROR_STATUS register stays at 0. Default is 1'b1.	ECC byte error enable – if this bit is 1, 1-bit ECC error is reported. Otherwise, bit[1] of the ERROR_STATUS register stays at 0. Default is 1'b1.	CRC error enable – if this bit is 1, CRC error is reported. Otherwise, bit[0] of the ERROR_STATUS register stays at 0. Default is 1'b1.
0x30	Payload CRC [7:0] Default is 0x00.							
0x31	Payload CRC [15:8] Default is 0x00.							
0x32	Unused Default is 0x0.				This bit asserts when an incorrect state sequence is detected in Hard D-PHY data lane 3. Default is 1'b0.	This bit asserts when an incorrect state sequence is detected in Hard D-PHY data lane 2. Default is 1'b0.	This bit asserts when an incorrect state sequence is detected in Hard D-PHY data lane 1. Default is 1'b0.	This bit asserts when an incorrect state sequence is detected in Hard D-PHY data lane 0. Default is 1'b0.
0x33	Unused Default is 0x0.				This bit asserts when a 1-bit Start-of-Transmit error is detected in Hard D-PHY data lane 3. Default is 1'b0.	This bit asserts when a 1-bit Start-of-Transmit error is detected in Hard D-PHY data lane 2. Default is 1'b0.	This bit asserts when a 1-bit Start-of-Transmit error is detected in Hard D-PHY data lane 1. Default is 1'b0.	This bit asserts when a 1-bit Start-of-Transmit error is detected in Hard D-PHY data lane 0. Default is 1'b0.
0x34	Unused Default is 0x0.				This bit asserts when a Start-of-Transmit error is detected in Hard D-PHY data lane 3. Entire HS packet is dropped. Default is 1'b0.	This bit asserts when a Start-of-Transmit error is detected in Hard D-PHY data lane 2. Packet is dropped. Default is 1'b0.	This bit asserts when a Start-of-Transmit error is detected in Hard D-PHY data lane 1. Packet is dropped. Default is 1'b0.	This bit asserts when a Start-of-Transmit error is detected in Hard D-PHY data lane 0. Packet is dropped. Default is 1'b0.
0x35	Unused Default is 0x00.						0- extended virtual channel disabled. 1- extended virtual channel enabled. Default is 1'b0.	0 – blank and null packets are transmitted. 1- blank and null packets are dropped. Default is 1'b0.
0x36	Datasettlecyc[7:0] – used when the IP is configured as Soft D-PHY or CIL_bypassed Hard D-PHY. This is the number of clk_byte_o that the IP ignores for the HS data lanes after transitioning from LP mode (tHS-SETTLE protocol timing parameter). Check the t-HSZERO parameter of the D-PHY transmitter to ensure the tHS-SETTLE setting detects the Start-of-Transmit pattern. Default depends on the *Data Settle Cycle* attribute.							

ADDR[5:0]	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
0x37	RXFIFOReadDelay[7:0] – LSB of the RX FIFO read delay register. This input controls the number of byte clocks (clk_byte_fr_i) before the contents of the RX_FIFO is read out. This is applicable for pingpong or single RX_FIFO types.Default depends on the *Default FIFO Read Delay[7:0]* attribute. Bus width of internal delay counter is ceiling of log2(*Default FIFO Read Delay*).							
0x38	RXFIFOReadDelay[15:8] – MSB of the RX FIFO read delay register. This input controls the number of byte clocks (clk_byte_fr_i) before the contents of the RX_FIFO is read out. This is applicable for pingpong or single RX_FIFO types. Default depends on the *Default FIFO Read Delay[15:8]* attribute. Bus width of internal delay counter is ceiling of log2(*Default FIFO Read Delay*).							
0x39[1,2]	Unused Default is 0x0.				Asserts if Start-of-Transmit synchronization code is not detected in soft D-PHY lane 3. Default is 1'b0.	Asserts if Start-of-Transmit synchronization code is not detected in soft D-PHY lane 2. Default is 1'b0.	Asserts if Start-of-Transmit synchronization code is not detected in soft D-PHY lane 1. Default is 1'b0.	Asserts if Start-of-Transmit synchronization code is not detected in soft D-PHY lane 0. Default is 1'b0.

Notes:

1. When using the Lattice Avant soft D-PHY and *RX Line Rate per Lane* ≥ 1,000 Mbps, this status register may assert during calibration when enabled. To report status for valid packets, you need to clear these registers after edgemon_done_o asserts.
2. When *Enable Deskew Calibration Detection* is checked, SOT error checking is affected. 0xFF is taken as valid LEADING sequence for the Deskew Calibration packets.

5.3. Hard D-PHY Configuration Registers/Bits for Hard MIPI D-PHY IP

Table 5.3. Configuration Registers (MIPI Programmable Bits)

ADDR [5:0]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
0x00	HSEL RX High-Speed Select. [0] – Less than ≤ 1.5 Gbps [1] – Higher than 1.5 Gbps Default depends on the *RX Line Rate per Lane* attribute.	AUTO_PD_EN Powers down inactive lanes. [0] – Lanes are kept powered up and at LP11. [1] – Lanes powered down. Default is 1'b0.	PRIMARY_SECONDARY Selects the PHY IP configuration. [0] – Secondary [1] – Primary Default is 1'b0.	DSI_CSI Selects the PHY IP application. [0] – CSI2 [1] – DSI Default depends on the *Rx Interface Type* attribute.
0x01	RXCDRP[1:0][1] LP-CD threshold voltage. Default is 2'b01. Min – 200 mV, Max – 450 mV		RSEL Loop filter resistance selection. Set to 2'b01 for DPHY Tx, otherwise, set to 2'b00.	
0x02	EN_CIL Enables or disables CIL. [0] – CIL bypassed [1] – CIL enabled Default depends on the *CIL Bypass* attribute.	RXLPRP[2:0] [1] Adjusts the threshold voltage and hysteresis of LP-RX. Default setting is 3'b001.		
0x03	010[1]			DESKEW_EN Enables Deskew feature affects ERRSYNC/NOSYNC. [0] – Deskew disabled [1] – Deskew enabled Default depends on the *Enable Deskew Calibration Detection* attribute.

ADDR [5:0]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
0x09	Lane0_sel[0] (See MSB below at 0x0A)	RxDataWidthHS[1:0] High-Speed Receive Data Width Select. 2'b00 – 1/8 the HS bit rate 2'b01 – 1/16 the HS bit rate 2'b10 – 1/32 the HS bit rate Default depends on the *RX Gear* attribute.		0[1]
0x0A	uc_PRG_RXHS_SETTLE[0] (See MSB below at 0x0B)	cfg_num_lanes[1:0] Sets the number of active lanes. Value from 0 to 3. Default depends on the *Number of RX Lanes* attribute.		Lane0_sel[1] Determines which lane acts as data lane 0 in HS Operation mode. Value from 0 to 3. Default is 0x0.
0x0B	uc_PRG_RXHS_SETTLE[4:1] Bits used to program T_HS_SETTLE. For *clock* pin. *T_HS_SETTLE* = (*uc_PRG_RXHS_SETTLE* + 1) × (Tperiod of sync_clk_i) Default depends on the *CIL Clock Settle Cycle* attribute if *CIL Bypass* is unchecked. Otherwise, default value is 0x0.			
0x0C	000[1]			uc_PRG_RXHS_SETTLE[5] (See LSB above at 0x0B)
0x0F	u_PRG_RXHS_SETTLE[1:0] (See MSB below at 0x10)		00[1]	
0x10	u_PRG_RXHS_SETTLE[5:2] Bits used to program T_HS_SETTLE. For *data* pins. *T_HS_SETTLE* = (*u_PRG_RXHS_SETTLE* + 1) × (Tperiod of sync_clk_i) Default depends on the *CIL Data Settle Cycle* attribute if *CIL Bypass* is unchecked. Otherwise, default value is 0x0.			
0x1B	0010[2]			
0x1D	1000[2]			
0x1E	000[1]			cont_clk_mode Enables the clock lane of the secondary device to maintain HS reception state during continuous clock mode operation. [0] – Disabled [1] – Enabled Default depends on the *D-PHY Clock Mode* attribute.

Notes:

1. These bits must be set to the indicated value when writing to this register. Otherwise, the IP may malfunction.
2. This register defaults to the specified value when the data rate is ≤1.5 Gbps. For data rates >1.5 Gbps, the register is automatically set to 0x0. When writing to this register, the bits must be configured with the valid values indicated. Otherwise, the IP may malfunction.

6. Example Design

The CSI-2/DSI D-PHY Rx example design allows you to compile, simulate, and test the CSI-2/DSI D-PHY Rx IP on the following Lattice evaluation boards:

- Avant-E Evaluation Board (LAV-E70-EVN)
- CertusPro-NX Evaluation Board (LFCPNX-EVN)

6.1. Example Design Supported Configuration

The following IP configurations are used during the CSI-2/DSI D-PHY Rx IP Core IP generation. Other settings that are not specified in this table are set to default. This example design requires the CSI-2/DSI D-PHY Tx IP Core to have the same settings as the CSI-2/DSI D-PHY Rx IP Core.

Table 6.1. CSI-2/DSI D-PHY IP Configuration Supported by the Example Design

CSI-2/DSI D-PHY Rx IP GUI Parameter	CSI-2/DSI D-PHY Rx IP GUI Configuration
RX Interface Type	**CSI-2**, DSI
D-PHY RX IP	Soft D-PHY
Number of RX Lanes	1, 2, **4**
RX Gear	8
RX Line Rate per Lane (Mbps)	800
D-PHY Clock Mode	Continuous
Sync Clock Frequency (MHz)	100
Enable Packet Parser	Checked
Enable Miscellaneous Status Signals	Checked
RX_FIFO Enable	Checked
Type	PINGPONG
Implementation	EBR
Depth	512
Default FIFO Read Delay	8

6.2. Overview of the Example Design and Features

Key features of the example design are as follows:

- Byte generator
- Byte checker

Data is generated in the byte clock domain by the byte generator component and transmitted to the D-PHY Tx soft IP and byte checker simultaneously. D-PHY Tx converts byte data into MIPI traffic and loops-back to D-PHY Rx. D-PHY Rx converts back the MIPI traffic to byte domain and transmits to byte checker. Byte checker compares if the data received from D-PHY Rx and byte generator matches, and outputs an active high compare error signal when data mismatch is observed. All clocks required by the design are generated by the general PLL. Reference clock of the PLL is generated from the on-board oscillator.

6.3. Example Design Components

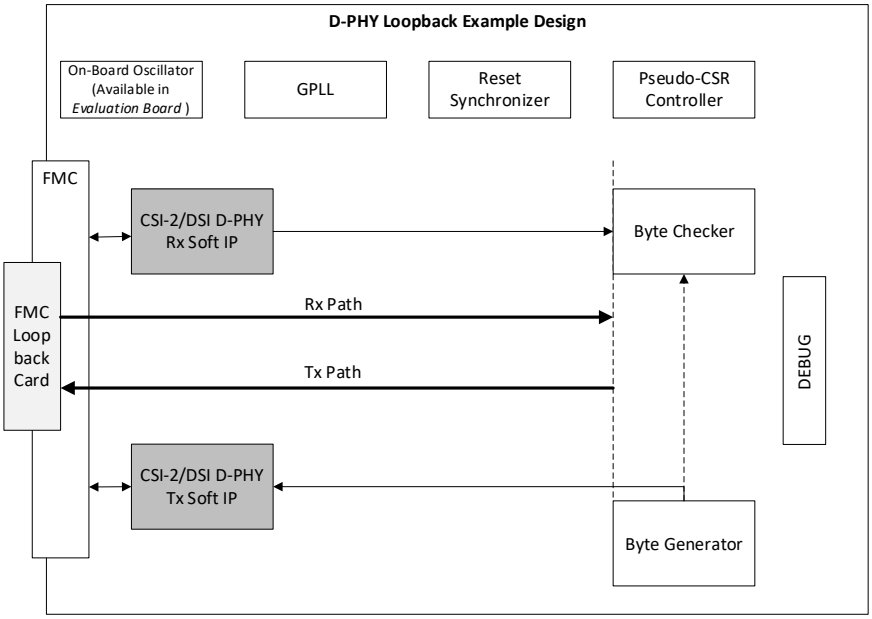

Figure 6.1. CSI-2/DSI D-PHY Tx to CSI-2/DSI D-PHY Rx Loopback Example Design Block Diagram

The example design includes the following blocks:

- Byte generator
- CSI-2/DSI D-PHY Tx soft IP
- CSI-2/DSI D-PHY Rx soft IP
- Byte checker
- General PLL
- Reset synchronizer

6.3.1. Byte Generator

This block generates data in byte domain and transmits to the CSI-2/DSI D-PHY Tx IP.

6.3.2. Byte Checker

This block receives byte data from byte generator and the CSI-2/DSI D-PHY Rx IP, and compares if data received matches.

6.3.3. CSI-2/DSI D-PHY Tx Soft IP

This block is the Lattice CSI-2/DSI D-PHY Tx soft IP, which serves as the MIPI Tx source.

6.3.4. CSI-2/DSI D-PHY Rx Soft IP

This block is the Lattice CSI-2/DSI D-PHY Rx soft IP, which receives MIPI traffic from the D-PHY Tx source.

6.3.5. PLL

This block generates the required clocks of the system.

6.3.6. Reset Synchronizer

This block synchronizes system reset into different clock domains.

6.4. Generating and Using the Example Design

You can use the Lattice Radiant software to generate and use the example design. A sample Lattice Radiant software project file for the Lattice Avant device is provided in the package. By using the sample project, you can run functional simulation, SW implementation flow, and hardware test.

Table 6.2. Example Design File List

Attribute	Description
eval/source	Contains all the design modules needed for example design implementation including testbench files for functional simulation.
eval/source/defines_avant.v	Contains the configuration and setting for the Lattice Avant device.
eval/source/defines_cpnx.v	Contains the configuration and setting for the Lattice CertusPro-NX device.
eval/sw/dphyrx_ip	Pre-generated CSI-2/DSI D-PHY Rx soft IP.
eval/sw/dphytx_ip	Pre-generated CSI-2/DSI D-PHY Tx soft IP.
eval/sw/pll_0_ip	Pre-generated general PLL soft IP.
eval/sw/dphy_loopback_ed1.sty	Sample Lattice Radiant software project strategy file.
eval/sw/post_syn_sys_avant.pdc	Sample post-synthesis constraint file in PDC format for the example design. Pin location constraints are pre-generated for the Avant Evaluation Board (LAV-E70-EVN) only.
eval/sw/post_syn_sys_cpnx.pdc	Sample post-synthesis constraint file in PDC format for the example design. Pin location constraints are pre-generated for the CertusPro-NX Evaluation Board (LFCPNX-EVN) only.
eval/sw/dphy_loopback_ed.rdf	Sample Lattice Radiant software project in RDF format.

6.4.1. Using the Example Design Sample Project

The sample project includes all the files required by the example design including the PDC file. To use the example design sample project, follow these steps:

1. Open the sample project provided: *eval/sw/dphy_loopback_ed.rdf*.

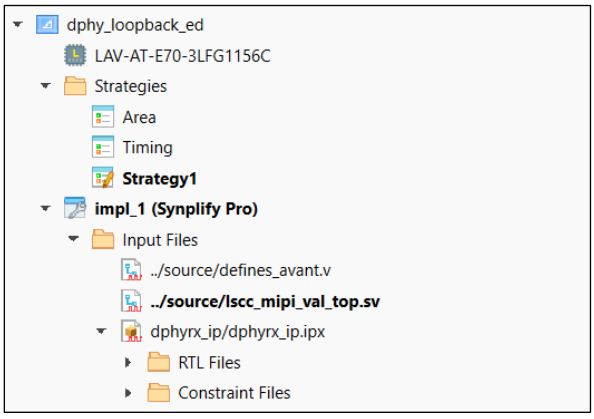

Figure 6.2. Sample File List

2. Click Run All to perform the Lattice Radiant software full design compilation, which generates the example design bitstream file for the hardware test.

6.4.2. Changing Configuration of the Example Design

To change to a different supported configuration of the example design, follow these steps:

1. Modify the compiler directives under *COMMON IP SETTING* in the defines_avant.v file and regenerate the soft IPs accordingly.

2. Update the *Generated IP Settings* section in the post_syn_sys_avant.pdc file and replace the file with the new settings. This ensures that the correct settings and constraints are applied during the implementation flow.

```
//-------------------------------------------------------------------------
// 3. COMMON IP SETTINGS
//-------------------------------------------------------------------------
`define FAMILY "LAV-AT"          // Device Family
`define FAM_LAVAT

`define DATA_RATE 800            // DPHY Rate (in Mbps)
//`define SKEWCAL_EN                //**** Comment out if data is <= 1500Mbps

// Gear selection (default: 8, uncomment for 16)
//`define GEAR_16

// Number of DPHY lanes (uncomment ONE only)
//`define NUM_LANE_1
//`define NUM_LANE_2
//`define NUM_LANE_3
`define NUM_LANE_4

// Protocol Formatter/Parser (comment out if bypassed)
`define PKT_MODE_ON              // Enable Protocol Formatter/Parser
```

Figure 6.3. Example IP Settings

```
#-------------------------------------------------------------------
# Generated IP Settings
#-------------------------------------------------------------------
# Extracted from constraint_eval.pdc of dphyrx_ip
set dphyrx_ip_device "LAV-AT-E70"
set dphyrx_ip_device_int "ap6a400ce"
set dphyrx_ip_package "LFG1156"
...

#-------------------------------------------------
# Extracted from constraint_eval.pdc of dphytx_ip
set dphytx_ip_device "LAV-AT-E70"
set dphytx_ip_device_int "ap6a400ce"
set dphytx_ip_package "LFG1156"
...
```

Figure 6.4. Example Generated IP Settings Section of the PDC File

You can change the configuration for the CertusPro-NX device by following the steps:

1. Change the project device to CertusPro-NX (LFCPNX-100-9LFG672C).
2. Replace the active defines_avant.v and post_syn_sys_avant.pdc files with the defines_cpnx.v and post_syn_sys_cpnx.pdc files respectively.
3. Regenerate all the IPs such as PLL, DPHY Rx, and DPHY Tx. For PLL, you need to create a new IP instance from IP Catalog with the same instance name, output frequency, and phase settings as for the Lattice Avant device.
4. Comment out FAM_LAVAT in *eval/source/defines_tb.v* and uncomment FAM_LFCPNX.

You must have a thorough understanding of the effect of any modification to modify the settings of the example design project provided. The example design works only when using the supported and pre-generated settings for the specific device stated.

6.5. Simulating the Example Design

To run the functional simulation, follow these steps:

1. Make sure that testbench file tb_top.sv is included in the **Input Files** section. Set the file to include in Simulation only, as shown in the following diagram.

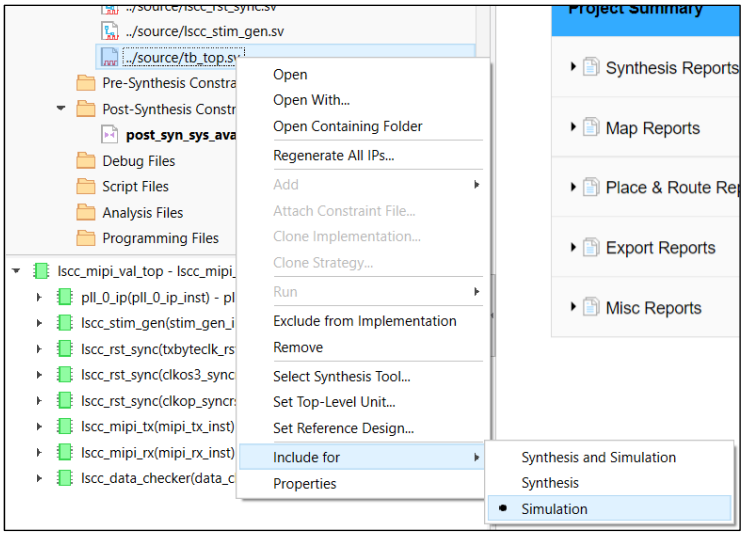

Figure 6.5. Testbench Top File

2. Click the  button located on the **Toolbar** to initiate the **Simulation Wizard** shown in the following diagram.

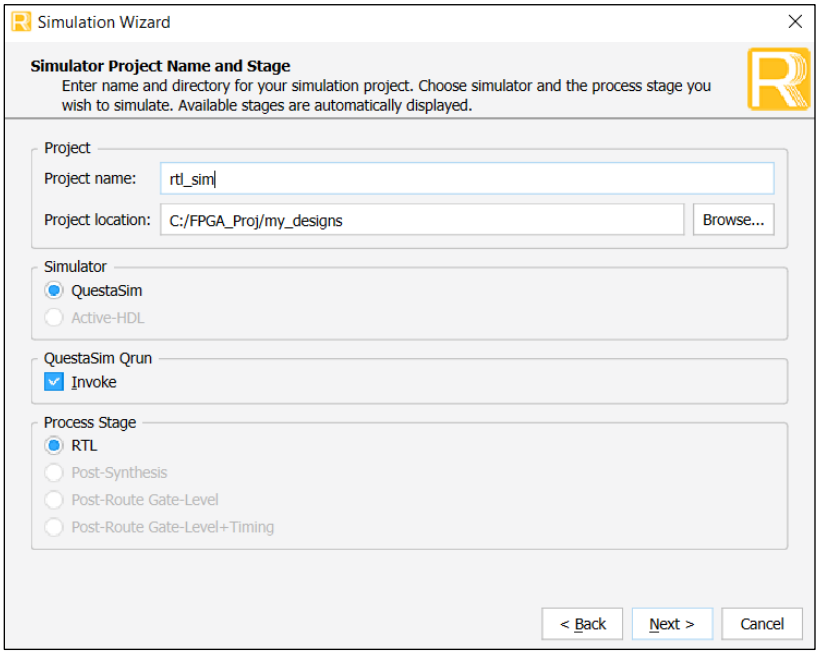

Figure 6.6. Simulation Wizard GUI

3. Click **Next** to open the **Add and Reorder Source** window.
4. Click **Next**. The **Summary** window opens.
5. Set **Run Simulation** to 0 to ensure the simulation runs completely. Click **Finish** to run the simulation.

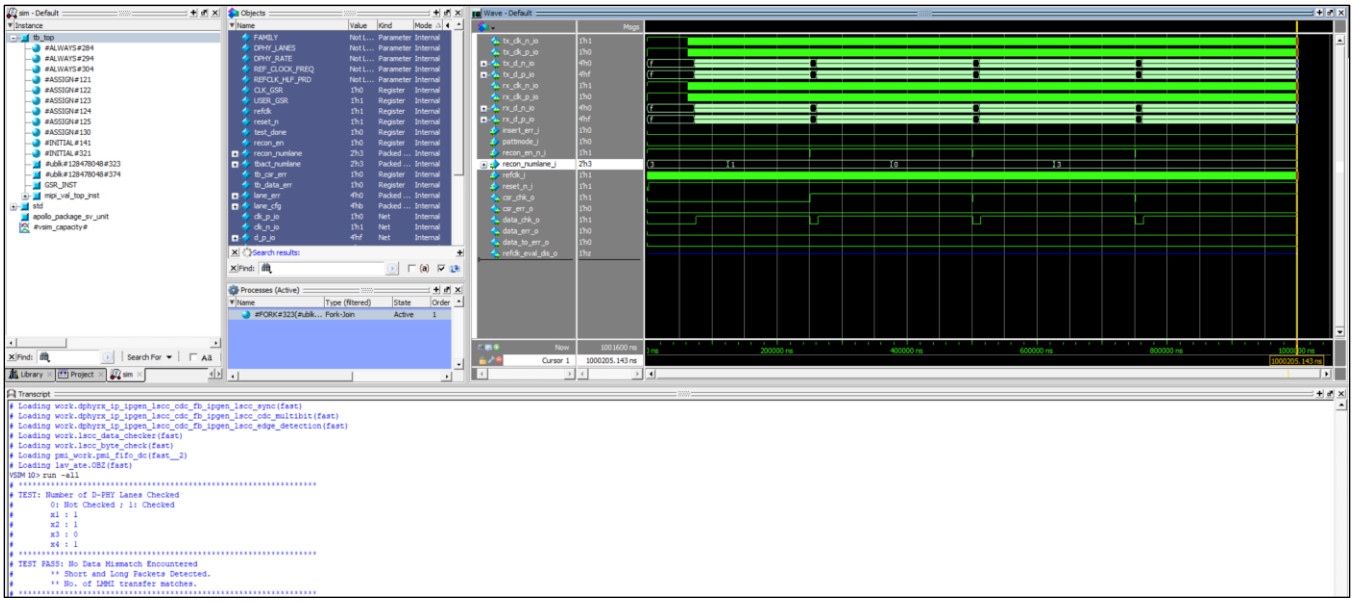

Figure 6.7. Simulation Result

If compilation error is encountered because of missing compiler directives, you can try adding the argument *mfcu* in the original QRUN command.

```
qrun -f "<filelist_path>" -mfcu
```

Figure 6.8. Sample QRUN Command with MFCU Argument

If you want to run gate-level simulations, uncomment the GATE_SIM compiler directive in the *eval/source/defines_tb.v* file.

```
//-- Define when running Gate-level simulations
`define GATE_SIM
```

Figure 6.9. Gate-Level Simulation Example Design Compiler Directive

The duration of the simulation depends on the mode selected.

By default, dynamic lane reconfiguration is enabled in the pre-generated example design through the compiler directive RECON_EN, which is defined in the device-specific defines file located in *eval/source/*.

When this feature is active, the testbench automatically cycles through the supported lane configurations in descending order, then returns to the original setting. For instance, in a pre-compiled 4-lane configuration, the test sequence proceeds as follows:

1. x4 lanes
2. x2 lanes
3. x1 lane
4. x4 lanes

6.6. Hardware Testing

The generated bitstream from the procedure in the Generating and Using the Example Design section is downloaded to the evaluation boards using the Lattice Radiant Programmer. You need an external FMC Loopback Card for the D-PHY Tx to D-PHY Rx loopback connection.

If you use the Avant-E Evaluation Board (LAV-E70-EVN), the following jumper settings are required:

- JP36: close (V_{CCIO6} = 1.8 V)
- JP61: close (V_{CCIO7} = 1.2 V)

You also need to make sure that DIP_SW3 (insert_err_i) is positioned towards ON (1'b0).

If the design is generated successfully, LED D22 lights up and LED D23 is off as shown in the following figures.

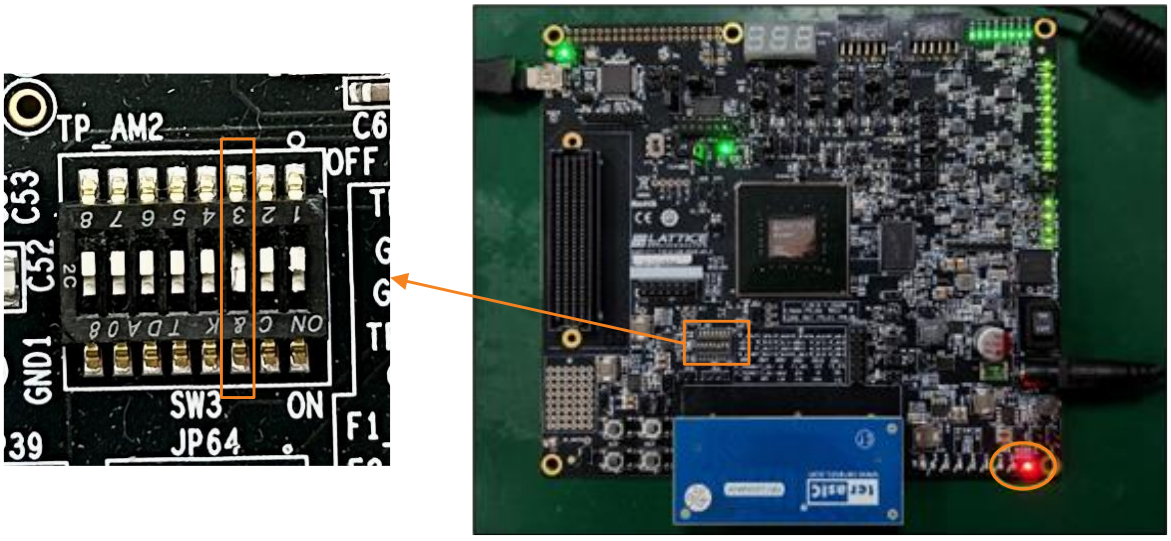

Figure 6.10. Avant-E Evaluation Board with Terasic® FMC Loopback Card on FMC2 Connector (J54)

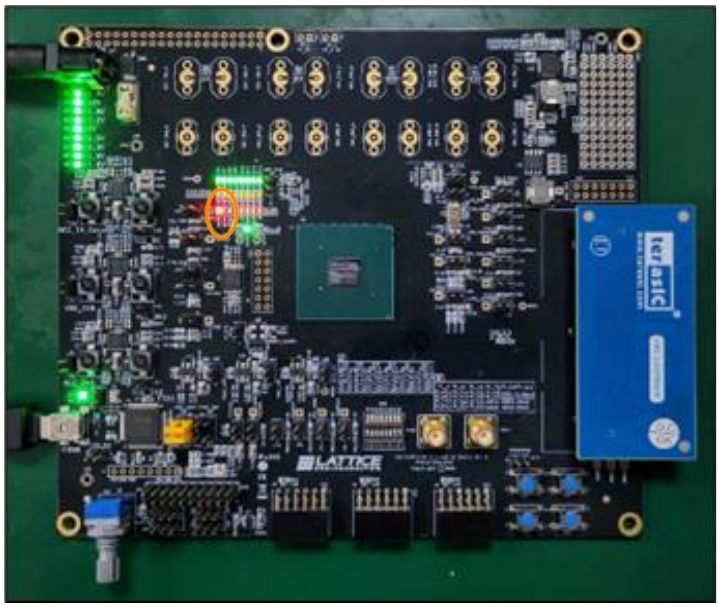

Figure 6.11. CertusPro-NX Evaluation Board with FMC Loopback Card on FMC Connector (J48)

To perform dynamic lane reconfiguration in hardware, follow these steps:

1. After the initial bitstream loading, position DIP_SW6 (recon_numlane_i[1]) and DIP_SW5 (recon_numlane_i[0]) to the desired number of lanes. Positioning DIP_SW towards the ON position corresponds to logic level 1'b0.
   - x1 Lane: {DIP_SW6, DIP_SW5} == 2'b00
   - x2 Lane: {DIP_SW6, DIP_SW5} == 2'b01
   - x3 Lane: {DIP_SW6, DIP_SW5} == 2'b10
   - x4 Lane: {DIP_SW6, DIP_SW5} == 2'b11

   Example: To configure from x4 lane (pre-compiled configuration) to x2 lane (dynamic lane reconfiguration setting), set {DIP_SW6, DIP_SW5} to 2'b01 as shown below.

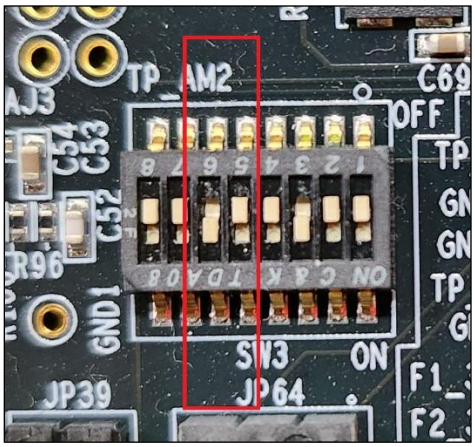

Figure 6.12. DIP_SW Setting to Two Lanes

2. Trigger lane reconfiguration by pressing and releasing recon_en_n_i pushbutton (SW4 for Avant-E Evaluation Board and SW5 for CertusPro-NX Evaluation Board). Pressing and releasing the pushbutton automatically performs the dynamic lane reconfiguration sequence described in the Dynamic Reconfiguration section.
3. If reconfiguration is done successfully, LED D22 and LED D25 light up, while LED D23, LED D24, and LED D26 are off as shown in the following figure.

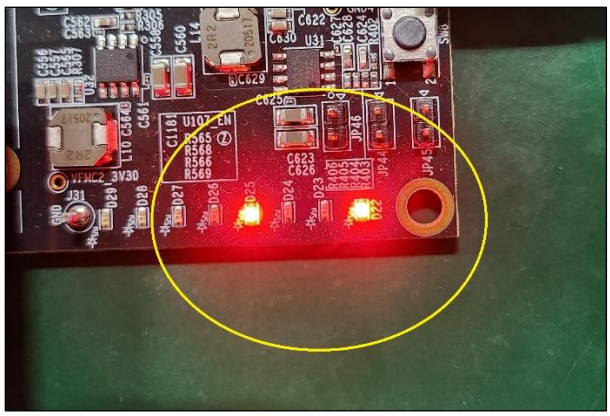

Figure 6.13. Avant-E Evaluation Board LED Status for Successful Lane Reconfiguration

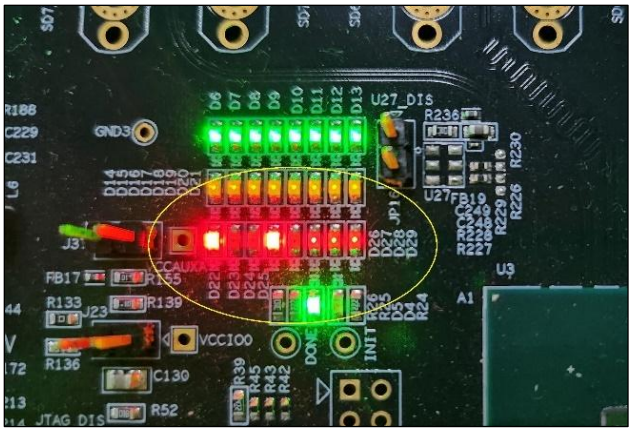

Figure 6.14. CertusPro-NX Evaluation Board LED Status for Successful Lane Reconfiguration

The corresponding LED lights up, indicating the following checker results:

- LED D22 – Data check valid
- LED D25 – CSR check valid

If there are errors, the corresponding LED lights up indicating the following errors:

- LED D23 – Data compare mismatch
- LED D24 – CSR compare mismatch
- LED D26 – Timeout

The IP must be compiled with the maximum intended lane width to ensure proper functionality of dynamic lane reconfiguration across all supported configurations.

7. Designing with the IP

This section provides information on how to generate the IP Core using the Lattice Radiant software and how to run simulation and synthesis. For more details on the Lattice Radiant software, refer to the Lattice Radiant Software User Guide.

Note: The screenshots provided are for reference only. Details may vary depending on the version of the IP or software being used. If there have been no significant changes to the GUI, a screenshot may reflect an earlier version of the IP.

7.1. Generating and Instantiating the IP

You can use the Lattice Radiant software to generate IP modules and integrate them into the device architecture. To generate the D-PHY Rx IP in the Lattice Radiant software, follow these steps:

1. Create a new Lattice Radiant software project or open an existing project.
2. In the **IP Catalog** tab, double-click **CSI-2/DSI D-PHY Receiver** under **IP, Audio_Video_and_Image_Processing** category. The **Module/IP Block Wizard** opens as shown in Figure 7.1. Enter values in the **Component name** and the **Create in** fields and click **Next**.

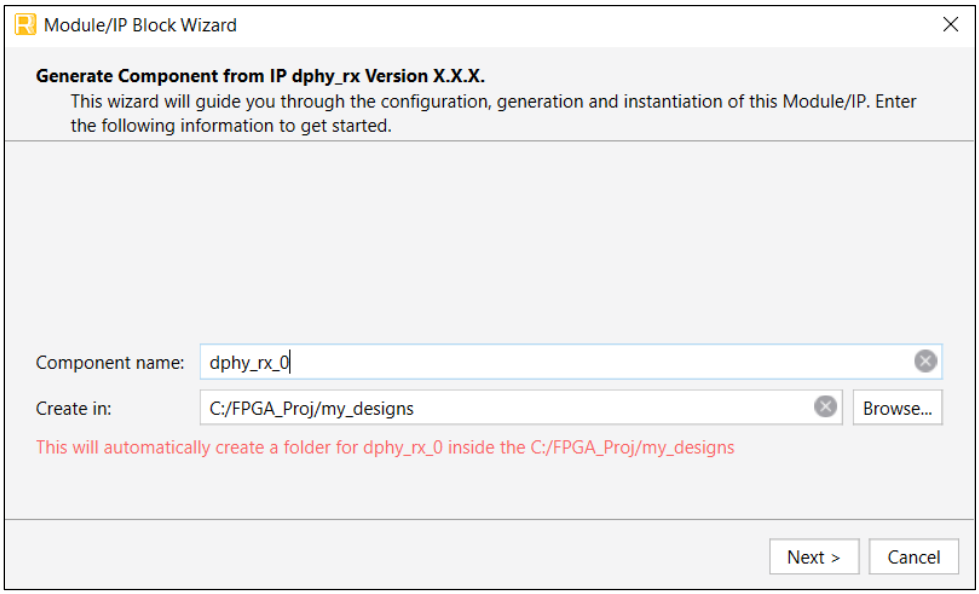

Figure 7.1. Module/IP Block Wizard

3. In the next **Module/IP Block Wizard** window, customize the selected CSI-2/DSI D-PHY Receiver IP using drop-down lists and check boxes. Figure 7.2 shows an example configuration of the CSI-2/DSI D-PHY Receiver IP. For details on the configuration options, refer to the IP Parameter Description section.

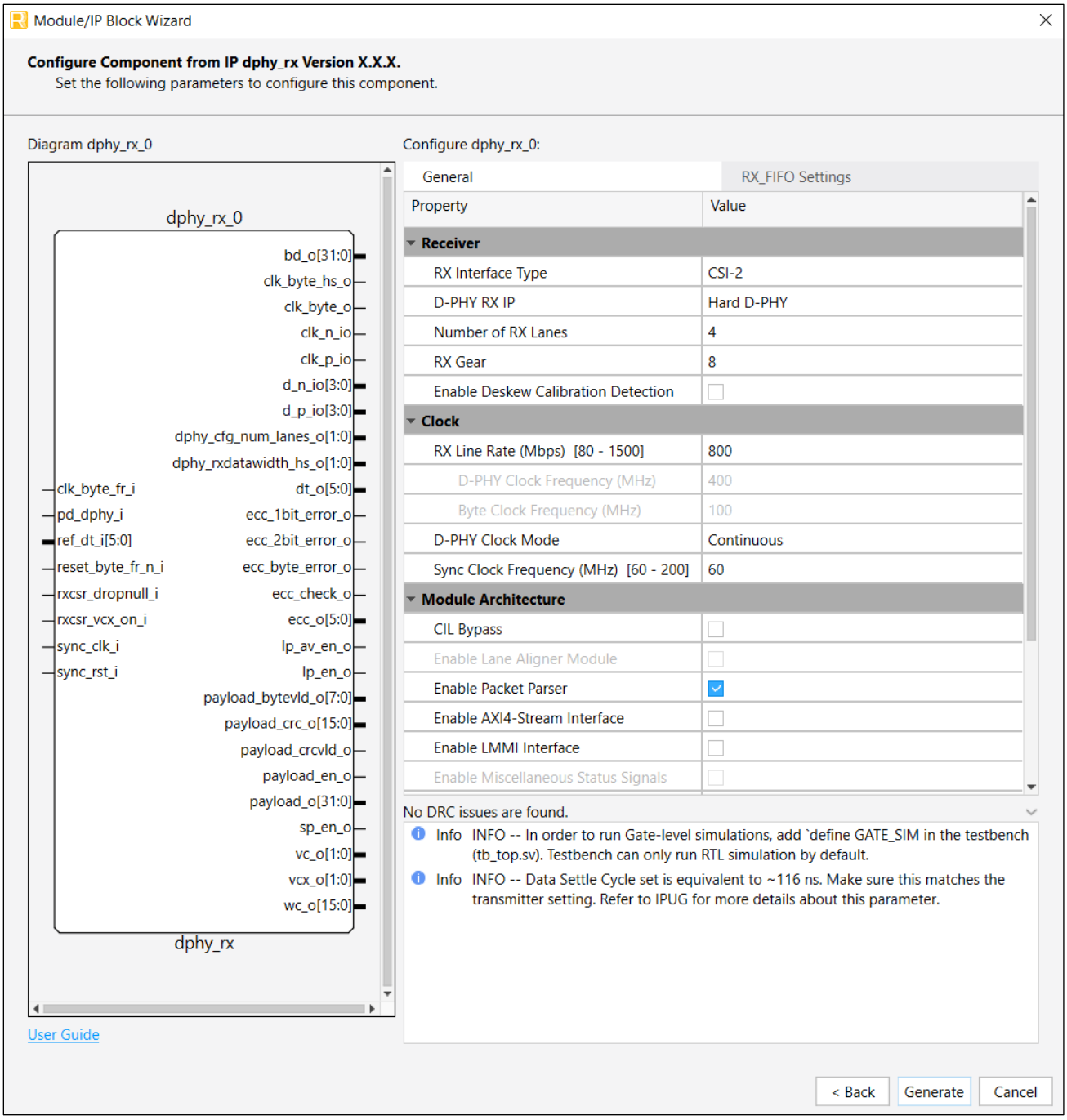

Figure 7.2. IP Configuration

4. Click **Generate**. The **Check Generated Result** dialog box opens, showing design block messages and results as shown in Figure 7.3.

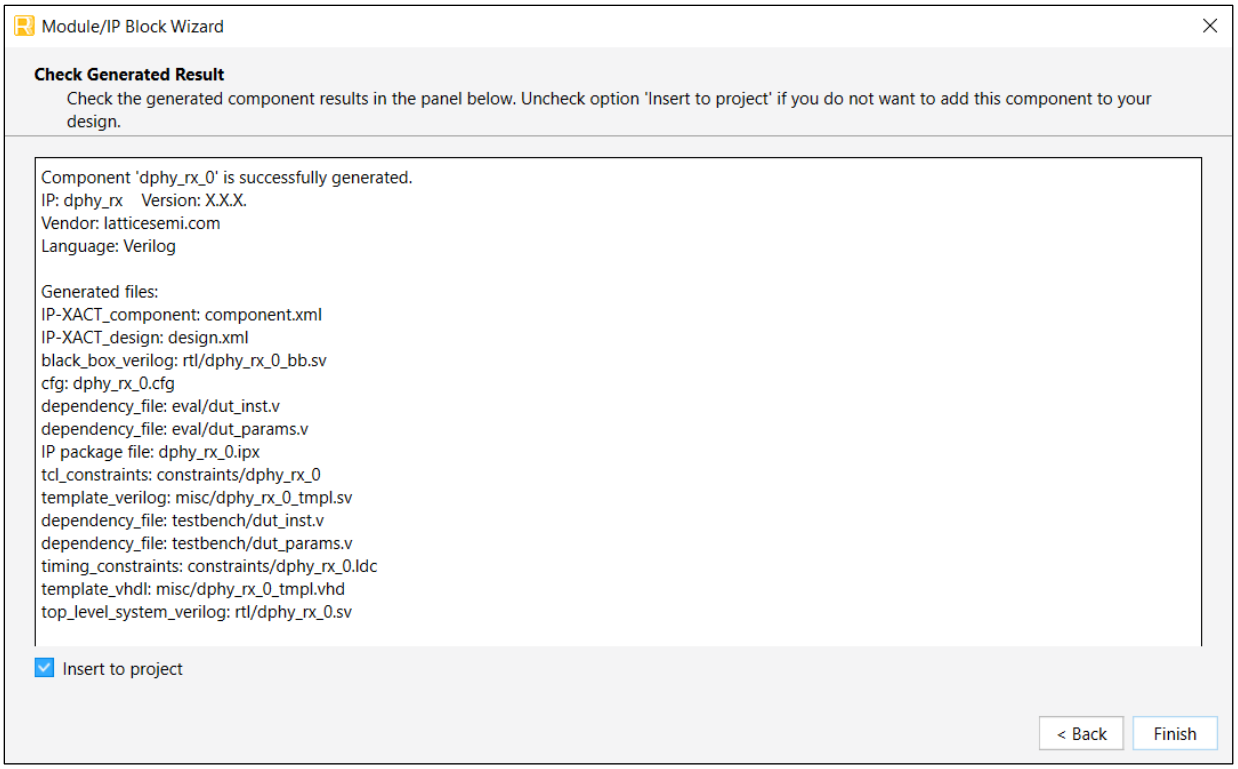

Figure 7.3. Check Generated Result

5. Click **Finish**. All the generated files are placed under the directory paths in the **Create in** and the **Component name** fields shown in Figure 7.1.

7.1.1. Generated Files and File Structure

The generated CSI-2/DSI D-PHY Receiver module package includes the closed-box (*<Component name>_bb.v*) and instance templates (*<Component name>_tmpl.v/vhd*) that can be used to instantiate the core in a top-level design. An example RTL top-level reference source file (*<Component name>.sv*) that can be used as an instantiation template for the module is also provided. You may also use this as the starting template for the top-level for your complete design. The generated files are listed in Table 7.1.

Table 7.1. Generated File List

Attribute	Description
<Component name>.ipx	This file contains the information on the files associated to the generated IP.
<Component name>.cfg	This file contains the parameter values used in IP configuration.
component.xml	Contains the ipxact:component information of the IP.
design.xml	Documents the configuration parameters of the IP in IP-XACT 2014 format.
rtl/<Component name>.sv	This file provides an example RTL top file that instantiates the module.
rtl/<Component name>_bb.v	This file provides the synthesis closed-box.
misc/<Component name>_tmpl.v misc /<Component name>_tmpl.vhd	These files provide instance templates for the module.

An evaluation wrapper file (*eval/eval_top.sv*) that instantiates the reference source file is also generated. This file provides an example wrapper file that can be used for evaluation purposes.

7.2. Design Implementation

Completing your design includes additional steps to specify analog properties, pin assignments, and timing and physical constraints. You can add and edit the constraints using the Device Constraint Editor or by manually creating a PDC File.

Post-Synthesis constraint files (.pdc) contain both timing and non-timing constraint .pdc source files for storing logical timing/physical constraints. Constraints that are added using the Device Constraint Editor are saved to the active .pdc file. The active post-synthesis design constraint file is then used as input for post-synthesis processes.

Refer to the relevant sections in the Lattice Radiant Software User Guide for more information on how to create or edit constraints and how to use the Device Constraint Editor.

7.3. Timing Constraints

The CSI-2/DSI D-PHY Receiver IP generates the following constraint files:

- A legacy pre-synthesis constraint file in LDC format (*<ip_instance_path>/constraints/<instance_name>.ldc*) that is automatically used and propagated by the SW tool.
- A constraint file in SDC format (*<ip_instance_path>/constraints/constraint.sdc*) that contains both pre-synthesis and post-synthesis IP constraints. These constraints are automatically used and propagated by the software tool starting from the Lattice Radiant software version 2024.1. These constraints can be modified if you have a thorough understanding of the effect of each constraint.
- An evaluation post-synthesis constraint file in PDC format (*<ip_instance_path>/eval/constraint_eval.pdc*). In this constraint file, sections 1 and 2 are for evaluation purposes and can be used as a starting point for constraints of the system-level design. You must define the correct clock targets based on your design.

```
#-------------------------------------------------------------------------------
# GENERAL NOTES
#
# This file contains 2 sections:
#
# Section 1: Settings
#   This section is provided to complement Section 2. This is for evaluation
#   purposes only. You must define the correct clock targets based on system-
#   level design.
#
# Section 2: Evaluation Part
#   This section is provided for evaluation purposes only of the IP and should
#   be used to give you starting point for constraints of the system-level
#   design. You need to provide proper timing and physical design constraints
#   to ensure that your design meets the desired performance goals on the FPGA.
#
#-------------------------------------------------------------------------------
```

Figure 7.4. Header of Generated Evaluation PDC File

To run the software implementation flow using the provided evaluation file after the IP is generated, follow these steps:

1. In the **Input Files** section of Lattice Radiant software project, add the evaluation wrapper file *<ip_instance_path>/eval/eval_top.sv*.
2. In the **Post-Synthesis Constraint Files** section, add *<ip_instance_path>/eval/constraint_eval.pdc*.
3. Run the implementation flow.

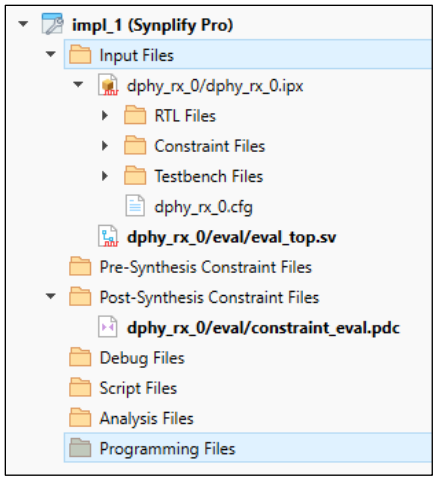

Figure 7.5. Example Evaluation Project Settings

Notes:

- You need to provide proper timing and physical design constraints to ensure that your design meets the desired performance goals for the FPGA.
- The constraint files have been verified during IP evaluation with the evaluation wrapper instantiated directly in the top-level module. The remaining unconstrained paths in the evaluation report are for the input and output delay constraints of the top-level ports of the IP. These ports are expected to be driven and utilized in FPGA fabric and not mapped to FPGA I/O in your system-level design.
- During synthesis, you can ignore clock related warnings as the evaluation IP does not include clock-related constraints at pre-synthesis level.
- During post-synthesis, there may be warnings related to dropped constraints. As the IP supports many configurations and parameter combinations, some default constraints may not be applicable to the selected configuration.

Refer to Lattice Radiant Timing Constraints Methodology for details on how to constrain your design.

7.4. Physical Constraints

For Soft D-PHY mode, define the MIPI pins (clk_p_i, d_p_io_*) with IO_TYPE of MIPI_DPHY in the .pdc file. An example is shown in Figure 7.6.

```
284 ldc_set_port -iobuf {IO_TYPE=MIPI_DPHY} [get_ports clk_p_i]
285 ldc_set_port -iobuf {IO_TYPE=MIPI_DPHY} [get_ports {d_p_io[*]}]
```

Figure 7.6. Defining MIPI DPHY Port Pins Using MIPI_DPHY IO_TYPE

7.5. Specifying the Strategy

The Lattice Radiant software provides two predefined strategies: Area and Timing. The software also enables you to create customized strategies. For details on how to create a new strategy, refer to the Strategies section of the Lattice Radiant Software user guide.

7.6. Running Functional Simulation

An example simulation environment is provided after you generate the IP. You can find the files in *<ip_instance_path>/testbench/*. This example environment supports limited testing features as the primary intent is to provide a starting point on checking the functionality of the IP. Official IP verification is done through Universal Verification Methodology (UVM).

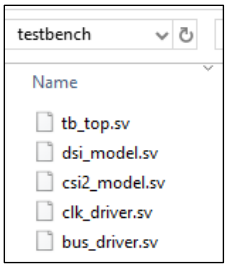

Figure 7.7. Example Simulation Environment File Directory

Default simulation environment instantiates the generated IP *<ip_instance_path>/rtl/<Component name>.sv* as DUT. To instantiate the DUT with the evaluation wrapper file *<ip_instance_path>/eval/eval_top.sv* as top, uncomment the USE_EVAL_TOP_DUT compiler directive on top of the tb_top.sv file.

```
// Testbench Local Settings
// Selects which DUT to instantiate in the testbench.
// When USE_EVAL_TOP_DUT is defined, testbench instantiates eval_top
// as DUT. Otherwise, testbench instantiates the generated IP (IPX).
`define USE_EVAL_TOP_DUT
```

Figure 7.8. Adding USE_EVAL_TOP_DUT in the tb_top.sv File

To run functional simulation, follow these steps:

1. Add testbench file *tb_top.sv* in the **Input Files** section. Set the file to include in Simulation only, as shown in the following diagram.

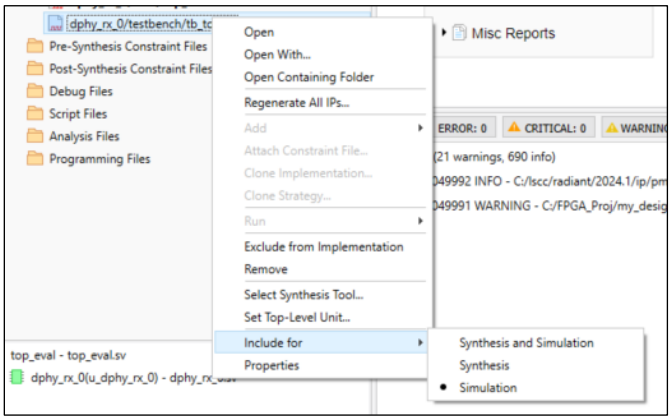

Figure 7.9. Example Steps on How to Include File for Simulation Only

2. Click the  button located on the **Toolbar** to initiate the **Simulation Wizard** shown in the following diagram.

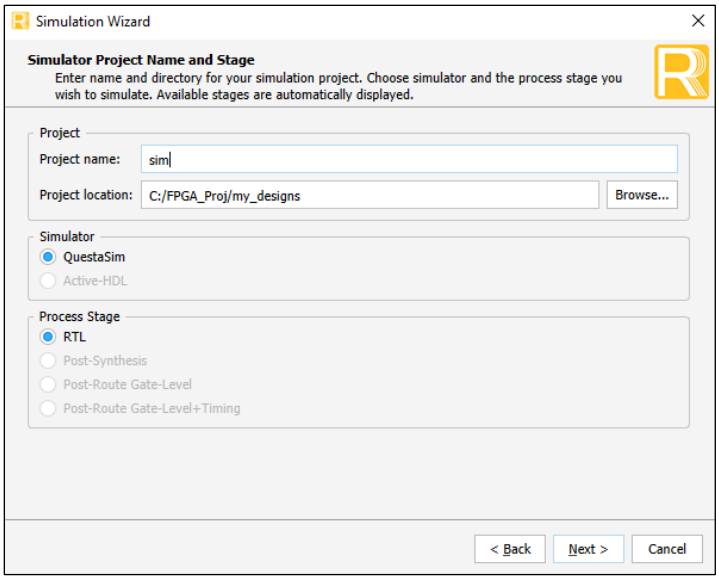

Figure 7.10. Simulation Wizard

3. Click **Next** to open the **Add and Reorder Source** window as shown in the following diagram.

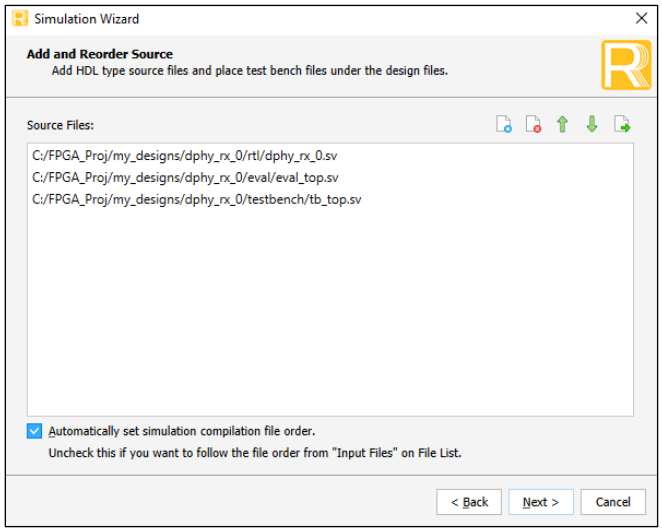

Figure 7.11. Add and Reorder Source

4. Click **Next**. The **Summary** window opens.
5. Set **Run Simulation** to 0 to ensure the simulation runs completely. Click **Finish** to run the simulation.

The waveform in the following figure shows an example simulation result.

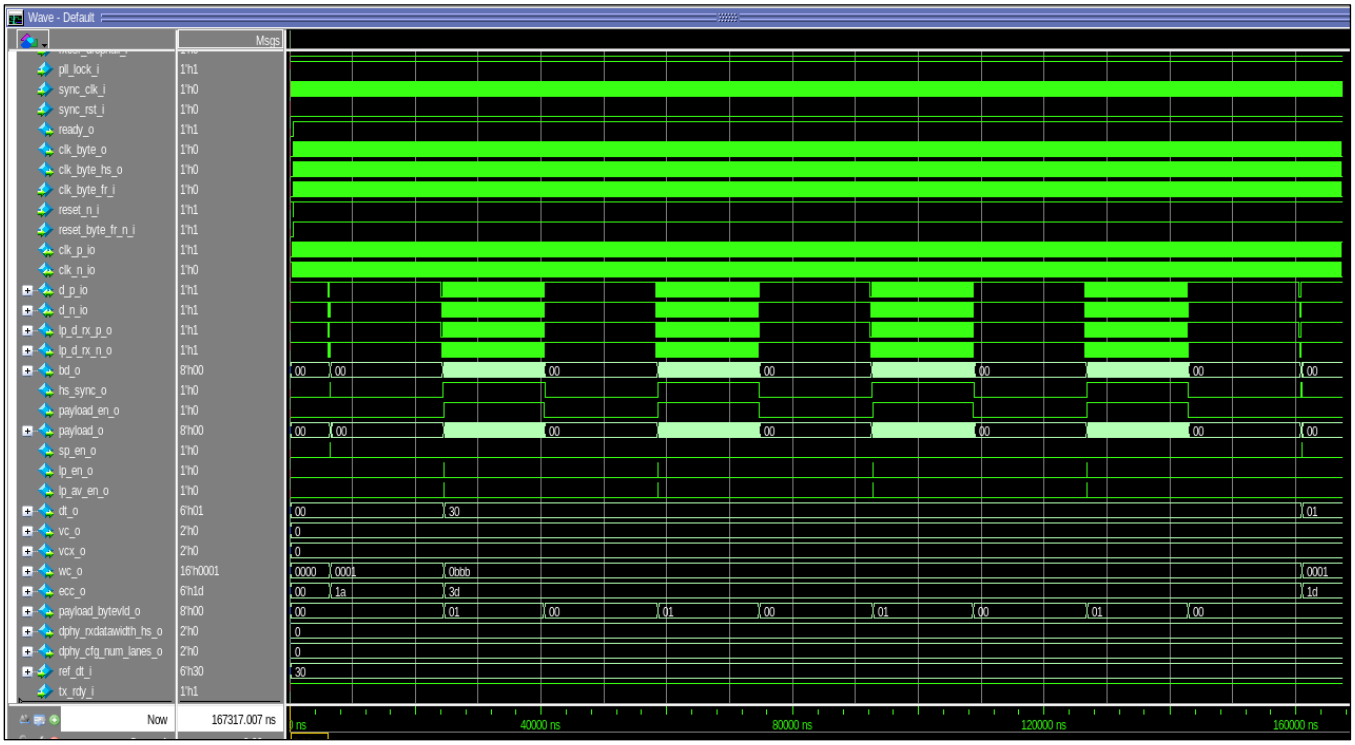

Figure 7.12. Simulation Waveform

7.6.1. Simulation Results

When the simulation is complete, the output in the Transcript window is shown in the following figure.

```
# Start of data comparing
# End of data comparing
# ***PAYLOAD DATA PASS***
# **SIMULATION PASSED**
# All data received and transmitted
# Test end
```

Figure 7.13. Passing Simulation Log

If your simulation failed, ensure that the reset signals and clock signals are set up as described in the Functional Description section. You can also enable the Miscellaneous status signals and the FIFO Misc signals to debug the functional simulation.

If you want to run gate-level simulations, uncomment the GATE_SIM compiler directive on top of the *tb_top.sv* file.

```
// Define if intended to run Gate-level simulations. Leave commented out if
// running RTL sim.
`define GATE_SIM
```

Figure 7.14. Adding GATE_SIM in the tb_top.sv File

For Lattice Avant devices with *RX Line Rate per Lane ≥ 1000 Mbps*, simulation time is significantly longer (can be > 40 ms) as the testbench is waiting for the edgemon_done_o signal to assert before doing any data comparison.

8. Debugging

This section lists the possible issues and the suggested troubleshooting steps.

8.1. Debug Methods

8.1.1. Geared Down D-PHY Clock (clk_byte_hs_o) Does Not Toggle

In non-continuous clock mode, clk_byte_hs_o toggles only during high-speed transmission on the MIPI D-PHY data lanes. In continuous clock mode, this output clock toggles continuously.

When this clock does not toggle as expected, check to ensure the upstream source (camera sensors, application processors, and so on) is alive. Verify that the upstream device configuration matches with the IP parameters settings (for example, clock mode, bit rates). Set up all the input clocks and reset signals going into the IP module as recommended.

8.1.2. Corrupted Output Data Packet

If you suspect corruption on the output data packets, follow these guidelines:

- Set the Data Settle Cycle per the range and equation in Table 3.1.
- Check the packet headers against the transmitted packet.
  - Example: Check if the word count in the packet header matches the number of clock cycle of payload_en_o = high.
- Configure the RX FIFO as recommended. Ensure the FIFO is full and FIFO is empty flags are not asserted during the high-speed transaction.

8.2. Debug Tools

You can use the tool described in the subsection to debug the CSI-2/DSI D-PHY Receiver IP design issues.

8.2.1. Reveal Analyzer

The Reveal™ Analyzer continuously monitors signals within the FPGA for specific conditions that range from simple to complex conditions. When the trigger condition occurs, the Reveal Analyzer saves signal values preceding, during, and following the event for analysis, including a waveform presentation. The data can be saved in the following format:

- Value change dump file (.vcd) that can be used with tools such as QuestaSim™.
- ASCII tabular format that can be used with tools such as Microsoft® Excel.

Before running the Reveal Analyzer, use the Reveal Inserter to add Reveal modules to your design. In these modules, specify the signals to monitor, define the trigger conditions, and set other preferred options. The Reveal Analyzer supports multiple logic analyzer cores using hard/soft JTAG interface. You can have up to 15 modules, typically one for each clock region of interest. When the modules are set up, regenerate the bitstream data file to program the FPGA.

During debug cycles, this tool uses a divide and conquer method to narrow down the problem areas into many small functional blocks to control and monitor the status of each block.

Refer to Reveal User Guide for Radiant Software for details on how to use the Reveal Analyzer.

Consider setting up triggers with the following signals:

- Start-of-Transmission pattern (SoTp) on the bd_o output pins.
- Transitions on the enable signals, such as payload_en_o, sp_en_o, lp_en_o, lp_en_av_o.
- Transitions on the Miscellaneous status flags and FIFO Misc flags.

9. Design Considerations

9.1. Design Considerations in Continuous Clock Mode

- Ensure the clock mode, bit rate, and number of lanes matches between the IP and the upstream devices.
- Synchronize the synchronized reset signals to the respective clock domains. Refer to the User Interfaces section.
- Ensure the Data Settle Cycle is within MIPI D-PHY specifications and IP range. Refer to the Data Settle Cycle attribute in Table 3.1.
- Drive clk_byte_fr_i clock pin from the clk_byte_hs_o clock pin. Refer to the User Interfaces section.
- Set the RX FIFO to OFF. Refer to the RX_FIFO OFF section.
- Ensure that the minimum duration requirement for tLPX, tHS-TRAIL, tHS-PREPARE + tHS-ZERO from the D-PHY source is met. Adjust timing parameters as needed. Refer to the Limitations section.

9.2. Design Considerations in Non-Continuous Clock Mode

- Ensure the clock mode, bit rate, and number of lanes matches between the IP and the upstream devices.
- Synchronize the synchronized reset signals to the respective clock domains. Refer to the User Interfaces section.
- Ensure the Data Settle Cycle is within MIPI D-PHY specifications and IP range. Refer to the Data Settle Cycle attribute in Table 3.1.
- If possible, generate a clock either from a PLL or OSC to drive clk_byte_fr_i pin that matches the frequency of the clk_byte_hs clock. Refer to the User Interfaces section.
- If the clk_byte_fr and clk_byte_hs clock frequencies match, generate the minimum depth of a single RX FIFO with the smallest number of packet delay. Refer to the RX_FIFO_TYPE = SINGLE section.
- Determine the Low Power Blanking period from the upstream device and choose a suitable RX FIFO with the appropriate parameters. Refer to the RX_FIFO section.
- Ensure that the minimum duration requirement for tLPX, tHS-TRAIL, tHS-PREPARE + tHS-ZERO from the D-PHY source is met. Adjust timing parameters as needed. Refer to the Limitations section.

9.3. Limitations

- AXI4-Stream interface does not support back-pressure.
- Escape Mode, Ultra Low Power State (ULPS), and Bus Turnaround sequences are not yet supported.
- For Lattice Avant devices, packets may be missing after a local system reset is performed because of the current design limitation of using the delay block.
- The IP only supports even word count for multiple DSI packets transmitted within a single HS transmission, including EoTp, Null and Blanking (when *DSI Back-to-Back HS Packets* == *ON*).
- When *DSI Back-to-Back HS Packets* == *ON*, ECC and CRC checks are not supported.
- When *D-PHY RX IP* == *Soft D-PHY* or *CIL Bypass* is checked, follow these guidelines:
  - To ensure proper detection of the Start-of-Transmit pattern, the minimum duration of the tHS-PREPARE + tHS-ZERO from D-PHY source must satisfy the following condition:

    $$t_{HS-PREPARE} + t_{HS-ZERO} \geq 145\ ns + 10\ \text{UI} + \max(X, Y)$$

    Where:
    - $X = 2 \times TCLK\_BYTE$, if the corresponding byte clock is ≤ 30 MHz, otherwise $X = 0$
      TCLK_BYTE is clk_byte_o for Soft D-PHY and clk_byte_fr_i for Hard D-PHY with CIL bypassed.
    - $Y = 8 \times TCLK\_SYNC$, if D-PHY RX IP == Soft D-PHY, otherwise $Y = 0$
      TCLK_SYNC is sync_clk_i.
  - When *D-PHY RX IP* == *Soft D-PHY* and the corresponding byte clock is ≤ 60 MHz, you must configure tHS-TRAIL duration closer to the upper limit as defined by the MIPI D-PHY specification. This ensures reliable data capture and proper end-of-transmission detection under low-frequency conditions.
  - For lower data rates, ensure the duration of tLPX and tHS-TRAIL is longer than the clk_byte_fr_i period with at least 1.5× duration.

- Some configurations may fail Static Timing Analysis when compiling your design using LSE, especially when used in devices with slow speed grade. If this happens, consider compiling your design using the Synopsis Synplify Pro. The following Fmax value is approximates and may vary depending on the system-level design:
  - Nexus devices: 177 MHz for Gear 8
- In Soft D-PHY, when *Enable Deskew Calibration Detection* == checked, the full flag signal of the internal buffer (for example, RX FIFO) may assert when deskew calibration sequence is received. This behavior is because of a current limitation where the deskew calibration sequence shares the same buffer as video packets. The assertion can be safely ignored as the assertion is automatically cleared after a few clock cycles.

Appendix A. Resource Utilization

The following tables show the maximum frequency and resource utilization for a certain IP configuration.

Table A.1. Device and Tool Tested

—	Value
Software Version	Lattice Radiant software 2025.2 production build
Device Used	LIFCL-40-9BG400C
Performance Grade	9_High-Performance_1.0V
Synthesis Tool	Synplify Pro® W-2025.03LR-SP1-Beta2, Build 038R, Oct 2 2025

Table A.2. Resource Utilization[1]

Lane (Gear)	RX Interface Type	IP Type	Bit Rate (Lane)	Parser	AXI Bus	LMMI Bus	Registers	Fmax (MHz)	LUT[2]	EBR	High-Speed I/O Resources
4(8)	CSI-2	Soft D-PHY	1000 Mbps	EN	EN	DIS	789	200	1141	2	4 x IDDRX4, 1 x ECLKDIV, 1 x ECLKSYNC
4(8)[3]	CSI-2	Soft D-PHY	1500 Mbps	EN	DIS	DIS	762	200	1293	2	4 x IDDRX4, 1 x ECLKDIV, 1 x ECLKSYNC
4(8)	DSI	Soft D-PHY	1500 Mbps	EN	DIS	DIS	791	200	1305	2	4 x IDDRX4, 1 x ECLKDIV, 1 x ECLKSYNC
4(16)	DSI	Hard D-PHY[4]	2000 Mbps	EN	EN	EN	1232	200	1251	8	1 x Hard D-PHY
4(8)	DSI	Hard D-PHY[4]	1200 Mbps	EN	EN	DIS	468	200	403	4	1 x Hard D-PHY
2 (8)	DSI	Hard D-PHY[4]	800 Mbps	EN	DIS	DIS	321	200	435	2	1 x Hard D-PHY
4(16)[3]	CSI-2	Hard D-PHY[4]	2500 Mbps	EN	DIS	EN	1104	200	1326	8	1 x Hard D-PHY
4(8)[3]	CSI-2	Hard D-PHY[4]	1500 Mbps	EN	DIS	EN	976	200	1230	4	1 x Hard D-PHY
2(8)	CSI-2	Hard D-PHY[4]	800 Mbps	EN	DIS	DIS	295	200	356	2	1 x Hard D-PHY

Notes:

1. All other settings are default.
2. The *distributed RAM* utilization is accounted for in the total LUT4s utilization. The actual LUT4 utilization is distribution among *logic*, *distributed RAM*, and *ripple logic*.
3. Data Settle settings change in these configurations to match the target bit rate per lane.
4. Hard D-PHY – CIL Enabled.

Table A.3. Device and Tool Tested

—	Value
Software Version	Lattice Radiant software 2025.2 production build
Device Used	LIFCL-40-7BG400I
Performance Grade	7_High-Performance_1.0V
Synthesis Tool	Synplify Pro® W-2025.03LR-SP1-Beta2, Build 038R, Oct 2 2025

Table A.4. Resource Utilization[1,6]

Lane (Gear)	RX Interface Type	IP Type	Bit Rate (Lane)	Parser	AXI Bus	LMMI Bus	Registers	Fmax (MHz)	LUT[2]	EBR	High-Speed I/O Resources
4(8)	CSI-2	Hard D-PHY[4]	1500 Mbps	EN	DIS	EN	979	190.33	1246	4	1 x Hard D-PHY
4(16)	CSI-2	Hard D-PHY[4]	2500 Mbps	EN	DIS	EN	1104	177.84	1331	8	1 x Hard D-PHY
4(8)	DSI	Hard D-PHY[4]	1500 Mbps	EN	DIS	EN	979	200.00	1232	4	1 x Hard D-PHY
4(8)	CSI-2	Soft D-PHY	1034 Mbps	EN	DIS	EN	1383	164.12	1983	2	4 x IDDRX4, 1 x ECLKDIV, 1 x ECLKSYNC
4(8)	DSI	Soft D-PHY	1034 Mbps	EN	DIS	EN	1371	176.21	2028	2	4 x IDDRX4, 1 x ECLKDIV, 1 x ECLKSYNC

Notes:

1. All other settings are default.
2. The *distributed RAM* utilization is accounted for in the total LUT4s utilization. The actual LUT4 utilization is distribution among *logic*, *distributed RAM*, and *ripple logic*.
3. Data Settle settings change in these configurations to match the target bit rate per lane.
4. Hard D-PHY – CIL Enabled.
5. Fmax is generated using multiple iterations of Place and Route.

Table A.5. Device and Tool Tested

—	Value
Software Version	Lattice Radiant software 2025.2 production build
Device Used	LAV-AT-E70-3LFG1156C
Performance Grade	3
Synthesis Tool	Synplify Pro® W-2025.03LR-SP1-Beta2, Build 038R, Oct 2 2025

Table A.6. Resource Utilization[1]

Lane (Gear)	RX Interface Type	IP Type	Bit Rate (Lane)	Parser	AXI Bus	LMMI Bus	Registers	Fmax (MHz)	LUT[2]	EBR	High-Speed I/O Resources
4(8)	CSI-2	Soft D-PHY	1500 Mbps	EN	DIS	DIS	2033	250	5328	6	4 x IDDRX4, 1 x ECLKDIV, 1 x ECLKSYNC 4 x DDRDLL
4(8)	DSI	Soft D-PHY	1500 Mbps	EN	DIS	DIS	2062	250	5336	6	4 x IDDRX4, 1 x ECLKDIV, 1 x ECLKSYNC 4 x DDRDLL

Notes:

1. All other settings are default.
2. The *distributed RAM* utilization is accounted for in the total LUT4s utilization. The actual LUT4 utilization is distribution among *logic*, *distributed RAM*, and *ripple logic*.

Table A.7. Device and Tool Tested

—	Value
Software Version	Lattice Radiant software 2025.2 production build
Device Used	LAV-AT-E70-1LFG1156C
Performance Grade	1
Synthesis Tool	Synplify Pro® W-2025.03LR-SP1-Beta2, Build 038R, Oct 2 2025

Table A.8. Resource Utilization[1]

Lane (Gear)	RX Interface Type	IP Type	Bit Rate (Lane)	Parser	AXI Bus	LMMI Bus	Registers	Fmax (MHz)	LUT[2]	EBR	High-Speed I/O Resources
4(8)	CSI-2	Soft D-PHY	1500 Mbps	EN	DIS	DIS	2033	250	5328	6	4 x IDDRX4, 1 x ECLKDIV, 1 x ECLKSYNC 4 x DDRDLL
4(8)	DSI	Soft D-PHY	1500 Mbps	EN	DIS	DIS	2062	250	5336	6	4 x IDDRX4, 1 x ECLKDIV, 1 x ECLKSYNC 4 x DDRDLL

Notes:

1. All other settings are default.
2. The *distributed RAM* utilization is accounted for in the total LUT4s utilization. The actual LUT4 utilization is distribution among *logic*, *distributed RAM*, and *ripple logic*.

For more information regarding a specific configuration, generate the IP, run synthesis and MAP, and check the MAP reports for resource utilization. Number may vary when using a different software version or targeting a different device density, synthesis tool, or speed grade. For better Static Timing Analysis performance, you are recommended to run multiple iterations of Place and Route and/or set Optimization Goal to Timing in the Strategy section of the software tool.

References

- CSI-2/DSI D-PHY Rx IP Release Notes (FPGA-RN-02040)
- Lattice Memory Mapped Interface and Lattice Interrupt Interface User Guide (FPGA-UG-02039)
- Lattice Radiant Timing Constraints Methodology (FPGA-AN-02059)
- CrossLink-NX High-Speed I/O Interface User Guide (FPGA-TN-02097)
- Certus-NX web page
- Certus-N2 web page
- CertusPro-NX web page
- CrossLink-NX web page
- MachXO5-NX web page
- Avant-E web page
- Avant-G web page
- Avant-X web page
- CSI-2/DSI D-PHY Receiver IP Core web page
- Lattice Radiant Software web page
- Lattice Insights for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Note: In some instances, the IP may be updated without changes to the user guide. The user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.

Revision 2.5, IP v2.1.0, December 2025

Section	Change Summary
All	• Added a note on IP version in Quick Facts and *Revision History* sections. • Performed minor formatting and editorial edits.
Acronyms in This Document	Updated list of acronyms.

Introduction	• Updated Table 1.1. CSI-2/DSI D-PHY Rx IP Core Quick Facts as follows:
	  • Added IP version.
	  • Removed earlier IP versions.
	• Updated the note for RX line rate for CrossLink-NX devices with DSI interface when packet parser and LMMI interface are disabled in non-continuous mode in Table 1.2. CSI-2/DSI D-PHY Rx IP Support Readiness.
	• Updated the support for dynamic lane and rate reconfiguration during run time in the Soft CSI-2/DSI D-PHY Rx IP Core Features section.
	• Updated the Licensing and Ordering Information section.

Functional Description	• Updated figure title from *AXI4-Stream is ON and Packet Parser is ON Data Format* to Figure 2.4. AXI4-Stream is ON and Packet Parser is ON Data Format (Active Payload). • Updated the Dynamic Reconfiguration section.

IP Parameter Description	• Updated Table 3.1. General Attributes as follows:
	  • Updated description for *RX Gear*, *Enable Lane Aligner Module*, *Enable LMMI Interface*, *Enable Miscellaneous Status Signals*, *CIL Data Settle Cycle*, and *CIL Clock Settle Cycle* attributes.
	  • Add a note on AXI4-Stream support.
	• Updated description for the *Misc Signals* attribute in Table 3.2. RX FIFO Settings Attributes.
	• Updated description for *Coarse Delay* and *Fine Delay* attributes in Table 3.3. Soft PHY Settings Attributes.

Signal Description	• Updated description for lmmi_resetn_i and lmmi_clk_i signals in Table 4.1. Clock and Reset Ports Description.
	• Updated Table 4.2. D-PHY Rx Port Description as follows:
	  • Updated mode/configuration for lp_d_rx_p_o[BUS_WIDTH – 1:0], lp_d_rx_n_o[BUS_WIDTH – 1:0], payload_en_o, payload_o[DW-1:0], capture_en_o, bd0_o[RX Gear-1:0], bd1_o[RX Gear-1:0], bd2_o[RX Gear-1:0], bd3_o[RX Gear-1:0], vcx_o, dt_o[5:0], vc_o[1:0], wc_o[15:0], ecc_o[5:0], dt2_o[5:0], vc2_o[1:0], wc2_o[15:0], ecc2_o[5:0] signals.
	  • Updated description for tx_rdy_i, skewcal_det_o[BUS_WIDTH – 1:0], skewcal_done_o[BUS_WIDTH – 1:0] signals.
	  • Updated signal name from bd_o[31:0] to bd_o[DW-1:0] and updated description.
	• Updated mode/configuration for rxemptyfr1_o, rxque_curstate_o[1:0], rxque_empty_o, rxque_full_o signals in Table 4.5. RX FIFO Status Interface Signals Description.
	• Updated mode/configuration for lp_hs_state_d_o[1:0] signal in Table 4.6. Miscellaneous Status Interface Signals Description.

Register Description	Updated Table 5.1. General Configuration Registers as follows: • Updated description for ERROR_CTRL_ADDR, ERROR_HS_SOT_ADDR1, and ERROR_HS_SOT_SYNC_ADDR1 registers. • Added a note on status updates delay for non-hard D-PHY registers.

Section	Change Summary

Example Design	• Set the default value to bold for RX Interface Type and Number of RX Lanes parameters in Table 6.1. CSI-2/DSI D-PHY IP Configuration Supported by the Example Design.
	• Updated the step on updating the *Generated IP Settings* section in the post_syn_sys_avant.pdc file in the Changing Configuration of the Example Design section.
	• Updated the following figures:
	  • Figure 6.3. Example IP Settings
	  • Figure 6.4. Example Generated IP Settings Section of the PDC File
	  • Figure 6.7. Simulation Result
	• Updated the testbench file and added description on dynamic lane reconfiguration in the Simulating the Example Design section.
	• Updated the Hardware Testing section.

Designing with the IP	• Added a note on IP version in GUI in the Designing with the IP section.
	• Updated the following figures:
	  • Figure 7.1. Module/IP Block Wizard
	  • Figure 7.2. IP Configuration
	  • Figure 7.3. Check Generated Result

Design Considerations	• Added guidelines on minimum duration requirement for tLPX, tHS-TRAIL, tHS-PREPARE + tHS-ZERO from the D-PHY source in the following sections:
	  • Design Considerations in Continuous Clock Mode
	  • Design Considerations in Non-Continuous Clock Mode
	• Updated the Limitations section as follows:
	  • Updated the guidelines when *D-PHY RX IP == Soft D-PHY* or *CIL Bypass* is checked.
	  • Added limitations for Soft D-PHY on the assertion of full flag signal of the internal buffer when deskew calibration sequence is received.

Resource Utilization	Updated resources utilization for the latest software version.
References	Updated references.

Revision 2.4, IP v2.0.0, June 2025

Section	Change Summary
All	Performed minor formatting and editorial edits.

Introduction	• Updated Table 1.1. CSI-2/DSI D-PHY Rx IP Core Quick Facts as follows:
	  • Renamed *Supported FPGA Families* to *Supported Devices*.
	  • Removed the *Targeted Devices* row.
	  • Added IP version.
	• Added description about the supported features in the IP Support Summary section.
	• Added 1800 Mbps support for Lattice Avant devices in Table 1.2. CSI-2/DSI D-PHY Rx IP Support Readiness.
	• Added features in the following sections:
	  • Hard CSI-2/DSI D-PHY Rx IP Core Features
	  • Soft CSI-2/DSI D-PHY Rx IP Core Features
	• Changed *Multi-site Perpetual* to *Single Seat Perpetual* in Table 1.3. Ordering Part Number.

Functional Description	• Updated the internal signals in the AXI4-Stream Device Transmitter Interface section. • Renamed the section from *Lane/Gear Dynamic Reconfiguration with CRC Checking Function* to Dynamic Reconfiguration, and updated the content.

IP Parameter Description	• Updated Table 3.1. General Attributes as follows:
	  • Updated the *RX Line Rate per Lane (Mbps)* attribute to add 1800 Mbps support for Lattice Avant devices.
	  • Updated the description of the attributes: *D-PHY Clock Frequency (MHz)*, *Byte Clock Frequency (MHz)*, *CIL Bypass*, *Enable LMMI Interface*, and *Enable CRC Check*.
	  • Added the *CRC Check Mode* attribute.
	  • Removed the *Enable Lane/Gear Dynamic Reconfiguration* attribute.

Section	Change Summary

	• Updated Table 3.2. RX FIFO Settings Attributes as follows:
	  • Added note to *RX_FIFO*.
	  • Updated the *Counter Width* attribute description.
	• Updated Table 3.3. Soft PHY Settings Attributes as follows:
	  • Added note to *Soft PHY*.
	  • Added the *Enable Dynamic Delay Control* attribute.

Signal Description	• Added the Clock and Reset Interface section.
	• Updated Table 4.2. D-PHY Rx Port Description as follows:
	  • Removed ports: reset_n_i, pd_dphy_i, clk_lp_ctrl_i, reset_lp_n_i, clk_byte_fr_i, reset_byte_fr_n_i, sync_rst_i, sync_clk_i, clk_byte_o, and clk_byte_hs_o.
	  • Added ports: pd_dphy_i, data_loadn_i, data_move_i, data_dir_i, data_coarsedly_i[1:0], and data_cflag_o[BUS_WIDTH – 1:0].
	  • Updated ports: pll_lock_i, ready_o, payload_o, bd0_o, bd1_o, bd2_o, bd3_o, lp2_en_o, sp2_en_o, lp2_av_en_o, dt2_o[5:0], vc2_o[1:0], wc2_o[15:0], ecc2_o[5:0], skewcal_det_o[BUS_WIDTH – 1:0], and skewcal_done_o[BUS_WIDTH – 1:0].
	  • Updated the note on bus width.
	  • Updated the note on sampling 2 different valid packet headers in 1 byte clock cycle.
	  • Added note on DW.
	• Updated Table 4.3. LMMI Device Target Interface Signals Description as follows:
	  • Removed the lmmi_clk_i and lmmi_resetn_i signals.
	  • Updated the lmmi_rdata_valid_o signal.
	• Updated Table 4.4. AXI4-Stream Device Transmitter Interface Signals Description as follows:
	  • Updated the axis_tdata_o signal.
	  • Added note on ADW.
	• Renamed *fifo_dly_err* to *fifo_dly_err_o* in Table 4.5. RX FIFO Status Interface Signals Description
	• Updated Table 4.6. Miscellaneous Status Interface Signals Description.

Register Description	• Updated Table 5.1. General Configuration Registers as follows:
	  • Updated *Gear x16* to *RX Gear == 16* and *NUM_RX_LANE* to *Number of RX Lanes*.
	  • Updated the note on the dynamic lane reconfiguration feature.
	  • Added a note on addresses within the 0x00 – 0x1E range.
	• Updated Table 5.2. Configuration Registers (MIPI Programmable Bits) as follows:
	  • Updated the header from ADDR to ADDR[5:0].
	  • Added note on SOT error checking.
	• Updated Table 5.3. Configuration Registers (MIPI Programmable Bits) as follows:
	  • Added 0x1B and 0x1D.
	  • Added a note to RXCDRP[1:0] and RXLPRP[2:0].
	  • Added a note on valid values.

Example Design	• Updated the device name for the Avant-E Evaluation Board in the following sections:
	  • Section 6 Example Design
	  • Table 6.2. Example Design File List
	  • Section 6.6 Hardware Testing
	• Updated the following figures:
	  • Figure 6.2. Sample File List
	  • Figure 6.4. Example Generated IP Settings Section of the PDC File

Designing with the IP	Updated the following figures: • Figure 7.1. Module/IP Block Wizard • Figure 7.2. IP Configuration • Figure 7.3. Check Generated Result
Design Considerations	• Added limitations for Avant devices when *D-PHY RX IP == Soft D-PHY* or *CIL Bypass* is checked.

Section	Change Summary
	• Updated limitations on Static Timing Analysis and Fmax value in the Limitations section.

Resource Utilization	• Updated resources utilization for the latest software version.
	• Updated the device used in the following tables:
	  • Table A.5. Device and Tool Tested
	  • Table A.7. Device and Tool Tested

References	Added references.

Revision 2.3, IP v1.9.0, December 2024

Section	Change Summary

Introduction	• Added support for Lattice Nexus 2 platform in the Introduction section.
	• Updated Table 1.1. CSI-2/DSI D-PHY Rx IP Core Quick Facts.
	  • Added Certus-N2 device.
	  • Added targeted devices: LFD2NX-9, LFD2NX-28, and LN2-CT-20.
	  • Added IP changes.
	  • Updated IP version**.**
	• Added the IP Support Summary section.
	• Added information on dynamic clock-to-data calibration for Lattice Avant devices in the Soft CSI-2/DSI D-PHY Rx IP Core Features section.
	• Updated Table 1.3. Ordering Part Number as follows:
	  • Added OPN for Certus-N2 devices.
	  • Changed from Single Machine Annual to Single Seat Annual.
	• Removed the *IP Validation Summary* section.
	• Added the Hardware Support section.

Functional Description	• Added information for the Lattice Avant devices in the Soft D-PHY section.
	• Changed term_clc_en_o to term_clk_en_o in the following figures:
	  • Figure 2.1. D-PHY Rx IP Block Diagram with AXI4-Stream Enabled, LMMI Enabled, and Packet Parser OFF
	  • Figure 2.2. D-PHY Rx IP Block Diagram with AXI4-Stream Enabled, and LMMI Disabled
	  • Figure 2.12. D-PHY Rx IP Configuration with AXI4-Stream Enabled and Packet Parser Disabled
	  • Figure 2.15. D-PHY Rx IP Configuration with AXI4-Stream Enabled and Packet Parser Enabled
	• Updated the following figures:
	  • Figure 2.16. D-PHY Rx IP Output Timing Diagram with Packet Parser
	  • Figure 2.18. Output Timing Diagram with Valid Second Set of Packet Information
	• Added Figure 2.17. Output Timing Diagram of a RX Gear == 8 Configuration.

IP Parameter Description	Updated the *RX Line Rate per Lane (Mbps)*, *D-PHY Clock Frequency (MHz)*, *Byte Clock Frequency (MHz)*, *Enable Lane Aligner Module*, and *Data Settle Cycle* attributes in Table 3.1. General Attributes.
Signal Description	Updated Table 4.1. D-PHY Rx Port Description as follows: • Updated description for *reset_byte_fr_n_i*. • Added the *edgemon_done_o* port.
Register Description	• Removed the description about both clk_byte_fr_i and lmmi_clk_i need to be active when accessing the registers in the Register Description section. • Added note on status reporting for registers when *DSI Back-to-Back HS Packets == ON* and gap between packets is small in Table 5.1. General Configuration Registers. • Added note to address *0x28*, *0x29*, and *0x39* in Table 5.2. Configuration Registers (MIPI Programmable Bits). • Removed address *0x14* to *0x1D* in Table 5.3. Configuration Registers (MIPI Programmable Bits).
Example Design	Added this section.

Section	Change Summary

Designing with the IP	• Updated the following figures:
	  • Figure 7.1. Module/IP Block Wizard
	  • Figure 7.2. IP Configuration
	  • Figure 7.3. Check Generated Result
	  • Figure 7.8. Adding USE_EVAL_TOP_DUT in the tb_top.sv File
	• Updated the Simulation Results section.

Design Considerations	Added Fmax value for Lattice Nexus 2 devices in the Limitations section.
Resource Utilization	Updated the resource utilization for the latest software version.
References	Added links to the Certus-N2 web page and IP release notes.

Revision 2.2, June 2024

Section	Change Summary
All	Performed minor formatting and typo edits.
Acronyms in This Document	• Added definition for CSR. • Updated acronym from EoTP to EoTp.
Introduction	• Updated Table 1.1. CSI-2/DSI D-PHY Rx IP Core Quick Facts. • Added OPNs for Lattice Avant-G, Avant-X, and MachXO5-NX device family in Table 1.2. Ordering Part Number. • Updated Table 1.3. IP Validation Level. • Added signal name for bidirectional signals in the Signal Names section.
Functional Description	• Added the Clocking section. • Updated the supported protocol for device transmitter and description for control in Table 2.1. User Interfaces and Supported Protocols. • Updated the description in the LMMI Device Target Interface section. • Updated the signals when the AXI4-Stream device is not enabled and the D-PHY Rx IP is configured with Packet Parser in the AXI4-Stream Device Transmitter Interface section. • Updated Figure 2.4. AXI4-Stream is ON and Packet Parser is ON Data Format. • Defined $T_{CLK-POST}$ for the equations in the Hard D-PHY section. • Updated the output clock in the RX_FIFO section. • Updated the time interval configuration using the LMMI interface in the Global Operations Controller section. • Updated the Inputs to Packet Parser waveforms in Figure 2.17. Output Timing Diagram with Valid Second Set of Packet Information. • Updated the step to assert the reset in the Lane/Gear Dynamic Reconfiguration with CRC Checking Function section.

IP Parameter Description	• Updated Table 3.1. General Attributes.
	  • Updated the *RX Interface Type* attribute.
	  • Added the *DSI Back-to-Back HS Packets* attribute under Parser Configuration.
	  • Updated the values for Data Settle Cycle, CIL Data Settle Cycle, and CIL Clock Settle Cycle attributes.
	  • Updated the description for the *Configurable Data Settle Count* attribute.
	• Updated the value for the *Depth* attribute and added a note in Table 3.2. RX FIFO Settings Attributes.

Signal Description	Updated the following tables: • Table 4.1. D-PHY Rx Port Description • Table 4.2. LMMI Device Target Interface Signals Description • Table 4.3. AXI4-Stream Device Transmitter Interface Signals Description • Table 4.4. RX FIFO Status Interface Signals Description • Table 4.5. Miscellaneous Status Interface Signals Description
Register Description	• Added condition when accessing the registers in the Register Description section.

Section	Change Summary

	• Updated the following tables:
	  • Table 5.1. General Configuration Registers
	  • Table 5.2. Configuration Registers (MIPI Programmable Bits)
	  • Table 5.3. Configuration Registers (MIPI Programmable Bits)

Designing with the IP	• Updated the following diagrams in the Generating and Instantiating the IP section:
	  • Figure 6.1. Module/IP Block Wizard
	  • Figure 6.2. IP Configuration
	  • Figure 6.3. Check Generated Result
	• Updated the Generated Files and File Structure section.
	• Updated the Timing Constraints section.
	• Updated the Running Functional Simulation section.
	• Updated Figure 6.13. Passing Simulation Log.

Debugging	Updated ModelSim to QuestaSim in the Reveal Analyzer section.
Design Considerations	Added limitations in the Limitations section.
Resource Utilization	Updated this section.

Revision 2.1, January 2024

Section	Change Summary
All	Renamed document from CSI-2/DSI D-PHY Rx IP Core - Lattice Radiant Software to CSI-2/DSI D-PHY Rx IP.
Disclaimers	Updated disclaimers.
Introduction	• Reworked section contents. • Changed *LAV-AT-500E* to *LAV-AT-E70* in Table 1.1. CSI-2/DSI D-PHY Rx IP Core Quick Facts. • Reworked section 7 *Ordering Part Number* and renamed to subsection 1.4 Licensing and Ordering Information. • Reworked subsection 6.4 *IP Evaluation* and renamed to subsection 1.5 IP Validation Summary. • Added subsection 1.6 Minimum Device Requirements. • Reworked subsection 1.5 *Conventions* and renamed to subsection 1.7 Naming Conventions.
Functional Description	• Reworked section 2 *Functional Description* and renamed to subsection 2.1 IP Architecture Overview. • Added subsection 2.2 User Interfaces. • Reworked subsection 2.10 *LMMI Device* and renamed to subsection 2.2.1 LMMI Device Target Interface. • Reworked subsection 2.9 *AXI4-Stream Device Transmitter* and renamed to subsection 2.2.2 AXI4-Stream Device Transmitter Interface. • Reworked subsection 2.2.1 *Hard D-PHY* and moved to subsection 2.4.1 Hard D-PHY. • Reworked subsection 2.3 *RX_FIFO* and moved to subsection 2.5 RX_FIFO. • Reworked subsection 2.4 *Global Operations Controller* and moved to subsection 2.6 Global Operations Controller. • Reworked subsection 2.5 *D-PHY Rx IP without Packet Parser* and moved to subsection 2.7 D-PHY Rx IP without Packet Parser. • Reworked subsection 2.7 *Packet Parser* and moved to subsection 2.9 Packet Parser. • Reworked subsection 2.8 *Word Aligner and Optional Lane Aligner* and moved to subsection 2.10 Word Aligner and Optional Lane Aligner. • Added subsection 2.11 Lane/Gear Dynamic Reconfiguration with CRC Checking Function.
IP Parameter Description	Reworked section 4 *Attribute Summary* and renamed to section 3 IP Parameter Description.
Signal Description	Reworked section 3 *Signal Description* and moved to section 4 Signal Description.
Register Description	Reworked section 5 *Internal Registers* and renamed to section 5 Register Description.
Designing with the IP	• Reworked section 6 *IP Generation, Simulation, and Validation* and renamed to section 6 Designing with the IP.

Section	Change Summary
	• Reworked subsection 6.1 *Generating the IP* and renamed to subsection 6.1 Generating and Instantiating the IP. • Added subsection 6.2 Design Implementation. • Reworked subsection 6.3 *Constraining the IP* and renamed to subsection 6.3 Timing Constraints and 6.4 Physical Constraints. • Added subsection 6.5 Specifying the Strategy. • Reworked subsection 6.2 *Running Functional Simulation* and moved to subsection 6.6 Running Functional Simulation.
Debugging	Added this section.
Design Considerations	Added this section.
Resource Utilization	Updated for the latest software version.
References	Reworked section contents.

Revision 2.0, August 2023

Section	Change Summary
Inclusive Language	Newly added this section.
All	• Changed all instances of Device Master to Device Transmitter. • Changed all instances of *Device Slave* to *Device Target*.
Introduction	Table 1.1. CSI-2/DSI D-PHY Rx IP Core Quick Facts: • newly added *MachXO5-NX* to Supported FPGA Families; • newly added LIFCL-33, LFCPNX-50, LFMXO5-25, LFMXO5-55T, and LFMXO5-100T to Targeted Devices; • newly added IP Core v1.5.x - Lattice Radiant software 2022.1 to Lattice Implementation.
Signal Description	Changed *AXI4 Master Stream* to *AXI4 Stream Transmitter* in Table 3.1. D-PHY Rx Port Description.

Functional Description	• In the D-PHY Module section:
	  • divided the contents of this section into Hard D-PHY and Soft D-PHY;
	  • updated the descriptions of hard D-PHY and soft D-PHY.
	• Changed *Init Slave* to *Init* in Figure 2.6. MIPI D-PHY Rx LP to HS Transition Flow Diagram on Data Lanes and Figure 2.7. MIPI D-PHY Rx LP to HS transition on Clock Lane.

Attribute Summary	Table 4.1. Attributes Table: • newly added the following attributes under soft PHY: *Delay Mode*, *Coarse Delay*, and *Fine Delay*; • newly added the following table note: In the IP version 1.6.0 onwards, a GUI tab for modifying the delay cell within the soft PHY is available.

Internal Registers	• Updated the Offset column of Table 5.1. General Configuration Registers.
	• In Table 5.2. Configuration Registers (MIPI Programmable Bits):
	  • changed MASTER_SLAVE to PRIMARY_SECONDARY;
	  • changed Slave to Secondary;
	  • changed *Master* to *Primary*;
	  • changed slave clock lane to clock lane of the secondary device.

Ordering Part Number	Removed the following OPNs: D-PHY-TX-CTNX-US, D-PHY-TX-CNX-U, D-PHY-TX-CNX-UT, D-PHY-TX-CNX-US, D-PHY-TX-CTNX-U, D-PHY-TX-CTNX-UT, D-PHY-TX-CPNX-U, D-PHY-TX-CPNX-UT, D-PHY-TX-CPNX-US, DPHY-TX-AVE-U, DPHY-TX-AVE-UT, DPHY-TX-AVE-US.
References	Newly added links to Lattice Radiant Software Web Page, CertusPro-NX Devices Web Page, Certus-NX Devices Web Page, CrossLink-NX Devices Web Page, MachXO5-NX Devices Web Page, Lattice Avant-E Devices Web Page, Lattice Insight for Training Series and Learning Plans.

Revision 1.9, December 2022

Section	Change Summary
Introduction	• Added Lattice Avant to Supported FPGA Family and added LAV-AT-500E to Targeted Devices in Table 1.1. CSI-2/DSI D-PHY Rx IP Core Quick Facts. • Added bullet *Hard D-PHY is supported on Crosslink-NX devices only* in Section 1.3. • Added bullets Maximum rate of up to 1500 Mbps per lane for Crosslink-NX, Certus-NX, and CertusPro-NX devices and Maximum rate of up to 1800 Mbps per lane for Avant devices in Section 1.4.
Functional Description	Updated below figures to remove *reset_byte_n_i*: • Figure 2.1. D-PHY Rx IP Block Diagram with AXI4-Stream Enabled, LMMI Enabled and Packet Parser OFF • Figure 2.2. D-PHY Rx IP Block Diagram with AXI4 Stream Enabled and LMMI Disabled • Figure 2.9. D-PHY Rx IP Configuration with AXI4-Stream Disabled and Packet Parser Disabled • Figure 2.11. D-PHY Rx IP Output Timing Diagram without Packet Parser • Figure 2.12. D-PHY Rx IP Configuration with AXI4-Stream Disabled and Packet Parser Enabled • Figure 2.13. D-PHY Rx IP Configuration with AXI4-Stream Enabled and Packet Parser Enabled
Signal Description	• Added ports fifo_dly_err, fifo_undflw_err, and fifo_ovflw_err and deleted reset_byte_n_i in Table 3.1. D-PHY Rx Port Description.
Attribute Summary	• Added foot note The maximum data rate depends on the gear, as well as the family, package and speed grade of the device. Please check the device data sheet for more information to RX Line Rate per Lane (Mbps) in Table 4.1. Attributes Table.
IP Generation, Simulation and Validation	• Changed the title of section 6 from Core Generation, Simulation and Validation to IP Generation, Simulation and Validation. • Changed the title of section 6.1 from *Generation and Synthesis* to *Generating the IP*. • Changed the title of section 6.2 from *Functional Simulation* to *Running Functional Simulation*. • Added section 6.3. • Changed the title from Core Validation to IP Evaluation and updated description in section 6.4. • Deleted Licensing and Evaluation section.
Ordering Part Number	Added Avant-E OPNs.

Revision 1.8, September 2022

Section	Change Summary
Functional Description	Updated vc_o for Virtual Channel ID and dt_o for Data Type in Figure 2.17 in the AXI4-Stream Device Master section.

Revision 1.7, July 2022

Section	Change Summary
Functional Description	Updated the AXI4-Stream Device Master section. • Removed the payload_en_o signal from the axis_mtdata_ o group in In Figure 2.17. • Reordered the internal signals list.

Revision 1.6, September 2021

Section	Change Summary
Functional Description	Updated D-PHY Module section to add information on skew calibration.
Signal Description	Updated Table 3.1 to add rows for RX FIFO Status Signals, updated description for pd_dphy_i. lp_hs_state_clk_o[1:0] and lp_hs_state_d_o[1:0], and updated mode/configuration for

Section	Change Summary
	skewcal_done_o.
Attribute Summary	Updated Table 4.1 to increase supported packet delay count and modify attribute descriptions for RX_FIFO.
Internal Registers	Updated Table 5.1 to move 0x39 to Always Available row.

Revision 1.5, June 2021

Section	Change Summary
Introduction	Updated section content, including Table 1.1 to include CertusPro-NX support.
Attribute Summary	Updated Table 4.1.
Licensing and Evaluation	Updated content in Licensing the IP and removed Hardware Evaluation section.
Ordering Part Number	Updated part number to include CertusPro-NX.

Revision 1.4, February 2021

Section	Change Summary
Introduction	• Removed ADC IP Core Native Interface from Table 1.1. • Updated MIPI D-PHY and the MIPI CSI-2 specifications to v1.2 in the Features section.

Revision 1.3, November 2020

Section	Change Summary

Introduction	• Updated Table 1.1. CSI-2/DSI D-PHY Rx IP Core Quick Facts.
	  • Updated Lattice Implementation.
	  • Updated reference to the Lattice Radiant Software User Guide.
	• Added support for optional periodic deskew detection to the Features section.

Functional Description	• Added contents to the RX_FIFO section. • Added skewcal_det_o and skewcal_done_o output ports to Figure 2.1, Figure 2.2, Figure 2.9, Figure 2.10, and Figure 2.12. • Updated Figure 2.6. • Updated heading to Word Aligner and Optional Lane Aligner. • Removed Figure 2.18.
Signal Description	• Added skewcal_det_o and skewcal_done_o output ports to Table 3.1. D-PHY Rx Port Description.
Attribute Summary	• Added Enable Deskew Calibration Detection to Table 4.1. Attributes Table.
Core Generation, Simulation, and Validation	• Updated reference to the Lattice Radiant Software User Guide • Updated Figure 6.1. Configure Block of D-PHY Rx. • Updated Figure 6.2. Check Generating Result.
References	Updated reference to the Lattice Radiant Software User Guide

Revision 1.2, August 2020

Section	Change Summary
Acronyms in This Document	Updated content.
Introduction	• Updated Table 1.1. • Updated content of Hard CSI-2/DSI D-PHY Rx IP Core Features and Soft CSI-2/DSI D-PHY Rx IP Core Features section.
Functional Description	• Updated content of D-PHY Rx Common Interface Wrapper, RX_FIFO, Global Operations Controller, Word Aligner and Optional Line Aligner, AXI4-Stream Device Master, and LMMI Device section. • Updated the following figures:

Section	Change Summary
	• Figure 2.1 • Figure 2.2 • Figure 2.9 • Figure 2.10 • Figure 2.12 • Figure 2.13 • Figure 2.14 • Figure 2.15 • Figure 2.16
Signal Description	Updated Table 3.1.
Attribute Summary	Updated Table 4.1.
Internal Registers	Updated Table 5.2.
Core Generation, Simulation, and Validation	Updated step 1 in Functional Simulation section.
Ordering Part Number	Updated section content.
Appendix A. Resource Utilization	Updated Table A.2.

Revision 1.1, February 2020

Section	Change Summary
Attribute Summary	Updated Table 4.1. Attributes Table.
Port Description	Updated Table 3.1. D-PHY Rx Port Description.
Functional Description	Added RX_FIFO section.

Revision 1.0, December 2019

Section	Change Summary
All	Initial release.

www.latticesemi.com