iCE40 UltraPlus Display Frame Buffer - Radiant Software

User Guide

FPGA-UG-02059 Version 1.0

June 2018

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
SPRAM	Single Port RAM Memory
PLL	Phase-Locked Loop
SSP	System Solution Platform
HS	High Speed
LP	Low Power
FPGA	Field-Programmable Gate Array
MDP	Mobile Development Platform
SPI	Serial Peripheral Interface
USB	Universal Serial Bus

1. Introduction

The iCE40 UltraPlus™ Display Frame Buffer demo consists of the following modules:

- Clock Generator
- SPRAM (Single Port RAM Memory)
- Main Control
- Decompress
- 8BIT2RGB
- MIPI DSI TX

2. Functional Description

Figure 2.1 shows the demo structure diagram.

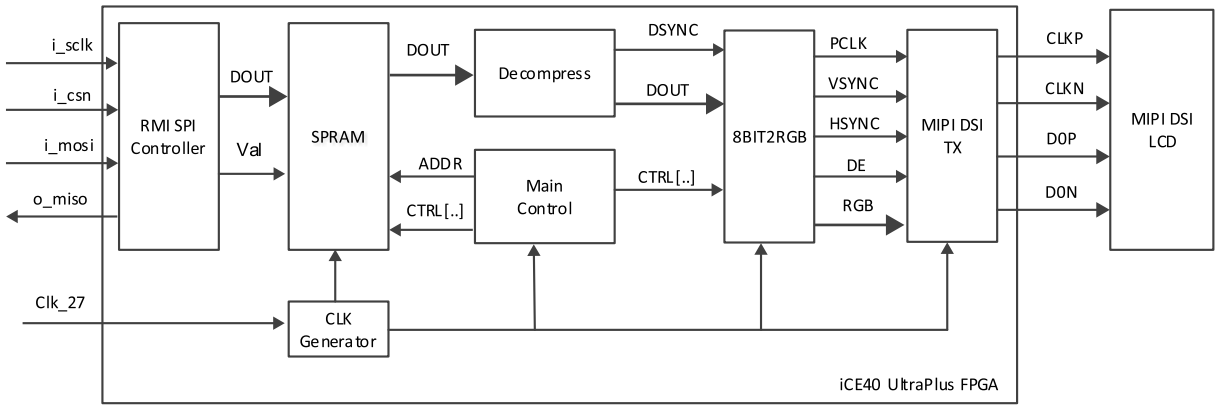

Figure 2.1. Display Frame Buffer Demo Block Diagram

2.1. Clock Generator Module

The Clock Generator Module uses the sysClock PLL of the iCE40 UltraPlus device to generate two 54 MHz DDR clock outputs. Each clock has a 90-degree phase shift relative to the other.

2.2. Main Control Module

The basic functions of the main control module include:

- Reading image data from the internal SPRAM
- Sending the read data synchronously to the decompress module

In this demo, three images are stored in the internal SPRAM. The main control module continuously reads each image between an interval of three seconds.

2.3. SPRAM Module

iCE40 UltraPlus has a 1-Mbit sysMEM SPRAM. The SPRAM block is implemented to be accessed only as a single port. Each block of SPRAM is designed to be 16 Kb x 16 Kb (256 Kb) in size. In this demo, the System Solution Platform (SSP) tool is used to write three compressed image data to the SPRAM.

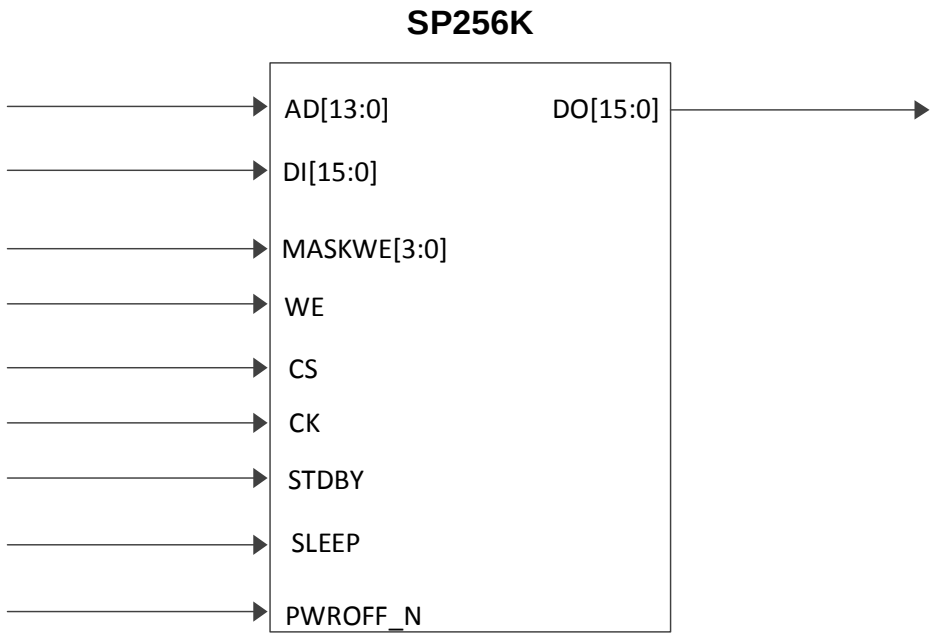

Figure 2.2. SPRAM Primitive

2.4. Decompress Module

The Decompress module decompresses the image data from the SPRAM and sends it to the 8BIT2RTB module.

2.5. 8BIT2RGB Module

The 8BIT2RGB module receives data from the Decompress module, generates synchronous signals, and sends pixel data to the MIPI DSI TX module.

2.6. MIPI DSI TX Module

The MIPI DSI TX module packages standard parallel data into DSI byte packets. The input interface of the design consists of the following:

- data bus (PIXDATA))
- vertical and horizontal sync flags (VSYNC and HSYNC))
- data enable and clock (DE and PIXCLK)).

This parallel bus is converted to the appropriate DSI output format. The DSI output serializes HS (High Speed) data and controls LP (Low Power) data and transfers them using the Lattice MIPI D-PHY Reference IP.

3. Demo Setup

The iCE40 UltraPlus display frame buffer demo setup consists of the following hardware platforms and software operation tools.

3.1. Hardware Requirements

- iCE40 UltraPlus Mobile Development Platform (MDP) (Revision C)
- USB to mini-USB cable

3.2. Software Requirements

- Radiant Programmer 1.0 (or higher)
- System Solution Platform (SSP)

Note: SSP installer and installation guide are included with this solution under the SSP folder. Follow the instructions in the guide to install this application properly.

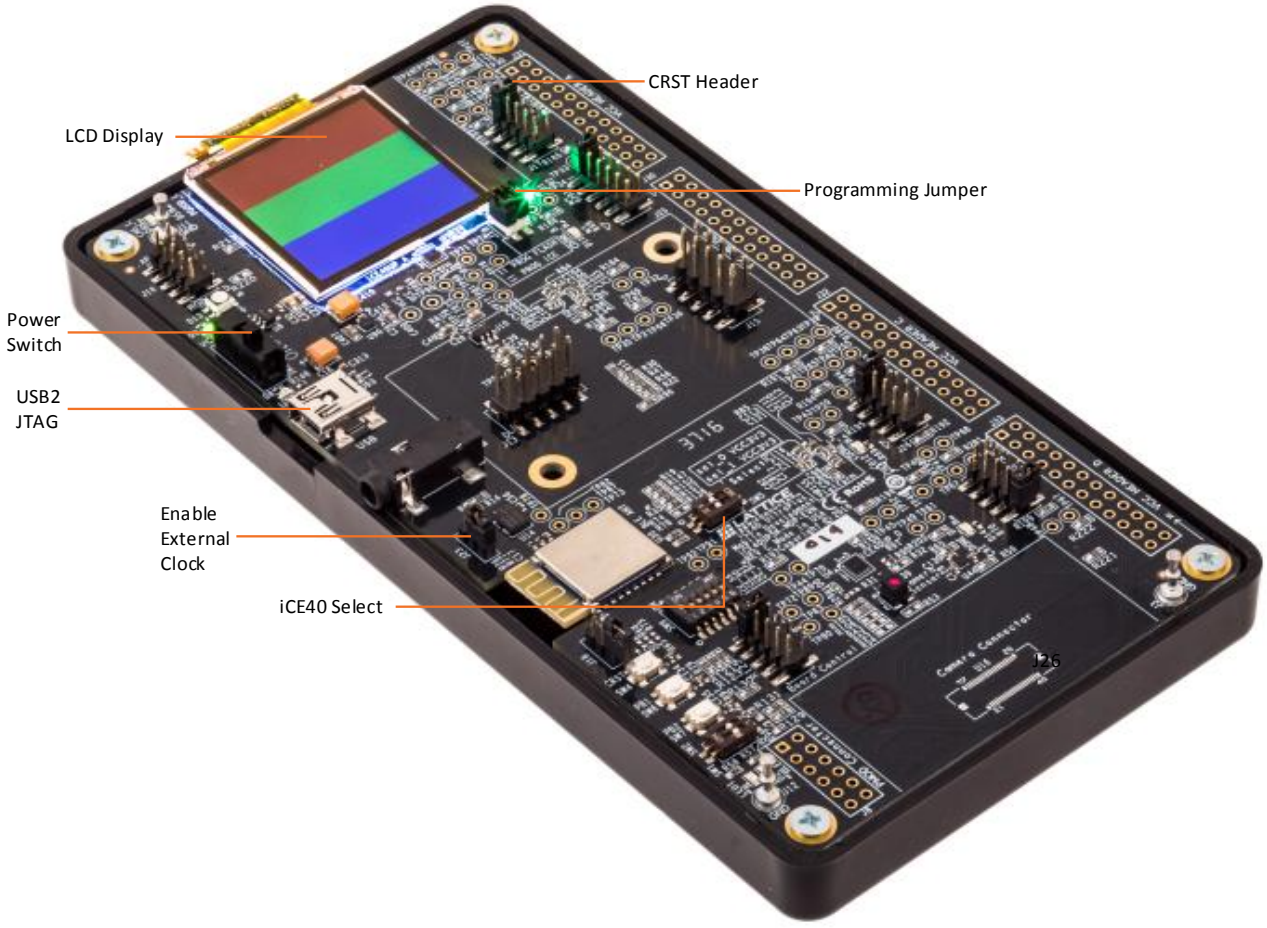

Figure 3.1. iCE40 UltraPlus MDP Board Details

3.3. Setting Jumpers and Switches

Board reconfiguration is needed before running this demo. The LCD display should be connected to J2 before you apply the settings. Figure 3.2 highlights (in orange boxes) all switches and jumpers needed to be verified or reconfigured on the Mobile Development Platform (MDP) board.

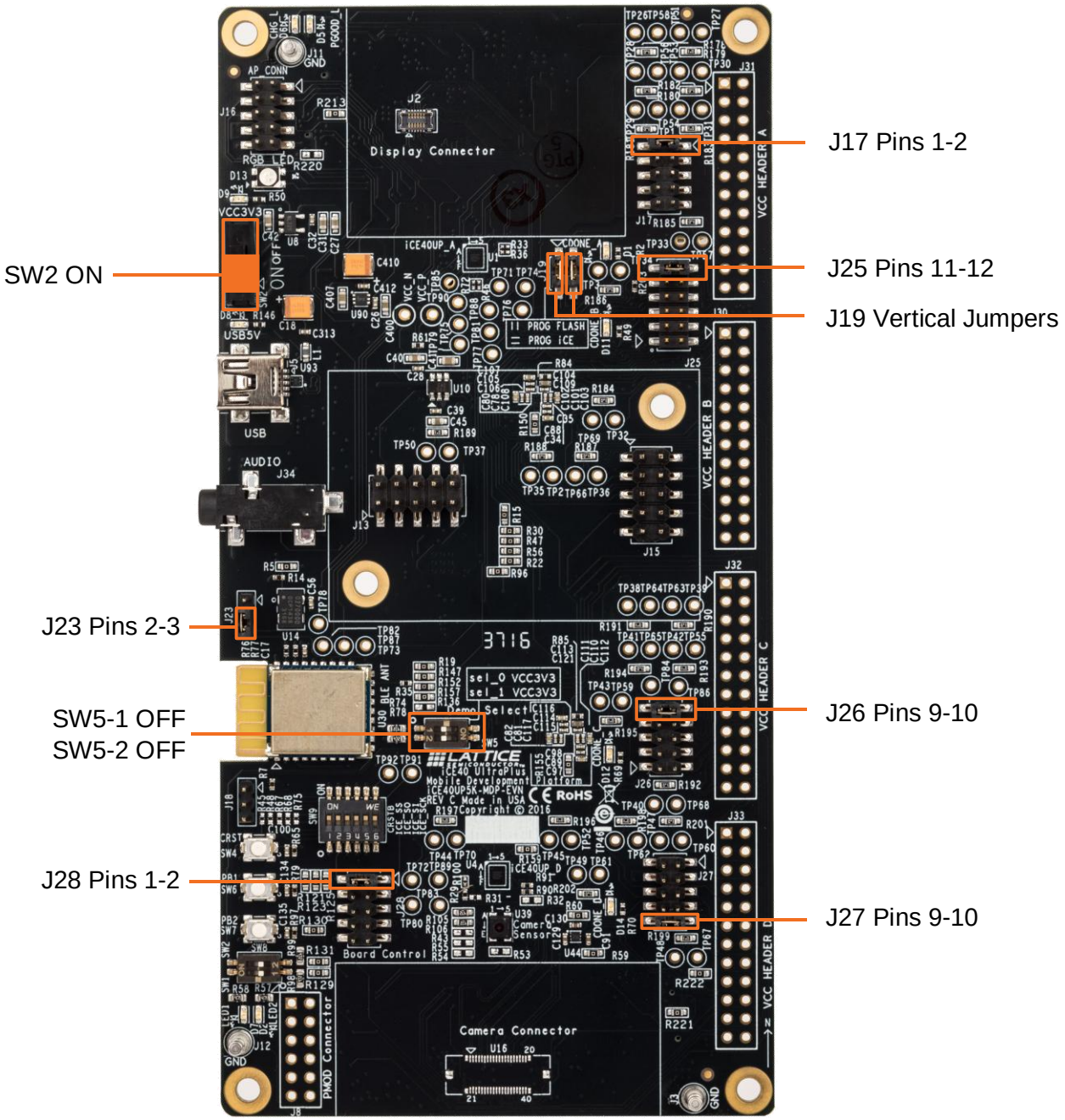

Figure 3.2. MDP Board Configuration

Table 3.1 lists the detailed information of these configurations on switches and jumpers.

Table 3.1. Detailed Information of the Board Configuration

Items	Configuration	Description
J17	Shunt pins 1-2	Enable ICE40UP5K_A device.
J25	Shunt pin 11-12	Disable ICE40UP5K_B device.
J26, J27	Shunt pin 9-10	Disable ICE40UP5K_C/D devices.
SW5	Set SW5-1 to OFF, and SW5-2 to OFF.	Select ICE40UP5K_A as target device.
J28	Shunt pin 1-2	Enable Board control for programming SPI Flash.
J19	Shunt pins 1-3, 2-4 (vertical)	Enable programming SPI Flash
J23	Shunt pin 2-3	Use Xtal U14 as clock source.
SW2	Set to ON	Power switch, slide down for power-on.

4. Programming the Bitmaps to the MDP Board

To program the bitmaps to the MDP board:

1. Install the Lattice SSP tool for this demo. For more details on the Lattice SSP tool, refer to **SSP Installation and Deployment Usage Guide.pdf** and **SSP Operation Tool Kits Usage Guide.pdf**.
   Note: The default installation directory is **C:\Program Files (x86)\LSCC_LSH\LSCC_SSP**, and the aforementioned documents are placed in the **doc** folder.
2. Connect the iCE40 UltraPlus MDP to the PC using a USB mini port (J5).
3. Switch SW2 to ON to power up the iCE40 UltraPlus MDP.
4. Start the Radiant Programmer tool.
5. In the Getting Started dialog box, select **Create a new blank project** as shown in Figure 4.1.

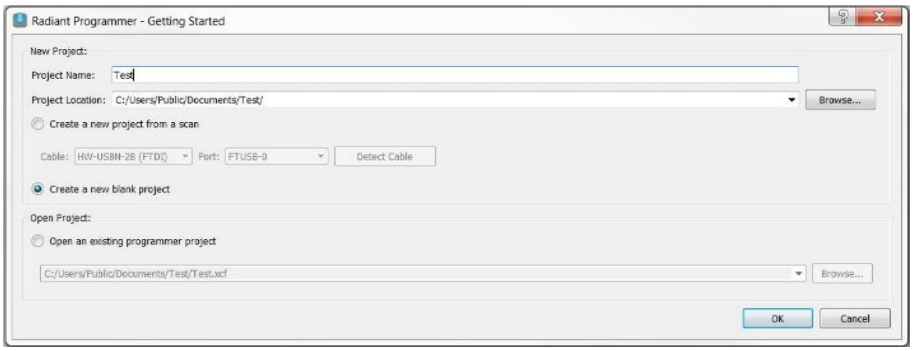

Figure 4.1. Radiant Programmer Getting Started Dialog Box

6. Click **OK**. This opens the Radiant Programmer main interface as shown in Figure 4.2.
7. Select **iCE40 UltraPlus** under **Device Family**.
8. Select **iCE40UP5K** under **Device**.
9. Set **Cable** to **HW-USBN-2B (FTDI)**.
10. Set Port to **FTUSB-0**.

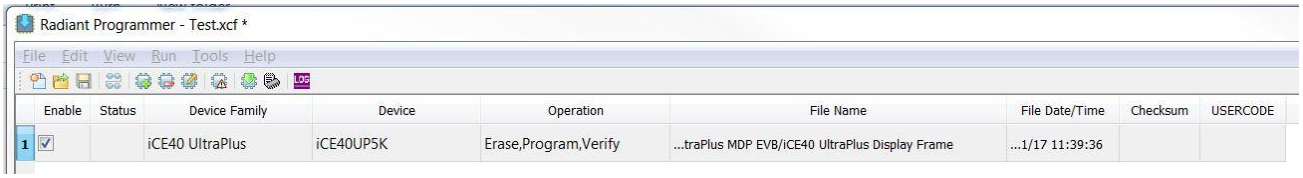

Figure 4.2. Radiant Programmer Main Interface

11. From the menu bar, select **Edit > Device Properties** to open the Device Properties window. Apply the settings as shown in Figure 4.3.

    Target Memory: External SPI Flash Programming

    Port Interface: SPI

    Access mode: Direct Programming

    Operation: Erase, Program, Verify

    Programming File: load bitstream file **Display_Frame_Buffer_bitmap.hex**.

    Family: SPI Serial Flash

    Vendor: Micron

    Device: SPI-M25P80

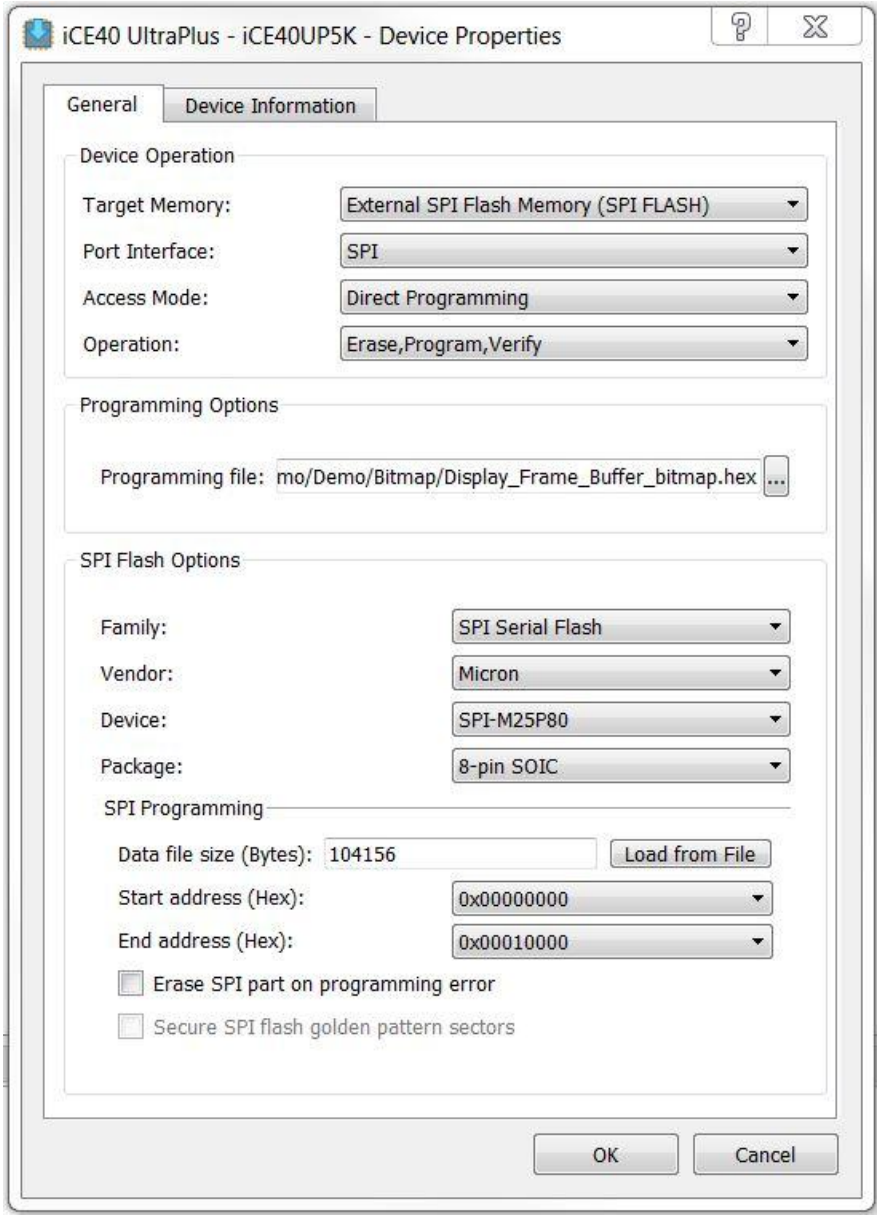

Figure 4.3. Device Properties Dialog Box

12. Click the **Program Device** button to program the FPGA.

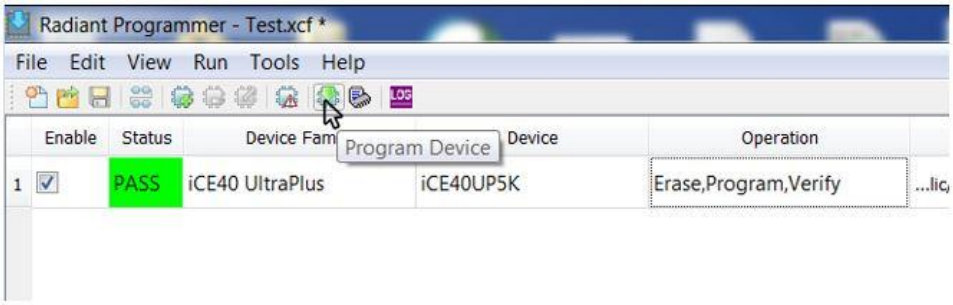

Figure 4.4. Program Button

5. Running the Demo

To run the demo:

1. Follow the steps in the Programming the Bitmaps to the MDP Board section so that the iCE40 UltraPlus MDP and SSP are ready with the necessary bitmap and picture data files.
2. Power ON the iCE40 UltraPlus MDP. DONE_A lights up and the LCD display shows a color bar.
3. Start CMD prompt, change directory to where the **Frame_buffer_demo.bat** file is located and run this file to write the picture data to the iCE40 UltraPlus SPRAM.
4. Picture images are displayed on the DSI LCD one after the other in an interval of three seconds.

Technical Support Assistance

For assistance, submit a technical support case at www.latticesemi.com/techsupport.

Revision History

Date	Version	Change Summary
June 2018	1.0	Initial release.

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