![LATTICE SEMICONDUCTOR logo]

Release Notes for
Lattice Diamond 3.10 SP2

Welcome to Lattice Diamond®, the complete design environment for Lattice Semiconductor FPGAs. Lattice Diamond design software offers leading-edge design and implementation tools optimized for cost-sensitive, low-power Lattice FPGA architectures.

Diamond is available for both the Windows and Linux operating systems. For details, see "System Requirements" on page 8.

This version of Diamond adds a variety of enhancements to make designing for Lattice Semiconductor programmable devices easier than ever. The design tools also include support for the latest Lattice Semiconductor devices.

Lattice Semiconductor offers a rich variety of information sources, including the Help system, PDF manuals, tutorials, and online discussions. The easiest way to reach them all is through the online Help. The first topic in the Help provides links to all the other sources of information.

You can also find extensive information about Diamond and its capabilities, tools, and workflow on the Lattice Semiconductor website under:

www.latticesemi.com/latticediamond

What's New in Diamond 3.10 SP2

Installation of SP2 includes all the changes and features in SP1.

This SP2 release of Diamond provides the following new items:

ECP5U/UM/5G Family Support

▶ New ECP5U 45K caBGA256 package is generally available.

> ▶ Family LFE5U-45F-xBG256C/I (x = Grades 6,7,8).

▶ ECP5U/UM/5G 85K 285csfBGA package is in FINAL status.

> ▶ Other densities 12K/25K/45K data already in FINAL status as of SP1.

> ▶ All devices support COM/IND/AUTO. (Except ECP5UM5G does not support AUTO.)

Crosslink Family Support

▶ 80ckfBGA package is generally available.

▶ 80ctfBGA now requires a license.

▶ Timing data is in FINAL status for IND/AUTO.

▶ Package and SSO data are in FINAL status for: 36WLCP, 64ucfBGA, 80ctfBGA (IND/AUTO) and 81csfBGA.

New SPI Flash Support

The following flash are supported:

> ▶ Cypress-Spansion (S25FL128L, S25FL512S, S25FL064L, S25FL256S, S25FL256L).

> ▶ ISSI (IS25LP032D).

> ▶ Macronix (MX25L12845G, MX25L12835F, MX66L51235F, MX25L25635F).

> ▶ Micron (MT25QL128).

> ▶ Windbond (W25Q128JV, W25Q128FV, W25Q32JV).

What's New in Diamond 3.10 SP1

This SP1 release of Diamond provides the following new items:

ECP5U12/25 Family Support

> ▶ caBGA256 package is generally available.

> ▶ Family LFE5U-12F-xBG256C/I (x = Grades 6,7,8).

> ▶ Family LFE5U-25F-xBG256C/I (x = Grades 6,7,8).

New SPI Flash Support
The following three Macronix flash (MX25L25635F, MX25L12835F,

▶ MX25L12845G) are supported.

What's New in Diamond 3.10

This release of Diamond provides a variety of new features.

CrossLink Family Support

▶ Power Calculator Improvements - support power pin sharing to be the same voltage for small package

▶ Improved power number calculations - Power Calculator uses 5th order exponential power model

ECP5U/UM/5G Family Support

▶ ECP5 Automotive Devices (ECP5U 12K, ECP5UM 25K/45K)

　　▶ 381caBGA package is generally available

　　▶ Added -7 speed grade

▶ Removal of IBIS_AMI support for ECP5UM/5G families

▶ Power Saving Improvement - allow disabling of INBUF for unused input or output I/Os

MachXO3L/LF Family Support

▶ MachXO3L/LF 9400E caBGA256/400/484 is generally available

▶ Power Saving Improvement - allow disabling of INBUF for unused input or output I/Os

▶ Final characterized data for Package, Timing, SSO and IBIS hardware data files

Supported Devices

Lattice Diamond can be used with either a free license or a subscription license. The two licenses provide access to different device families.

Device Family	Free License	Subscription License
ASC	◄	◄
ECP5U	◄	◄
ECP5UM		◄
ECP5UM5G		◄
LatticeEC™	◄	◄
LatticeECP™	◄	◄

Device Family	Free License	Subscription License
LatticeECP2™	◀	◀
LatticeECP2M™		◀
LatticeECP2S		◀
LatticeECP2MS		◀
LatticeECP3™		◀
LatticeSC™		◀
LatticeSCM™		◀
LatticeXP™	◀	◀
LatticeXP2™	◀	◀
LIFMD (CrossLink)	◀	◀
MachXO™	◀	◀
MachXO2™	◀	◀
MachXO3L	◀	◀
MachXO3LF	◀	◀
Platform Manager™	◀	◀
Platform Manager 2	◀	◀

Updating Projects from an Earlier Version

If you want to work on a design project created with an earlier version of Diamond, start with the following procedures. These procedures adapt the project for the changes in Diamond.

Find out which version of Diamond your project was created with. Then work through the changes for that and every later version, starting with the earliest and going to the most recent. For example, if your project was created with Diamond 1.1, you would start with the changes for 1.1. After completing those changes, you would work on the changes for 1.2, then 1.4, and so on.

When you open a project from Diamond 1.2 or earlier, Diamond opens a dialog box warning that Diamond will automatically move all SDC files to the Synthesis Constraint Files folder in File List view and remove the "Input SDC Constraint File" options from the strategies. If the project is using LSE, the file names will be changed to use an .ldc extension.

Once saved, the project will not be compatible with earlier Diamond versions.

2.2 Projects

ECP5 does not use the CIN port of the CCU2C Carry Chain primitive. This port should not be connected to anything. If the port is connected, the Design Map stage will fail with an error message. If you see such a failure, correct the design in one of the following ways:

▶ Rerun synthesis. This should correct the problem if the CCU2C primitive is part of an IPexpress module.

▶ If the CCU2C primitive was added to your HDL manually, edit the code to remove the connection. See the following examples:

In Verilog:

```
CCU2C addsub_0 (.A0(scuba_vlo), .A1(DataA[0]),
  .B0(scuba_vlo), .B1(DataB[0]), .C0(scuba_vhi),
  .C1(scuba_vhi), .D0(scuba_vhi), .D1(scuba_vhi),
  .CIN(), .S0(), .S1(Result[0]), .COUT(co0));
```

In VHDL:

```
signal tmp: std_logic := 'X';
cnt_cia: CCU2C
  generic map (INJECT1_1=> "NO", INJECT1_0=> "NO",
  INIT1=> X"0000", INIT0=> X"0000")
  port map (A0=>scuba_vhi, A1=>scuba_vhi, B0=>scuba_vhi,
  B1=>scuba_vhi, C0=>scuba_vhi, C1=>scuba_vhi,
  D0=>scuba_vhi, D1=>scuba_vhi,
  CIN=>tmp, S0=>open,S1=>open, COUT=>cnt_ci);
```

2.0.1 Projects

Several strategy options have new default values. If you are using Synplify Pro in integrated mode (running synthesis automatically in Diamond), check that the following settings are still as you want them. Also, check the setting of the Auto Hold-Time Correction option under Place & Route Design. Its default changed to On for all devices. This is still current in Synplify Pro versions.

Table 1: New Default Values for Synplify Pro for Lattice

Option	Before	Now
Fanout Limit is now Fanout Guide	100	1000
Export Diamond Settings to Synplify Pro GUI (new in 2.2)	Not available	No
Fix Gated Clocks and Fix Generated Clocks combined into new Clock Conversion	3 (converts and reports all sequential elements)	True (converts with no report)
Frequency	200	auto (blank means "auto")
Number of Critical Paths	3	blank (unspecified)
Number of Start/End Points	0	blank (unspecified)

Table 1: New Default Values for Synplify Pro for Lattice (Continued)

Option	Before	Now
Output Preference File	False	True
Pipelining and Retiming	False	Pipelining Only
Resolved Mixed Drivers	True	False
Use Clock Period for Unconstrained I/O	True	False

1.4 Projects

For Diamond 1.4 and earlier, there might be some constraints that are not honored because of the Synplify Pro cross-probing feature. This EDIF renaming is usually related to bus names.

If such a problem occurs, you can turn off the renaming feature by placing the following line in the "Command line Options" text box of the Synplify Pro section of the active strategy:

set_option -syn_edif_array_rename 0

1.2 Projects

There were several enhancements for IP and MachXO2.

IP Incompatibilities

SPI4.2 2.7 is not compatible with Diamond 1.3 or later. If you are using this IP, check the Lattice Semiconductor Web site for a more recent version.

MachXO2 Changes

See if your design involves any of the following features:

▶ For EFB modules with user flash memory (UFM), regenerate the module.

▶ For IO_TYPE=PCI33 on a MachXO2-1200 or larger device, check if the CLAMP is using the default setting. With Diamond 1.3 the CLAMP default changes from ON to PCI and the I/O will be placed in bank 2. If you were using the default and still want the setting to be ON, you need to set it explicitly.

▶ For PCI33 MT 6.5 and PCI33 T 6.4 IP, either set the CLAMP to ON explicitly or choose a bigger package (256 or more).

1.1 or 1.0 Projects

There were several enhancements for IP and MachXO2.

IP Incompatibilities

The following IP versions are not compatible with Diamond 1.2 or later. If you are using any of these IP, check the Lattice Semiconductor Web site for a more recent version.

▶ Convolution Block Encoder 3.6   ▶ Interleaver Deinterleaver 3.5

▶ DDR1 6.9   ▶ PCI_MT_33 6.4

▶ DDR2 7.1   ▶ PCIe RC Lite 1.2

▶ DDR3 1.2.1   ▶ Tri-Speed MAC 3.4

▶ DDR1_CP 1.1 with MachXO2   ▶ Viterbi Block Decoder 4.6

▶ DDR2_CP 1.1 with MachXO2

MachXO2 Support

Some aspects of the software support for MachXO2 designs have been improved. See if your design involves any of the following features:

▶ The 4K/7K design with PLL has a CIB-to-PLL jump change. If you are using this design, recompile it.

▶ The EFB simulation model has changed. If you are using the EFB module, rerun your simulation tests to see more accurate results.

▶ In the DDR_GENERIC module of IPexpress, the GDDRX1_RX.Aligned with PLL interface is no longer supported. If you are using such a module, use IPexpress to regenerate it without the PLL option.

Also, MachXO2 has IP evaluation capability and TransFR mode for all I/Os.

Other Information Resources

Other available information resources for the Diamond software include the following.

▶ General Information: General information on Lattice Diamond can be found on the Lattice Web site at:

www.latticesemi.com/latticediamond

▶ Online Help: Start Lattice Diamond and choose **Help > Lattice Diamond Help**.

▶ *Lattice Diamond User Guide*: This document can be found from a link on the Start Page view.

▶ Training Videos: Several short videos are available on different aspects of the Lattice Diamond software. These can be viewed online at:

www.latticesemi.com/latticediamond

Click the **Videos** tab.

System Requirements

The basic system requirements for Lattice Diamond are:

▶ Intel Pentium or Pentium-compatible PC, or AMD Opteron system support (Linux only)

▶ CPU with the SSE3 instruction set to run the Aldec Active-HDL Lattice Edition simulator

▶ One of the following operating systems:

　▶ Windows 7 (64-bit), Windows 8/8.1 (64-bit), or Windows 10 (64-bit).

　▶ Red Hat Enterprise Linux 6.7/7.3. The host operating system is supported in 64-bit only.

▶ Approximately 5.75 GB free disk space

▶ RAM adequate for your FPGA design. For guidelines see "Memory Requirements" on page 8.

▶ Network adapter and, for a floating license, network connectivity

A node-locked license is based on the physical (hard-coded) address provided by the network adapter. Network connectivity is not required for a node-locked license. In the absence of a network connection, you can install the NWLink IPX/SPX protocol to force recognition of your NIC card ID (see the Installation Notice).

A floating license requires access to the license server, so both a network adapter and connectivity are required.

▶ JavaScript-capable Web browser

▶ Microsoft Internet Explorer 8 or higher if using the included Aldec Active-HDL Lattice Edition simulator

▶ Acrobat Reader 5.0 or later

Memory Requirements

Table 2 lists the minimum memory requirements and the recommended memory for the Lattice Semiconductor devices supported by Diamond.

Designing for LatticeECP3 with more than 95K LUT on a Windows system requires a 64-bit operating system.

Table 2: Recommended Memory

Device	Size	64-Bit Operating Systems	
		Minimum	Recommended
ECP5U/UM/UM5G	All	4 GB	6 GB
LatticeEC, LatticeECP	Up to 20K LUT	1 GB	1.5 GB
	Up to 50K LUT	1.5 GB	2 GB
LatticeECP2/M	Up to 20K LUT	1.5 GB	2 GB
	Up to 50K LUT	2 GB	3 GB
	Up to 100K LUT	2 GB	4 GB
LatticeECP3	Up to 95K LUT	4 GB	6 GB
	Up to 150K LUT	6 GB	8 GB
LatticeSC/M	Up to 40K LUT	1.5 GB	2 GB
	Up to 115K LUT	2 GB	5 GB
LatticeXP, LatticeXP2	Up to 20K LUT	1 GB	1.5 GB
	Up to 50K LUT	1.5 GB	2 GB
MachXO, MachXO2, MachXO3L	All	512 MB	1 GB
LIFMD (CrossLink)	All	512 MB	1 GB
Platform Manager, Platform Manager 2	All	512 MB	1 GB

Issues Fixed

The following known issues are fixed with this release. Their workarounds are no longer needed. For the complete list of known issues, see
www.latticesemi.com/view_document?document_id=50676

External Memory non-Support for Advanced SPI Flash

External memory is not supported for MachXO2 devices but the operation was completed successfully in the deployment tool. Such an operation is now prohibited.

Versions affected: Diamond 3.7
Devices affected: MachXO2
Fixed_3.10
CR126188

Error message "FTD2XX.dll is missing"

When batch programming command was issued with USB cable type, above error message was issued.

Versions affected: Diamond 3.7
Devices affected: All
Fixed_3.10
CR126554

Support for protecting golden image of STMicro SPI flash

The Diamond programmer formerly did not support protecting/securing golden pattern sectors for STMicro SPI flash SPI-M25P64.

Versions affected: Diamond 3.8
Devices affected: LatticeECP3
Fixed_3.10
CR127215

Known Issues

Following are known issues with this release and workarounds for them. For the complete list, see:
www.latticesemi.com/view_document?document_id=50676

Missing feature in PMI FIFO modules for VHDL

An error occurs when using the VHDL version of the generated code.The workaround is to is to use the Verilog version.

Versions affected: Diamond 3.10
Devices affected: All
CR128114

Some Intellectual Property (IP) modules may not meet targeted timing on LatticeECP3 or LatticeXP2 devices

Some IP modules may not meet targeted fMAX when used with LatticeECP3 or LatticeXP2 devices. The following table lists the IP and affected devices:

IP	LatticeECP3	LatticeXP2
2.5G Ethernet PCS	◀	
JESD207	◀	
PCI Master Target 66		◀
PCI Target 66		◀
PCS PIPE	◀	
SRIO	◀	
DDR2 SDRAM Controller	◀	

If you need assistance with this issue, contact Lattice Technical Support.

Versions affected: Diamond 3.10
Devices affected: LatticeECP3, LatticeXP2

Some CrossLink Soft IPs will fail during implementation if missing DCS Initialization file

The following Crosslink Soft IPs require a user-created DCS Initialization file during IP generation. If the file does not exist at the location path entered by the user in the IP generation GUI, an empty DCS Initialization file will be automatically generated. Then the IP generation can still go through without issue. However, this empty DCS Initialization file will cause issues when users try to run through the implementation flow later on. The following IPs are affected:

- ▶ CMOS to DPHY (in DSI mode)
- ▶ CSI-2/DSI D-PHY Transmitter (in DSI mode)
- ▶ DSI to DSI
- ▶ FPD-LINK to DSI
- ▶ DSI to Dual DSI Bandwidth Reducer

It is also important to note that when generating the IP by loading the .sbx file, users need to make sure the valid DCS Initialization file still exists in the same location previously specified.

For information on how to create a DCS Initialization file, please refer to each Soft IP's User Guide.

Versions affected: Diamond 3.10
Devices affected: CrossLink
CR127902

Median Filter IP cannot install

This IP was supported in Diamond 1.3. It is currently not supported for 64-bit platforms. Contact Lattice Technical Support if using this IP.

Versions affected: Diamond 3.10
Devices affected: All
CR127595

I/O Power or Total Power does not change with INBUF On or Off

For I/Os configured as output-only mode (with tristate control), or as unused I/Os, the input buffer can be drawing current from VCCIO if not disabled (with the INBUF option to be ON) in the Diamond software. The amount of current depends on the voltage on the pin. If the voltage on the pin (when the output is tri-stated, or the pin is unused) is not pulled up to VCCIO, or is pulled down to GND, this input buffer current can be observed on VCCIO. The Power Calculator does not include this current, and is calculated based on the assumption that these inputs are pulled to either VCCIO or GND.

Versions affected: Diamond 3.10
Devices affected: MachXO2, MachXO3L/LF, ECP5U/UM/5G
CR128098

Contacting Technical Support

FAQs   The first place to look. The Answer Database on the Lattice Semiconductor Web site provides solutions to questions that many of our customers have already asked. Lattice Applications Engineers are continuously adding to the Database.

Technical Support Assistance   Submit a technical support case via www.latticesemi.com/techsupport.

For Local Support   Contact your nearest Lattice Sales Office

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