THE INDUSTRY CASE FOR DISTRIBUTED HETEROGENEOUS PROCESSING

A Lattice Semiconductor White Paper

December 2016

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Introduction

Pushing buttons to interact with consumer electronics is a thing of the past. Human to machine interaction has changed dramatically over the past few years and continues to evolve. This paper will provide examples of the changing nature of human machine interface. In addition, the reader will better understand a specific architecture that offers an energy efficient solution to improve the user experience for battery-powered applications. This architecture is comprised of a power efficient heterogeneous processing element using an FPGA fabric.

Human Machine Interface (HMI) Trends

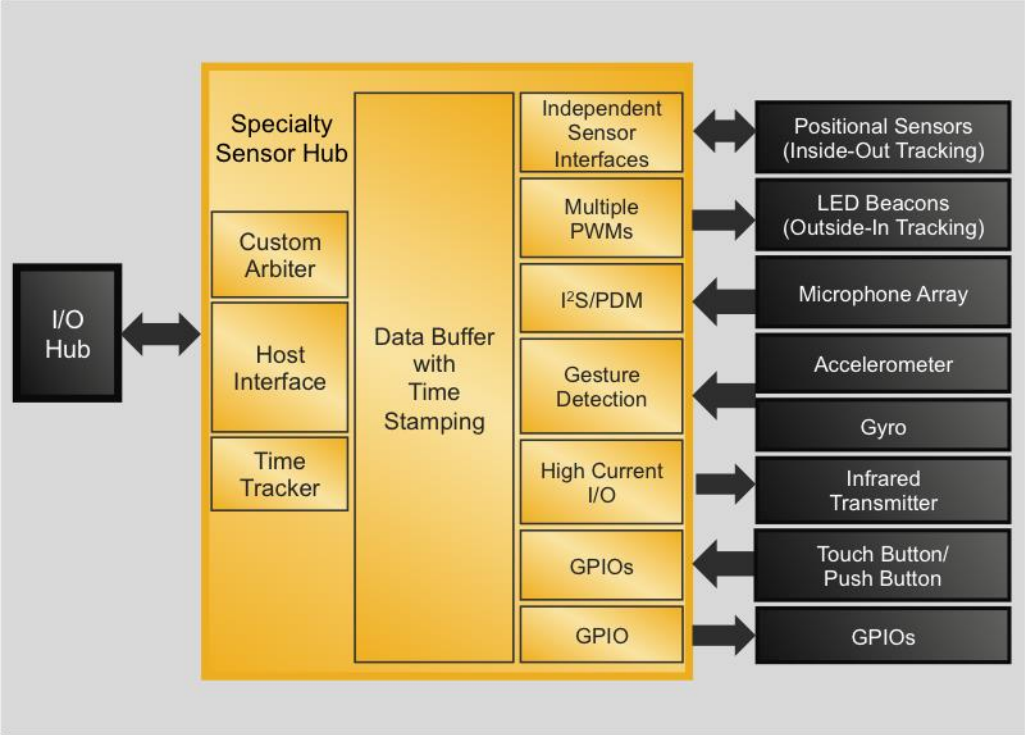
Most mobile devices enter a sleep or low power mode until they are ready to be utilized, so the first interaction with your device is to wake it up. This "wake up" can occur by wrist rotation, shaking, single or double tapping, incoming calls or messages, mechanical button presses, and unique phrases, gestures or sounds such as a clap or a snap. Each "wake-up" methodology requires a sensor and a monitoring device for the specific action. The "wake up" operation has to happen with extremely low power consumption. Today's low power FPGAs consume around 100uW of power in always-on, always-aware situations with a trend towards drastically lower power consumption in the future.

The variety of sensors needed to implement innovative HMI solutions are rapidly changing the I/O landscape. Today's mobile devices require ever faster I/O speeds. The proliferation of low cost sensors over the past few years and the adoption of new, higher performance interfaces have increased the computational demands of these systems. So, too, has the escalating demand for always-on functionality. Sensors in a wide variety of applications ranging from drones, phones, wearables, and industrial equipment are constantly collecting a large amount of data. System designers need to speed up data processing time while reducing system power to maintain the consumer's demand for a full day of device operation without re-charging.

A more holistic, systems-based approach to mobile system design is required instead of the traditional CPU-centric design methodology. System designers need to take advantage of the diversity of processors to maximize energy efficiency while addressing the escalating computational requirements of today's mobile devices.

Welcome to the Era of Distributed Heterogeneous Processing (DHP)

DHP defines a new energy-efficient approach of computing algorithms locally rather than in the Cloud using dissimilar processors instead of power-hungry APs. With this approach, designers can use parallel processing techniques to address new demands for complex co-processing. With DHP, mobile system designers can perform repetitive number-crunching tasks locally on Digital Signal Processors (DSPs) that offer better power efficiency and frees the applications processor (AP) from some processing tasks, allowing it to remain in sleep mode longer to conserve system power and extend battery life.



Distributed Heterogeneous Processing – Localized processing for improved power efficiency and quicker response time

More Memory, More DSPs

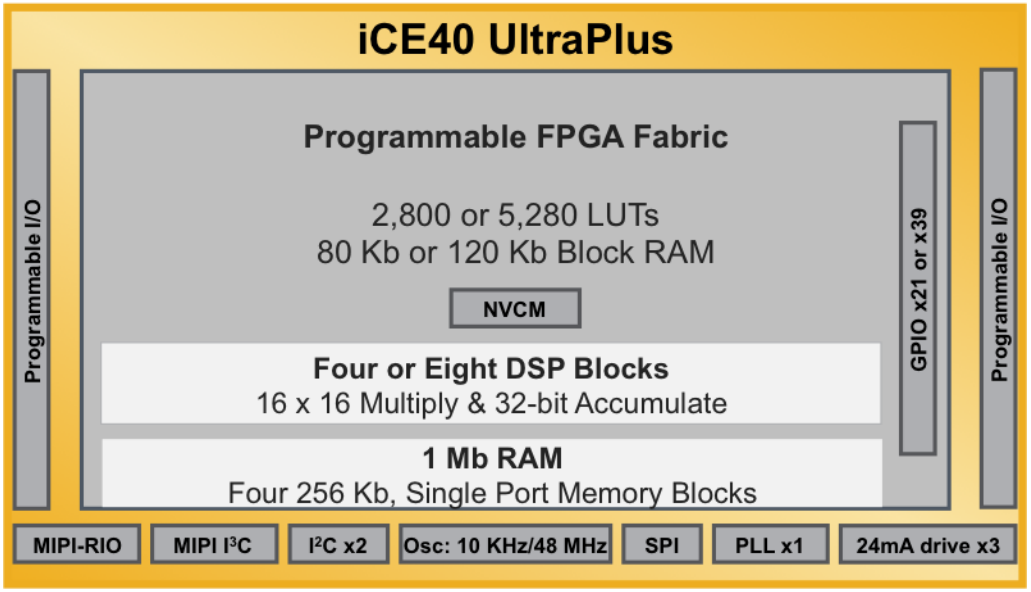
Lattice Semiconductor has added a new product to its iCE40 Ultra family of FPGAs to address DHP computing needs. The new iCE40 UltraPlus device helps designers craft more energy-efficient solutions with eight times the memory and twice the number of DSPs as previous generation products. Even with the increased resources, the new

iCE40 UltraPlus device only draws 75µA of static current, while its predecessor draws 71µA.

Available in multiple package sizes, the iCE40 UltraPlus FPGA device will allow designers in today's highly competitive mobile markets to quickly build unique and compelling solutions that meet the rigorous processing demands of next generation consumer, mobile, IoT edge, and industrial products.

At the heart of this new FPGA is Lattice's highly power efficient iCE40 product line. The iCE40 Ultra family combines low power operation with extensive integrated functionality, including multiple 16 x 16 multiplier blocks, in an extremely small footprint.

The new iCE40 UltraPlus builds on this foundation by providing all of the critical elements needed to support the most energy efficient parallel processing solutions for repetitive number crunching. Combining 1.1 Mbit of low power SP-SRAM, eight multiply/accumulate blocks for signal processing, up to 5280 LUTs for custom logic, and non-volatile configuration memory for instant-on applications, the iCE40 UltraPlus solution offers the ideal blueprint for designers building always-on sensor buffers, acoustic beamforming audio subsystems, and other repetitive compute heavy applications. This same device can also be used to support a variety of bridging, buffering and display applications to accelerate innovation in next generation mobile and industrial applications.



Lattice iCE40 UltraPlus Block Diagram

In addition, the new iCE40 UltraPlus device adds programmable I/Os for design flexibility, an I^3C interface (a new high bandwidth data and control interface for sensors defined by MIPI) to support always-on camera applications, and built-in oscillators to reduce power and BOM cost.

Complementing that extensive feature set, the solution is designed to function in power-stingy, space-constrained consumer applications by consuming as little as 75 µA in static power mode and coming in packages as small as 2.15 x 2.55 mm. The new device is also available in a QFN package to support lower cost PCB assembly used in industrial and other consumer applications.

To accelerate product development, Lattice Semiconductor is supporting the iCE40 UltraPlus FPGA family with a comprehensive tool set as well as evaluation samples and boards. Another way Lattice's iCE40 UltraPlus is helping designers get to market quickly is by recognizing the prevalent skill sets of embedded systems developers. Despite their long history and widespread adoption, FPGAs remain a less familiar product to designers than MCUs. Not surprisingly, far more designers today know how to program an MCU than an FPGA. Developers have responded to this by implementing soft core processors into the iCE40 UltraPlus device. In fact, the large amount of SPRAM and hardened DSP blocks make the iCE40 UltraPlus an ideal platform for soft processor implementations. To support these solutions the RISC-V organization (www.riscv.org) has released an open sourced, extensible, highly efficient processor. At a recent RISC-V workshop two companies introduced RISC-V implementations on Lattice's iCE40 UltraPlus devices using a combination of RISC-V open source software tools and Lattice FPGA tools. These companies have demonstrated that they can develop specialized soft processors with tightly integrated parallel accelerators with minimal development costs. This brings unprecedented flexibility to engineers with existing MCU skillsets.

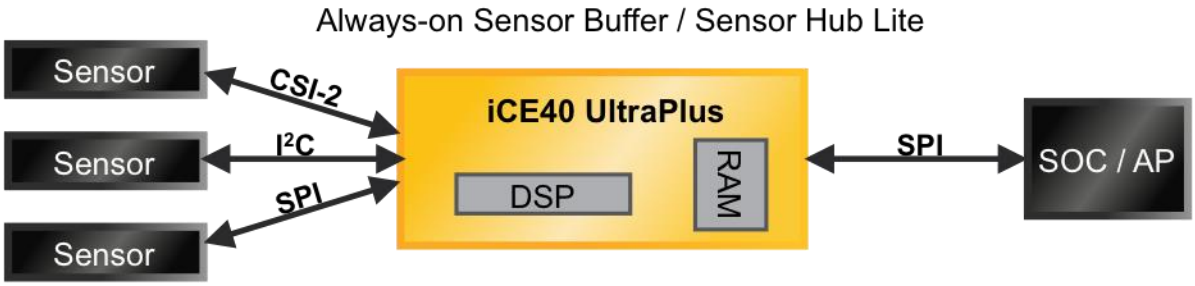
Potential Applications

The embedded DSPs in the iCE40 UltraPlus gives designers the ability to compute higher quality algorithms while the 1 Mbit of on-chip SRAM allows the system to buffer data longer in lower power states. In a growing number of systems, designers need a device that serves as a coprocessor to the AP and can process and analyze data while the system is off and then wake up the AP to perform more complex functions.

Potential applications are virtually limitless. For example, many solutions in the wearable or white goods markets need a device that can serve as both a large frame buffer and an interface bridge. With its extensive on-chip SRAM, the iCE40 UltraPlus FPGA can support an always-on display while the AP remains in sleep mode. At the same time the iCE40 UltraPlus can serve as an interface bridge between the MCU and

the display. The FPGA offers a flexible fabric for custom graphics acceleration as well as I/O expansion by supporting MIPI DSI or parallel interfaces. This combination of a display driver and graphics engine mirrors the performance of a low cost GPU, but at significantly reduced power.

In another application, many battery-powered devices need an always-on sensor buffer to perform sense and detect acceleration while the AP is in sleep mode. These devices must mask false wake-up calls to permit the AP to remain in sleep mode longer. In this application, the iCE40 UltraPlus FPGA sits between various sensors and the AP and processes wake up calls like double tap or “shake-to-wake” techniques used on pedometers. Similar applications could include motion detection, fingerprint, gesture or iris scan.



Always-on Sensor Buffer

Each of these functions require a two-step process. First, the system must determine if the appropriate wake-up action did occur. Secondly, the system must determine if the gesture or fingerprint used was correct to gain access to the system. In the past if the appropriate action did occur, the FPGA would wake up the AP. With its extensive on-chip memory, the iCE40 UltraPlus FPGA can now perform both functions before system wake-up, allowing the AP to remain in sleep mode longer.

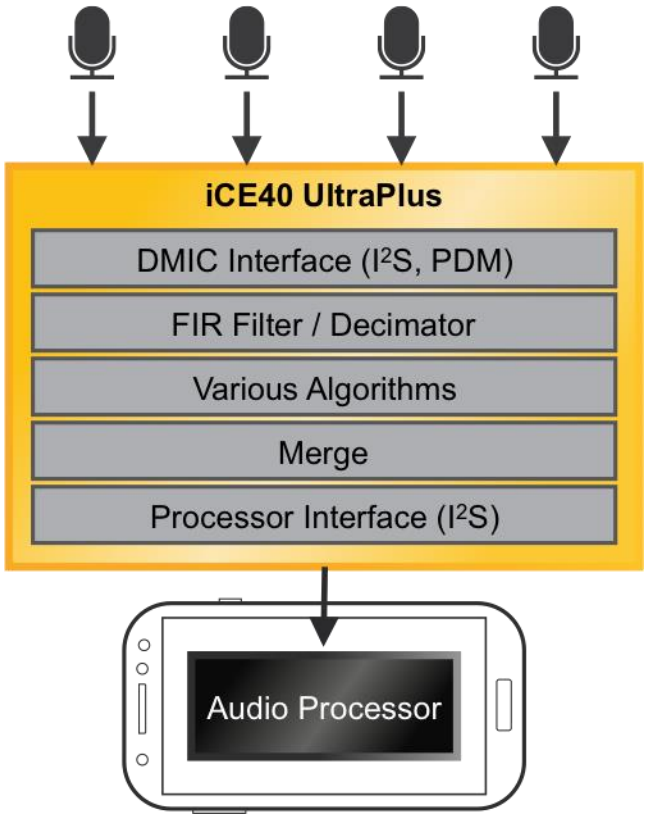
A third potential use for the iCE40 UltraPlus FPGA lies in acoustic beamforming applications. Today’s systems often require enhanced levels of audio processing capable of isolating specific audio signals from highly noisy environments. In a typical application the system must detect and accept commands from one person’s voice in a room where multiple people are talking.

Using multiple microphone arrays, beamforming technology detects a specific voice and filter out unwanted noise. Amazon’s recently introduced Echo platform offers an excellent example. Using beamforming technology and seven mics, this hands-free speaker can discern the user’s voice from across the room even when music is playing.

However, most APs are designed to only support the use of two microphones. Moreover, these systems must typically be always on and operate from battery power, a difficult task for power-hungry APs. So how does the designer implement a

beamforming solution that may require inputs from up to seven different mics and do it 24 x 7 while consuming minimal power?

One way is to interface the microphone array to a low power iCE40 UltraPlus FPGA.



Microphone Array Beam Forming

The solution depicted above supports multiple digital mic PDM inputs. On-chip multiply and accumulate (MAC) blocks can be used for PDM decimation and filtering and the FPGA's deep memory supports microphone delay lines. This approach also gives system designers more latitude to innovate. They can use on-chip MACs and the FPGA fabric to build highly flexible beamforming filters or noise cancelling systems as well as audio equalization capabilities.

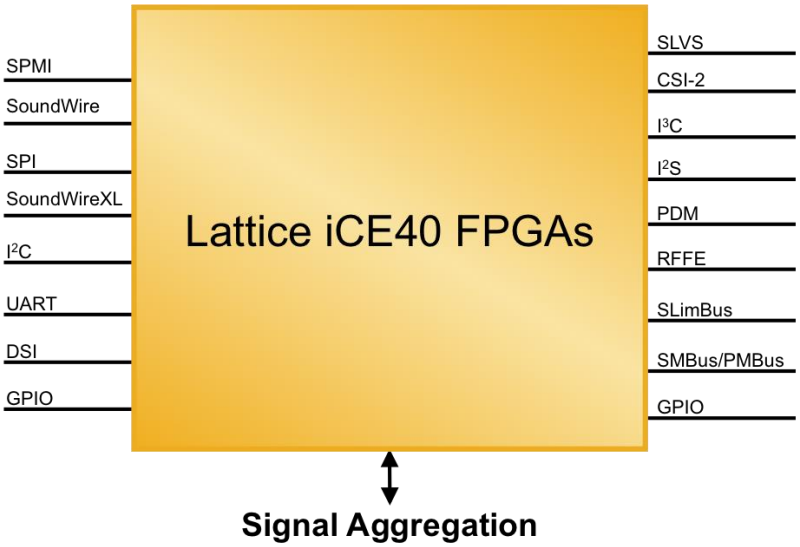
The iCE40 UltraPlus FPGA interfaces to the acoustic processor via various industry interface options, such as I^2S, soundwire, SlimBus, etc. As with any FPGA-based solution, designers can use the embedded DSP, logic and memory resources of the chip to build highly customized solutions and go to market quickly.

Signal Aggregation to the Rescue

The resources embedded in Lattice's iCE40 UltraPlus FPGAs can also be used to dramatically simplify printed circuit board (PCB) layout in mobile devices. The rapid proliferation of low-cost sensors and the emergence of always-on monitoring and context-aware computing have brought new challenges to PCB designers. Every sensor in this new generation of mobile devices must communicate with the applications processor (AP). More often than not these systems employ a wide array of interfaces from I^2C, I^3C and SPI to UARTs and MIPI DPHY CSI-2. The designer might have to manage up to 40 signals coming from the device's sensors to the AP in a single product.

Typically, mobile devices have two PCBs around the battery. These PCBs are connected with a flex cable that typically offers limited EMI shielding. Usually that flex cable is limited to two layers to minimize cost. Thus, the board layout engineer must grapple with the challenging job of routing up to 40 signals across a two-layer cable with a high propensity for ringing and other reliability issues.

One way to simplify this task is to employ the unique attributes of Lattice's iCE40 UltraPlus FPGA to aggregate the many signals in these systems. By mounting the iCE40 UltraPlus FPGA next to the sensors, the PCB designer can replace multiple disparate signals to the AP with a simple one or two pin interface.



Lattice iCE40 FPGAs Offer a Flexible I/O Hub for Signal Aggregation and Quick Layout Adjustments

But the benefits of signal aggregation don't end there. As previously discussed each Lattice iCE40 UltraPlus FPGA offers significant computational resources. The on-chip

Look Up Tables (LUTs) and DSPs can be used to perform more localized DHP. For example, the acoustic beamforming systems must wake up the AP to detect and verify the key phrase in a command. Using signal aggregation, however, designers can employ the local resources of the iCE40 UltraPlus FPGA to detect and verify the key phrase before waking up the AP. This approach not only offers the user a faster response time to the key phrase, it also improves system power efficiency by keeping the AP in sleep mode longer.

Signal aggregation dramatically simplifies PCB layout for the AP board. By minimizing the number of signals routed across the board, the designer can more easily comply with complex layout rules and complete the board layout faster.

Last but not least, signal aggregation with iCE40 UltraPlus brings tremendous design flexibility. Designers can reprogram the location of any interface on the iCE40 UltraPlus to simplify board layout. In this case, the ideal board layout dictates FPGA pinout not the other way around.

Conclusion

The current revolution in I/O interfaces promises to bring exciting new capabilities to mobile system designs. The proliferation of low-cost sensors and the widespread adoption of “always-on” functionality will enable designers to personalize devices like never before. But to implement these new capabilities, designers must adopt a heterogeneous processing approach for mobile devices that utilizes different processing blocks that preserve battery life. By combining the DSP blocks and on-chip memory that designers need, Lattice Semiconductor’s iCE40 UltraPlus FPGAs will enable OEMs to add these compelling new features while meeting the challenging power and computational requirements of next generation mobile devices.

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