March 1, 2016

Subject: PCN# 02A-16 ECP5/ECP5-5G updates on Diamond v3.7 release and datasheet update

Dear Lattice Customer,

Lattice is providing this notification regarding Lattice ECP5™ product family. It is relating to specific updates in the Lattice Diamond® v3.7 software release. The details are as listed below.

Affected Products

All products under ECP5 product family.

Areas Impacted by the Update

- Embedded Block RAM (EBR): Low DPM data corruption correction under certain use case of the EBR. Diamond v3.7 completely corrected the use case condition for data corruption. The impact of the update is that the following timing parameters surrounding the EBR were affected.
    - Clock to Output timing for the non-registered data output in the order of <0.5 ns. Registered EBR output f_{MAX} remains unchanged.
    - Setup and Hold time for the EBR control signals (WE, CS) in the order of <0.14 ns.
    - Reset Recovery time for the EBR registers in the order of <1.4 ns
- Distributed RAM: Certain placement and packing of Distirbuted RAM into logic Slices cause functional error. Distributed RAM placement and port assignment algorithm was updated in Diamond v3.7. Previous functional error related to Distributed RAM functions are corrected. Note that user logic functions that are emulated with the Distributed RAM are also impacted.
- sysDSP™: DSP block reset port and Pre-Adder port assignment were incorrect for certain inference of DSP block implementation. Diamond v3.7 along with the subsequent Service Pack (SP), to be released by end of March 2016, corrects this issue. Contact your local Field Applications Engineer if SP is needed before the end of March 2016.
- Datasheet change for the Power Up Sequence for ECP5UM device family only:
    - Previous version DS1044 v1.5 sequence specifies V_{CCAUXA}, before the V_{CCA}/V_{CCHRX}/V_{CCHTX} are powered up.
    - Updated version DS1044 v1.6 sequence specifies V_{CCA}, before V_{CCAUXA}

Expected User Action for Impacted Areas

It is recommended that any current and future ECP5 designs use the Diamond v3.7 or later version. For existing ECP5 designs, follow the guideline provided below.

- EBR: Check the current ECP5 design netlist via trace analysis on Diamond v3.7. If timing is met, simply re-generate the new bitstream with command line bitgen in Diamond v3.7. Use the new bitstream for the future

build of the ECP5. If there are any timing errors, the customer will have to correct the timing errors before re-generating the bitstream.

- Distributed RAM: Regenerate bitstream with Diamond v3.7 only if there is functional errors with the current user design on ECP5
- sysDSP: Regenerate bitstream with Diamond v3.7 only if there is functional errors with the current user design on ECP5
- Datasheet change: Follow the updated version v1.6 power sequence requirement. The consequence of not following the specified sequence is I_{CCHRX} could be as high as 140mA during power up sequence.

Response

These changes are effective immediately.

Lattice PCNs are available on the Lattice website. Please sign up to receive e-mail PCN alerts by registering here. If you already have a Lattice web account and wish to receive PCN alerts, you can do so by logging into your account and making edits to your subscription options.

Contact

If you have any questions or require additional information, please contact pcn@latticesemi.com.

For technical support please contact through www.latticesemi.com/techsupport.

Sincerely,

Lattice Semiconductor PCN Administration