SERDES Eye Demo for the ECP5/ECP5-5G Versa Development Kit

User Guide

FPGA-UG-02166-1.4

July 2022

Disclaimers

Lattice makes no warranty, representation, or guarantee regarding the accuracy of information contained in this document or the suitability of its products for any particular purpose. All information herein is provided AS IS, with all faults and associated risk the responsibility entirely of the Buyer. Buyer shall not rely on any data and performance specifications or parameters provided herein. Products sold by Lattice have been subject to limited testing and it is the Buyer's responsibility to independently determine the suitability of any products and to test and verify the same. No Lattice products should be used in conjunction with mission- or safety-critical or any other application in which the failure of Lattice's product could create a situation where personal injury, death, severe property or environmental damage may occur. The information provided in this document is proprietary to Lattice Semiconductor, and Lattice reserves the right to make any changes to the information in this document or to any products at any time without notice.

Contents

Figures

Tables

1. Introduction

This document provides technical information and instructions on the ECP5/ECP5-5G SERDES Eye Demo. The demo has been designed to demonstrate the performance of the ECP5/ECP5-5G SERDES I/O at 3.125 Gbps. The document provides a description as well as instructions for running the demo using the ECP5/ECP5-5G Versa Development Kit.

2. Demo Package

The demo package includes the following

- Verilog source code for the FPGA design
- Lattice Diamond® project file and preference file for the demo project

3. Hardware Requirements

- ECP5/ECP5-5G Versa Development Board
- 12 V DC power supply for the ECP5/ECP5-5G Versa Development Board
- USB cable for programming the ECP5/ECP5-5G device
- Eye viewing instrument - DCA, DSO, etc. (not provided)
- SMA cables (not provided)

4. Software Requirements

- Lattice Diamond design software, version 3.8 or later
- Programmer software for bitstream downloading

5. SERDES Eye Demo Design Overview

A pattern generator (PRBS or counter pattern) transmits parallel data to a PCS/SERDES. The PCS SERDES channels serialize the data in the transmit direction and de-serialize it in the receive direction. This device has two PCS dual and one of them (Dual #0 channel #1) is used for this demo. The demo is generated at 3.125 Gbps per channel. A SERDES debugger is instantiated in the design and the user can access SERDES registers with it in Reveal Analyzer.

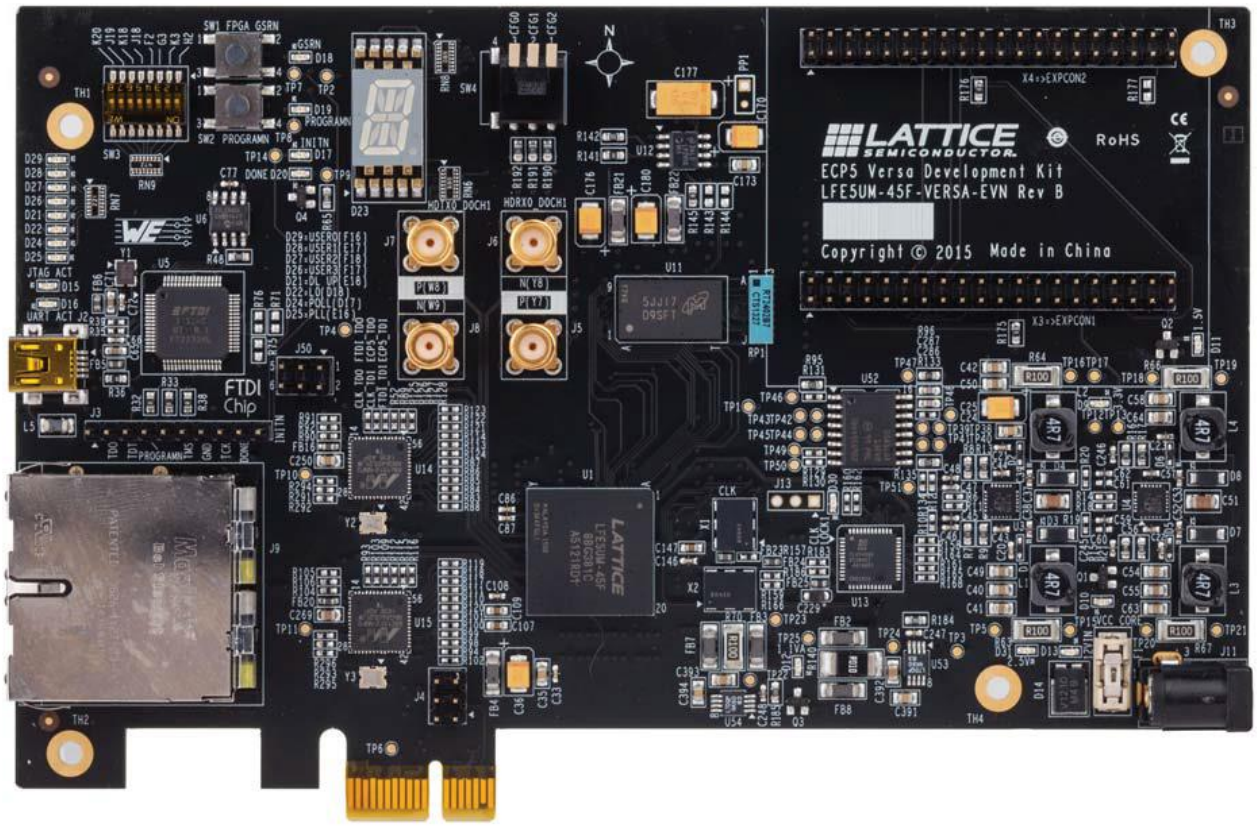

Figure 5.1. ECP5 Versa Development Board

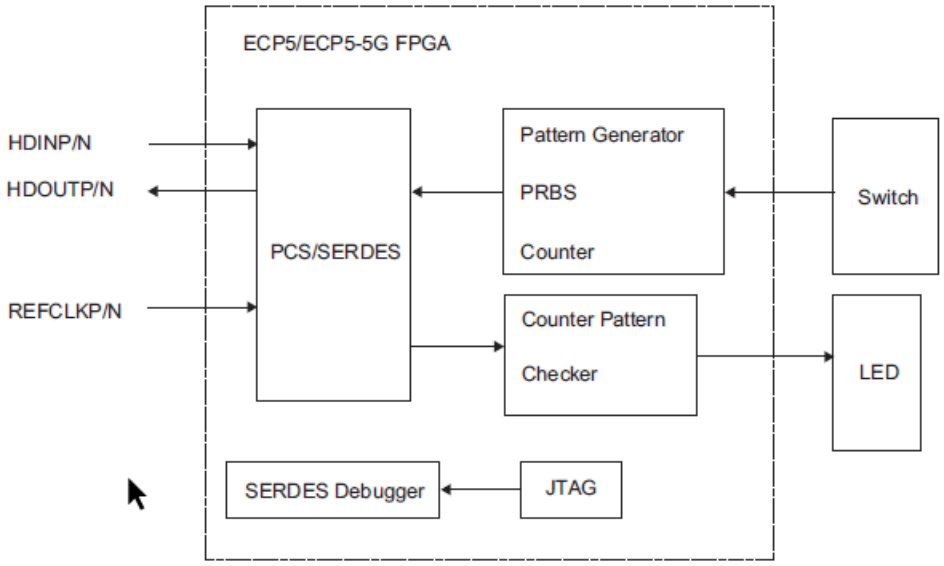

Figure 5.2. SERDES Eye Demo Design Block Diagram

5.1. Clock Sources

The SERDES reference clock is driven by a differential clock input. The reference clock frequency is 156.25 MHz and is from the ispClock™5406D device (U13 on the ECP5/ECP5-5G Versa Development Board). Internally to the PCS, the reference clock is multiplied by a factor of 20 to generate the 3.125 Gbps per channel data rate. At the PCS/FPGA interface, a 20-bit data interface is used. This requires 156.25 MHZ receive and transmit clocks for user logic.

6. Port Assignments and Descriptions

Table 6.1. FPGA Demo Design Ports

Port Name	Direction	Description	Board Connection
rstn	Input	Asynchronous reset for FPGA	GSRN button on board, SW1
ref_clk_refclk	Input	Reference clock for SERDES	From ispClock5406D
test1_hdin	Input	SERDES input	SMA J5 and J6
test1_hdout	Output	SERDES output	SMA J7 and J8
sw[1:0]	Input	DIP switch on board	SW3 #8, #7
led[7:0]	Output	LEDs on board	
HB	Output	Heartbeat LED indicating demo is active	Dot on segment LED D23
X2_EN	Output	Enable for X2 Oscillator	Pin 1 of X2 Oscillator
CLK_RESETn	Output	Reset signal for ispClock5406D	To ispClock5406D

Table 6.2. DIP Switch Definitions

SW3 On Board	Position Definition	Description
#8	OFF	PRBS pattern generator
	ON	Non-PRBS pattern generator
	When #8 is ON	
#7	OFF	Fixed non-counter pattern
	ON	Counter pattern

Table 6.3. LED Definitions

LED On Board	Description
D25	PLL loss of lock if lit
D24	CDR loss of lock if lit
D29	Counter pattern detected if lit
Dot on segment LED D23	Indicate SERDES TX parallel clock available if blinking

7. Demo Package Directory Structure

The demo bitstreams for the ECP5 Versa Development Board are located in \SERDES_eye_demo\bitstream\SERDES_ECP5. The demo bitstreams for the ECP5-5G Versa Development Board are located in \SERDES_eye_demo\bitstream\SERDES_ECP5_5G.

The Diamond project for the ECP5 Versa Development Board is located in SERDES_eye_demo\ SERDES_project\ECP5_SERDES. The Diamond project for the ECP5-5G Versa Development Board it is located in \SERDES_eye_demo\SERDES_project\ECP5_5G_SERDES.

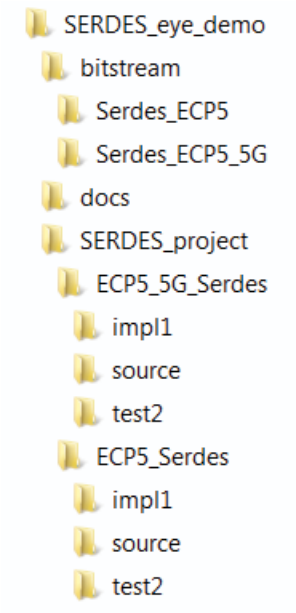

Figure 7.1. SERDES Demo Package Directory Structure

8. Running the Demo

8.1. Board Setup

In addition to the user logic design itself, a Diamond software feature called SERDES Debug can be used to change the SERDES register settings. To make use of this feature, a SERDES Debugger has been included in the demo design. With SERDES Debug included, the following evaluations can be done with this demo design:

- SERDES TX only for eye diagram viewing. The different data patterns are generated in the FPGA as defined by the DIP switches. In SERDES Debug GUI, some SERDES TX register values can be changed, such as differential amplitude, output termination and De-emphasis.
- SERDES TX > SERDES RX loopback. The loopback connection can be either outside of FPGA (external loopback) or inside FPGA (internal loopback). In other words, user has options of either using SMA cables to connect pair J5/J6 with J7/J8 or loopback mode of TX output to RX from SERDES Debug GUI. Some SERDES RX register values can also be changed, such as input termination, AC/DC coupling, and equalization parameter settings.

With the provided demo bitstream, both of the above evaluations can be done. The SMA cables need to be connected as follows:

- For eye diagram viewing, SMA cables need to connect J7/J8 pair to a DCA or DSO.
- For TX > RX external loopback, SMA cables need to connect pair J5/J6 with J7/J8.
- For TX > RX internal loopback, SMA cables are not needed.

8.2. Device Programming

To program the device:

1. Before the board is powered up:

   J50 should have three separate jumpers connecting pin #1 and pin #2, pin #3 and pin #4, and pin #5 and pin #6. This puts ECP5/ECP5-5G and ispClock™5406D devices in the JTAG scan chain. See EB98, ECP5 Versa

   Development Board User Guide or EB103, ECP5-5G Versa Development Board Guide for more details.

   DIP switch SW3 should have all positions to OFF.
2. Power up the board with 12 V power supply. Connect the board to a PC with a USB cable.
3. Launch the Programmer software.

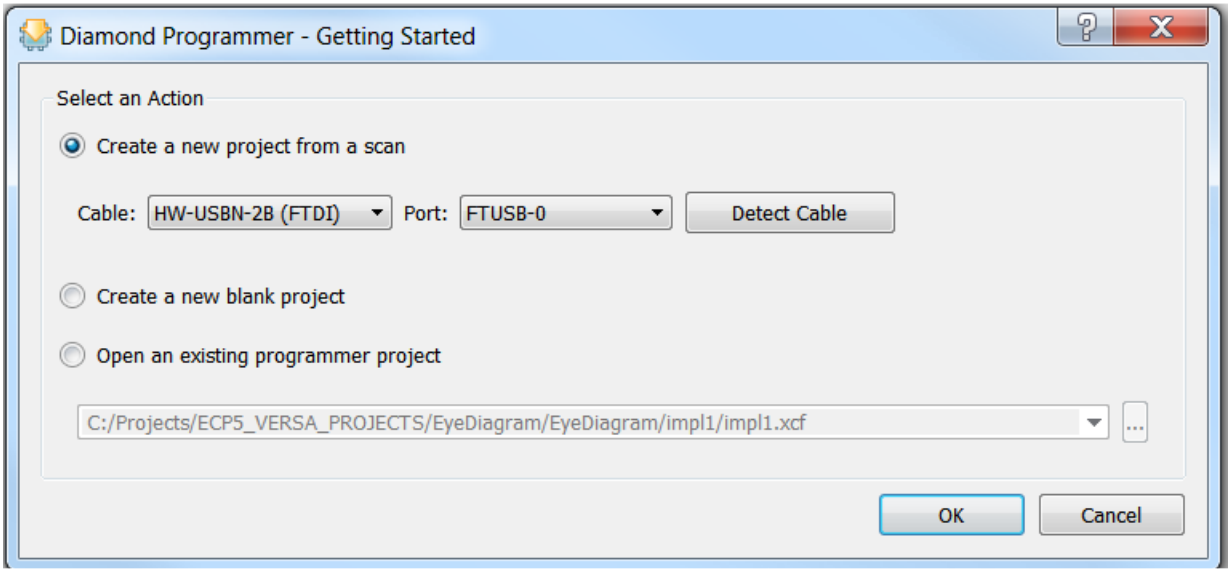

Figure 8.1. Getting Started

4. Scan the JTAG chain by selecting the **Scan** button if the device is not detected. There are two devices in the chain, one is ECP5UM (ECP5) or ECP5UM5G (ECP5-5G) and the other is ispCLOCK.
5. Select the **LFE5UM-45F** device for ECP5UM device family or **LFE5UM5G-45F** device for ECP5UM5G device family.

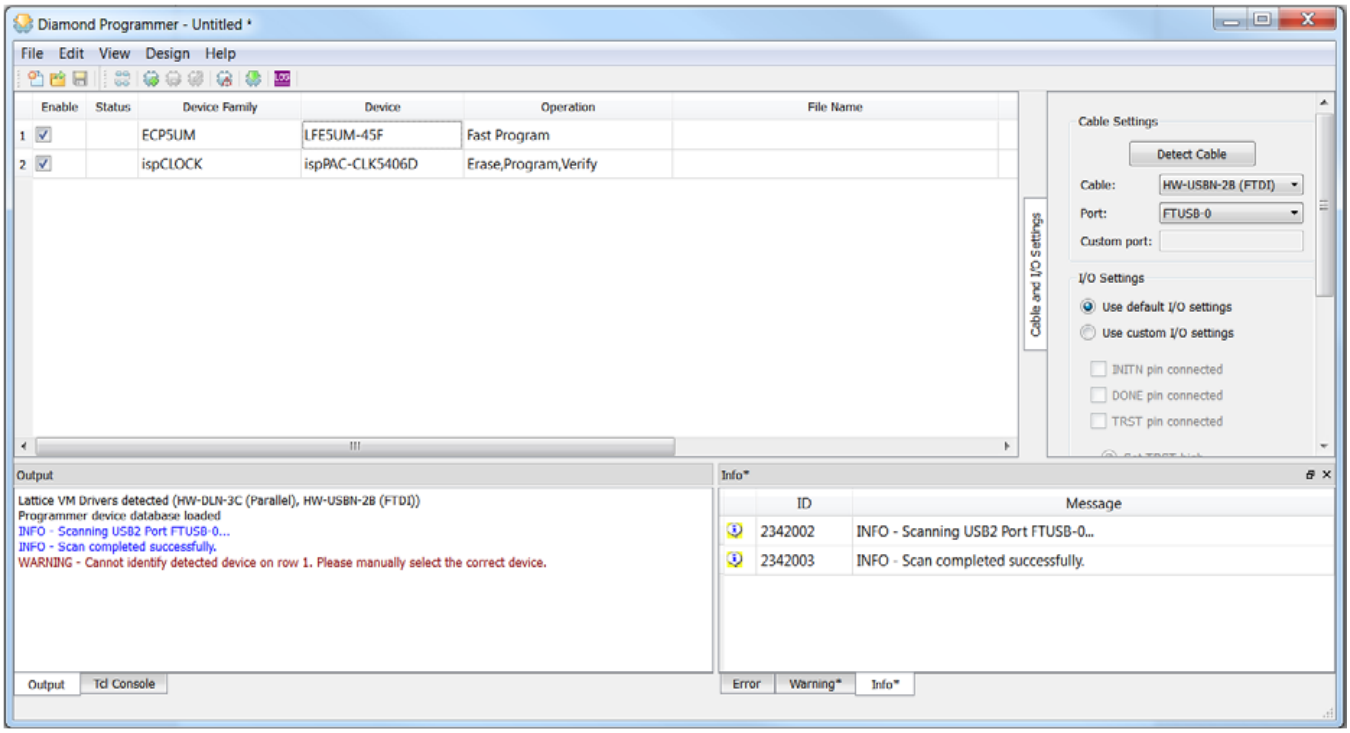

Figure 8.2. Selecting the Device

6. Select **Fast Program** for LFE5UM-45F/LFE5UM5G-45F and **Erase**, **Program**, **Verify** for ispPAC-CLK5406D.

   Navigate to the demo package folder.

   The bitstream for ECP5 is SERDES_eye.bit and ispClock_Versa_Demos_156p25MHz.jed for ispCLOCK5406D. The bitstream for ECP5-5G is SERDES_eye_5G.bit and ispClock_Versa_Demos_3124MHz.jed. Specify the files to be programmed then start programming. Dot on segment LED D23 should be blinking once the programming is completed.

This completes the device programming.

8.3. Eye Diagram Demo

To generate the eye diagram:

1. Connect the DSA or DSO to J7/J8.
2. Set the switch position for SW3-8 (labeled K20) to OFF. This selects the PRBS pattern generator.

The eye diagram example as shown in Figure 8.3 is for ECP5 device.

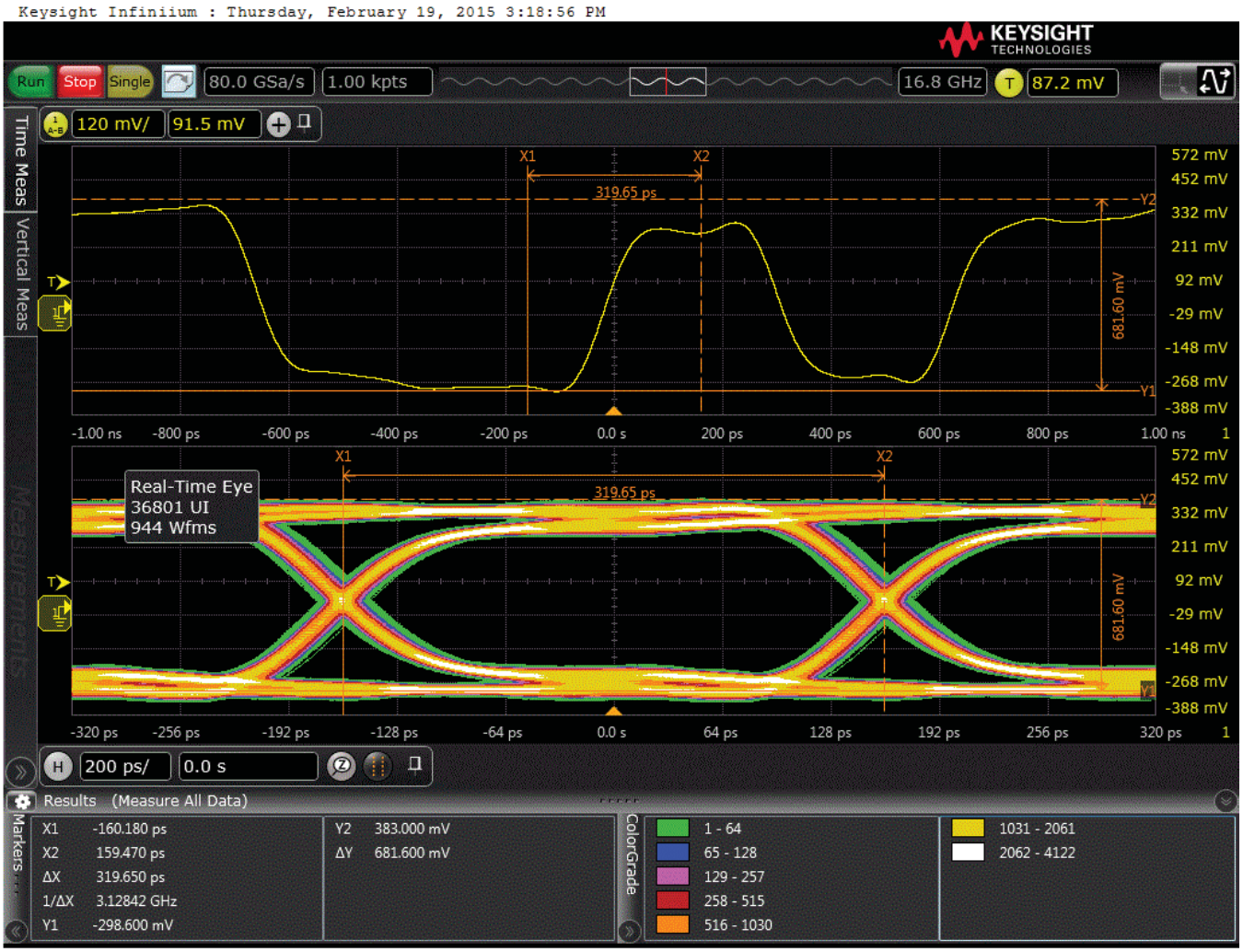

Figure 8.3. Eye Diagram Example

3. To use SERDES Debug, remove the jumpers on J50 first and then connect one jumper between pin #1 and pin #2 and a second jumper between pin #3 and pin #5. This puts ECP5/ECP5-5G as the only device in the chain.
4. To run the SERDES debug tool, first open the eye.ldf/eye_5G.ldf file (found in the ECP5_SERDES/ECP5_5G_SERDES project directory) in Lattice Diamond Software.
5. Launch the SERDES debug tool by double-clicking the **untitled.rva** file in the Debug Files area of the project.

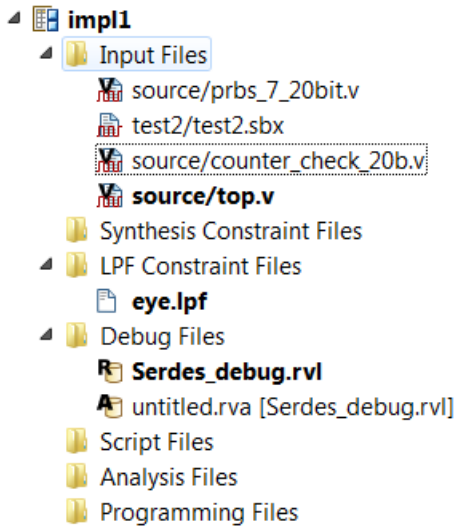

Figure 8.4. Launching the SERDES Debug Tool

6. Figure 8.5 shows the SERDES Debug window in Reveal Analyzer. The transmit behavior of the SERDES can be updated using the drop-down menus shown. Once the transmit configuration is changed in SERDES Debug, click the **Apply** button.

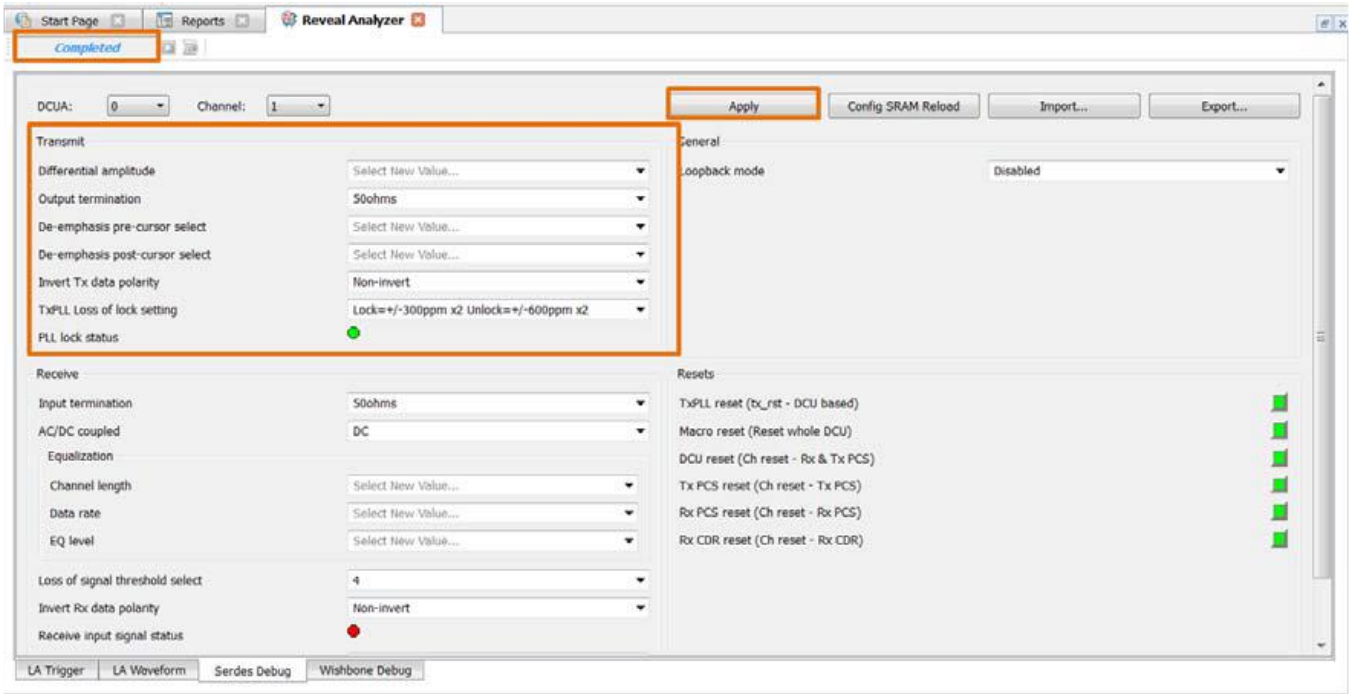

Figure 8.5. SERDES Debug Window

7. The top left corner of the interface indicates the status of new SERDES setting as shown in Figure 9. The SERDES behavior can be observed at this point.

8.4. Loopback Demo (External Loopback)

1. Connect pair J5/J6 with J7/J8 using the SMA cables.
2. Set the switch position for both SW3-8 and SW3-7 to ON. This enables the FPGA counter pattern generator. LED D29 should be lit, which indicates that a counter pattern is detected for SERDES RX.
3. Set switch position for SW3-8 to OFF and SW3-7 to ON. This enables the FPGA fixed non-counter pattern generator. Then press SW1 GSRN. LED D29 should be no longer lit, which indicates that a counter pattern is not detected for SERDES RX.
4. To use SERDES Debug, remove the jumpers on J50 first and then connect one jumper between pin #1 and pin #2 and a second jumper between pin #3 and pin #5. This puts ECP5/ECP5-5G as the only device in the chain.
5. To run the SERDES debug tool, first open the eye.ldf file (found in the ECP5_SERDES project directory) in Lattice Diamond Software.
6. Launch the SERDES debug tool by double-clicking the untitled.rva file in the debug files area of the project.
7. Figure 8.5 shows the SERDES Debug window in Reveal Analyzer. The transmit & receive behavior of the SERDES can be updated using the drop-down menus shown. Once the SERDES configuration is changed, click the Apply button. The top left corner of the interface indicates the status of new SERDES setting.

8.5. Loopback Demo (Internal Loopback)

1. The SERDES Debug tool is used to enable internal loopback. To use SERDES debug, remove the jumpers on J50 first and then connect one jumper between pin #1 and pin #2 and a second jumper between pin #3 and pin #5. This puts ECP5/ECP5-5G as the only device in the chain.
2. To run the SERDES debug tool, first open the eye.ldf file (found in the ECP5_SERDES project directory) in Lattice Diamond Software.
3. Launch the SERDES debug tool by double-clicking the untitled.rva file in the debug files area of the project.
4. Figure 8.6 shows the SERDES Debug window in Reveal Analyzer. The internal loopback setting in the SERDES can be updated using the drop-down menus shown. Once the mode is enabled, click the apply button to update the active SERDES setting.
5. Set the switch position for both SW3-8 and SW3-7 away to ON. This enables the FPGA counter pattern generator. LED D29 should be lit, which indicates that a counter pattern is detected for SERDES RX.
6. Set switch position for SW3-8 to OFF and SW3-7 to OFF. This enables the FPGA fixed non-counter pattern generator. Then press SW1 GSRN. LED D29 should be no longer lit, which indicates that a counter pattern is not detected for SERDES RX.

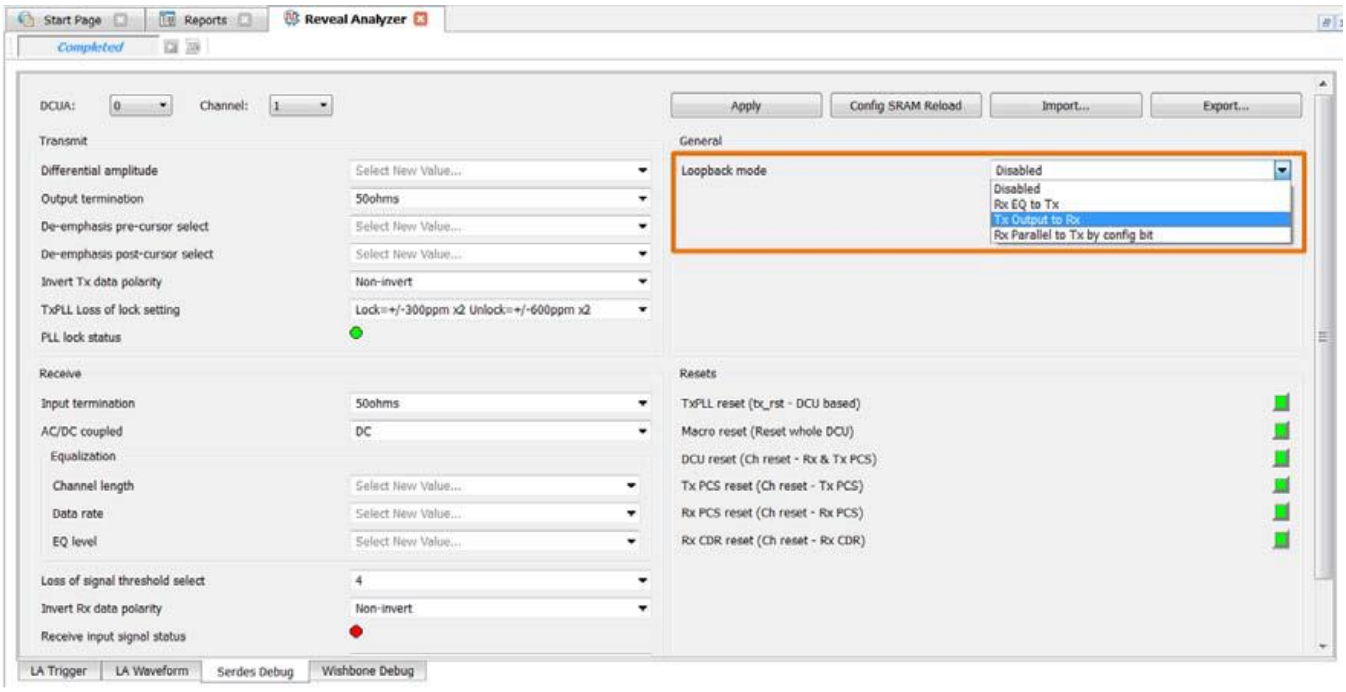

Figure 8.6. Enabling Internal Loopback

9. Developer Notes

- SERDES/PCS module is generated using Clarity Designer in Diamond. The Clarity Designer generated file type is .sbx. In this design example, test2.sbx is generated from Clarity Designer. Under test2, there are two modules, test1 is SERDES/PCS and refclk is reference clock for SERDES. You should manually connect these two modules.

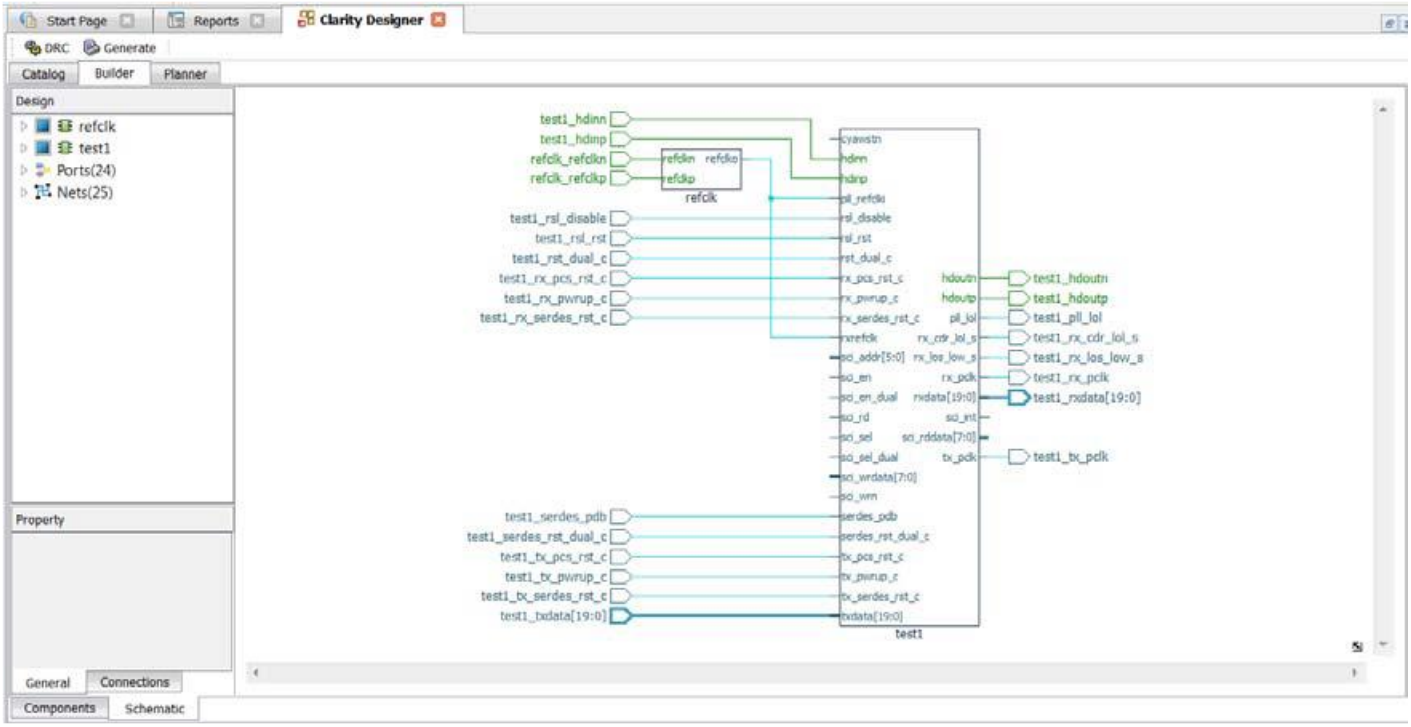

Figure 9.1. SERDES/PCS Module Generated in Clarity Designer

- To make use of SERDES Debug, select **SCI Port Enable** in the Advanced Setup tab. Otherwise, SERDES Debug will not be able to access SERDES registers.

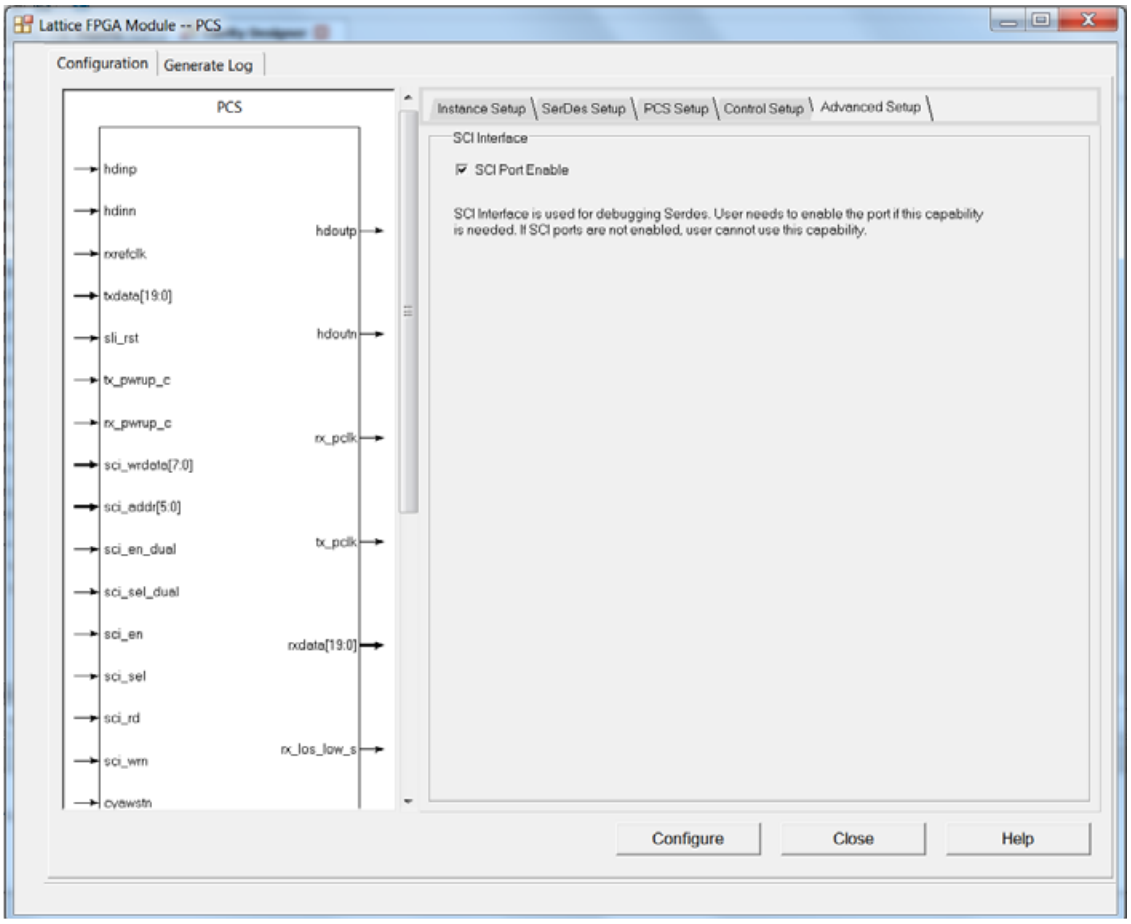

Figure 9.2. Enabling SCI Port

- To add SERDES Debug, open the Reveal Inserter tool in Diamond and select **Debug > Add New Core > Add SERDES Debug**. Specify sample clock and reset signals.

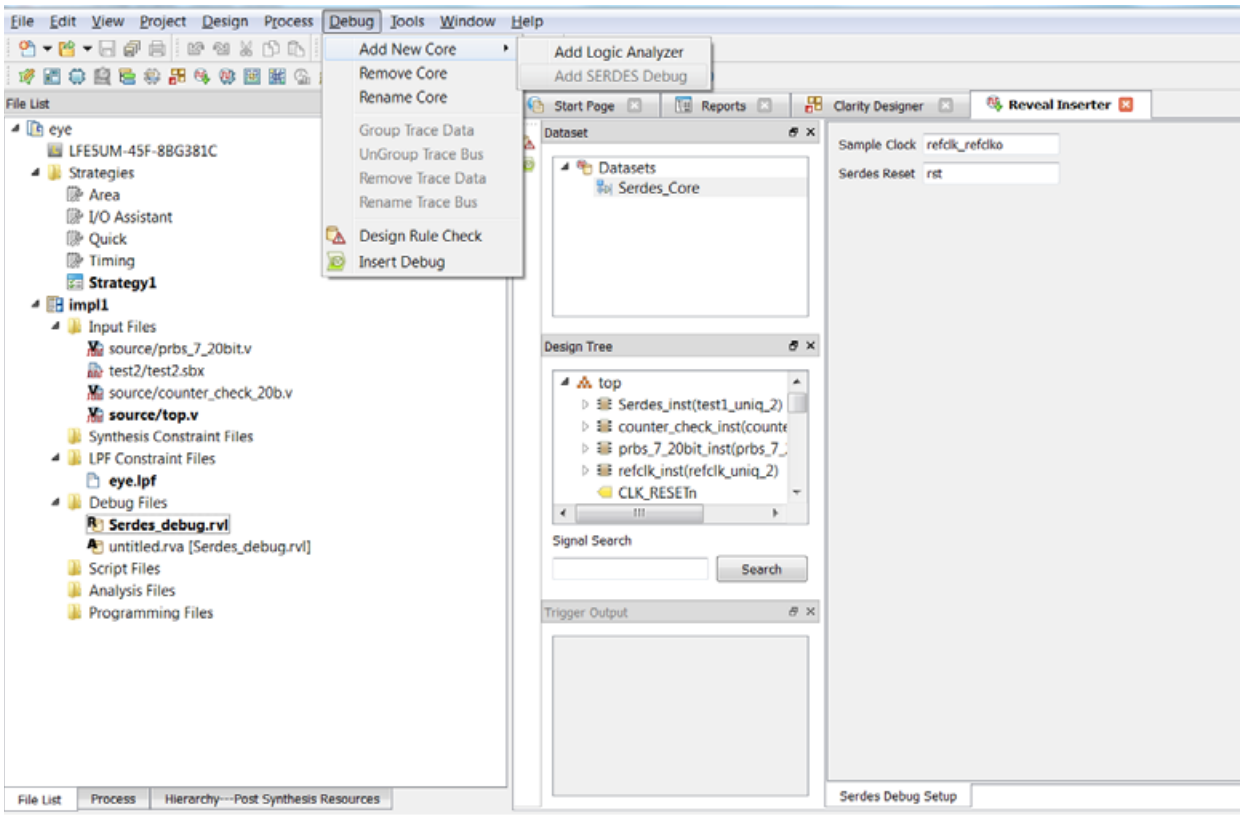

Figure 9.3. Adding SERDES Debug

10. Demo Design Dependencies per Development Board Revision

For the ECP5 demo, the bitstream included with the demo design has been developed for the ECP5 Versa Development Board Revision B. The key updates to the Revision B development Board with respect to the SERDES Eye demo include the following:

1. Revision B uses SW4 to set the configuration mode for ECP5. Revision A uses a resistor population scheme to set the configuration mode. The demo operation described in this user guide is independent of the switch setting or resistor population. For more details see the ECP5 Versa Development Board User Guide.
2. The ECP5 pinout with respect to the on-board DIP switches and LEDs has been updated for Revision B of the hardware. Specifically the SW[1] assignment in the demo project is location K19 for Revision B. SW[1] is assigned to location J19 for Revision A.
3. The demo bitstreams have been built with Diamond 3.8 for use with Revision B of the ECP5 Versa Development Board. The demo project must be rebuilt with Diamond 3.4 for use with Revision A.

References

- ECP5 Versa Development Board User Guide (FPGA-EB-02021)
- ECP5-5G Versa Development Board User Guide (FPGA-EB-02048)

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.4, July 2022

Section	Change Summary
All	• Changed document title from "SERDES Eye Demo for the ECP5 and ECP5-5G Versa Development Boards" to "SERDES Eye Demo for the ECP5/ECP5-5G Versa Development Kit". • Changed document number from UG93 to FPGA-UG-02166. • Updated document template.

Revision 1.3, January 2017

Section	Change Summary
Device Programming	Revised procedure steps 4, 5, and 6to add ECP5-5G information.
Eye Diagram Demo	• Indicated that the eye diagram example (Figure 8.3) is specifically for ECP5 device. • Revised step 4 to add ECP5-5G information.

Revision 1.2, October 2016

Section	Change Summary
All	• Document title changed to SERDES Eye Demo for the ECP5™ and ECP5-5G™ Versa Development Boards User Guide. • Added support for ECP5-5G Versa Development Board. • Updated the demo package directory structure. • Updated Diamond version to 3.8. • Added EB103 to References section.

Revision 1.1, August 2015

Section	Change Summary
All	Document update to support ECP5 Versa Development Board Rev B.

Revision 1.0, April 2015

Section	Change Summary
All	Initial Release

www.latticesemi.com