Release Notes for Lattice Diamond 3.4.1

Welcome to Lattice Diamond®, the complete design environment for Lattice Semiconductor FPGAs. Lattice Diamond design software offers leading-edge design and implementation tools optimized for cost-sensitive, low-power Lattice FPGA architectures.

Diamond is available for both the Windows and Linux operating systems. For details, see “System Requirements” on page 10.

This version of Diamond adds a variety of enhancements to make designing for Lattice Semiconductor programmable devices easier than ever. The design tools also include support for the latest Lattice Semiconductor devices. See “What’s New” on page 2.

Lattice Semiconductor offers a rich variety of information sources, including the Help system, PDF manuals, tutorials, and online discussions. The easiest way to reach them all is through the online Help. The first topic in the Help provides links to all the other sources of information.

You can also find extensive information about Diamond and its capabilities, tools, and workflow on the Lattice Semiconductor Web site under:

www.latticesemi.com/latticediamond

What's New

This release of Diamond provides a variety of new features in the following areas. See the online Help for details. Also see "Issues Fixed" on page 12 for known issues of the previous release that have been fixed.

What's New in Diamond 3.4.1

New Device Support The following new devices are available with device programming enabled:

- MachXO3LF

FPGA Libraries Embedded Function Block (EFB) for MachXO3LF support User Flash Memory (UFM).

Programmer: Flash programming support has been added for MachXO3LF devices.

A new "Recovery Erase Only" operation has been added for MachXO2, MachXO3L, and Platform Manager 2 devices.

What's New in Diamond 3.4

New Device Support The following new devices are available with device programming enabled:

- MachXO3L with csfBGA packages

The following new devices are available with device programming disabled:

- ECP5-85 without ES suffix

The following devices are available with device programming enabled:

- ECP5-45

Operating System Diamond is no longer supported on Windows XP.

Clarity Designer The Schematic view has added drag-and-drop functionality to connect available components, ports, and pins to other available components, ports, and pins. For more information, open the online Help and go to Entering the Design > Creating Clarity Designer Modules > Building > Building with the Schematic View.

The Planning tab now contains a Usage report that allows you to monitor the resource usage during the planning phase. The usage information is updated after each planning operation. The report displays used resources and total available resources. For more information, open the online Help and go to Entering the Design > Creating Clarity Designer Modules > Clarity Designer Benefits and Features > Planning and Determining Usage.

EPIC The version of EPIC used prior to Diamond 3.0 has been removed. Please use the new version of EPIC.

IPexpress IPexpress™ includes updates to many modules. For more information, open the online Help and go to Lattice Module Reference Guide.

LatticeMico System LatticeMico™ System allows you to choose between using Embedded Block RAM (EBR) or Distributed RAM for the SPI Flash, LatticeMico8 Microcontroller, and LatticeMico32 Microprocessor components. For more information, refer to the "LatticeMico System Software Release Notes for Diamond." To access the release notes:

- If LatticeMico System is installed with Diamond, go to the Windows Start menu and choose **Programs > Lattice Diamond > Accessories > LatticeMico System Release Notes**.
- If LatticeMico System is installed as a stand-alone tool, go to the Windows Start menu and choose **Programs > Lattice Diamond > LatticeMico System Release Notes**.

Netlist Analyzer Netlist Analyzer now has a Post-Mapping View that shows how the design is mapped to the device's architecture.

Two new commands help you focus on part of a design:

- Isolate Path reduces the schematic to selected modules and modules connected to the selected modules. Only nets connecting the modules are included.
- Less hides selected objects that are in the way.

For more information, open the online Help and go to Managing Projects > Analyzing a Design > About Netlist Analyzer.

SEI Editor SEI Editor is a new tool that allows you to insert errors into a programmed ECP5 for testing purposes. SEI Editor requires a special license. Please contact Lattice technical support. For more information, open the online Help and go to Implementing the Design > Bit Generation > Analyzing your Design using Soft Error Injection.

Simulation (Windows version) The Aldec® Active-HDL™ Lattice Edition simulator has been updated.

Mentor Graphics Questa simulator is now supported. For more information, open the online Help and go to Simulating the Design > Third-Party Simulators > Performing Simulation with Mentor Graphics ModelSim / Questa.

Synthesis Tools The Synopsys® Synplify Pro® for Lattice and Lattice Synthesis Engine (LSE) synthesis tools have been updated.

LSE has expanded support for Synopsys Design Constraints (SDC):

- create_clock can specify when the clock's rising and falling edges happen during the clock period (-waveform).
- create_generated_clock can specify a duty cycle as a percentage of the clock period (-duty_cycle).

- set_clock_groups can have multiple clocks in a group.
- set_input_delay and set_output_delay can specify that the delay value refers to the shortest or longest path (-min, -max).
- set_min_delay is a new constraint that specifies the minimum delay for the timing paths.

For more information, open the online Help and go to Constraints Reference Guide > Lattice Synthesis Engine (LSE) Constraints > Synopsys Design Constraints (SDC).

Supported Devices

Lattice Diamond can be used with either a free license or a subscription license. The two licenses provide access to different device families.

Device Family	Free License	Subscription License
ASC	◀	◀
ECP5™		◀
LatticeEC™	◀	◀
LatticeECP™	◀	◀
LatticeECP2™	◀	◀
LatticeECP2M™		◀
LatticeECP2S		◀
LatticeECP2MS		◀
LatticeECP3™		◀
LatticeSC™		◀
LatticeSCM™		◀
LatticeXP™	◀	◀
LatticeXP2™	◀	◀
MachXO™	◀	◀
MachXO2™	◀	◀
MachXO3L	◀	◀
MachXO3LF	◀	◀
Platform Manager™	◀	◀
Platform Manager 2	◀	◀

Note

ECP5 is under license control. To use one of these controlled devices, contact Lattice Semiconductor for a license.

Installing Diamond 3.4.1

Important: For Diamond 3.4.1, you must already have Diamond 3.4 installed.

See the Diamond 3.4 installation guide for more information.

To install on Windows:

- Double-click the installation file.

To install on Linux:

- Run one of the following commands depending on where you want to install:
  - To install to the default location (/usr/local/diamond):

    ```
    % sudo rpm -Uvh <path_to_package>/<diamond_3_4-sp1-213-file>.rpm
    ```

  - To override the default location:

    ```
    % sudo rpm -Uvh --prefix <install_path>
    <path_to_package>/<diamond_3_4-sp1-213-file>.rpm
    ```

To install stand-alone tools:

The following “stand-alone” tools should be installed as described in the Diamond 3.4 installation guide. The 3.4 version does *not* need to be installed first:

- LatticeMico System
- Power Estimator
- Programmer
- Reveal Analyzer

Updating Projects from an Earlier Version

If you want to work on a design project created with an earlier version of Diamond, start with the following procedures. These procedures adapt the project for the changes in Diamond.

Find out which version of Diamond your project was created with. Then work through the changes for that and every later version, starting with the earliest and going to the most recent. For example, if your project was created with

Diamond 1.1, you would start with the changes for 1.1. After completing those changes, you would work on the changes for 1.2, then 1.4, and so on.

When you open a project from Diamond 1.2 or earlier, Diamond opens a dialog box warning that Diamond will automatically move all SDC files to the Synthesis Constraint Files folder in File List view and remove the “Input SDC Constraint File” options from the strategies. If the project is using LSE, the file names will be changed to use an .ldc extension.

Once saved, the project will not be compatible with earlier Diamond versions.

2.2 Projects

ECP5 does not use the CIN port of the CCU2C Carry Chain primitive. This port should not be connected to anything. If the port is connected, the Design Map stage will fail with an error message. If you see such a failure, correct the design in one of the following ways:

- Rerun synthesis. This should correct the problem if the CCU2C primitive is part of an IPexpress module.
- If the CCU2C primitive was added to your HDL manually, edit the code to remove the connection. See the following examples:

  In Verilog:

```
CCU2C addsub_0 (.A0(scuba_vlo), .A1(DataA[0]),
  .B0(scuba_vlo), .B1(DataB[0]), .C0(scuba_vhi),
  .C1(scuba_vhi), .D0(scuba_vhi), .D1(scuba_vhi),
  .CIN(), .S0(), .S1(Result[0]), .COUT(co0));
```

  In VHDL:

```
signal tmp: std_logic := 'X';
cnt_cia: CCU2C
  generic map (INJECT1_1=> "NO", INJECT1_0=> "NO",
  INIT1=> X"0000", INIT0=> X"0000")
  port map (A0=>scuba_vhi, A1=>scuba_vhi, B0=>scuba_vhi,
  B1=>scuba_vhi, C0=>scuba_vhi, C1=>scuba_vhi,
  D0=>scuba_vhi, D1=>scuba_vhi,
  CIN=>tmp, S0=>open,S1=>open, COUT=>cnt_ci);
```

2.0.1 Projects

The default values of several strategy options were changed. If you are using Synplify Pro in integrated mode (running synthesis automatically in Diamond), check that the following settings are still as you want them. Also, check the setting of the Auto Hold-Time Correction option under Place & Route Design. Its default changed to On for all devices.

Table 1: New Default Values for Synplify Pro for Lattice

Option	Before	Now
Fanout Limit is now Fanout Guide	100	1000
Export Diamond Settings to Synplify Pro GUI (new in 2.2)	Not available	No
Fix Gated Clocks and Fix Generated Clocks combined into new Clock Conversion	3 (converts and reports all sequential elements)	True (converts with no report)
Frequency	200	auto (blank means “auto”)
Number of Critical Paths	3	blank (unspecified)
Number of Start/End Points	0	blank (unspecified)
Output Preference File	False	True
Pipelining and Retiming	False	Pipelining Only
Resolved Mixed Drivers	True	False
Use Clock Period for Unconstrained I/O	True	False

1.4 Projects

For Diamond 1.4 and earlier, there might be some constraints that are not honored because of the Synplify Pro cross-probing feature. This EDIF renaming is usually related to bus names.

If such a problem occurs, you can turn off the renaming feature by placing the following line in the “Command line Options” text box of the Synplify Pro section of the active strategy:

set_option -syn_edif_array_rename 0

1.2 Projects

There were several enhancements for IP and MachXO2.

IP Incompatibilities

SPI4.2 2.7 is not compatible with Diamond 1.3 or later. If you are using this IP, check the Lattice Semiconductor Web site for a more recent version.

MachXO2 Changes

See if your design involves any of the following features:

- For EFB modules with user flash memory (UFM), regenerate the module.
- For IO_TYPE=PCI33 on a MachXO2-1200 or larger device, check if the CLAMP is using the default setting. With Diamond 1.3 the CLAMP default changes from ON to PCI and the I/O will be placed in bank 2. If you were using the default and still want the setting to be ON, you need to set it explicitly.
- For PCI33 MT 6.5 and PCI33 T 6.4 IP, either set the CLAMP to ON explicitly or choose a bigger package (256 or more).

1.1 or 1.0 Projects

There were several enhancements for IP and MachXO2.

IP Incompatibilities

The following IP versions are not compatible with Diamond 1.2 or later. If you are using any of these IP, check the Lattice Semiconductor Web site for a more recent version.

- Convolution Block Encoder 3.6
- DDR1 6.9
- DDR2 7.1
- DDR3 1.2.1
- DDR1_CP 1.1 with MachXO2
- DDR2_CP 1.1 with MachXO2
- Interleaver Deinterleaver 3.5
- PCI_MT_33 6.4
- PCIe RC Lite 1.2
- Tri-Speed MAC 3.4
- Viterbi Block Decoder 4.6

MachXO2 Support

Some aspects of the software support for MachXO2 designs have been improved. See if your design involves any of the following features:

- The 4K/7K design with PLL has a CIB-to-PLL jump change. If you are using this design, recompile it.

- The EFB simulation model has changed. If you are using the EFB module, rerun your simulation tests to see more accurate results.
- In the DDR_GENERIC module of IPexpress, the GDDRX1_RX.Aligned with PLL interface is no longer supported. If you are using such a module, use IPexpress to regenerate it without the PLL option.

Also, MachXO2 has IP evaluation capability and TransFR mode for all I/Os.

Migrating ispLEVER Projects

Diamond uses a different project structure than ispLEVER and cannot directly open an ispLEVER project. However, design projects created in ispLEVER can easily be imported into Diamond. The process is automatic except for the ispLEVER process properties, which are similar to the Diamond strategy settings, and some modules and IPs. All of your ispLEVER project source will be automatically handled.

Projects created using ispLEVER can be imported into Lattice Diamond through two different paths:

- On the Start Page, click **Import ispLEVER Project** (in the upper-left corner).
- From the File menu, choose **Open > Import ispLEVER Project**.

Follow the directions in the dialog box that opens to convert your ispLEVER project into a Lattice Diamond project.

Limitations to the import/conversion process include:

- NGO files in ispLEVER projects need to be manually copied into the Lattice Diamond project if the NGO files were originally copied into the ispLEVER project. For example, NGO files that were copied from Lattice IP generation.
- The .lpc files are replaced with .ipx files in Lattice Diamond. You need to regenerate your IP by double-clicking on the .lpc file. The resultant wizard will help you generate the new .ipx file, replacing the old .lpc file.

More information on importing ispLEVER projects can be found in the *Lattice Diamond User Guide*, online Help (see Managing Projects > Importing ispLEVER Projects), and training videos on the Lattice Web site.

Other Information Resources

Other available information resources for the Diamond software include the following.

- General Information: General information on Lattice Diamond can be found on the Lattice Web site at:

  www.latticesemi.com/latticediamond

- Online Help: Start Lattice Diamond and choose **Help > Lattice Diamond Help**.
- *Lattice Diamond User Guide*: This document can be found from a link on the Start Page view.
- Training Videos: Several short videos are available on different aspects of the Lattice Diamond software. These can be viewed online at:

  www.latticesemi.com/latticediamond

  Click the **Videos** tab.

System Requirements

The basic system requirements for Lattice Diamond are:

- Intel Pentium or Pentium-compatible PC running the SSE3 instruction set, or AMD Opteron system support (Linux only)
- One of the following operating systems:
  - Windows Vista (32-bit), Windows 7 (32-bit or 64-bit), or Windows 8 (32-bit or 64-bit).
  - Red Hat Enterprise Linux 4.X, 5.3, or 6. The host operating system can be either 32-bit or 64-bit.

    Version 5.3 of Red Hat Enterprise Linux has some extra installation requirements. See “Configuring Red Hat 5.3” on page 12.
  - Novell SUSE Linux Enterprise 10 SP1 or 11 operating system. Novell SUSE Linux supports 32-bit only.
- Approximately 5.75 GB free disk space
- RAM adequate for your FPGA design. For guidelines see “Memory Requirements” on page 11.
- Network adapter and, for a floating license, network connectivity

  A node-locked license is based on the physical (hard-coded) address provided by the network adapter. Network connectivity is not required for a node-locked license. In the absence of a network connection, you can install the NWLink IPX/SPX protocol to force recognition of your NIC card ID (see the installation notice).

  A floating license requires access to the license server, so both a network adapter and connectivity are required.
- JavaScript-capable Web browser
- Microsoft Internet Explorer 8 or higher if using the included Aldec Active-HDL Lattice Edition simulator
- Acrobat Reader 5.0 or later

Memory Requirements

Table 2 lists the minimum memory requirements and the recommended memory for the Lattice Semiconductor devices supported by Diamond.

On Windows, designing for the largest FPGAs may require more than the usual 2 GB of memory found in 32-bit computers. For help in extending your memory to 3 GB, see “Extending Memory on Windows” on page 11. Designing for LatticeECP3 with more than 95K LUT on a Windows system requires a 64-bit operating system.

Table 2: Recommended Memory

Device	Size	32-Bit Operating Systems		64-Bit Operating Systems	
		Minimum	Recommended	Minimum	Recommended
ECP5	All	2 GB	3 GB	4 GB	6 GB
LatticeEC, LatticeECP	Up to 20K LUT	512 MB	768 MB	1 GB	1.5 GB
	Up to 50K LUT	768 MB	1 GB	1.5 GB	2 GB
LatticeECP2/M	Up to 20K LUT	768 MB	1 GB	1.5 GB	2 GB
	Up to 50K LUT	1 GB	1.5 GB	2 GB	3 GB
	Up to 100K LUT	1 GB	2 GB	2 GB	4 GB
LatticeECP3	Up to 95K LUT	2 GB	3 GB	4 GB	6 GB
	Up to 150K LUT	3 GB	4 GB	6 GB	8 GB
LatticeSC/M	Up to 40K LUT	768 MB	1 GB	1.5 GB	2 GB
	Up to 115K LUT	1 GB	2.5 GB	2 GB	5 GB
LatticeXP, LatticeXP2	Up to 20K LUT	512 MB	768 MB	1 GB	1.5 GB
	Up to 50K LUT	768 MB	1 GB	1.5 GB	2 GB
MachXO, MachXO2, MachXO3L	All	256 MB	512 MB	512 MB	1 GB
Platform Manager, Platform Manager 2	All	256 MB	512 MB	512 MB	1 GB

Extending Memory on Windows

Designing for LatticeECP3 or ECP5 may require more than the 2 GB normally available with 32-bit Windows systems. But you can configure Windows to use up to 3 GB of memory.

Note that increasing the amount of memory available to applications decreases the amount available for the file cache, paged pool, and nonpaged pool, which can affect applications with heavy networking or I/O.

Use the **BCDEdit /set increaseuserva 3072** command to set the boot entry option to 3 GB. For details, see Microsoft article “BCDEdit /set”: msdn.microsoft.com/en-us/library/ff542202.aspx

Configuring Red Hat 5.3

Red Hat Enterprise Linux 5.3 has some extra requirements for Diamond:

- In addition to the basic installation of Red Hat 5.3, under Development/ Legacy Software Development, select:

  ```
  1:gtk+-1.2.10-56.el5.i386 - GIMP Toolkit (GTK+) sb:(9 of 9)
  ```

  Under Base System/Legacy Software Support, add the following to the default items:

  ```
  Openmotif22-2.2.3-18.i386 - Open Motif runtime
  ```

  Proper Diamond operation depends upon these libraries being installed.

- When installing the Red Hat Enterprise Linux version, be sure to install the PERL modules XML::Parser, XML::DOM, and XML::RegExp. These PERL modules are available at www.cpan.org.

Issues Fixed

The following known issues are fixed with Diamond 3.4. Their workarounds are no longer needed.

Hysteresis is not set for the LVTLL33 IO_TYPE

Hysteresis bits are not set for the LVTLL33 IO_TYPE. Changing the Hysteresis setting in the software will not have any effect if you select the IO_TYPE to be LVTTL33.

Change the IO_TYPE to LVCMOS33 and then use the Hysteresis settings. LVCMOS33 and LVTLL33 are exactly the same.

Devices affected: MachXO2
CR122740

EPIC Help does not display in Firefox

EPIC cannot open its online Help if Firefox is your default browser. Instead, Firefox displays, “The address wasn’t understood.”

To work around this problem, do one of the following:

- Set a different browser, such as Chrome or Internet Explorer, as your default browser. Then open the Help from EPIC.

- In Firefox, enter the path to the Help:

  <*Diamond directory*>\ispfpga\webhelp\epichelp\index.htm

Devices affected: All
CR122659

Clock placed in Clarity generated without buffer

When generating a Clarity Designer module that includes a DDR interface, you may get a warning message similar to the following:

> WARNING - Clock input 'clkop' of interface 'eclk_group0' in component 'abc' is generated without any buffer. Planning for each interface needs special attention. Consult document for more information.

This can happen if you use the Planner tab of Clarity to place the clock signal of the DDR module. Clarity does not properly place the clock signal.

If you see this message, place the DDR clock without using Clarity. See *Applying Design Constraints* in the online help.

Or, if you need a PLL in the design, drive the clock input from the PLL.

Devices affected: ECP5
CR122392

Known Issues

Following are new known issues with this release and workarounds for them. This list is preliminary. For the complete list of known issues, see: www.latticesemi.com/view_document?document_id=50676

EFB not enabled with MachXO3LF when creating a LatticeMico System Builder platform

When creating a platform in LatticeMico System Builder for a MachXO3LF design, if you choose MachXO3LF in the Platform Wizard, the EFB component will not be enabled.

As a workaround, you can create a platform specifying a MachXO2 device instead. This will enable the EFB component, and your MachXO3LF design will work properly.

Devices affected: MachXO3LF
CR124013

Contacting Technical Support

FAQs The first place to look. The Answer Database provides solutions to questions that many of our customers have already asked. Lattice Applications Engineers are continuously adding to the Database.

Telephone Support Hotline Receive direct technical support for all Lattice products by calling Lattice Applications from 5:30 a.m. to 6 p.m. Pacific Time.

- For USA & Canada: 1-800-LATTICE (528-8423)
- For other locations: +1 503 268 8001

In Asia, call Lattice Applications from 8:30 a.m. to 5:30 p.m. Beijing Time (CST), +0800 UTC. Chinese and English language only.

- For Asia: +86 21 52989090

E-mail Support

- techsupport@latticesemi.com

For Local Support Contact your nearest Lattice Sales Office.

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