LA-MachXO Product Family AEC-Q100 Qualification Summary

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Dear Customer,

Enclosed is Lattice Semiconductor's LA-MachXO Product Family AEC-Q100 Qualification Summary for the Mie101 wafer fabrication facility.

This report was created to assist you in the decision making process of selecting and using our products. The information contained in this report represents the entire qualification effort for this device family.

The information is drawn from an extensive qualification program of the wafer technology and packaging assembly processes used to manufacture our products. The program adheres to JEDEC and Automotive Industry standards for qualification of the technology and device packaging. This program ensures you only receive product that meets the most demanding requirements for Quality and Reliability.

Your feedback is valuable to Lattice. If you have suggestions to improve this report, or the data included, we encourage you to contact your Lattice representative.

Sincerely,

James M. Orr
Vice President,
Corporate Quality & Product Development
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1.0 INTRODUCTION

The new class of versatile Non-Volatile PLD's from Lattice, LA-MachXO automotive family, offers a non-volatile, infinitely reconfigurable solution that is tested and qualified to the AEC-Q100 standard.

The LA-MachXO automotive family combines Flash and SRAM technology to provide "instant-on" capabilities in a single low-cost device. This combination of Flash and SRAM enables easy field updates via Lattice's unique TransFR technology.

The LA-MachXO automotive family offers flexible LUT architectures (256 to 2280 LUTs) and multiple density-I/O combinations in Thin Quad Flat Pack (TQFP) and Fine-Pitch Thin BGA (ftBGA) packages with user I/O counts ranging from 78 to 271 I/Os. Table 1 shows the density (LUTs), package and I/O options, along with other key parameters for each member of the family.

The LA-MachXO automotive family features Lattice's exclusive sysCLOCK PLLs, sysMEM embedded memory blocks (EBRs) and high-performance I/Os. The LA-MachXO automotive family also offers flexible I/O buffer support with wide range of interfaces including LVCMOS 3.3/2.5/1.8/1.5/1.2, LVTTL, PCI, LVDS, Bus-LVDS, LVPECL and RSDS. The LA-MachXO automotive family is in-system programmable through the standard IEEE 1532 interface. IEEE Standard 1149.1 boundary scan testing capability also allows product testing on automated test equipment.

The LA-MachXO automotive family is built on the 130nm Flash cell based CMOS process at Fujitsu Mie fabs and assembled at ASE Malaysia. This report details the automotive reliability qualification and device characterization results of the LA-MachXO Product Family products at the Fujitsu Mie fabs.

The LA-MachXO datasheet is available on the Lattice Semiconductor website (www.latticesemi.com).

Table 1.1. LA-MachXO Automotive Product Family Attributes

Part Attributes	LAMXO 256C/E	LAXMO 640C/E	LAXMO 640C/E	LAMXO 1200E	LAMXO 1200E	LAMXO 2280E	LAMXO 2280E	LAXMO 640C/E	LAMXO 1200E	LAMXO 2280E	LAMXO 2280E
	TN100	TN100	TN144	TN100	TNI44	TN100	TN144	FTN256	FTN256	FTN256	FTN324
Die Fabrication Site	Fujitsu - Mie, Japan										
Package Assembly Site	ASE Malaysia										
Final Test Site	ASE Malaysia										
Wafer Size	300mm										
Die Family (Product Line)	LAMXO 256C/E	LAXMO 640C/E		LAXMO 1200E		LAMXO 2280E		LAXMO 640C/E	LAMXO 1200E	LAMXO 2280E	
Die Mask Set Revision	02	03		02		02		03	02	02	
Fabrication Technology	EE12 (0.13um CMOS)										
Die Channel Length	0.12 micron										
Number of Transistors/Gates	12 types = (S,H,U @1.2volt; F @3.3volt; Int,Enh @5.5volt) * P,N										
Number of Mask Steps	48										
Die Dimensions (W x L x T) in microns (um)	1940 x 2030 x 254-305	2650 x 2650 x 254-305		3350 x 3350 x 254-305		4080 x 3850 x 254-305		2650 x 2650 x 229-305	3350 x 3350 x 229-305	4080 x 3850 x 229-305	
Die Metallization	8-Cu/1-Al										
# of Metallization Layers	9										
Thickness (per metallization layer)	M1 295, M2-5 IL 275, M6-8 SGL 475, M9 top-Al 1140 (nm units)										
% of alloys (if present)	Cu, Al+0.5wt%Cu										
Die Interconnect Dielectric	SiO/SiO/SiN										
Die Passivation	SiO2 / SiN / Polyimide										
# of Passivation Layers	3										
Passivation Thickness	Oxide 1400; Nitride 500; Polyimide 2000 (nm units)										
Die Overcoat Material											
Die Prep Backside Method	Wafer Saw										
Die Prep Backside Metallization	N/A										
Die Prep Backside Thickness & Tolerances	N/A										
Die Separation Method	Full cut										
Die Separation Kerf Width (um)	25-35										
Die Separation Kerf Depth (if not 100% saw)	NA										
Die Attach Material	Silver-filled epoxy										
Die Attach Method	Dispensing	Dispensing	Dispensing	Dispensing	Dispensing	Dispensing	Dispensing	Dispensing	Dispensing	Dispensing	Dispensing
Die placement diagram	Refer Bonding Diagram										
Package Type / Pin Count	TQFP / 100	TQFP / 100	TQFP / 144	TQFP / 100	TQFP / 144	TQFP / 100	TQFP / 144	FTBGA / 256	FTBGA / 256	FTBGA / 256	FTBGA / 324
Package Outline Drawing	please refer to: PackageDiagrams in latticesemi.com										

Part Attributes	LAMXO 256C/E	LAXMO 640C/E	LAXMO 640C/E	LAMXO 1200E	LAMXO 1200E	LAMXO 2280E	LAMXO 2280E	LAMXO 640C/E	LAMXO 1200E	LAMXO 2280E	LAMXO 2280E
	TN100	TN100	TN144	TN100	TNI44	TN100	TN144	FTN256	FTN256	FTN256	FTN324
Mold Compound Supplier/ID	Hitachi							Sumitomo			
Mold Compound Type	CEL9220HFA							EMEG770HJ			
Flammability Rating	UL94 V-0										
Fire retardant type/Composition	Organic Phosphorus(P1) and Nitrogen(N2) type							Multi-Aromatic Resin			
Glass Transition Temperature, Tg	110degc							140degc			
Coefficient of Thermal Expansion, CTE (above & below Tg) (ppm/C)	CTE 1 - 8 ppm/degc ; CTE 2- 33 ppm/degc							CTE 1 - 8 ppm/degc ; CTE 2- 40 ppm/degc			
Wire Bond Material/Diameter	Au / 0.9 mil							Au / 1.0 mil			
Wire Bond Methods	Thermosonic ball										
Type of wire bond at die	Ball Bond										
Type of wire bond at leadframe	Stitch Bond										
Wirebonding diagram	84-106133	84-106118	84-106119	84-106223	84-106228	84-106224	84-106226	84-106276	84-106229	84-106230	84-106225
Leadframe Material	Cu Alloy							NA			
Leadframe Bonding Plating Composition	Ag							NA			
Leadframe Bonding Plating Thickness	100-350	100-350		100-350		70-250		100-350	70-250	100-350	NA
Paddle/Flag Material	Cu Alloy							NA			
Paddle/Flag Width/Length (mils)	180SQ	180SQ		276SQ		200SQ		276SQ	200SQ	276SQ	NA
Paddle/Flag Plating Composition	Ag	Ag		Ag		Ag		Ag	Ag	Ag	NA
Paddle/Flag Plating Thickness (uinch)	100-350	100-350		100-350		70-250		100-350	70-250	100-350	NA
External Lead Plating Composition	Matte Sn (annealed)							NA			
External Lead Plating Thickness (uinch)	400-800							NA			
Substrate Material	NA							BT Resin : CCL-HL832 ; Solder Mask : AUS303	BT Resin : CCL-HL832 ; Solder Mask : AUS303	BT Resin : CCL-HL832 ; Solder Mask : AUS303	BT Resin : CCL-HL832 ; Solder Mask : AUS303
Substrate Thickness (mm)	NA							0.36	0.36	0.36	0.36
Number of Substrate Metal Layers	NA							2	2	2	2
Plating Composition of Ball Solderable Surface	NA							NiAu	NiAu	NiAu	NiAu
Substrate Panel Singulation Method	NA							Package Saw	Package Saw	Package Saw	Package Saw
Substrate Solder Ball Composition	NA							SAC305	SAC305	SAC305	SAC305
Substrate Solder Ball Diameter	NA							20mils	20mils	20mils	25mils
Die Header Material	Cu							BT substrate			

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Part Attributes	LAMXO 256C/E	LAXMO 640C/E	LAXMO 640C/E	LAMXO 1200E	LAMXO 1200E	LAMXO 2280E	LAMXO 2280E	LAMXO 640C/E	LAMXO 1200E	LAMXO 2280E	LAMXO 2280E
	TN100	TN100	TN144	TN100	TNI44	TN100	TN144	FTN256	FTN256	FTN256	FTN324
Thermal Resistance, qja	please refer to: Thermal Management p.9 in latticesemi.com										
Thermal Resistance, qjc	please refer to: Thermal Management p.9 in latticesemi.com										
Moisture Sensitivity Level	3										
Operating Supply Voltage Range (Vcc)	E: 1.14-1.26V			E: 1.14-1.26V				E: 1.14-1.26V	E: 1.14-1.26V		
	C: 1.71-3.465V							C: 1.71-3.465V			
Operating Temperature Range T_j	Comm: 0°C to +85°C										
	Ind: -40°C to +100°C										
	Auto: -40°C to +125°C										
Operating Frequency Range	configuration dependent										
	see datasheet										
Analog Features/Blocks	n/a										
Digital Features/Blocks	235 LUT4s	640 LUT4s		1200 LUT4s		2280 LUT4s		640 LUT4s	1200 LUT4s	2280 LUT4s	
Embedded Memory - Dist RAM (Kbits)	2	6.1		6.4		7.7		6.1	6.4	7.7	
Embedded Memory - EBR SRAM (Kbits)	0	0		9.2		27.6		0	9.2	27.6	
Number of PLLs	0	0		1		2		0	1	2	
Number of I/Os	78	74	113	73	113	73	113	159	211	211	271

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2.0 LATTICE AEC-Q100 QUALIFICATION PLAN

The LA-MachXO automotive family was qualified for automotive applications using the Stress Test Qualification for Integrated Circuits, AEC-Q100-Rev-H (May 17, 2014), test requirements and methods. The LA-MachXO automotive family operates over the Automotive Grade 2 (-40°C to +105°C) ambient operation temperature range. All low and high temperature test read-outs were performed at the Grade 2 temperature extremes.

Today, The LA-MachXO product family is in high volume production. The MachXO devices are implemented on a cost-effective, production-proven, low-k, 130nm Flash CMOS process with copper metallization fabricated by Fujitsu Semiconductor Limited. The devices for this AEC-Q100 qualification were assembled in Thin Quad Flat Pack (TQFP) packages and Saw-Singulated Pb-free Fine Pitch Thin Ball Grid Array (FTBGA) packages at ASE Malaysia. To verify product reliability, Lattice Semiconductor maintains an active Reliability Monitor program on the MachXO products. Lattice Semiconductor publishes the Reliability Monitor Data quarterly.

Deviations to AEC-Q100- Rev-H (May 17, 2014): None

3.0 LATTICE AEC-Q100 QUALIFICATION DATA

Table 3.1. LA-MachXO Product Family AEC-Q100 Test Plan and Summary of Results

Automotive Grade Level: 2 (-40 to +105C); MSL Level: 3

Supplier Name:	**Lattice Semiconductor Corp.**	General Specification:	**AEC-Q100 Rev. H (May 17, 2014)**
Supplier Code:		Supplier Wafer Fabrication:	**Fujitsu, Mie**
Supplier Part Number:	**LAMXO Family**	Supplier Wafer Test:	**Lattice Semiconductor Corp.**
Supplier Contact:		Supplier Assembly Site:	**ASE, Malaysia**
Supplier Family Type:	**LA-MachXO family**	Supplier Final Test Site:	**ASE, Malaysia**
Device Description:	**FPGA**	Supplier Reliability Signature:	

TEST GROUP A – ACCELERATED ENVIRONMENTAL TESTS

Test	#	Reference	Test Conditions	DEVICE	Lots	SS/Lot (units)	Total	RESULTS
PC (Surface Mount Preconditioning)	**A1**	JESD22-A113F J-STD-020D.1 JESD22-A104D	Test @ Rm/Hot 5cycles -55 to 125°C TC, 24h 125C Bake, 192h 30°C/60%RH TH, 260°C Reflow	LAMXO2280E-02-FTN324	3		738	0 failures
				LAMXO2280E-02-FTN256	1		231	0 failures
				LAMXO2280E-02-TN100	3		738	0 failures
				LAMXO2280E-02-TN144	3		231	0 failures
BHAST (Biased Highly Accelerated Stress Test)	**A2**	JESD22-A110D AEC-Q100 RevG/H	Test @ Rm/Hot +130°C/85%RH, 96 hours; V_{CC}=1.26V, V_{CCIO}=3.47, V_{CCAUX}=3.47V, alternate pin biasing	LAMXO2280E-02-TN100	3	77	231	0 failures
			Test @ Rm/Hot +110°C/85%RH, 264 hours; V_{CC}=1.26V, V_{CCIO}=3.47, V_{CCAUX}=3.47V, alternate pin biasing	LAMXO2280E-02-FTN324	3		231	0 failures
UHAST (Unbiased Highly Accelerated Stress Test)	**A3**	JESD22-A118A AEC-Q100 RevG/H	Test @ Rm/Hot +130°C/85%RH, 96 hours	LAMXO2280E-02-TN100	3	77	231	0 failures
			Test @ Rm/Hot +110°C/85%RH, 264 hours	LAMXO2280E-02-FTN324	3		231	0 failures
TC (Temperature Cycling)	**A4**	JESD22-A104D AEC-Q100 RevG/H	Test @ Hot 1000 cycles -55 to 125°C	LAMXO2280E-02-FTN324	3	77	231	0 failures
				LAMXO2280E-02-FTN256	1		231	0 failures
				LAMXO2280E-02-TN100	3		231	0 failures
				LAMXO2280E-02-TN144	3		231	0 failures
HTSL (High Temp Storage Life)	**A6**	JESD22-A103D AEC-Q100 RevG/H	Test @ Rm/Hot +150°C, 500 hours	LAMXO2280E-02-FTN324	3	45	45	0 failures
				LAMXO2280E-02-TN100	3		45	0 failures

TEST GROUP B – ACCELERATED LIFETIME SIMULATION TESTS

Test	#	Reference	Test Conditions	DEVICE	Lots	SS/Lot (units)	Total	RESULTS
HTOL (High Temp Operating Life)	B1	JESD22-A108D AEC-Q100 RevG/H	Test @ Rm/Hot/Cold +105°C ambient, 1000 hours; pattern continuously exercised at V_{CC}=1.26V, V_{CCIO}=2.63, V_{CCAUX}=3.47V	LAMXO2280E-02-FTN324	3	77	231	0 failures
			Test @ Rm/Hot/Cold +105°C ambient, 1000 hours; pattern continuously exercised at V_{CC}=3.47V, V_{CCIO}=3.47, V_{CCAUX}=3.47V	LAMXO640C-03-FTN256	3	77	231	0 failures
ELFR (Early Life Failure Rate)	B2	JESD22-A108D AEC-Q100-008A AEC-Q100 RevG/H	Test @ Rm/Hot/Cold +105°C ambient, 48 hours; pattern continuously exercised at V_{CC}=1.26V, V_{CCIO}=2.63, V_{CCAUX}=3.47V	LAMXO2280E-02-FTN324	3	800	2400	0 failures
NVCE + HTDR (Non-volatile Cycling Endurance + High Temp Data Retention)	B3	AEC-Q100-005D1 AEC-Q100 RevG/H	Test @ Rm/Hot 1000 hours, +150°C ambient	LAXP2-17E-FTN256*	3	77	231	0 failures
Extended NVCE			Test @ Rm/Hot 20u split between room/hot and chk/chk# running at 40k cycles	LAMXO2280E-02-TN100	1	80	80	0 failures

* The LAMXO uses the same Flash memory cells and are fabricated in the same wafer fab as the LAXP2 which follows AEC-Q100 Appendix 1: Definition of a Product Qualification Family. Therefore, the LAMXO Flash Non-volatile Cycling Endurance + High Temp Data Retention is Qualified-by-Similarity from the LAXP2 Non-volatile Cycling Endurance + High Temp Data Retention qualification data.

TEST GROUP C – PACKAGE ASSEMBLY INTEGRITY TESTS

Test	#	Reference	Test Conditions	DEVICE	Lots	SS/Lot (units)	Total	RESULTS
WBS (Wire Bond Shear Test)	C1	AEC-Q100-001C AEC-Q100 RevG/H	5 bonds tested per device, 45 bonds total/package	LAMXO2280E-02-FTN324	3	3	9	Cpk >2.01
				LAMXO2280E-02-TN144	3		9	Cpk >1.74
WBP (Wire Bond Pull Test)	C2	MIL-STD-883G, Method 2011.7 AEC-Q100 RevG/H	5 bonds tested per device, 45 bonds total/package	LAMXO2280E-02-FTN324	3	3	9	Cpk >2.70
				LAMXO2280E-02-TN144	3		9	Cpk >1.70

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TEST GROUP D – DIE FABRICATION RELIABILITY TESTS

Test	#	Reference	Test Conditions	RESULTS
EM (Electromigration)	D1	JESD61A.01	0.1% cumulative failure rate @ +125°C and design rule limits for current density	PASS, > 16 years
TDDB (Time Dependent Dielectric Breakdown)	D2	JESD35-A	@ +125°C and Vccmax, for 0.1% cumulative failure rate for the maximum allowed gate area device	PASS, > 220 years
HCI (Hot Carrier Injection)	D3	JESD28-1 JESD60A	@ Vccmax, room temperature and Isubmax	PASS, > 18 years
NBTI (Negative Bias Temperature Instability)	D4	JESD90	@ Vccmax, +125°C temperature for ΔSAT = 10%.	PASS, > 68 years
SM (Stress Migration)	D5	JESD87	@ +125°C	PASS, > 11 years

TEST GROUP E – ELECTRICAL VERIFICATION

Test	#	Reference	Test Conditions	DEVICE	Lots	SS/Lot (units)	Total	RESULTS
TEST (Pre and Post-Stress Electrical Test)	E1	AEC Q100-007			All	All	All	Testing Completed
HBM (Electrostatic Discharge - Human Body Model)	E2	AEC Q100-002	Test @ Rm/Hot 3 units at each stress voltage	LAMXO2280E-02-FTN324	1	12	12	>2000V (H2)
				LAMXO1200E-02-FTN256	1		12	>1500V (H1C)
				LAMXO640E-03-FTN256	1		12	>2000V (H2)
				LAMXO640C-03-FTN256	1		12	>2000V (H2)
				LAMXO256E-02-TN100	1		12	>2000V (H2)
				LAMXO256C-02-TN100	1		12	>2000V (H2)

Test	#	Reference	Test Conditions	DEVICE	Lots	SS/Lot (units)	Total	RESULTS
CDM (Electrostatic Discharge - Charge Device Model)	E3	AEC-Q100-011C1 AEC-Q100 RevG/H	Test @ Rm/Hot) 3 units at each stress voltage	LAMXO2280E-02-FTN324	1	12	12	>1000V (C6)
				LAMXO1200E-02-FTN256	1		12	>1000V (C6)
				LAMXO640E-03-FTN256	1		12	>1000V (C6)
				LAMXO640C-03-FTN256	1		12	>1000V (C6)
				LAMXO256E-02-TN100	1		12	>1000V (C6)
				MXO256C-02-TN100	1		12	>1000V (C6)
LU (Latch Up)	E4	AEC-Q100-004D JEDEC EIA/JESD78 AEC-Q100 RevG/H	Test @ Rm/Hot 6units/test (I-test/Vsupply over-voltage test)	LAMXO2280E-02-FTN324	1	3	3	>100mA & >1.5X supply (Class II)
				LAMXO1200E-02-FTN256	1		3	>100mA & >1.5X supply (Class II)
				LAMXO640E-03-FTN256	1		3	>100mA & >1.5X supply (Class II)
				LAMXO640C-03-FTN256	1		3	>100mA & >1.5X supply (Class II)
				LAMXO256E-02-TN100	1		3	>100mA & >1.5X supply (Class II)
				LAMXO256C-02-TN100	1		3	>100mA & >1.5X supply (Class II)
ED (Electrical Distributions)	E5	AEC-Q100-009	Test @ Rm/Hot/Cold	All		3	300	Pass
FG (Fault Grading)	E6	AEC-Q100-007B	Design Simulations of Test Coverage					Fault coverage = 91.3%
CHAR (Characterization)	E7	AEC-Q003	Test @ Rm/Hot/Cold	All		3	2,933	Pass

TEST GROUP F – DEFECT SCREENING TESTS

Test	#	Reference	DEVICE	Lots	SS/Lot (units)	Total	RESULTS
PAT (Process Average Testing)	F1	AEC-Q001	All	All	All	All	Pass
SBA (Statistical Bin/Yield Analysis)	F2	AEC-Q002A	Wafer	All	All	All	Pass

3.1 TEST GROUP A – ACCELERATED ENVIRONMENTAL TESTS

3.1.1 SURFACE MOUNT PRECONDITIONING

The Surface Mount Preconditioning (SMPC) Test is used to model the surface mount assembly conditions during component solder processing. All devices, stressed through Biased HAST, Unbiased HAST, Temperature Cycling and Power Temp Cycling and High Temperature Storage Life were preconditioned.
Consistent with JEDEC JESD22-A113F "Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing", the devices are subjected to 5 temperature cycles between -55°C and +125°C in an air environment, a moisture bake out for 24 hours at +125°C, a controlled moisture soak for 192 hours at 30°C/60% relative humidity, followed by 3 cycles through Pb-free 260°C reflow simulation temperature profile as defined in IPC/JEDEC J-STD-020D.1 "Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices". This preconditioning is consistent with JEDEC Moisture Sensitivity Level 3 package moisture sensitivity and dry-pack storage requirements. 40x visual inspection was performed pre and post-SMPC process.

All units were tested and data-logged at +25°C/+105°C for the LAMXO2280E devices pre and post- reliability stress. No failures were observed.

PRODUCT	PACKAGE	LOT	FABLOT	QTY	FAIL
LAMXO2280E-02	FTN324	QM424MXOA	4K6416701	276	0
		QM424MXOB	4K6426901	276	0
		QM424MXOC	4K6435601	276	0
	TN100	QM424MXOD	4K6416701	276	0
		QM424MXOE	4K6426901	276	0
		QM424MXOF	4K6463001	276	0
	TN144	QM424MXOG	4K6416701	77	0
		QM424MXOH	4K6426901	77	0
		QM424MXOI	4K6463001	77	0
	FTN256	QM424MXOJ	4K6416701	224	0

3.1.2 BIASED HAST

Highly Accelerated Stress Test (HAST) testing uses both pressure and temperature to accelerate penetration of moisture into the package and to the die surface. The Biased HAST test is used to accelerate threshold shifts in the MOS device associated with moisture diffusion into the gate oxide region as well as electrochemical corrosion mechanisms within the device package. Consistent with JEDEC JESD22-A110D "Highly-Accelerated Temperature and Humidity Stress Test (HAST)", the biased HAST conditions are with V_{CC} and $V_{CCI/O}$/V_{CCAUX} bias of 1.26V and 3.47V, respectively and alternate pin biasing in an ambient of either +130°C, 85% relative humidity for 96 hrs or +110°C, 85% relative humidity for 264 hrs.

All units were tested and data-logged at +25°C/+105°C for the LAMXO2280E devices pre and post- reliability stress. No failures were observed.

PRODUCT	PACKAGE	LOT	FABLOT	QTY	FAIL (110C/264hrs)
LAMXO2280E-02	FTN324	QM424MXOA	4K6416701	77	0
		QM424MXOB	4K6426901	77	0
		QM424MXOC	4K6435601	77	0
	PACKAGE	**LOT**	**FABLOT**	**QTY**	**FAIL (130C/96hrs)**
	TN100	QM424MXOD	4K6416701	77	0
		QM424MXOE	4K6426901	77	0
		QM424MXOF	4K6463001	77	0

3.1.3 UNBIASED HAST

Unbiased Highly Accelerated Stress Test (uHAST) testing uses both pressure and temperature to accelerate penetration of moisture into the package and to the die surface. The Unbiased HAST test is designed to detect ionic contaminants present within the package or on the die surface, which can cause galvanic corrosion. Consistent with JEDEC JESD22-A118A, "Accelerated Moisture Resistance - Unbiased HAST," the uHAST conditions are +130°C, 85% relative humidity for 96 hrs or +110°C, 85% relative humidity for 264 hrs.

All units were tested and data-logged at +25°C/+105°C for the LAMXO2280E devices pre and post- reliability perstress. No failures were observed.

PRODUCT	PACKAGE	LOT	FABLOT	QTY	FAIL (110C/264hrs)
LAMXO2280E-02	FTN324	QM424MXOA	4K6416701	77	0
		QM424MXOB	4K6426901	77	0
		QM424MXOC	4K6435601	77	0
	PACKAGE	**LOT**	**FABLOT**	**QTY**	**FAIL (130C/96hrs)**
	TN100	QM424MXOD	4K6416701	77	0
		QM424MXOE	4K6426901	77	0
		QM424MXOF	4K6463001	77	0

3.1.4 TEMPERATURE CYCLING

The Temperature Cycling (TC) Test is used to accelerate those failures resulting from mechanical stresses induced by differential thermal expansion of adjacent films, layers, and metallurgical interfaces in the die and package. Devices are exposed for 1000 cycles between -55°C and +125°C in an air environment consistent with JEDEC JESD22-A104D "Temperature Cycling" and AEC-Q100 RevG Grade 2 Temperature Cycling Stress requirements.

The LAMXO2280E in the FTN256 and TN100 has the largest die-to-package ratio while the FTN324 and TN144 has the largest package size in Saw Singulated and Thin Quad Flat Pack packages, respectively. These were chosen as the generic qualification vehicle for Temperature Cycling.

All units were tested and data-logged at +25°C/+105°C for the LAMXO2280E devices pre and post- reliability stress. No failures were observed. Wire bond pull strength was found to be >2.5 grams on 9 devices from FTN324 and TN144 sampled post-temperature cycling stress.

PRODUCT	PACKAGE	LOT	FABLOT	QTY	FAIL
LAMXO2280E-02	FTN324	QM424MXOA	4K6416701	77	0
		QM424MXOB	4K6426901	77	0
		QM424MXOC	4K6435601	77	0
	TN100	QM424MXOD	4K6416701	77	0
		QM424MXOE	4K6426901	77	0
		QM424MXOF	4K6463001	77	0
	TN144	QM424MXOG	4K6416701	77	0
		QM424MXOH	4K6426901	77	0
		QM424MXOI	4K6463001	77	0
	FTN256	QM424MXOJ	4K6416701	224	0

3.1.5 HIGH TEMPERATURE STORAGE LIFE

High Temperature Storage Life (HTSL) Test is typically used to determine the effect of time and temperature, under storage conditions, for thermally accelerated failure mechanisms of solid state electronic devices. Devices were stressed at +150°C for 500 hrs consistent with JEDEC JESD22-A103D "High Temperature Storage Life" and AEC-Q100 RevG Grade 2-4 High Temp Storage Life stress requirements.

All units were tested and data-logged +25°C/+105°C for the LAMXO2280E devices pre and post- reliability stress. No failures were observed.

PRODUCT	PACKAGE	LOT	FABLOT	QTY	FAIL
LAMXO2280E-02	FTN324	QM424MXOA	4K6416701	45	0
		QM424MXOB	4K6426901	45	0
		QM424MXOC	4K6435601	45	0
	TN100	QM424MXOD	4K6416701	45	0
		QM424MXOE	4K6426901	45	0
		QM424MXOF	4K6463001	45	0

3.2 TEST GROUP B – ACCELERATED LIFETIME SIMULATION TESTS

3.2.1 HIGH TEMPERATURE OPERATING LIFE

The High Temperature Operating Life (HTOL) Test is used to thermally accelerate those wear out and failure mechanisms that would occur as a result of operating the device continuously in a system application. A pattern specifically designed to exercise the maximum amount of circuitry is programmed into the device and this pattern is continuously exercised at V_{CC} and $V_{CCI/O}$ bias of 1.26V and 2.63V (V_{CCAUX} = 3.47V), respectively for the low voltage (MOX2280E) devices and 3.47V and 3.47V (V_{CCAUX} = 3.47V), respectively, for the upper voltage (MXO640C) devices at +105°C ambient for 1000 hrs consistent with JEDEC JESD22-A108D "Temperature, Bias, and Operating Life" and AEC-Q100 RevG Grade 2 High Temperature Operating Life stress requirements.

All units were tested and data-logged at -40°C/+25°C/+105°C for the LAMXO2280E and LAMXO640C devices pre and post- reliability stress. No failures or significant parameter shifts were observed.

PRODUCT	PACKAGE	LOT	FABLOT	QTY	FAIL
LAMXO2280E-02	FTN324	QM424MXOA	4K6416701	77	0
		QM424MXOB	4K6426901	77	0
		QM424MXOC	4K6435601	77	0
LAMXO640C-03	FTN256	QM424MXOM	4K6564601	77	0
		QM424MXON	4K6581801	77	0
		QM424MXOO	4K6590801	77	0

3.2.2 EARLY LIFE FAILURE RATE

An Early Life Failure Rate (ELFR) evaluation is generated using the HTOL test conditions to verify device quality. ELFR is used to thermally accelerate those wear out and failure mechanisms that would occur as a result of operating the device continuously in a system application. A pattern specifically designed to exercise the maximum amount of circuitry is programmed into the device and this pattern is continuously exercised at V_{CC} and $V_{CCI/O}$ bias of 1.26V and 2.63V (V_{CCAUX} = 3.47V), respectively, for the low voltage (MOX2280E) devices at +105°C ambient for 48 hrs consistent with AEC-Q100-008 RevA "Early Life Failure Rate" .

All units were tested and data-logged at +25°C/+105°C for the LAMXO2280E devices pre and post- reliability stress. No failures were observed.

PRODUCT	PACKAGE	LOT	FABLOT	QTY	FAIL
LAMXO2280E-02	FTN324	QM424MXOA	4K6416701	800	0
		QM424MXOB	4K6426901	800	0
		QM424MXOC	4K6435601	800	0

3.2.3 NON-VOLATILE MEMORY CYCLING ENDURANCE & HIGH TEMP DATA RETENTION

The LAMXO uses the same Flash memory cells and are fabricated in the same wafer fab as the LAXP2. *(See AEC-Q100 Appendix 1: Definition of a Product Qualification Family).* Therefore, the LAMXO Flash NVM Cycling Endurance & Data Retention is Qualified-by-Similarity from the LAXP2 HTRX data.

Since the LAXP2 uses Flash memory cells, qualification testing includes the AEC-Q100-005-Rev-B, Nonvolatile Memory Program/Erase Endurance, Data Retention, and Operational Life Test. The normal mode of the LAXP2 Flash Array is unbiased (Idle mode).

High Temperature Data Retention test measures the Flash cell reliability while the High Temperature Operating Life test is structured to measure functional operating circuitry failure mechanisms. The High Temperature Data Retention test is specifically designed to accelerate charge gain on to or charge loss off of the floating gates in the device's array. Since the charge on these gates determines the actual pattern and function of the device, this test is a measure of the reliability of the device in retaining programmed information. During normal operation, the Flash cells are unbiased after initial power on configuration. Therefore, in High Temperature Data

Retention, the Flash cell reliability is determined by monitoring the cell margin after unbiased 150°C storage. All cells in all arrays are life tested in both programmed and erased states.

Prior to data retention testing, all LAXP2 devices are programmed and erased 10,000 times.

All units were tested and data-logged at -+25°C/+105°C prior to reliability stress and after reliability stress. No failures or significant parameter shifts were observed.

PRODUCT	PACKAGE	LOT	QTY	FAIL
LAXP2-17E	FTN256	8	100	0
		9	80	0
		10	80	0

Additionally, 80u of LAMXO2280E devices are split into 20u room/hot/chk/chk# matrix combination and are subjected to extended program/erase cycles in order to exercise high voltage control circuits in the flash array that will verify no difference in 300mm reliability.

All units were tested and data-logged at +25°C/+105°C for the LAMXO2280E devices pre and post- reliability stress. No failures were observed up to 40,000 program/erase cycles.

PRODUCT	PACKAGE	LOT	FABLOT	CONDITION	QTY	FAIL
LAMXO2280E-02	TN100	QM411MXOJ	4K6416701	CHK @ 25C	20	0
				CHK @ 85C	20	0
				CHK# @ 25C	20	0
				CHK# @ 85C	20	0

3.3 TEST GROUP C – PACKAGE ASSEMBLY INTEGRITY TESTS

3.3.1 WIRE BOND SHEAR

Wire Bond Shear (WBS) Test is used to measure the strength of the interface between a gold ball bond and a package bonding surface on post-encapsulation devices. This strength measurement is extremely important in determining the integrity of the metallurgical bond which has been formed and the reliability of gold wire bonds to die or package bonding surfaces. Wire bond shear was tested consistent with the AEC-Q100-001 RevC "Wire Bond Shear Test".

Forty-five bonds from nine devices per package were used for the Wire Bond Shear test. All bond shear readings were >23.7 grams and >23.4 grams passing the minimum shear strength for a 324-ball ftBGA package with 1.7 mils ball bond diameter and a 144-ball TQFP package with 1.9 mils ball bond diameter, respectively.

The average measured bond shear results were Cpk of >2.01 for FTN324 and Cpk of >1.74 for TN144.

3.3.2 WIRE BOND PULL

Wire Bond Pull (WBP) Test is used to measure the wire bond strength at the ball joints and stitch bonds. Wire bond strength was tested consistent with Military Standard MIL-STD-883G, Method 2011.7 "Bond Strength".

Forty-five bonds from nine devices per package were used for Wire Bond Pull test. All bond pull readings were >5.7 grams and >4.2 grams for a 324-ball ftBGA package and a 144-ball TQFP package, respectively, passing the minimum bond strength for a 0.9 mil gold wire post-seal.

The average measured bond pull strength results were Cpk of >2.70 for FTN324 and Cpk of >1.70 for TN144.

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3.4 TEST GROUP D – DIE FABRICATION RELIABILITY TESTS

3.4.1 ELECTROMIGRATION

When a metal conductor conducts electrons some degree of metal atom fluence occurs due to electron impact with the metal conductor atoms. Over time this fluence of metal atoms results in a voiding of the metal upstream from the electron current and a pile-up of metal atoms downstream. The metal line will eventually fail due to an “open” upstream or due to shorting to adjacent metal lines downstream (extrusion).

The Electromigration Lifetime (EML) of a given conductor is highly dependent on current density and temperature. MOS technology features a high density of metal conductors at more than one level on the chip. This results in large current density in numerous areas on chip and a definite susceptibility to EML failure. The 130 nm Flash technology design rules prevent extrusion by minimum spacing requirements and prevents “opens” by imposing current density limits.

The EML resistance of a MOS technology also depends upon the conductor material properties and upon the conductor line width and thickness control, especially over “terrain”.

The EML lifetime is monitored by applying accelerated conditions of constant current density and temperature. The stress data is used to predict conductor lifetime under maximum design rule current density and maximum device temperature. A minimum 10 year lifetime for EML is required by Lattice Semiconductor for all technologies in production.

The LA-MachXO family electromigration lifetimes for a 0.1% cumulative failure rate are >16 years @ +125°C and design rule limits for current density.

3.4.2 TIME DEPENDENT DIELECTRIC BREAKDOWN

The lifetimes of the insulator elements of MOS technology depend upon their inherent material properties and also upon their environment, e.g. the electric field strength applied and the temperature.

When any insulator in a MOS circuit fails the circuit itself either fails or exhibits errors in operation. The most critical insulators are the MOSFET Gate oxides because the electric field strength applied to them is much greater than that applied to any other part of the circuit.

When an electric field (voltage) is applied to an oxide a small current flows in the direction of the field vector. The charge carriers are normally electrons and some of them become trapped in the oxide. The total amount of trapped charges (electrons) is a function of time, temperature, and oxide quality. The trapped charge eventually reaches the point where the internal electric field generated by these trapped charges overcomes the (opposite) applied field and then exceeds the dielectric strength of the oxide. At this point the oxide fails (becomes shorted). The effect is called Time Dependent Dielectric Breakdown (TDDB).

TDDB stress is monitored by accelerated conditions of constant applied electric field strength and temperature. The stress time to fail data is used to predict dielectric lifetime under constant worst case circuit conditions. All Lattice Semiconductor technologies require the gate oxides to survive 10 years lifetime under maximum design rule conditions.

The TDDB lifetimes for the LA-MachXO family are >220 years @ +125°C and V_{CCMAX}, for 0.1% cumulative failure rate for the maximum allowed gate area device.

3.4.3 HOT CARRIER INJECTION

The lifetime of a MOSFET is determined by the rate of change of its operational device parameters.

When one or more of these device parameters degrades in excess of the limits of the circuit design requirements for the device, the circuit can; lose speed, intermittently lose data, exhibit logic errors, and eventually fail to operate.

Two of the MOSFET parameters that have been observed to be the most problematical are the Threshold Voltage and the Transconductance. For an N-Channel MOSFET the transconductance decreases and the threshold voltage increases with time. This effect is a result of charge trapping in the gate oxide which is induced by excess substrate current and is dependent upon the actual device's bias conditions within the circuit configuration. The degradation mechanism is called "hot" carrier (HC) because the channel charge carriers have energy in excess of that required to breach the oxide-silicon barrier and then cause trapping in the oxide.

Transconductance is directly proportional to the linear region current and is not an extrapolated measurement. However, the drive current, I_{DSAT}, is the most useful parameter to monitor. A degradation of 10% in I_{DSAT} is considered to be the point where many circuits will start to exhibit some form of circuit performance effects. Therefore, for purposes of monitoring, a 10% decrease in I_{DSAT} is considered a "fail".

Despite the name, Hot Carrier degradation is worse at low temperatures than at higher temperatures largely because the substrate current decreases with increasing temperature. Hot carrier degradation is monitored at room temperature in order to accelerate the test and to provide a safety factor in lifetime predictions. Lattice Semiconductor requires greater than 10 years predicted lifetime for all of its production technologies.

The LA-MachXO products' Hot Carrier Injection AC lifetime is >18 years @ V_{CCMAX}, room temperature and I_{SUBMAX}.

3.4.4 NEGATIVE BIAS TEMPERATURE INSTABILITY

Degradation of P Channel transistors at negative Vg when all other terminals are zero has been shown to represent a significant circuit condition below 130 nm gate widths. A similar positive Vg effect exists for N channels at 90nm gate widths and smaller. Negative Bias Temperature Instability (NBTI) is dominant at elevated temperature and Vg. The same degradation parameters and percentage as for HCI are applied to NBTI. Stress is performed at Tjrel at 3 or more elevated Vg (>2*Vcc). The time to fail (TTF) is plotted vs Vg or 1/Vg and extrapolated to nominal VG to obtain the lifetime.

The most commonly reported parameters are Idsat and Vth. It is also useful to use a specific Vth shift in place of "10%" to quote lifetime (e.g. 50 mV). TTF is reported at Tstress = Tjrel.

The LA-MAchXO products' NTBI is >68 years @ V_{CCMAX}, +125°C temperature for Δ_{DSAT} = 10%.

3.4.5 STRESS MIGRATION

Microscopic voids exist in Dual Damascene Copper structures. These voids can migrate when driven by elevated temperature and they can coalesce into larger voids, which eventually cause open metal lines. Stress in surrounding material (e.g. the IMD) also drives void migration. In most cases the highest stress point is where the top of the Via meets the metal line. For each metal group a large Via chain (typically >1e6 Vias total) is designed which incorporates all metal lines and vias within the metal group. A change in via resistance of 10% is the convention for a failure. Stress is conducted unbiased at Tjrel (or higher). Readpoints are taken at selected intervals usually with a given maximum stress time limit (1000hr). The Arrhenius equation (and a geometrical form factor for the DUT) is used to calculate the min TTF from the max stress limit if no fails occur. Otherwise, a lognormal plot is used.

The LA-MachXO family Stress Migration lifetimes are >11 years @ 125°C.

3.5 TEST GROUP E – ELECTRICAL VERIFICATION

3.5.1 PRE/POST-ELECTRICAL TEST AND ELECTRICAL DISTRIBUTIONS

All the pre and post-stress electrical tests performed on the LA-MachXO production test system included DC, AC, and functional tests with datalogging of key parameters enabled.

Electrical Distribution assessment was done using material sampled from nominal wafers from production tested at -40°C/+25°C and +105°C for the LAMXO2280E, LAMXO1200E, LAMXO640E/C and LAMXO256E/C devices. All data is within PAT limits for all test temps.

A Parametric Drift of Individuals assessment was also done using the parametric data collected at each readout of each stress to determine any significant device performance changes for each stress test consistent with reference document AEC-Q100-009 RevB "Electrical Distributions Assessment", section 3.6. A copy of the results is available upon request.

3.5.2 ELECTROSTATIC DISCHARGE – HUMAN BODY MODEL

Each member of the LA-MachXO product family was tested per the AEC-Q100-002 RevD "Human Body Model (HBM) Electrostatic Discharge (ESD) Test" criteria for measuring HBM ESD Sensitivity of electronic devices. *All units were tested and data-logged at +25°C/+105°C for the LAMXO2280E, LAMXO1200E, LAMXO640E/C and LAMXO256E/C devices pre and post- reliability stress. HBM performance for this product meets AEC-Q100-002D Classification H1C.*

PRODUCT	PACKAGE	LOT	HBM PASSING VOLTAGE	AEC-Q100-002 Component Classification
LAMXO2280E-02	FTN324	QM411MXOE	>2000V	H2
LAMXO1200E-02	FTN256	QM424MXOL	>1500V	H1C
LAMXO640E-03		QM424MXOP	>2000V	H2
LAMXO640C-03		QM424MXOM	>2000V	H2
LAMXO256E-02	TN100	QM424MXOR	>2000V	H2
LAMXO256C-02		QM424MXOQ	>2000V	H2

3.5.3 ELECTROSTATIC DISCHARGE – CHARGE DEVICE MODEL

Each member of the LA-MachXO product family was tested per the AEC-Q100-011 RevB "Charge Device Model (CDM) Electrostatic Discharge Test" criteria for measuring CDM ESD sensitivity of electronic devices.

All units were tested and data-logged at +25°C/+105°C for the LAMXO2280E, LAMXO1200E, LAMXO640E/C and LAMXO256E/C devices pre and post- reliability stress. CDM performance for this product meets AEC-Q100-011B Classification C6.

PRODUCT	PACKAGE	LOT	CDM PASSING VOLTAGE	AEC-Q100-011 Component Classification
LAMXO2280E-02	FTN324	QM411MXOE	>1000V	C6
LAMXO1200E-02	FTN256	QM424MXOL	>1000V	C6
LAMXO640E-03		QM424MXOP	>1000V	C6
LAMXO640C-03		QM424MXOM	>1000V	C6
LAMXO256E-02	TN100	QM424MXOR	>1000V	C6
LAMXO256C-02		QM424MXOQ	>1000V	C6

3.5.4 LATCH-UP

Each member of the LA-MachXO product family was tested per the AEC-Q100-004 RevC “IC Latch-up Test” criteria, which references the JEDEC EIA/JESD78 IC Latch-up Test procedure.

All units were tested and data-logged at +25°C/+105°C for the LAMXO2280E, LAMXO1200E, LAMXO640E/C and LAMXO256E/C devices pre and post- reliability stress. No failures were observed within the passing classification.

PRODUCT	PACKAGE	LOT	I-TEST LATCHUP RESULTS	JEDEC/JESD78 LATCH UP LEVEL
LAMXO2280E-02	FTN324	QM411MXOE	>100mA @ +105C	Class II
LAMXO1200E-02	FTN256	QM424MXOL	>100mA @ +105C	Class II
LAMXO640E-03		QM424MXOP	>100mA @ +105C	Class II
LAMXO640C-03		QM424MXOM	>100mA @ +105C	Class II
LAMXO256E-02	TN100	QM424MXOR	>100mA @ +105C	Class II
LAMXO256C-02		QM424MXOQ	>100mA @ +105C	Class II

PRODUCT	PACKAGE	LOT	V-SUPPLY OVERVOLTAGE TEST LATCHUP RESULTS	JEDEC/JESD78 LATCH UP LEVEL
LAMXO2280E-02	FTN324	QM411MXOE	>1.5x V-supply @ +105C	Class II
LAMXO1200E-02	FTN256	QM424MXOL	>1.5x V-supply @ +105C	Class II
LAMXO640E-03		QM424MXOP	>1.5x V-supply @ +105C	Class II
LAMXO640C-03		QM424MXOM	>1.5x V-supply @ +105C	Class II
LAMXO256E-02	TN100	QM424MXOR	>1.5x V-supply @ +105C	Class II
LAMXO256C-02		QM424MXOQ	>1.5x V-supply @ +105C	Class II

3.5.5 FAULT GRADING

The fault coverage for the LA-MachXO family was calculated to be 91.3%.

```
-- *****************************************************************************
-- *                                                                           *
-- *   SynTest TurboFault 2005                                                 *
-- *                                                                           *
-- *   Fault Simulation Coverage Report                                        *
-- *                                                                           *
-- *****************************************************************************

-- *****************************************************************************
-- *                                                                           *
-- *   Statistic Data                                                          *
-- *                                                                           *
-- *****************************************************************************

-- Number of Faults:                                 844791
-- Number of Collapsed Faults:                       709762

-- Number of Hard Detected Faults:                   457098 ( 54.1078%)
-- Number of Probably Detected Faults:               176015 ( 20.8353%)
-- Number of Potentially Detected Faults:            138177 ( 16.3564%)
-- Number of Undetected Faults:                       62677 (  7.4192%)
-- Number of Hyperactive Faults:                          0 (  0.0000%)
-- Number of Hypertrophic Faults:                         0 (  0.0000%)
-- Number of Oscillatory Faults:                          7 (  0.0008%)
-- Number of Untestable Faults:                       10815 (  1.2802%)
-- Number of Error Faults:                                2 (  0.0002%)
-- Number of Uncompleted Faults:                          0 (  0.0000%)

-- Coverage Number:                                 54.1078%
-- Optimal Coverage Number:                         74.9432%

-- Total Fault Coverage (Hard + Probable + Pot)    91.2995%
```

All fault simulations were performed using the Syntest TurboFault 2005 fault simulator.

Fault simulation and analysis was performed by generating a gate-level model of the MachXO-256 device and applying all applicable functional test vectors from the manufacturing test programs.

The LA-MachXO family of devices was developed using a design-reuse methodology (i.e.: all family members were built from a "common design element" library). Similarly, the manufacturing test patterns and test methodologies were also common to all family members and, as such, the MachXO-256 fault simulation results are deemed to be representative of all devices in the family.

3.5.6 CHARACTERIZATION

Each device in the Automotive LA-MachXO family was characterized at the time of product release over the automotive temperature range of –40°C to +125°C. In all cases, characterization was performed over CD and Vt process splits in order to gather performance data across the entire process distribution for those parameters. These reports are available upon request.

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3.6 TEST GROUP F – DEFECT SCREENING

3.6.1 PART AVERAGE TESTING

Part Average Testing (PAT) is a method for removing units with statistically abnormal characteristics (outliers) from semiconductors supplied to automotive customers. PAT based on LA-MachXO device characterization has been implemented into the automotive flow manufacturing test programs per the AEC-Q001 RevC "Guidelines for Part Average Testing". A copy of the PAT results is available upon request.

3.6.2 STATISTICAL BIN ANALYSIS

Statistical Bin Yield Analysis (SBYA) is a method for screening rogue wafers using statistically generated screens. SBYA based on LA-MachXO device characterization has been implemented into the automotive flow manufacturing test programs per the AEC-Q002-Rev-A Guidelines for Statistical Yield Analysis. A copy of the SBYA results is available upon request.

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