



Release Notes for Lattice Diamond 3.3

Welcome to Lattice Diamond[®], the complete design environment for Lattice Semiconductor FPGAs. Lattice Diamond design software offers leading-edge design and implementation tools optimized for cost-sensitive, low-power Lattice FPGA architectures. Diamond is the next generation replacement for ispLEVER[®], featuring design exploration, ease of use, improved design flow, and numerous other enhancements. Diamond is available for both the Windows and Linux operating systems. For details, see “System Requirements” on page 10.

This version of Diamond adds a variety of enhancements to make designing for Lattice Semiconductor programmable devices easier than ever. The design tools also include support for the latest Lattice Semiconductor devices. See “What’s New” on page 2.

Lattice Semiconductor offers a rich variety of information sources, including the Help system, PDF manuals, tutorials, and online discussions. The easiest way to reach them all is through the online Help. The first topic in the [Help](#) provides links to all the other sources of information.

You can also find extensive information about Diamond, its capabilities, tools, and workflow on the Lattice Semiconductor Web site under:

www.latticesemi.com/latticediamond

What's New

This release of Diamond provides a variety of new features in the following areas. See the online Help for details. Also see "Issues Fixed" on page 12 for known issues of the previous release that have been fixed.

Device Support All MachXO3L devices with csfBGA packages are now under license control because the package pinouts in this and previous releases will not match the final product. Lattice recommends that you target an alternate package until the csfBGA pinouts are finalized. To use one of these controlled devices, contact Lattice Semiconductor for a license.

Operating System Diamond is now supported on Windows 8, 32-bit or 64-bit.

Clarity Designer Clarity Designer has added a Schematic view to its Builder tab. In the Schematic view you can do all the same connection functions as in the previous spreadsheet view (now called the Components view of Builder) but with a schematic interface showing the modules and their connections. For more information, open the online Help and go to [Entering the Design > Creating Clarity Designer Modules > Building](#).

Deployment Tool Support has been added for 512 Mbits SPI Flash. For more information, open the online Help and go to: [Programming the FPGA > Deploying the Design with the Deployment Tool > Deployment Function Types > External Memory Deployment Type](#).

Documentation there's a new online Help system with major improvements involving Google Chrome and text search.

Chrome is now supported by the online help system. The new system can be opened with the popular Google Chrome browser in addition to the other major browsers.

The search system has been improved in several ways. Differences include:

- ▶ Search box in the toolbar. You can type in your search terms in the box next to the magnifying glass  (Search) button. The Search button takes you to a separate page for the results.
- ▶ Search while you type for faster results. While in the Search page, the list of hits appears and is modified while you're typing (after the first three letters). This is not visible when using the Search box in the main toolbar. Click the  (Search) button to go to the Search page and see the results.
- ▶ Search results have context. Each search hit includes the first few lines of the topic to help you decide if the topic is relevant to your question.
- ▶ Search results re-organized. Search results are no longer organized by book and no longer have relevance scores. Instead, hits from all the

books are listed in relevance order. The first few hits are the most likely to be relevant..

Search Navigation Tip

Your browser's forward and back buttons may not work the way you expect with the Search page. To go to the Search page, always click the  (Search) button. If you're on the Search page and want to go back to the topic you were looking at, click the  (Contents) button.

For more information, open the online Help and go to: [Help for Lattice Diamond > Getting Help > Using the Help](#).

EPIC Info, Warning, and Error message tabs have been added. For more information, open the EPIC online Help and go to [General Operations > Viewing Info, Warning and Error Messages](#).

There are also new short cut functions. For more information, open the EPIC online Help and go to [General Operations](#).

The version of EPIC used prior to Diamond 3.0 will be removed in the next major release of Diamond. This version of EPIC is only available in Diamond 3.0-3.3 through the command line.

LatticeMico System LatticeMico™ System has a new LatticeMico PMBus Adapter (V1.0) component. The PMBus Adaptor supports new functionality when using Platform Designer with MachXO2 and Platform Manager 2.

For more information, refer to the “LatticeMico System Software Release Notes for Diamond.” To access the release notes:

- ▶ If LatticeMico System is installed with Diamond, go to the Windows Start menu and choose **Programs > Lattice Diamond > Accessories > LatticeMico System Release Notes**.
- ▶ If LatticeMico System is installed as a stand-alone tool, go to the Windows Start menu and choose **Programs > Lattice Diamond > LatticeMico System Release Notes**.

LDC Editor Three new tabs have been added to provide enhanced LDC File editing capability. You can now define clock groups, generated clocks, and set attributes using LDC Editor. You can also edit an LDC file by selecting objects in the Netlist Analyzer and dragging-and-dropping the objects into LDC Editor. For more information, open the online Help and go to [Applying Design Constraints > Using SDC Constraints > Applying Lattice Synthesis Engine Constraints > Defining Synthesis Constraints Using the LDC Editor](#).

Netlist Analyzer Netlist Analyzer is a new tool that works with Lattice Synthesis Engine (LSE) to produce schematic views of your design while it is being implemented. Use the schematic views to better understand the hierarchy of the design and how the design is being implemented. Key features include multiple views, cross-probing, and multiple ways to view and filter data. For more information, open the online Help and go to [Managing Projects > Analyzing a Design > About Netlist Analyzer](#).

Platform Designer Support has been added for configuring PMBus. PMBus is a serial communication bus that allows a microcontroller to configure and monitor Digital Point of Load (DPOL) DC-DC Converters. The PMBus Adapter allows the connection of analog POLs to the PMBus controller using the FPGA and ASC. Multiple POLs may be mapped to different pages configured in the PMBUS adapter. Dedicated pages for voltage, current, and temperature monitoring are provided. For more information, open the online Help and go to [Designing with Lattice Diamond Platform Designer > Configuring PMBus Adapter](#).

Power Calculator A page has been added to display calculated power consumed by Analog Sense and Control (ASC) devices used in MachXO2 and Power Manager 2 designs. For more information, open the online Help and go to [Analyzing Power Consumption > Power Calculator Window Features > Power Calculator Pages](#) and [Designing with Lattice Diamond Platform Designer > Working with Power Calculator](#).

Programmer The new FTDI cable (HW-USBN-2B) is now officially supported. For more information, open the online Help and go to [Programming the FPGA > Using Programmer > Detecting a Cable](#).

Simulation (Windows version) The Aldec® [Active-HDL™ Lattice Edition](#) simulator has been updated.

Strategy Options The Strategy options for Lattice Synthesis Engine (LSE) now include:

- ▶ Loop Limit, which specifies the maximum number of iterations of “for” and “while” loops in the source code. The limit is applied when the loop index is a variable, not when it is a constant. The higher the loop_limit, the longer the run time. The default value is 1950. Setting a higher value may cause stack overflow during some of the optimizations during synthesis.
- ▶ Disable Distributed RAM, which prevents inferred memory from using the distributed RAM.

Synthesis Tools The Synopsys® [Synplify Pro®](#) for Lattice and Lattice Synthesis Engine (LSE) synthesis tools have been updated.

LSE supports four new Synopsys Design Constraints (SDC) directives: full_case, parallel_case, syn_enum_encoding, and syn_sharing. For more information, open the online Help and go to [Constraints Reference Guide > Lattice Synthesis Engine \(LSE\) Constraints > Synopsys Design Constraints \(SDC\)](#).

Supported Devices

Lattice Diamond can be used with either a free license or a subscription license. The two licenses provide access to different device families.

Device Family	Free License	Subscription License
ASC	◀	◀
ECP5™		◀
LatticeEC™	◀	◀
LatticeECP™	◀	◀
LatticeECP2™	◀	◀
LatticeECP2M™		◀
LatticeECP2S		◀
LatticeECP2MS		◀
LatticeECP3™		◀
LatticeSC™		◀
LatticeSCM™		◀
LatticeXP™	◀	◀
LatticeXP2™	◀	◀
MachXO™	◀	◀
MachXO2™	◀	◀
MachXO3L	◀	◀
Platform Manager™	◀	◀
Platform Manager 2	◀	◀

Note

ECP5 and MachXO3L devices with csfBGA packages are under license control. To use one of these controlled devices, contact Lattice Semiconductor for a license.

Updating Projects from an Earlier Version

If you want to work on a design project created with an earlier version of Diamond, start with the following procedures. These procedures adapt the project for the changes in Diamond.

Find out which version of Diamond your project was created with. Then work through the changes for that and every later version, starting with the earliest and going to the most recent. For example, if your project was created with

Diamond 1.1, you would start with the changes for 1.1. After completing those changes, you would work on the changes for 1.2, then 1.4, and so on.

When you open a project from Diamond 1.2 or earlier, Diamond opens a dialog box warning that Diamond will automatically move all SDC files to the Synthesis Constraint Files folder in File List view and remove the "Input SDC Constraint File" options from the strategies. If the project is using LSE, the file names will be changed to use an .lsc extension.

Once saved, the project will not be compatible with earlier Diamond versions.

2.2 Projects

ECP5 does not use the CIN port of the CCU2C Carry Chain primitive. This port should not be connected to anything. If the port is connected, the Design Map stage will fail with an error message. If you see such a failure, correct the design in one of the following ways:

- ▶ Rerun synthesis. This should correct the problem if the CCU2C primitive is part of an IPexpress module.
- ▶ If the CCU2C primitive was added to your HDL manually, edit the code to remove the connection. See the following examples:

In Verilog:

```
CCU2C addsub_0 (.A0(scuba_vlo), .A1(DataA[0]),
               .B0(scuba_vlo), .B1(DataB[0]), .C0(scuba_vhi),
               .C1(scuba_vhi), .D0(scuba_vhi), .D1(scuba_vhi),
               .CIN(), .S0(), .S1(Result[0]), .COUT(co0));
```

In VHDL:

```
signal tmp: std_logic := 'X';
cnt_cia: CCU2C
  generic map (INJECT1_1=> "NO", INJECT1_0=> "NO",
              INIT1=> X"0000", INIT0=> X"0000")
  port map (A0=>scuba_vhi, A1=>scuba_vhi, B0=>scuba_vhi,
           B1=>scuba_vhi, C0=>scuba_vhi, C1=>scuba_vhi,
           D0=>scuba_vhi, D1=>scuba_vhi,
           CIN=>tmp, S0=>open, S1=>open, COUT=>cnt_ci);
```

2.0.1 Projects

The default values of several strategy options were changed. If you are using Synplify Pro in integrated mode (running synthesis automatically in Diamond), check that the following settings are still as you want them. Also, check the setting of the Auto Hold-Time Correction option under Place & Route Design. Its default changed to On for all devices.

Table 1: New Default Values for Synplify Pro for Lattice

Option	Before	Now
Fanout Limit is now Fanout Guide	100	1000
Export Diamond Settings to Synplify Pro GUI (new in 2.2)	Not available	No
Fix Gated Clocks and Fix Generated Clocks combined into new Clock Conversion	3 (converts and reports all sequential elements)	True (converts with no report)
Frequency	200	auto (blank means "auto")
Number of Critical Paths	3	blank (unspecified)
Number of Start/End Points	0	blank (unspecified)
Output Preference File	False	True
Pipelining and Retiming	False	Pipelining Only
Resolved Mixed Drivers	True	False
Use Clock Period for Unconstrained I/O	True	False

1.4 Projects

For Diamond 1.4 and earlier, there might be some constraints that are not honored because of the Synplify Pro cross-probing feature. This EDIF renaming is usually related to bus names.

If such a problem occurs, you can turn off the renaming feature by placing the following line in the "Command line Options" text box of the Synplify Pro section of the active strategy:

```
set_option -syn_edif_array_rename 0
```

1.2 Projects

There were several enhancements for IP and MachXO2.

IP Incompatibilities

SPI4.2 2.7 is not compatible with Diamond 1.3 or later. If you are using this IP, check the Lattice Semiconductor Web site for a more recent version.

MachXO2 Changes

See if your design involves any of the following features:

- ▶ For EFB modules with user flash memory (UFM), regenerate the module.
- ▶ For IO_TYPE=PCI33 on a MachXO2-1200 or larger device, check if the CLAMP is using the default setting. With Diamond 1.3 the CLAMP default changes from ON to PCI and the I/O will be placed in bank 2. If you were using the default and still want the setting to be ON, you need to set it explicitly.
- ▶ For PCI33 MT 6.5 and PCI33 T 6.4 IP, either set the CLAMP to ON explicitly or choose a bigger package (256 or more).

1.1 or 1.0 Projects

There were several enhancements for IP and MachXO2.

IP Incompatibilities

The following IP versions are not compatible with Diamond 1.2 or later. If you are using any of these IP, check the Lattice Semiconductor Web site for a more recent version.

- ▶ Convolution Block Encoder 3.6
- ▶ Interleaver Deinterleaver 3.5
- ▶ DDR1 6.9
- ▶ PCI_MT_33 6.4
- ▶ DDR2 7.1
- ▶ PCIe RC Lite 1.2
- ▶ DDR3 1.2.1
- ▶ Tri-Speed MAC 3.4
- ▶ DDR1_CP 1.1 with MachXO2
- ▶ Viterbi Block Decoder 4.6
- ▶ DDR2_CP 1.1 with MachXO2

MachXO2 Support

Some aspects of the software support for MachXO2 designs have been improved. See if your design involves any of the following features:

- ▶ The 4K/7K design with PLL has a CIB-to-PLL jump change. If you are using this design, recompile it.

- ▶ The EFB simulation model has changed. If you are using the EFB module, rerun your simulation tests to see more accurate results.
- ▶ In the DDR_GENERIC module of IPexpress, the GDDR1_RX.Aligned with PLL interface is no longer supported. If you are using such a module, use IPexpress to regenerate it without the PLL option.

Also, MachXO2 has IP evaluation capability and TransFR mode for all I/Os.

Migrating ispLEVER Projects

Diamond uses a different project structure than ispLEVER and cannot directly open an ispLEVER project. However, design projects created in ispLEVER can easily be imported into Diamond. The process is automatic except for the ispLEVER process properties, which are similar to the Diamond strategy settings, and some modules and IPs. All of your ispLEVER project source will be automatically handled.

Projects created using ispLEVER can be imported into Lattice Diamond through two different paths:

- ▶ On the Start Page, click **Import ispLEVER Project** (in the upper-left corner).
- ▶ From the File menu, choose **Open > Import ispLEVER Project**.

Follow the directions in the dialog box that opens to convert your ispLEVER project into a Lattice Diamond project.

Limitations to the import/conversion process include:

- ▶ NGO files in ispLEVER projects need to be manually copied into the Lattice Diamond project if the NGO files were originally copied into the ispLEVER project. For example, NGO files that were copied from Lattice IP generation.
- ▶ The .lpc files are replaced with .ipx files in Lattice Diamond. You need to regenerate your IP by double-clicking on the .lpc file. The resultant wizard will help you generate the new .ipx file, replacing the old .lpc file.

More information on importing ispLEVER projects can be found in the *Lattice Diamond User Guide*, online Help (see [Managing Projects > Importing ispLEVER Projects](#)), and training videos on the Lattice Web site.

Other Information Resources

Other available information resources for the Diamond software include the following.

- ▶ General Information: General information on Lattice Diamond can be found on the Lattice Web site at:

www.latticesemi.com/latticediamond

- ▶ Online Help: Start Lattice Diamond and choose **Help > Lattice Diamond Help**.
- ▶ *Lattice Diamond User Guide*: This document can be found from a link on the Start Page view.
- ▶ Training Videos: Several short videos are available on different aspects of the Lattice Diamond software. These can be viewed online at:
www.latticesemi.com/latticediamond
Click the **Videos** tab.

System Requirements

The basic system requirements for Lattice Diamond are:

- ▶ Intel Pentium or Pentium-compatible PC, or AMD Opteron system support (Linux only)
- ▶ One of the following operating systems:
 - ▶ Windows XP, Windows Vista (32-bit), Windows 7 (32-bit or 64-bit), or Windows 8 (32-bit or 64-bit).

Note

This is the last major release of Diamond to support Windows XP and Vista.

- ▶ Red Hat Enterprise Linux 4.X, 5.3, or 6. The host operating system can be either 32-bit or 64-bit.

Version 5.3 of Red Hat Enterprise Linux has some extra installation requirements. See “Configuring Red Hat 5.3” on page 12.
- ▶ Novell SUSE Linux Enterprise 10 SP1 or 11 operating system. Novell SUSE Linux supports 32-bit only.
- ▶ Approximately 5.75 GB free disk space
- ▶ RAM adequate for your FPGA design. For guidelines see “Memory Requirements” on page 11.
- ▶ Network adapter and, for a floating license, network connectivity

A node-locked license is based on the physical (hard-coded) address provided by the network adapter. Network connectivity is not required for a node-locked license. In the absence of a network connection, you can install the NWLink IPX/SPX protocol to force recognition of your NIC card ID (see the installation notice).

A floating license requires access to the license server, so both a network adapter and connectivity are required.
- ▶ JScript-capable Web browser
- ▶ Acrobat Reader 5.0 or later

Memory Requirements

Table 2 lists the minimum memory requirements and the recommended memory for the Lattice Semiconductor devices supported by Diamond.

On Windows, designing for the largest FPGAs may require more than the usual 2 GB of memory found in 32-bit computers. For help in extending your memory to 3 GB, see “Extending Memory on Windows” on page 11. Designing for LatticeECP3 with more than 95K LUT on a Windows system requires a 64-bit operating system.

Table 2: Recommended Memory

Device	Size	32-Bit Operating Systems		64-Bit Operating Systems	
		Minimum	Recommended	Minimum	Recommended
ECP5	All	2 GB	3 GB	4 GB	6 GB
LatticeEC, LatticeECP	Up to 20K LUT	512 MB	768 MB	1 GB	1.5 GB
	Up to 50K LUT	768 MB	1 GB	1.5 GB	2 GB
LatticeECP2/M	Up to 20K LUT	768 MB	1 GB	1.5 GB	2 GB
	Up to 50K LUT	1 GB	1.5 GB	2 GB	3 GB
	Up to 100K LUT	1 GB	2 GB	2 GB	4 GB
LatticeECP3	Up to 95K LUT	2 GB	3 GB	4 GB	6 GB
	Up to 150K LUT	3 GB	4 GB	6 GB	8 GB
LatticeSC/M	Up to 40K LUT	768 MB	1 GB	1.5 GB	2 GB
	Up to 115K LUT	1 GB	2.5 GB	2 GB	5 GB
LatticeXP, LatticeXP2	Up to 20K LUT	512 MB	768 MB	1 GB	1.5 GB
	Up to 50K LUT	768 MB	1 GB	1.5 GB	2 GB
MachXO, MachXO2, MachXO3L	All	256 MB	512 MB	512 MB	1 GB
Platform Manager, Platform Manager 2	All	256 MB	512 MB	512 MB	1 GB

Extending Memory on Windows

Designing for LatticeECP3 or ECP5 may require more than the 2 GB normally available with 32-bit Windows systems. But you can configure Windows to use up to 3 GB of memory.

Note that increasing the amount of memory available to applications, decreases the amount available for the file cache, paged pool, and nonpaged pool, which can affect applications with heavy networking or I/O.

In Windows XP

In Windows XP Professional, add the **/3GB** switch to the end of the startup line in the boot.ini file. For details, see the following Microsoft articles:

- ▶ “Windows XP SP1 May Not Start with the /3GB or /USERVA Switch”: support.microsoft.com/?kbid=328269
- ▶ “How to edit the Boot.ini file in Windows XP”: support.microsoft.com/default.aspx?scid=kb;en-us;q289022
- ▶ “Memory Support and Windows Operating System” shows an example of the boot.ini with the /3GB switch: msdn.microsoft.com/en-us/windows/hardware/gg487508.aspx

In All Other Versions of Windows

Use the **BCDEdit /set increaseuserva 3072** command to set the boot entry option to 3 GB. For details, see Microsoft article “BCDEdit /set”:

msdn.microsoft.com/en-us/library/ff542202.aspx

Configuring Red Hat 5.3

Red Hat Enterprise Linux 5.3 has some extra requirements for Diamond:

- ▶ In addition to the basic installation of Red Hat 5.3, under Development/Legacy Software Development, select:

```
1:gtk+-1.2.10-56.el5.i386 - GIMP Toolkit (GTK+) sb: (9 of 9)
```

Under Base System/Legacy Software Support, add the following to the default items:

```
Openmotif22-2.2.3-18.i386 - Open Motif runtime
```

Proper Diamond operation depends upon these libraries being installed.

- ▶ When installing the Red Hat Enterprise Linux version, be sure to install the PERL modules XML::Parser, XML::DOM, and XML::RegExp. These PERL modules are available at www.cpan.org.

Issues Fixed

The following known issues are fixed with this release. Their workarounds are no longer needed.

Clarity cannot reconfigure a module

When trying to reconfigure a module in Clarity Designer, you may see an error message that says that the component “is not supported for reconfiguration in this version of Diamond.”

If you see this message, contact Lattice support for a patch.

Devices affected: ECP5
CR121072

Device Selector shows 8 EBR for MachXO3L 640 and 1300

For MachXO3L 640 and 1300, the Device Selector dialog box shows 8 EBR blocks. It should show 7.

Devices affected: MachXO3L
CR121054

LDC Editor may cause errors in SDC files

When editing SDC files using LDC Editor, the target may be incorrect after synthesis and some uses won't be supported.

As a workaround, write the .ldc file manually.

Devices affected: All
CR120924

Errors occur in ecp5um_serdes.ibs file at some pin declarations

The ecp5um_serdes.ibs file contains some pin names that exceed the 5-character maximum, and will therefore cause errors.

Pin strings "prvlp_t" and "prvln_t" are too long, and will be truncated to five characters, causing errors.

As a workaround, rename the pins with names that are five characters or less and that do not conflict with other pin names. For example, change "prvlp_t" to "prp_t", and change "prvln_t" to "prn_t".

Devices affected: All
CR120315

Reveal Analyzer fails to open on Windows 8

Diamond does not support the Windows 8 operating system. Reveal Analyzer fails to open.

Run Diamond on a different operating system.

Devices affected: All
CR118978

Synthesis fails with schematic file on Windows 8

Diamond does not support the Windows 8 operating system. Synthesizing a design with a schematic file fails with error code 1.

Run Diamond on a different operating system.

Devices affected: All
CR118394

Help does not work in Google Chrome browser

When you try to open the help with Google Chrome, the browser displays an empty window. If you get the help from a server it works fine, but if you get the help from your local computer there's nothing.

This is because Google added a security feature in March 2010 that interfered with the file:// protocol, which is at the heart of browser-based help that Diamond and other Lattice software uses. (This affects the help of many other companies' software too.)

Workarounds include:

- ▶ Open a different kind of browser (such as Internet Explorer) and browse to the index.htm file of the software's help.
- ▶ Set a different kind of browser as your default browser.
- ▶ Install the Lattice software on a server.
- ▶ Open Chrome from a command prompt with the following flag:

```
chrome --allow-file-access-from-files
```

Note: Doing this means that when you open any Web page that is resident on your computer—not just Diamond Help—the page will automatically run any active content that it has. While active content is common and can be very useful, malicious content can damage your files. Be sure you trust the software on your computer.

Devices affected: All
CR53868

Known Issues

Following are known issues with this release and workarounds for them. This list is preliminary. For the complete list, see www.latticesemi.com/view_document?document_id=50676.

Hysteresis is not set for the LVTTLL33 IO_TYPE

Hysteresis bits are not set for the LVTTLL33 IO_TYPE. Changing the Hysteresis setting in the software will not have any effect if you select the IO_TYPE to be LVTTLL33.

Change the IO_TYPE to LVCMOS33 and then use the Hysteresis settings. LVCMOS33 and LVTTLL33 are exactly the same.

Devices affected: MachXO2
CR122740

EPIC Help does not display in Firefox

EPIC cannot open its online Help if Firefox is your default browser. Instead, Firefox displays, "The address wasn't understood."

To work around this problem, do one of the following:

- ▶ Set a different browser, such as Chrome or Internet Explorer, as your default browser. Then open the Help from EPIC.
- ▶ In Firefox, enter the path to the Help:

`<Diamond directory>\ispfpga\webhelp\epichelp\index.htm`

Devices affected: All
CR122659

Clock placed in Clarity generated without buffer

When generating a Clarity Designer module that includes a DDR interface, you may get a warning message similar to the following:

WARNING - Clock input 'clkop' of interface 'eclk_group0' in component 'abc' is generated without any buffer. Planning for each interface needs special attention. Consult document for more information.

This can happen if you use the Planner tab of Clarity to place the clock signal of the DDR module. Clarity does not properly place the clock signal.

If you see this message, place the DDR clock without using Clarity. See *Applying Design Constraints* in the online help.

Or, if you need a PLL in the design, drive the clock input from the PLL.

Devices affected: ECP5
CR122392

Spreadsheet View takes a long time to open

For large projects, it might take a minute or longer for Spreadsheet View to open. This is because of the time needed for real-time PIO design rule checking as the design is loaded.

Devices affected: All
CR56872

Regions and groups in Physical View are not displayed in the colors assigned to them

Physical View displays only fixed colors for different elements such as regions, groups, sites, and delay paths. It does not support customized color settings. Therefore, the borders of all regions and groups are displayed in the same default color on the layout. They are not displayed in the colors that were assigned to them.

To view regions and groups in their assigned colors on the layout, open Floorplan View.

Devices affected: All
CR50166

Physical View does not match delay path colors or allow custom colors

Physical View displays only fixed colors for different elements such as delay paths, regions, groups, and sites. Therefore, when you cross-probe a delay path from Timing Analysis View, Physical View highlights the path in the same default color. It does not show the path color that is displayed in Timing Analysis View or allow you to manually change the color. Currently there is no way to distinguish the color of individual delay paths in Physical View. However, if you cross-probe to Floorplan View from Timing Analysis View, you will see the delay paths distinguished by color.

Devices affected: All
CR47031, CR49201

Removing an implementation from Diamond does not delete the result files from the implementation directory

Removing an implementation from Diamond will not delete the result files from the implementation directory.

Manually delete the files or the implementation directory if needed. If deleting the implementation directory, be careful to make sure that there are no source files in the implementation directory.

Devices affected: All
CR48000

Contacting Technical Support

FAQs The first place to look. The [Answer Database](#) provides solutions to questions that many of our customers have already asked. Lattice Applications Engineers are continuously adding to the Database.

Telephone Support Hotline Receive direct technical support for all Lattice products by calling Lattice Applications from 5:30 a.m. to 6 p.m. Pacific Time.

- ▶ For USA & Canada: 1-800-LATTICE (528-8423)
- ▶ For other locations: +1 503 268 8001

In Asia, call Lattice Applications from 8:30 a.m. to 5:30 p.m. Beijing Time (CST), +0800 UTC. Chinese and English language only.

- ▶ For Asia: +86 21 52989090

E-mail Support

- ▶ techsupport@latticesemi.com

For Local Support Contact your nearest [Lattice Sales Office](#).

Trademarks

All Lattice trademarks are as listed at www.latticesemi.com/legal. Synopsys and Synplify Pro are trademarks of Synopsys, Inc. Aldec and Active-HDL are trademarks of Aldec, Inc. All other trademarks are the property of their respective owners.