iCEcube2 Software Release Notes

May 06, 2014 *Version 2014.04*

Contents

iCEcube2 Version 2014.04

1. Fixed routing to dedicated pins support for SPI & I2C Hard IP primitives.
2. More accurate power estimation support for iCE40LP1K, iCE40HX1K, iCE40LP4K, iCE40HX4K, iCE40LP8K, iCE40HX8K and iCE40LP384.

iCEcube2 Version 2013.12

1. This version of the iCEcube2 software introduces the following iCE40LM device family.
    a. iCE40LM4K - SWG25TR,CM36,CM49
    b. iCE40LM2K - SWG25TR,CM36,CM49
    c. iCE40LM1K - SWG25TR,CM36,CM49

2. This version of the iCEcube2 software adds support for the following iCE40 device-package combinations:
    a. iCE40LP1K - SWG16TR
    b. iCE40LP640 - SWG16TR
3. SPI/I2C Module Generator support for iCE40LM Hard IP configurations. Only Verilog RTL is supported.
4. LSE now supports VHDL-2008 standard RTL.
5. Removed JTAG feature support for iCE40 devices.
6. More accurate power estimation support for iCE40HX1K, iCE40LP4K, iCE40HX4K, iCE40LP8K, iCE40HX8K.
7. Updated iCEcube2 Tutorial.

iCEcube2 Version 2013.08

1. iCE40LP384-CM81 Package support is no longer available.
2. Synplify synthesis flow requires additional license “LSC_ICECUBE2_EDIFIMPORT’.
3. IP Reference designs are removed from iCEcube2 installation. Refer “IP Reference Designs” section for more details.
4. More accurate timing for iCE40LP/iCE40HX devices.

iCEcube2 Version 2013.03

1. The iCEcube2 software contains two synthesis tools.
    a) Lattice Synthesis Engine (LSE).
    b) Synopsys Synplify Pro.

    Synplify Pro is the default synthesis tool in iCEcube2 flow.
2. This version contains memory initializer command line utility to initialization the BRAM memory contents at post place and route stage.
3. More accurate timing for iCE40LP/iCE40HX devices.

iCEcube2 Version 2012.09 SP1

1. Improved static power estimation.
2. Operating condition is changed to include wider temperature ranges for commercial and industrial settings.
3. Improved placement support to place LUTs in the external feedback path of PLL at optimal location.
4. More accurate timing for iCE40LP/iCE40HX devices.

iCEcube2 Version 2012.09

1. Updated timing for iCE40LP/iCE40HX devices.
2. Improved placement support for various scenarios involving simultaneous constraints on PLL and LOCK/SDO buffers.

iCEcube2 Version 2012.06

1. Updated timing model for iCE40 in the Synthesis tool provides better correlation between the post-synthesis and post-placement timing.
2. Improved Power Estimator for iCE40 devices.
3. The Simulation Wizard GUI on the Windows platform supports creation of Aldec Active-HDL simulation projects at various stages in the flow.
4. Enhanced VHDL Simulation libraries now support iCE40 PLL simulations.

iCEcube2 Version 2012.03

1. This version of the iCEcube2 software adds support for the following device-package combinations: iCE40HX1K-CB132.
2. Cross-probing of timing paths from the Timing Viewer to the Floor Plan View has been enhanced to display the numeric values of the cell delays as well as the routing delays.
3. The Placer now has an option to perform Power-Driven optimizations. The default behavior remains Timing-Driven.
4. The iCEcube2 software now includes the Aldec Active-HDL simulator on the Windows platform.

iCEcube2 Version 2011.12

1. This version of the iCEcube2 software adds support for the following device-package combinations: iCE40LP1K-TQ144, iCE40LP4K-CM81, iCE40LP4K-CB132, iCE40HX8K-CB132.
2. SDC Timing constraints can now use wildcard characters to identify constrained objects.

3. The Data Sheet section of the Timing Viewer has been enhanced to report Hold Time of signals on input pads, Minimum Clock-to-out delays, and Minimum Pad-to-Pad delays.
4. Enhancements have been made to the GUI including sorting logic objects by physical constraints in the Floor Planner, and easier PLL configuration for LVDS display panels.
5. The installer has been enhanced to better manage the software installation.

iCEcube2 Version 2011.09 SP2

1. This version of the iCEcube2 software adds support for the following device-package combination: iCE40LP4K-CM81.
2. Delay models have been updated for the iCE40 family of devices.
3. For unused IO pins, the built-in pull-up resistor in the IO is disabled. This is different from the previous behavior of the software, wherein the pull-up resistor was enabled for unused IOs. Since the pull-up resistor is now disabled, board traces can be routed through the unused IO pins.

iCEcube2 Version 2011.09 SP1

1. This version of the iCEcube2 software adds support for the following device-package combinations: iCE40HX640-VQ100, iCE40LP4K-CM225, iCE40HX4K-TQ144.

iCEcube2 Version 2011.09

1. This version of the iCEcube2 software includes support for the following device-package combinations: iCE40LP640-CM81, iCE40LP640-CM49, iCE40LP640-CM36, iCE40HX1K-VQ100, iCE40HX8K-CT256.
2. The iCEcube2 software now supports user specified load capacitance on output pads for the iCE40 device family. This load capacitance is used by the Timing Analysis and Power Estimation tools, and is specified through the Pin Constraints Editor.
3. The software now permits the user to configure a different voltage for each IO Bank for the iCE40 device family. The user specified IO Bank Voltage is used by the Timing Analysis and Power Estimation tools, and is specified through the Device Options GUI.
4. The software now supports cross-probing of timing paths from the Timing Viewer to the Floor Planner.
5. The Timing Constraints Editor now supports the Source Clock Latency constraints.
6. Timing Reports generated by iCEcube2 have been enhanced as follows
   - Path details are now provided for the Clock-to-Out and Setup Time reports in the Datasheet section
   - The Path details section has been enhanced for all timing reports to improve readability, and make them self-explanatory. Improvements include adding separate delay entries for the delay or phase change components contributed by Source Clock

Latency, Generated Clocks, Input/Output delays, edge alignments of launch and capture clocks used. Registers packed into IO pads can now be identified in the timing reports.

7. The Physical Constraints flow now supports user specified location constraints for PLLs. This is applicable for the iCE40 devices with 2 PLLs.
8. The Physical Constraints flow has been enhanced to handle multiple groups per region.

iCEcube2 Version 2011.06 SP2

1. This version of the software is recommended for designs with BRAM configured as ROM. It addresses a non-optimum default connection of the WCLKE port of the BRAM cell, when configured in the ROM model.

iCEcube2 Version 2011.06 SP1

1. This version of the software includes support for the iCE40LP1K device in the following packages: CM121, CM81, CM49, CM36 and QN84.
2. The device configuration file, for applications requiring multiple images, has been corrected.

iCEcube2 Version 2011.06

1. This version of the software introduces preliminary support for SiliconBlue's iCE40 "Los Angeles" family of devices.
2. The Timing Viewer has been enhanced for better timing analysis of designs with DDR I/Os. Also, the Maximum Delay timing constraint is now handled as an exception, consistent with industry standard tools.
3. Improved utilization of the PLL input pad: In the scenario that the PLL input is driven by internal logic, the pad connected to the PLL input can now be configured as an output-only pad
4. The IP library now contains IP building blocks for the following functions:
    a. I2C Slave to SPI Master/GPIO Bridge
    b. SPI Slave to I2C Master/GPIO Bridge

iCEcube2 Version 2011.03

1. The Timing Viewer GUI now supports the generation of timing reports for Point-to-Point delay. It allows the user to specify cell pins as Start and Stop points, and reports the signal propagation delay for combinational paths between the selected pins.
2. The Data Sheet Report in the Timing Viewer GUI has been enhanced to report the data and clock path details for the paths used to calculate the Clock-to-Out, Setup, and Pad-to-Pad delays.

3. The Project Navigator GUI permits the user to run all the tools (including Synplify Pro) with a single mouse-click.
4. The iCEcube2 Project Navigator now permits users to open text files with their own text editor, as specified in their Windows File Extension Association.
5. The Microsoft Windows 7 operating system, both 32-bit and 64-bit versions, is now supported. *(Addresses: For a new project, the browse button does not go to the exact directory despite the exact path is filled in the blank)*
6. The IP library now contains IP building blocks for the following:
    a. UART – two IPs, compliant with the 16450 and 16550 standards respectively
    b. LVDS Tx

iCEcube2 Version 2010.12 SP1

1. The simulation flow for the IP library components has been enhanced to include parameterized and encrypted RTL simulation models. The encryption scheme is compatible with the industry-standard ModelSim simulator. For reference, the list of IP components and their user configurable parameters are included at the end of the Release Notes.
2. The LUT simulation models have been enhanced for improved handling of 'X' (don't care) at unconnected inputs.

iCEcube2 Version 2010.12

1. The Synplify Pro software now generates a hierarchical EDIF netlist, along with a hierarchical resource utilization report.
2. The Timing Analysis software now automatically detects signal polarity along clock networks. This results in improved accuracy of delay calculation along the clock path, and hence more accurate timing reports.
3. The Timing Viewer now permits modification of Speed Grade/Operation Conditions, and also regeneration of timing reports and SDF (timing simulation files), without having to recompile the design.
4. The Timing Viewer now provides the following additional controls to filter/view the number of reported paths
    a. FFs merged into IO pads can now be selected as start/stop points. (Note: to report these paths, input and output delay constraints are necessary)
    b. Maximum path slack
    c. Number of paths per start point / Paths per end point
    d. Timing results can be sorted on multiple keys
5. Timing Nodes (Logic Cells, RAMs, FFs, IO Pads) from the Timing Report can now be highlighted in the Floor Planner

6. The Timing Viewer now displays Clock Relationships and Data Sheet in GUI. These features are also included in the text timing report file (since iCEcube2 v2010.09), and are explained below:
    a. Clock Relationships: This is useful in identifying cross-clock domain paths that exist in the design, and ensure that they have been correctly constrained.
    b. Data-Sheet: This provides Setup, Clock-to-Out and Combinational path delays for the routed design. This information can be used to constrain board routing delays.
7. The iCEchip Programming software now supports 64-bit Windows operating systems.
8. The IP Library has been enhanced to include 31 IP components. The IP is now included in encrypted RTL format and also supports the IP EXACT v1.2 format, which is compatible with System Designer.
   The list of IP components and their user configurable parameters are included at the end of the Release Notes.

iCEcube2 Version 2010.09 SP3

1. This version of the software provides a fix for compilation problems with the simulation library, when compiled for timing simulation.

iCEcube2 Version 2010.09 SP2

1. Version 2010.09 SP2 includes support for the L08 device in the CS110 package.
2. The simulation models have been enhanced to ensure that IO flip-flops are initialized to the Logic 0 state. The LUT model has been improved to better handle uninitialized input signals. This improves the simulation co-relation with the actual device behavior.
3. The Floor Planner has been improved to display IO pad placement assignments specified through the PCF file, before placement.

iCEcube2 Version 2010.09 SP1

1. Design performance has improved by 5% due to better carry-chain packing.
2. Encrypted Verilog netlists and updated documentation for IP Blocks are included.
3. The service pack improves the user flow for IO assignments made to the left IO bank.

iCEcube2 Version 2010.09

1. The post-route timing report is now generated by default, and listed in the Project Navigator GUI under Output Files> Reports.
2. Cross-clock domain analysis is now reported in a section called Clock Relationships, in the timing report file. This is useful in identifying any cross-clock paths that may have been incorrectly constrained.

3. A Data-Sheet report is now provided in the timing report file. It provides Setup, Clock-to-Out and Combinational path delays for the routed design. This information can be used to constrain board routing delays.
4. Physical constraints (Groups/Regions) can now be specified to the Placer through the Floor Planner GUI.
5. User controls have been provided for promoting signals to the global clock network and vice versa.
6. User controls have been provided for merging/unmerging flip-flops into/from IO pads.
7. The software now supports Warmboot for iCEcable.
8. The Bitmap Configuration file size can now be reduced by appropriate selection of device quadrants for RAM4K initialization.

iCEcube2 Version 2010.06 SP2

1. Version 2010.06 SP2 includes support for the following device-package combinations: L01-CB81, P04-CB121, L08-CB132.
2. The Power Estimator now supports 3.3 V setting for the Left IO bank.
3. The Timing Viewer now provides better correlation at 1.0V, for the “-L” power grade.

iCEcube2 Version 2010.06 SP1

1. The accuracy of the PLL Timing Report has been improved for configurations using the Phase Shifter.
2. Timing Analysis for the PLL now includes appropriate frequency constraints for the derived clocks in the SIMPLE mode.
3. The Save As dialog box for the Timing Constraints Editor will now automatically append the .sdc extension, instead of expecting the user to specify it.

iCEcube2 Version 2010.06

1. IO assignments can now be made in the Pin Constraints Editor and the Package Viewer after importing a design netlist, and before running the Placer. Previous versions of the software required the Placer to be run before assigning IOs.
2. The Phase Shift functionality of the PLL (P04 device) is now supported.
3. The Project Navigator GUI includes several ‘ease-of-use’ enhancements including “Run All Tools” using one click.
4. The Magma BlastFPGA software is no longer supported, starting with Version 2010.06. Please use the Synopsys Synplify Pro synthesis software for your designs.
5. The messages issued by the iCEcube2 Placer have been improved.

iCEcube2 Version 2010.03 SP2

1. Version 2010.03SP2 includes support for the L01 device in the DI package.

2. Much improved Timing QoR.
3. The Static Timing Analysis software now supports false path exceptions for muxed clocks.

iCEcube2 Version 2010.03 SP1

1. Version 2010.03SP1 includes support for the L01 device in the CS36 package.
2. The Project Navigator GUI has been enhanced for better integration with Synplify Pro projects.

iCEcube2 Version 2010.03

1. Version 2010.03 is the first release of a new set of software tools, iCEcube2, which replaces the iCEcube software. It is recommended that users to upgrade to this version.
2. The iCEcube2 software includes Synopsys' Synplify Pro synthesis tool. Support for Magma BlastFPGA is included in iCEcube2, but it should be noted that Version 2010.03 is the last software release with Magma's synthesis software.
3. The Magma BlastFPGA placer has been replaced with a proprietary placer with tighter integration with flows supported by the tool suite.
4. Timing constraints for Placement and Routing can now be applied in iCEcube2, using a new Timing Constraints Editor.
5. Physical location constraints can now be applied in the Floor Planner, and are honored in subsequent placement and routing runs.
6. Key features of the Synplify Pro software are listed below.

Synplify Pro Features	Benefits
Timing-Driven Synthesis	Automatically optimizes for area once timing is met.
Proprietary BEST Algorithm	Globally optimized design acheives the best Quality of Results.
HDL Analyst	Generates an RTL block diagram from RTL for corss-probing with source code and identifies critical paths.
Comprehensive Language Support	Supports Verilog, VHDL, System Verilog, and mixed-language designs.
Automatic Retiming	Moves registers within combinatorial logic balancing delay and improving timing performance.
FSM Compiler and Explorer	Automatically extracts and optimizes Finite State Machines based on constraints.
Graphical State Machine Viewer	Automatic creation of bubble diagrams for debuggind and document FSMs.
Automatic RAM and DSP Inference	Extracts and optimizes memory and DSP functions from your RTL code.
Incremental Static Timing Analysis	Enables you to update timing exceptions and see results immediately, without re-synthesis.
Formal Verification Mode	Supports logical equivalency checking with popular logical equivalency checking tools.
ReadyIP™ Browser	Access to 3rd party IP for evaluation and download.
Incremental Design	Fast turnaround times with consistent results from one run to the next.
Contraints Checker and Advisor	Quickly configure RTL and constraints avoiding time-consuming pilot errors.

Known Issues and Workarounds

Installation Issues

Issue	Workaround
Installation of iCEcube2 software on Windows Vista requires User Account Control to be turned off. Failure to do so will result in the incorrect functioning of the Synplify software when launched from the iCEcube2 software.	Turn off the User Account Control (UAC) on your Windows Vista machine. Steps to turn off the UAC setting have been provided in the *iCEcube2_install_review.pdf* file included in your *<iCEcube2_install_dir>/doc* directory.
iCEcube2 may not work in VMWare environment	Install the “vcredist_x86.exe” available at <install_dir>\sbt_backend\bin\win32\opt.

Software Issues

Issue	Workaround
iCEcube2 will fail to access the database file if the total length of the file path of the working directory exceeds 200 characters.	Reduce the length of the file path of the working directory.
For designs containing RAM blocks with initialized content (RAM data needs to be read before any write operation occurs), if the WCLKE port is connected to ‘logic 1’, the initial data in the 0^{th} address location may be corrupted.	Instantiate the RAM block in your design, and ensure that the WE port of the BRAM is connected to ‘logic 1’, and all control logic is connected to the WCLKE port.
Synplify ignores false path constraints, and lists them under the Unused Constraints section of the SCF file.	For false path constraints on input or output ports, you must have I/O delays specified for the path from input or to the output ports. The false path constraint is only valid and forward-annotated when the delays are specified on the input and output ports as described in *Defining Input Delays*, on page 6 and *Defining Output Delays*, on page 8 of the Synopsys App Note: Using Timing Constraints in SiliconBlue Designs.
The Synplify Pro generated SCF file contains objects called “all_clocks” or “synplicity_global_clock”, which then causes	When specifying any delay constraint like input delay/output delay, always remember to specify the reference clock. Without the

an error in the iCEcube2 Place & Route software.	reference clock, the timing constraint will not be forward annotated correctly to the SCF file. Instead a dummy clock (synplicity_global_clock) will be written to the SCF, which can cause an error during Place & Route. It can also cause an unsupported Tcl collection called all_clocks, to be written to the SCF file. Please also refer to the Synopsys App Note: Using Timing Constraints in SiliconBlue Designs.
For designs with state machines, sometimes Synplify Pro memory utilization may exceed 4GB and run time increases significantly.	Turn off the state machine optimization using "FSM Compiler" switch in Synplify or use the "syn_state_machine" directive in RTL. Refer to <install_dir>\synpbase\doc\attribute_reference.pdf for more details about the RTL directive.
When using Lattice Synthesis Engine (LSE), duplicate instantiation names (due to names in generate statements) fail synthesis.	Make sure all instantiation names are unique.
Lattice Synthesis Engine (LSE) does not support curly braces {} in SDC commands.	Remove curly braces {} in the SDC commands.
VHDL and Verilog allow global signals to be defined and used anywhere in the user design. Currently, LSE does not support global signal usage.	Global signals should be connected to all the modules seeking to use it by an explicit port connection.
When an MTCL file with pin locations assignments is imported into iCEcube2, the pin placement is ignored.	First, check that the MTCL file contains pin assignments that are intended for the target device selected in iCEcube2. If the pin assignments are correct, but iCEcube2 complains that a clock pad is being assigned to a general purpose pad location, perform the following steps: In the RTL design, identify the top level design port that drives the global clock network, but is located at a general-purpose pin location. Modify the RTL such that this design

	port drives a SB_GB primitive (you will need to instantiate the SB_GB primitive) Connect the output of the SB_GB primitive to logic that was driven by the design port. The above steps will ensure that Synplify Pro infers a general-purpose pad i.e. SB_IO, for this design port, and the pin location assignment from the MTCL can be successfully honored.
When the Power Estimator is launched, instead of using the user assigned values, it uses the default clock and IO toggle rates to calculate the power.	Upon launching the Power estimator, click on the Calculate button to force a calculation of the power consumption, using the user assigned values for clock and IO toggle rates.
In the Power Estimation tool, the frequency listed for generated clocks is incorrectly reported. This can impact the reported power consumption.	Specify your own frequency for the generated clock by editing the appropriate field in the Clock Domain tab. You may also extract the frequency reported from the Static Timing Analysis tool, enter it in this field, and recalculate the estimated power.
iCEcube2 timing analysis does not support PLL Bypass mode.	Refer to iCE40 FPGA Family Data Sheet for more details.
When performing a simulation of a design with a PLL, the following message is issued: The verilog model has not been initialized yet! Neither the RESET nor BYPASS pin has been asserted. Please check the RESET and BYPASS pins. The PLL verilog model will not produce an out put signal until RESET is asserted and de-asserted, or BYPASS is asserted!	In the simulation testbench, assert the RESET (Active-Low) or BYPASS pins. In order to ensure the RESET pin is instantiated on the PLL, when generating a PLL through the PLL Configuration GUI, select “Create a Reset port to asynchronously reset the PLL”.
SPI/I2C module index number used in IP port connections in generated wrappers does not match with pin index numbers displayed in package viewer. I2C1 (upper left) module index in generated	Not Applicable

wrapper corresponds to I2C2 (upper left) in package viewer and vice versa. SPI1 (lower left) module index in generated wrapper corresponds to SPI2 (lower left) in package viewer and vice versa.	
Synplify pro synthesis may fail, if the SPI_CLK_DIVIDER/I2C_CLK_DIVIDER synthesis attribute is zero in the SPI/I2C module generated wrappers. Certain “system bus clock frequency” and “Master clock rate” settings specified in the SPI/I2C module generator results in zero clock divider value. Ex: I2C: 1 MHz (system clock), 400KHz (desired). SPI: 1 MHz (system clock), 1 MHz (desired).	The user can either 1. Use LSE synthesis tool. 2. Modify the system bus clock frequency and/or Master clock rate frequency values to results in non-zero clock divider value for synplify synthesis support.
The module generator does not set I2C_SLAVE_INIT_ADDR parameters with the value specified in the GUI’s “I2C Addressing” field. It will use the default value of I2C_SLAVE_INIT_ADDR for each I2C module. However, the state machine that loads the I2C address into the “I2C Slave Address MSB Register (I2CSADDR)” will use the specified address. As a result, when users look at the generated HDL, they will see a mismatch between I2C_SLAVE_INIT_ADDR value and the value loaded into I2CSADDR register. Furthermore, there will be a mismatch between functional simulation and hardware implementation: functional simulation will not behave as expected (i.e. I2C not responding to the user’s intended address) while hardware implementation behaves correctly (i.e. responding to the user’s intended address).	Every time module generator is used to generate I2C module, edit the I2C_SLAVE_INIT_ADDR so that it contains the user’s intended address.

IP Reference Designs

IP Reference Designs are now available from the Lattice website. Please go to: http://www.latticesemi.com/ice40 to download these reference designs.