ORT8850 Evaluation Board Tutorial

Overview

This tutorial will assist first-time users of the ORCA ORT8850 how to use the evaluation board to understand the device features as well as the capabilities of the evaluation board. To use the tutorial, the user must have an installed copy of ORCA Foundry 2001 software and an understanding of the ORCA Device Programming Download Cable which is described in the Lattice Semiconductor technical note TN1009. Users should also reference the ORT8850 Evaluation Board Users Manual.

The tutorial and the supporting design files can be downloaded from the design tools section of the Lattice web site at http://www.latticesemi.com. The tutorial design was created for use as a template for future designs. This design includes simple pattern generation for 8- ORT8850 LVDS channels and the appropriate register settings to enable the internal and external communication links.

Getting Started

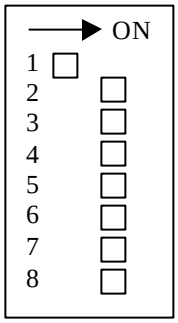
The following steps will make the proper board interconnections for power supplies, input signals, and output signals.

- Add push-on jumper shunts for the following.

Jumper	Pin	Pin
J71	1	2
J77	1	2
J78	1	2
J51	3	5
J53	3	5
J55	1	3
J57	1	3
J59	1	3
J22	1	2
JP3	1	2
JP3	7	8
JP4	1	2
JP4	7	8
J26	1	2
J72	2	4

- Connect short 20-contact IDC ribbon cable between J13 & J5
- Connect single patch cable between J4.1 and J16.1

- Place SW3.1 to “off” position (Figure 3)



SW3

Figure 3

- Connect DB-25 connector of download cable to DB-9 adapter
- Plug DB-9 connector in a serial PC port(COM1or COM2)
- Plug Condor Wall supply into J67 and Power source to power up board

Programming the Device

- Connect 8-pin dongle of download cable to J3
- Green LED on download cable should light
- From an MS-DOS command window (computer with ORCA Foundry 2001 installed)
  Type”devprog –c serial –p COM1(or 2) – j w ORT8850_eval_1.bit <enter>
  ORT8850_eval_1.bit can be downloaded from the design tools section of the Lattice web site at http://www.latticesemi.com
- Download cable LED should illuminate yellow while loading
- Downloading bit stream
- D19 LED lights and download cable LED goes green
- After D19 lights the following LEDS will light sequence (Figure 1)

  D1, 11, 2, 12, 3, 13, 4, 14, 5, 15, 6

D15,16,17,18

D11,12,13,14

D5, 6, 9, 10

D1, 2, 3, 4

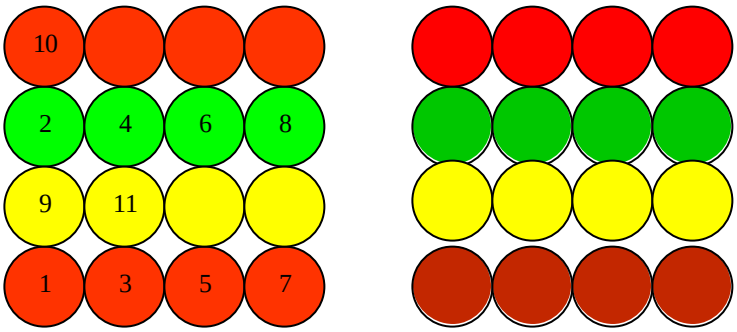


Figure 1 Figure 2

After the above sequence D5, 6, 9, 10, 15, 16,17, 18 will flash together (Figure 2)

Evaluating the Results

The sequential illumination of the LEDs indicate the successful writing of the core registers using the user master of the microprocessor interface. States 1 and 2 unlock the core registers. State 3 writes to the loop back register, and the remaining states indicate the initialization of the eight channels.

The evaluation design uses an external primary input connected to SW3.1 to enable and disable the internal(near-end) and external(far end) loop back modes. With SW3.1 in the “off” position near-end loop back is enabled. When the LED array is flashing as depicted in Figure 2, this indicated successful internal loop back traffic.

For evaluating far-end loop back the following DIP switches must be in the position shown in Figure 4.

SW6,SW7,SW8,SW9,SW10,SW11,SW12,SW13,SW14,SW15,SW16,SW17,SW18,SW9,SW20,SW21,SW22,SW23,SW24 ,SW25,SW26,SW27,SW28,SW29,SW30,SW31,SW32SW33,SW34,SW35,SW36,SW37

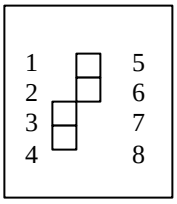


Figure 4

A cable(W.L. Gore P/N 2MMA3106-00) not provided with the evaluation kit can be used to make an external connection between CON 4 and CON3. This external connection will successfully loop back 8 channels when SW3.1 is in the ON position(loop back disabled).

CON4 and CON3 can also be used to observe the signal integrity of the ORT8850 LVDS channels. A cable similar to one from W.L Gore P/N 2MMA3143-01 adapts the 2mm Z-Pack to individual SMA connectors and is useful to observe the LVDS channels or connect to other test devices.

For cable information visit (http://www.wlgore.com/).