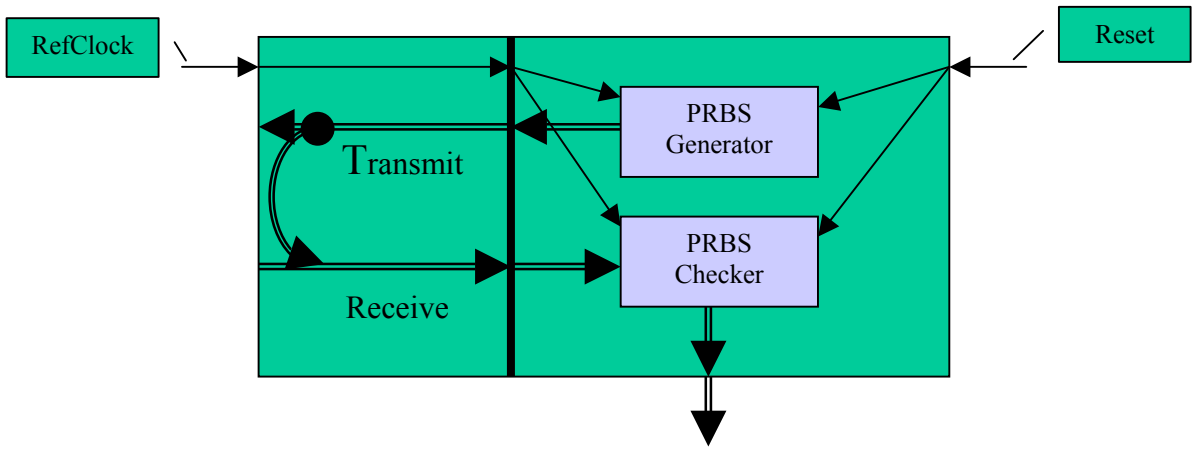
ORT82G5 Evaluation Board-1 Tutorial

Overview

This tutorial will assist first-time users of the ORCA ORT82G5 how to use the evaluation board to understand the device features as well as the capabilities of the evaluation board. To use the tutorial, the user must have an installed copy of ORCA Foundry 2001 software and an understanding of the ORCA Device Programming Download Cable which is described in the Lattice Semiconductor technical note TN1009. Users should also reference the ORT82G5 Evaluation Board Users Manual.

The tutorial and the supporting design files can be downloaded from the design tools section of the Lattice web site at http://www.latticesemi.com. The tutorial design was created for use as a template for future designs. This design includes simple pattern generation and the appropriate register settings to enable the internal and external communication links.



Getting Started

The following steps will make the proper board interconnections for power supplies, input signals, and output signals.

Add push-on jumper shunts for the following.

Jumper	Pin	Pin
JP7	1	2
JP25	1	2
JP26	1	2
JP28	1	2
JP30	1	2
JP31	1	2
JP19	3	4
JP20	3	4
JP21	3	4
JP22	3	4
JP23	3	4
JP32	2	3

Add patch cords between the following.

JP3.2	JP2.2
JP3.4	JP2.4
JP3.6	JP2.6
JP3.8	JP2.8
JP3.10	JP2.10
JP3.12	JP2.12
JP3.14	JP2.14
JP3.16	JP2.16
JP3.18	JP2.18
JP3.20	JP2.20
JP3.22	JP2.22
JP3.24	JP2.24
JP3.26	JP2.26
JP3.28	JP2.28
JP3.30	JP2.30
JP3.32	JP3.32

- Connect single patch cable between JP2.36 and JP2.35
- Connect DB-25 connector of download cable to DB-9 adapter
- Plug DB-9 connector in a serial PC port(COM1or COM2)
- Connect J50 to +5VDC power supply and J51 to GND of supply
- Connect Reference clock to SMA connections J22 and J23. Should be sourced from a differential source or single ended source if a 50 ohm termination is externally connected to one of the SMA connections.

Programming the Device

- Connect 7-pin dongle of download cable to JP4
- Green LED on download cable should light
- From an MS-DOS command window (computer with ORCA Foundry 2001 installed)
  Type"devprog –c serial –p COM1(or 2) ORT82G5_eval_1.bit <enter>
  ORT82G5_eval_1.bit can be downloaded from the design tools section of the Lattice web site at http://www.latticesemi.com
- Download cable LED should illuminate red while loading
- Downloading bit stream
- D17 LED lights and download cable LED goes green
- After D17 lights disconnect the patch cord from JP2.35 (GND) and reconnect it to JP20.6 (2.5V).
- The LEDS adjacent to JP3 will light in sequence from D1 to D16 indicating all channels of the "B" quad are active.

Control Register Configuration Performed by the Bitstream

•All channels except BA are powered down.
•Enable the TX 8b/10b for Channel BA
•RX signal detect alarm overwrite, RX 8b/10b enable, link state machine enable for channel BA
•GMASK and GTRISTN for Channel BA
•Enable High Speed loopback for Slice B
•Select High Speed loopback for Slice B
•Enable byte sync, lock RX to data for Channel BA
•Enable characterization for SLICE B
•Bypass channel align for Slice B
•After these events the PRBS sequence will be sent to the channel BA and looped back to the PRBS checker and the errors will be output to the LEDs on the Evaluation board.