LCD Controller

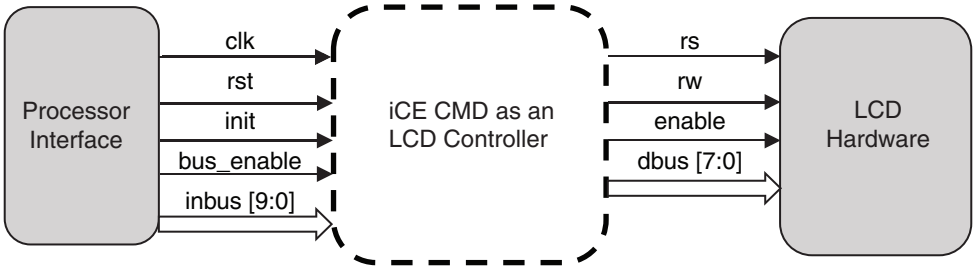
April 2013 **Reference Design RD1149**

Introduction

This application example illustrates the implementation of an LCD Controller using ultra low power FPGAs. The implementation is for a standard 16-character, two-line LCD display device. The 16x2 character LCD Controller is compatible with the Synopsys Synplify Pro® synthesis tool.

The design is implemented in VHDL. The Lattice iCEcube2™ Place and Route tool integrated with the Synplify Pro synthesis tool is used for the implementation of the design.

Figure 1. Block Diagram



Features

- 16x2 Character LCD Controller
- VHDL RTL, testbench and Aldec script for simulation

Signal Descriptions

Table 1. Signal Descriptions

Signal Name	Pin Type	Signal Description
Clk	Input	System clock operating at 32 Mhz
rst	Input	Asynchronous active high system reset
init	Input	A high triggers the initialization procedure
inbus[9:0]	Input	10-bit data bus to be written to LCD
bus_enable	Input	A high indicates valid data on inbus
dbus[7:0]	Output	8-bit data bus corresponding to the ASCII value of the character being written to the LCD
rw	Output	Used to indicate Read/Write Operation. A ‘0’ Specifies write operation.
rs	Output	Indicates whether the data on dbus is write data(I) or an LCD instruction
enable	Output	Enable signal used to latch the data to the LCD module

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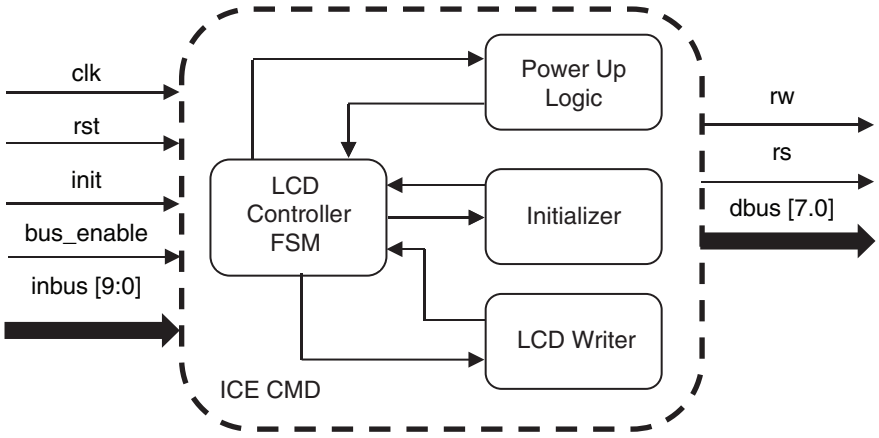
Design Module

Figure 2. Design Module Block Diagram



The design module consists of the blocks shown in Figure 1 and described below.

LCD Controller FSM

This FSM has the following states to interact with the LCD device:

- Start state
- Power Up state
- Initialization state
- LCD_write state

On reset, the FSM goes into Start state. Here, it waits for inputs from the host system. The inputs that are monitored by the Start state are init and bus_enable. Initially, the host places a high on the init line for at least one clock cycle while bus_enable is held low. When the host does this, the state machine goes to the Power Up state.

Power up logic

In the Power Up state, the FSM waits for 15 ms as required by the display to power up.

Initializer

Once power up is done, the FSM goes into the Initialization state. Here, the FSM sends out a set of seven commands to initialize the LCD display. This is clocked into the LCD at the falling edge of the enable signal generated by the initialization state. The whole initialization process lasts for approximately 120 ms after which the FSM returns to the Start state.

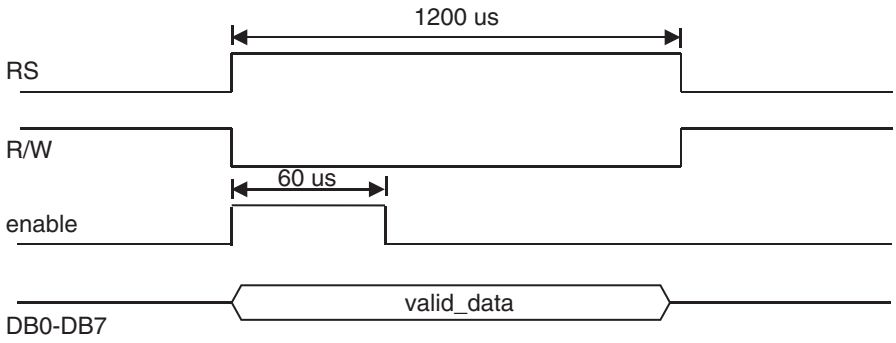
LCD Writer

The host can perform a Write operation or another initialization sequence as required. If the host chooses to perform a Write operation on the display, it places a '1' on the bus_enable line while holding the init pin low along with valid data to be displayed on the LCD.

Bus_enable should be held high for at least one clock cycle and should be made low before 20 clock cycles. In the LCD_write state, the host places appropriate data on the inbus. This is then clocked into the LCD on the falling edge of the enable signal which is generated by the lcd controller module. The whole write operation takes 20 clock cycles. Once the LCD_write state is complete, the FSM returns back to the Start state. The host can again go to the LCD_write state by placing high on the bus_enable line.

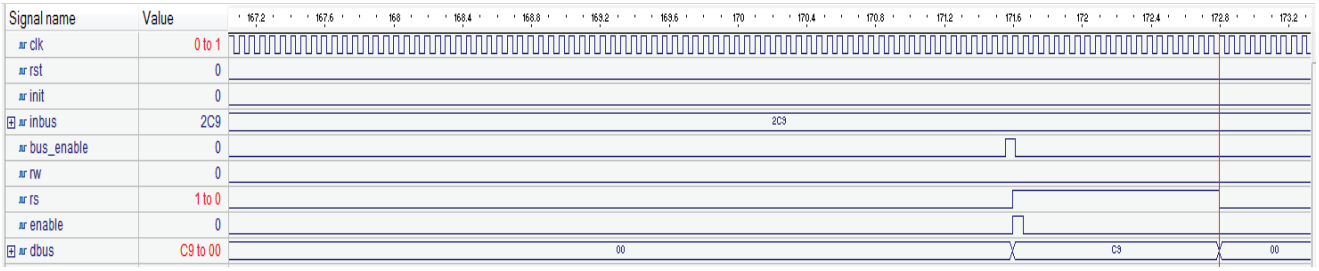
Timing Diagram

Figure 3. Timing Diagram for LCD Write Operation.



Simulation Waveforms

Figure 4. Simulation Waveforms



Implementation

This design is implemented in VHDL. When using this design in a different device, density, speed or grade, performance and utilization may vary.

Table 2. Performance and Resource Utilization

Family	Language	Utilization (LUTs)	f_{MAX} (MHz)	I/Os	Architecture Resources
iCE40[1]	VHDL	67	>50	26	(14/160) PLBs

1. Performance and utilization characteristics are generated using iCE40-LP1K-CM121 with iCEcube2 design software.

References

- iCE40 Family Handbook

Technical Support Assistance

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Revision History

Date	Version	Change Summary
April 2013	01.0	Initial release.