Designing for Migration from MachXO2-1200-R1 to Standard (Non-R1) Devices

Application Note

FPGA-AN-02012-1.3

November 2019

Disclaimers

Lattice makes no warranty, representation, or guarantee regarding the accuracy of information contained in this document or the suitability of its products for any particular purpose. All information herein is provided AS IS and with all faults, and all risk associated with such information is entirely with Buyer. Buyer shall not rely on any data and performance specifications or parameters provided herein. Products sold by Lattice have been subject to limited testing and it is the Buyer's responsibility to independently determine the suitability of any products and to test and verify the same. No Lattice products should be used in conjunction with mission- or safety-critical or any other application in which the failure of Lattice's product could create a situation where personal injury, death, severe property or environmental damage may occur. The information provided in this document is proprietary to Lattice Semiconductor, and Lattice reserves the right to make any changes to the information in this document or to any products at any time without notice.

© 2012-2019 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Contents

Figures

Tables

© 2012-2019 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

1. Introduction

The LCMXO2-1200ZE/HC “R1” devices have the same specifications as their Standard (non-R1) counterparts except as listed below:

1. The EFB UFM cannot be programmed through the WISHBONE interface.
2. The on-chip differential input termination resistor value is higher than intended.
3. The SRAM CRC Error Detection Circuit may not produce the correct result when it is run for the first time after configuration.
4. Under certain conditions, IIH exceeds data sheet specifications.
5. The user SPI interface does not operate correctly in some situations.
6. In GDDRX2, GDDRX4 and GDDR71 modes, ECLKSYNC may have a glitch.
7. When using the hard I2C IP core, the I2C status registers I2C_1_SR and I2C_2_SR may not update correctly.
8. PLL Lock signal will glitch high when coming out of standby.

The Standard MachXO2-1200 devices have no specification exceptions and will be available in September 2011. Along with the ordering part numbers the devices can be physically identified with the top side marking, as shown in Figure 1.1.

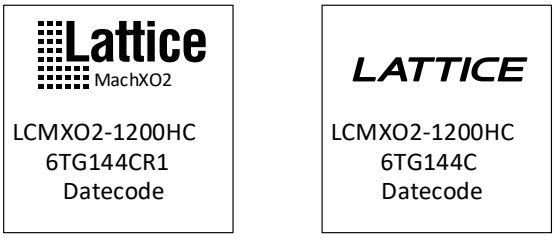

Figure 1.1. MachXO2-1200 Top Side Marking for R1 and Standard MachXO2-1200 Devices

To ensure JED file compatibility when migrating between the R1 and Standard devices, the exceptions must be designed for. The following table and flow chart can be used to determine the migration requirements between the R1 and Standard devices.

Table 1.1. Summary of the R1 and Standard Device Differences

Item	Migration Requirement	Summary of the R1 to Standard Device Differences
1	Optional Redesign	EFB UFM cannot be programmed through the WISHBONE interface
2	JED File Compatible	The on-chip differential input termination resistor value is higher than intended
3	Optional Redesign	SRAM CRC Error Detection Circuit may not produce the correct result when it is run for the first time after configuration
4	JED File Compatible	Under certain conditions, IIH exceeds data sheet specifications
5	Redesign Required	The user SPI interface does not operate correctly in some situations
6	JED File Compatible	In GDDRX2, GDDRX4 and GDDR71 modes, ECLKSYNC may have a glitch
7	Optional Redesign	When using the hard I^2C IP core, the I2C status registers I2C_1_SR and I2C_2_SR may not update correctly
8	Optional Redesign	PLL Lock signal will glitch high when coming out of standby

Notes:

1. “JED File Compatible” is defined as equivalent functionality and performance in either the R1 or the Standard device
2. “Optional Redesign” is defined as “JED File Compatible” but the design could be optimized to improve performance in the Standard device.
3. “Redesign Required” is defined as the design must be redesigned to ensure Standard device functionality.

© 2012-2019 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

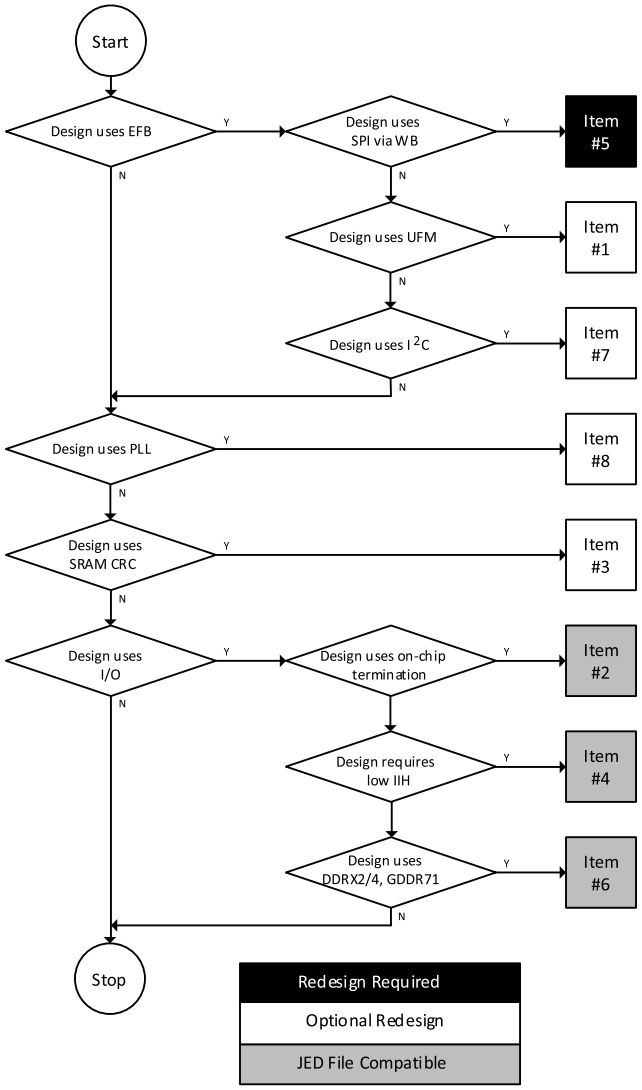

Figure 1.2. Logical Flow Chart for Design Migration

© 2012-2019 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

2. Details of Design Migration Considerations

1. When using the R1 device, the User Flash Memory (UFM) cannot be programmed through the internal WISHBONE interface.
   - R1 UFM can still be programmed through the JTAG/SPI/I2C ports
   - R1 UFM can be accessed via WISHBONE with certain requirements and limitations:
     - The hard SPI port or primary I2C port must be instantiated in the user design.
     - If instantiating the SPI port for this purpose, the four SPI signals must be routed to the dedicated
     - SPI pins of the device and the SN pulled to VCCIO either internally or externally.
     - If using the I2C port, the two I2C signals must be routed to the dedicated I2C pins of the device, and both pulled to VCCIO internally or externally.
2. The on-chip differential input termination resistor value is higher than intended. It is approximately 200 Ω as opposed to the intended 100 Ω.
   - When using R1 devices external termination resistors should be used for differential inputs.
   - Internal on-chip termination resistors can be disabled through Lattice Diamond® Spreadsheet View.
3. SRAM CRC Error Detection Circuit may not produce the correct result when it is run for the first time after configuration.
   - To use this feature, discard the result from the first operation, subsequent operations will produce the correct result.
- This has been documented in MachXO2 SRAM CRC Error Detection Usage Guide (FPGA-TN-02156).
4. Under certain conditions, IIH exceeds data sheet specifications.
   - The IIH limits from the data sheet are summarized below.

Condition	Clamp	Pad Rising IIH Max.	Pad Falling IIH Min.	Steady State Pad High IIH	Steady State Pad Low IIL
VPAD > VCCIO	OFF	1 mA	-1 mA	1 mA	10 µA
VPAD = VCCIO	ON	10 µA	-10 µA	10 µA	10 µA
VPAD = VCCIO	OFF	1 mA	-1 mA	1 mA	10 µA
VPAD < VCCIO	ON	10 µA	-10 µA	10 µA	10 µA

5. R1 user SPI interface does not operate correctly in some situations.
   - During master read access and slave write access, the last byte received does not generate the
   - RRDY interrupt in User mode SPI access through the WISHBONE.
   - Production devices requiring User mode SPI access through the WISHBONE should only use the
   - Standard device to ensure bitstream compatibility.
- For detailed information on the R1 workaround, refer to the Hardened SPI IP Cores section of Using User Flash Memory and Hardened Control Functions in MachXO2 Devices (FPGA-TN-02162).
   - The R1 device does support User mode SPI access but the design must be modified to ignore a bye of data.
   - Diamond 1.2 (and later versions) only include simulation libraries for the Standard device.
   - Contact Lattice Technical Support for instructions on download and installation for the R1 EFB simulation model.
6. In GDDRX2, GDDRX4 and GDDR71 modes, ECLKSYNC may have a glitch in the output under certain conditions, leading to possible loss of synchronization.
   - ECLKSYNC block uses rising edge flip-flops instead of falling edge flip-flops. As a result, there may be a timing violation which appears as a glitch.
   - Production designs using GDDRX2, GDDRX4 and GDDR71 interfaces should only use the Standard devices.

© 2012-2019 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

7. When using the hard I2C IP core, the I2C status registers I2C_1_SR and I2C_2_SR may not update correctly.
   - The I2C status registers I2C_1_SR and I2C_2_SR may not update correctly because there is a several microseconds of latency before the I2C status register reflects the proper status of BUSY/TIP.
   - To ensure compatibility with the Standard device these status bits should not be used. As an alternate TRRDY can be monitored.
- For detailed information on the instructions, refer to the Hardened I2C IP Cores section of Using User Flash Memory and Hardened Control Functions in MachXO2 Devices (FPGA-TN-02162).
   - R1 to Standard device migration can be verified through simulation. Diamond 1.2 (and later versions) only include simulation libraries for the Standard device. Contact Lattice Technical Support for instructions on download installation for the R1 EFB simulation model.
8. The PLL Lock signal will glitch high when coming out of standby.
   - The lock glitch lasts for about 10 µsec before returning low.
   - To ensure bitstream compatibility the PLL lock signal can be ignored or the PLL lock monitoring circuit should implement a delay when coming out of standby.
- For more information, refer to MachXO2 sysCLOCK PLL Design and Usage Guide (FPGA-TN-02157).

© 2012-2019 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

© 2012-2019 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Revision History

Revision 1.3, November 2019

Section	Change Summary
All	• Changed document number from AN8086 to FPGA-AN-02012. • Updated document template.
Disclaimers	Added this section.

Revision 1.2, April 2012

Section	Change Summary
All	• Updated document with new corporate logo. • Update to remove dummy page restriction in UFM algorithm.
Introduction	Figure 1.1., topside marks updated.

Revision 1.1, August 2011

Section	Change Summary
All	Clarified UFM access requirements and limitations.

Revision 1.0, July 2011

Section	Change Summary
All	Initial release.

© 2012-2019 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

www.latticesemi.com