



# Release Notes for Lattice Diamond 1.3

Welcome to Lattice Diamond<sup>®</sup>, the complete design environment for Lattice Semiconductor FPGAs. Lattice Diamond design software offers leading-edge design and implementation tools optimized for cost-sensitive, low-power Lattice FPGA architectures. Diamond is the next generation replacement for ispLEVER<sup>®</sup>, featuring design exploration, ease of use, improved design flow, and numerous other enhancements. Diamond is available for both the Windows and Linux operating systems. For details, see “Windows System Requirements” on page 8 or “Linux System Requirements” on page 10.

This version of Diamond adds a variety of enhancements to make designing for Lattice Semiconductor programmable devices easier than ever. The design tools also include support for the latest Lattice Semiconductor devices. See “What’s New” on page 2.

Known issues and workarounds are described in the Lattice Forums on the Lattice Semiconductor Web site: [www.latticesemi.com/latticeforums](http://www.latticesemi.com/latticeforums). Under “Questions & Answers,” find “Lattice Diamond Known Issues” and click on the version number.

Under Design Tools and IP, click **Lattice Diamond** for the latest questions and answers. You can also ask questions in the Lattice Forums.

Lattice Semiconductor offers a rich variety of information sources, including the Help system, PDF manuals, tutorials, and online discussions. The easiest way to reach them all is through the online Help. The first topic in the [Help](#) provides links to all the other sources of information.

You can also find extensive information about Diamond, its capabilities, tools, and workflow on the Lattice Semiconductor Web site under:

[www.latticesemi.com/latticediamond](http://www.latticesemi.com/latticediamond)

## What's New

This release of Diamond provides a variety of new features in the following areas. See the online Help for details.

**New Device Support** Support with JEDEC file output is available for the following devices:

- ◆ Platform Manager
- ◆ New LCMXO2-2000ZE-1UWG49ITR, which is the MachXO2-2000ZE with a WLCSP package
- ◆ MachXO2

Also, data for MachXO2-1200 has been updated as shown in Table 1.

**Table 1: MachXO2-1200 Data Levels**

Data Type	WLCSP Package	Other Packages	Change from Diamond 1.2?
Package	Advanced	Final	Yes
Timing	Preliminary	Preliminary	No
Power	Preliminary	Preliminary	No
SSO	Advanced	Final	Yes
IBIS	Preliminary	Preliminary	No
Bit stream	Final	Final	Yes

**Hierarchy and Module Library** For VHDL, Verilog HDL, and mixed VHDL/Verilog HDL projects, after synthesizing your project, you can see how different modules use device resources in the Hierarchy view. For more information, open the online Help and go to: [Managing Projects > Analyzing a Design > Viewing Synthesis Resource Utilization](#).

**LatticeMico System** Changes to LatticeMico<sup>®</sup> System include a new Memory Passthrough component and updates to the LatticeMico32 microprocessor. For more information, refer to the "LatticeMico System Software Release Notes for Diamond 1.3." To access the release notes:

- ◆ If LatticeMico System is installed with Diamond, go to the Windows Start menu and choose **Programs > Lattice Diamond 1.3 > Accessories > LatticeMico System Release Notes**.
- ◆ If LatticeMico System is installed as a stand-alone tool, go to the Windows Start menu and choose **Programs > Lattice Diamond 1.3 > LatticeMico System Release Notes**.

**Programmer** Programmer has been upgraded with a new user interface that incorporates many of the programming features that are included in ispVM<sup>®</sup> System. Features include:

- ◆ Programmer project files (.xcf) supported directly in the Diamond file list.
- ◆ Easier to use interface for programming devices.

- ◆ Ability to manage multiple .xcf files within a Diamond project.
- ◆ Tcl scripting support.

The Universal File Writer tool is now available as an accessory.

For more information, open the online Help and go to: [Programming the FPGA > About Programmer](#).

Programmer contains the same features as ispVM System for directly programming FPGAs. However, this release of Programmer does not contain the advanced ispVM System features listed in Table 2. If you require any of these features, you should install and use ispVM System to program devices. The ispVM System software is available as a separate download from the Lattice Web site.

**Table 2: Advanced ispVM System Features Not in Programmer**

◆ Lattice ISP (non-JTAG) devices	◆ VME Processor
◆ Obsolete Lattice JTAG devices	◆ Support for JTAG-ISC
◆ Generate files based on the scan chain .xcf file	◆ Support for JTAG-STAPL
◆ Display Registers	◆ BSCAN2 support
◆ Dual Boot SPI Flash Programming	◆ ispEditor
◆ Encryption Key Programming	◆ UES/USERCODE Editor
◆ Custom Device Database	◆ Control Register0 Editor
◆ FPGA Loader	◆ Control Register1 Editor
◆ I/O Vector Editor	◆ Security and Persistent Fields Editor
◆ I/O State, BSDL, I/O Vector File settings	◆ TAG Memory Editor
◆ Feature Row Editor	◆ Feature Row Editor
◆ Model300	◆ Board Diagnostics
◆ ispVM-DLx Connect	◆ Cable Signal Tests
◆ SVF Debugger	◆ Application Specific BSDL File Generator
◆ STAPL Debugger	◆ Repetitive Download
◆ STAPL Processor	◆ Convert Composite to JEDEC File

**Reveal Analyzer** Reveal Analyzer has significantly increased speed for cable connections. Configuring modules and uploading trace data for larger debug configurations or larger trace buffers is more than 10 times faster than previous releases.

**Run Manager** Run Manager supports running multiple place-and-route passes on individual implementations along with running multiple implementations. You can select the best result for further analysis and

processing. For more information, open the online Help and go to: [Managing Projects > Working with Run Manager](#).

**Simulation File Support** You can now mark source files as being for simulation only, synthesis only, or simulation and synthesis. By default, files are marked as being for both simulation and synthesis. In the File List view, right-click the filename and choose **Include for**. This allows support for simulation only files such as test benches or modules with different representations for simulation and synthesis. For more information, open the online Help and go to: [Managing Projects > Setting Options for Synthesis and Simulation > Specifying Input Files for Simulation](#).

**Simulation Wizard** Simulation Wizard will now parse the design and allow you to select the top level of the design for simulation, such as a test bench. The simulation top no longer has to be the same top as used for synthesis. Also, the Simulation Wizard can be launched from a toolbar icon. For more information, open the online Help and go to: [Simulating the Design > Simulation in Diamond > Creating a New Simulation Project in Diamond](#).

**Spreadsheet View** The Pin Layout File, available from Spreadsheet View, allows you to export a complete report of device pins, pin assignments, and IOBUF attributes. It is available at any stage of the design flow. The Export dialog box allows you to customize the Pin Layout File by selecting the types of items to be included in the report and then export the file using the value separator of your choice. You can open the file in an external spreadsheet program, edit the assignments, and then import the file into Spreadsheet View. For more information, open the online Help and go to: [Applying Design Constraints > Exporting/Importing Pin Files and Preference Sheets > Exporting and Importing a Pin Layout File](#).

For LatticeECP3 and MachXO2 devices, pin compatibility information is provided to help you migrate pin assignments to a different device of the same family and package. The new “Incompatible Pins” dialog box allows you to select one or more devices for possible pin migration and then view the incompatible pins in Spreadsheet View and Package View. For more information, open the online Help and go to: [Applying Design Constraints > Setting Preferences > Migrating Pin Assignments](#).

Spreadsheet View also enables you to export a comma-separated value pinout file of the targeted device. The pinout file is available for bonded pads at any stage of the design flow and includes pin/ball function, pin type, bank number, dual function names, differential definition, pin number, DQS, and I/O grouping.

**Synthesis Tools** The Synopsys® [Synplify Pro](#)® for Lattice and Lattice Synthesis Engine (LSE) synthesis tools have been updated.

Also, the application of Synopsys design constraint (SDC) files has changed. To make managing the files easier, the File List view now includes a “Synthesis Constraint Files” folder. Multiple files can be added to this folder and desired ones marked as active. The “Input SDC Constraint File” options are no longer available in strategies. Also, LSE now uses a different file extension for its constraint files: .lsc. The commands and syntax stay the same.

Projects created in earlier versions of Diamond will automatically have their SDC files added to the Synthesis Constraint Files folder. If the project is using LSE, the filenames will be changed to use the .ldc extension.

**Tcl Console** The Tcl Console view will show all output, including the correct error status, for all Tcl commands entered in the Console.

**Trace Static Timing Analysis** Trace now supports jitter analysis. Trace includes the effect of clock jitter in its static timing analysis based on the peak-peak jitter defined on any clocks pins. You can specify jitter with the preferences FREQUENCY, PERIOD, and SYSTEM\_JITTER. You can see this updated analysis both in the Trace report and Timing Analysis View. For more information, see the application note “Jitter Timing Analysis in Diamond” on the Lattice Web site.

---

## Updating Projects from an Earlier Version

---

If you want to work on a design project created with an earlier version of Diamond, start with the following procedures. These procedures adapt the project for the following changes in Diamond.

Find out which version of Diamond your project was created with. Then work through the changes for that and every later version, starting with the earliest and going to the most recent. For example, if your project was created with Diamond 1.1, you would start with the changes for 1.1. After completing those changes you would work on the changes for each later version (1.2).

When you open a project from Diamond 1.2 or earlier, Diamond opens a dialog box warning that Diamond will automatically move all SDC files to the Synthesis Constraint Files folder in File List view and remove the “Input SDC Constraint File” options from the strategies. If the project is using LSE, the filenames will be changed to use an .ldc extension.

Once saved, the project will not be compatible with earlier versions of Diamond.

### 1.2 Projects

There were several enhancements for IP and MachXO2.

#### IP Incompatibilities

SPI4.2 2.7 is not compatible with Diamond 1.3 or later. If you are using this IP, check the Lattice Semiconductor Web site for a more recent version.

#### MachXO2 Changes

See if your design involves any of the following features:

- ◆ For EFB modules with user flash memory (UFM), regenerate the module.
- ◆ For IO\_TYPE=PCI33 on a MachXO2-1200 or larger device, check if the CLAMP is using the default setting. With Diamond 1.3 the CLAMP default changes from ON to PCI and the I/O will be placed in bank 2. If you were

using the default and still want the setting to be ON, you need to set it explicitly.

- ◆ For PCI33 MT 6.5 and PCI33 T 6.4 IP, either set the CLAMP to ON explicitly or choose a bigger package (256 or more).

## 1.1 or 1.0 Projects

There were several enhancements for IP and MachXO2.

### IP Incompatibilities

The following IP versions are not compatible with Diamond 1.2 or later. If you are using any of these IP, check the Lattice Semiconductor Web site for a more recent version.

- ◆ Convolution Block Encoder 3.6
- ◆ Interleaver Deinterleaver 3.5
- ◆ DDR1 6.9
- ◆ PCI\_MT\_33 6.4
- ◆ DDR2 7.1
- ◆ PCIe RC Lite 1.2
- ◆ DDR3 1.2.1
- ◆ Tri-Speed MAC 3.4
- ◆ DDR1\_CP 1.1 with MachXO2
- ◆ Viterbi Block Decoder 4.6
- ◆ DDR2\_CP 1.1 with MachXO2

### MachXO2 Support

Some aspects of the software support for MachXO2 designs have been improved. See if your design involves any of the following features:

- ◆ The 4K/7K design with PLL has a CIB-to-PLL jump change. If you are using this design, recompile it.
- ◆ The EFB simulation model has changed. If you are using the EFB module, rerun your simulation tests to see more accurate results.
- ◆ In the DDR\_GENERIC module of IPexpress, the GDDR1\_RX.Aligned with PLL interface is no longer supported. If you are using such a module, use IPexpress to regenerate it without the PLL option.

Also, MachXO2 has IP evaluation capability and TransFR mode for all I/Os.

---

## Supported Third-Party Tools

---

This version of Diamond has been tested with the following third-party tools:

- ◆ Active-HDL 8.2 SP1
- ◆ MATLAB<sup>®</sup>/Simulink 2010b
- ◆ Modelsim<sup>®</sup> (SE) 6.6d
- ◆ NC-Sim 10.20-P008
- ◆ Riviera 2010.10
- ◆ Synplify Pro E-2011.03L

- ◆ Precision 2010a Update 2
- ◆ VCS 2010.06-SP1

---

## Supported Devices

---

Lattice Diamond can be used with either a free license or a subscription license. The two licenses provide access to different device families.

Device Family	Free License	Subscription License
LatticeEC™	●	●
LatticeECP™	●	●
LatticeECP2™	●	●
LatticeECP2M™		●
LatticeECP2S		●
LatticeECP2MS		●
LatticeECP3™		●
LatticeSC™		●
LatticeSCM™		●
LatticeXP™	●	●
LatticeXP2™	●	●
MachXO™	●	●
MachXO2™	●	●
Platform Manager™	●	●

---

## Migrating ispLEVER Projects

---

Diamond uses a different project structure than ispLEVER and cannot directly open an ispLEVER project. However, design projects created in ispLEVER can easily be imported into Diamond. The process is automatic except for the ispLEVER process properties, which are similar to the Diamond strategy settings, and some modules and IPs. All of your ispLEVER project source will be automatically handled.

Projects created using ispLEVER can be imported into Lattice Diamond through two different paths:

- ◆ On the Start Page, click **Import ispLEVER Project** (in the upper-left corner).
- ◆ From the File menu, choose **Open > Import ispLEVER Project**.

Follow the directions in the dialog box that opens to convert your ispLEVER project into a Lattice Diamond project.

Limitations to the import/conversion process include:

- ◆ NGO files in ispLEVER projects need to be manually copied into the Lattice Diamond project if the NGO files were originally copied into the ispLEVER project. For example, NGO files that were copied from Lattice IP generation.
- ◆ The .lpc files are replaced with .ipx files in Lattice Diamond. You need to regenerate your IP by double-clicking on the .lpc file. The resultant wizard will help you generate the new .ipx file, replacing the old .lpc file.

More information on importing ispLEVER projects can be found in the *Lattice Diamond User Guide*, online Help (see Managing Projects > [Importing ispLEVER Project](#)), and training videos on the Lattice Web site.

---

## Other Information Resources

---

Other available information resources for the Diamond software include the following.

- ◆ General Information: General information on Lattice Diamond can be found on the Lattice Web site at:  
[www.latticesemi.com/latticediamond](http://www.latticesemi.com/latticediamond)
- ◆ Online Help: Start Lattice Diamond and choose **Help > Lattice Diamond Help**.
- ◆ *Lattice Diamond User Guide*: This document can be found from a link on the Start Page view or downloaded from:  
[www.latticesemi.com/latticediamond/downloads](http://www.latticesemi.com/latticediamond/downloads)
- ◆ Training Videos: Several short videos are available on different aspects of the Lattice Diamond software. These can be viewed online at:  
[www.latticesemi.com/latticediamond/videos](http://www.latticesemi.com/latticediamond/videos)

---

## Windows System Requirements

---

The basic system requirements for Lattice Diamond on Windows are:

- ◆ Intel Pentium or Pentium-compatible PC
- ◆ Windows XP, Windows Vista (32-bit), or Windows 7 (32-bit or 64-bit)

### Note

---

If your operating system is Windows Vista, make sure you have installed all the latest patches from Microsoft.

---

- ◆ Approximately 5.75 GB free disk space

- ◆ Network adapter

#### Note

A node-locked license is based on the physical (hard-coded) address provided by the network adapter. Network connectivity is not necessarily required for a node-locked license. In the absence of a network connection, you can install the NWLink IPX/SPX protocol to force the recognition of your NIC card ID (see the installation notice).

A floating license requires access to the license server, so both a network adapter and connectivity are required.

- ◆ JScript-capable Web browser
- ◆ Acrobat Reader 5.0 or later
- ◆ 1024 X 768 graphics display
- ◆ Microsoft-compatible mouse and mouse driver

## Memory Requirements

Table 3 lists the minimum memory requirements and the recommended memory for all the Lattice Semiconductor FPGA families. Designing for the largest FPGAs may require more than the usual 2 GB of memory. For help in extending your memory to 3 or 4 GB, see “Extending Memory” on page 10.

**Table 3: Recommended Memory for Windows**

Device	Size	Minimum	Recommended
LatticeEC, LatticeECP	Up to 20K LUT	512 MB	768 MB
	Up to 50K LUT	768 MB	1 GB
LatticeECP2/M	Up to 20K LUT	768 MB	1 GB
	Up to 50K LUT	1 GB	1.5 GB
	Up to 100K LUT	1 GB	2 GB
LatticeECP3	Up to 95K LUT	2 GB	3 GB
	Up to 150K LUT <sup>1</sup>	3 GB	4 GB
LatticeSC/M	Up to 40K LUT	768 MB	1 GB
	Up to 115K LUT	1 GB	2.5 GB
LatticeXP, LatticeXP2	Up to 20K LUT	512 MB	768 MB
	Up to 50K LUT	768 MB	1 GB
MachXO, MachXO2	All	256 MB	512 MB
Platform Manager	All	256 MB	512 MB

1. Designing for LatticeECP3 with more than 95K LUT, requires a Windows 7 64-bit operating system.

## Extending Memory

Designing for the largest FPGAs may require more than the usual 2 GB of memory. For help in extending your memory to 3 or 4 GB, see the following.

### In Windows XP

Normally, the Windows XP platform limits the amount of memory to a maximum of 2 GB for any Diamond program. You can configure Windows XP to allow 2-3 GB of memory by adding the **/3GB** switch to the end of the startup line in the boot.ini file. Before you take advantage of this capability, it is important that you read the following information:

- ◆ Microsoft Knowledge Base Article #328269, which addresses a potential problem with the /3GB switch:  
[support.microsoft.com/?kbid=328269](http://support.microsoft.com/?kbid=328269)
- ◆ Microsoft article, “Memory Support and Windows Operating Systems,” which explains the use of the physical address extension (PAE) for Windows XP Professional and Windows Server 2003 Memory Support:  
[www.microsoft.com/whdc/system/platform/server/PAE/PAEmem.mspx](http://www.microsoft.com/whdc/system/platform/server/PAE/PAEmem.mspx)
- ◆ Microsoft article, “How to edit the Boot.ini file in Windows XP”:  
[support.microsoft.com/default.aspx?scid=kb;en-us;q289022](http://support.microsoft.com/default.aspx?scid=kb;en-us;q289022)

### In Windows 7

Lattice Diamond is a 32-bit application that can run in a Windows 7 64-bit system. With a Windows 7 32-bit system, Diamond can access up to 3 GB. With a Windows 7 64-bit system, Diamond can access up to 4 GB. See also the Microsoft article, “Memory Limits for Windows Releases” at:

[msdn.microsoft.com/en-us/library/aa366778\(VS.85\).aspx](http://msdn.microsoft.com/en-us/library/aa366778(VS.85).aspx)

---

## Linux System Requirements

---

The basic system requirements for Lattice Diamond on Linux are:

- ◆ Intel Pentium or Pentium-compatible PC, or AMD Opteron system support  
For Programmer and ispVM System, it contains a 32-bit driver to support the 32-bit system only.
- ◆ Red Hat Enterprise Linux version 4.X or 5.3, or Novell SUSE Linux Enterprise 10 SP1 or 11 operating system

The host operating system can be either 32-bit or 64-bit. Diamond is a 32-bit application requiring 32-bit support libraries in order run on a 64-bit host operating system.

Note that Programmer, Reveal Analyzer, LatticeMico System, and ispVM System may not download JEDEC or bitstream files on systems running Linux Red Hat 64-bit operating systems. If this occurs, delete the libusb-0.1.so.4 file in the bin/lin directory, and retry the download.

Version 5.3 of Red Hat Enterprise Linux has some extra installation requirements. See “Configuring Red Hat 5.3” on page 11.

- ◆ Approximately 5.75 GB free disk space
- ◆ 1024 x 768 graphics display
- ◆ JScript-capable Web browser
- ◆ Adobe Acrobat Reader, or equivalent PDF reader
- ◆ Network adapter and network connectivity

#### Note

A floating license requires access to the license server, so both a network adapter and connectivity are required.

## Memory Requirements

Table 4 lists the minimum memory requirements and recommended memory for all the Lattice Semiconductor FPGA families.

**Table 4: Recommended Memory for Linux**

Device	Size	Minimum	Recommended
LatticeEC, LatticeECP	Up to 20K LUT	512 MB	768 MB
	Up to 50K LUT	768 MB	1 GB
LatticeECP2/M	Up to 20K LUT	768 MB	1 GB
	Up to 50K LUT	1 GB	1.5 GB
	Up to 100K LUT	1 GB	2 GB
LatticeECP3	Up to 95K LUT	2 GB	3 GB
	Up to 150K LUT	3 GB	4 GB
LatticeSC/M	Up to 40K LUT	768 MB	1 GB
	Up to 115K LUT	1 GB	2.5 GB
LatticeXP, LatticeXP2	Up to 20K LUT	512 MB	768 MB
	Up to 50K LUT	768 MB	1 GB
MachXO, MachXO2	All	256 MB	512 MB
Platform Manager	All	256 MB	512 MB

## Configuring Red Hat 5.3

Red Hat Enterprise Linux 5.3 has some extra requirements for Diamond:

- ◆ In addition to the basic installation of Red Hat 5.3, under Development/ Legacy Software Development, select:

```
1:gtk+-1.2.10-56.e15.i386 - GIMP Toolkit (GTK+) sb:(9 of 9)
```

Under Base System/Legacy Software Support, add the following to the default items:

```
Openmotif22-2.2.3-18.i386 - Open Motif runtime
```

Proper Diamond operation depends upon these libraries being installed.

- ◆ When installing the Red Hat Enterprise Linux version, be sure to install the PERL modules XML::Parser, XML::DOM, and XML::RegExp. These PERL modules are available at [www.cpan.org](http://www.cpan.org).

---

## Contacting Technical Support

---

**FAQs** The first place to look. The [Lattice FAQs](#) (frequently asked questions) provide solutions to questions that many of our customers have already asked. Lattice Applications Engineers are continuously adding to the FAQs.

**Online Forums** [Lattice Forums](#) contain a wealth of knowledge and are actively monitored by Lattice Applications Engineers.

**Telephone Support Hotline** Receive direct technical support for all Lattice products by calling Lattice Applications from 5:30 a.m. to 6 p.m. Pacific Time.

- ◆ For USA & Canada: 1-800-LATTICE (528-8423)
- ◆ For other locations: +1 503 268 8001

In Asia, call Lattice Applications from 8:30 a.m. to 5:30 p.m. Beijing Time (CST), +0800 UTC. Chinese and English language only.

- ◆ For Asia: +86 21 52989090

### E-mail Support

- ◆ [techsupport@latticesemi.com](mailto:techsupport@latticesemi.com)
- ◆ [techsupport-asia@latticesemi.com](mailto:techsupport-asia@latticesemi.com)

**For Local Support** Contact your nearest [Lattice Sales Office](#).

## Trademarks

Lattice Semiconductor Corporation, L Lattice Semiconductor Corporation (logo), L (stylized), L (design), Lattice (design), LSC, CleanClock, E<sup>2</sup>CMOS, Extreme Performance, FlashBAK, FlexiClock, flexiFlash, flexiMAC, flexiPCS, FreedomChip, GAL, GDX, Generic Array Logic, HDL Explorer, IPexpress, ISP, ispATE, ispClock, ispDOWNLOAD, ispGAL, ispGDS, ispGDX, ispGDXV, ispGDX2, ispGENERATOR, ispJTAG, ispLEVER, ispLeverCORE, ispLSI, ispMACH, ispPAC, ispTRACY, ispTURBO, ispVIRTUAL MACHINE, ispVM, ispXP, ispXPGA, ispXPLD, Lattice Diamond, LatticeCORE, LatticeEC, LatticeECP, LatticeECP-DSP, LatticeECP2, LatticeECP2M, LatticeECP3, LatticeMico, LatticeMico8, LatticeMico32, LatticeSC, LatticeSCM, LatticeXP, LatticeXP2, MACH, MachXO, MachXO2, MACO, ORCA, PAC, PAC-Designer, PAL, Performance Analyst, Platform Manager, ProcessorPM, PURESPEED, Reveal, Silicon Forest, Speedlocked, Speed Locking, SuperBIG, SuperCOOL, SuperFAST, SuperWIDE, sysCLOCK, sysCONFIG, sysDSP, sysHSI, sysI/O, sysMEM, The Simple Machine for Complex Design, TraceID, TransFR, UltraMOS, and specific product designations are either registered trademarks or trademarks of Lattice Semiconductor Corporation or its subsidiaries in the United States and/or other countries. ISP, Bringing the Best Together, and More of the Best are service marks of Lattice Semiconductor Corporation.

Other product names used in this publication are for identification purposes only and may be trademarks of their respective companies.