Flexibilis Ethernet Switch

Flexibilis Ethernet Switch (FES) is a triple-speed (10Mbps/100Mbps/1Gbps) Ethernet Layer 2 switch compatible with IEEE 802.1D. FES is available in three different Ethernet interface configurations:

- 3-port
- 4-port
- 8-port

All of the ports can be either copper or fiber Ethernet interfaces, or connected to other FPGA blocks. FPGA resource usage varies from about 14,500 FPGA registers (3-port) to about 38,000 FPGA registers (8-port). FES is suitable for applications such as:

- Wireless Backhaul
- Wireline Access
- Data Center Bridging

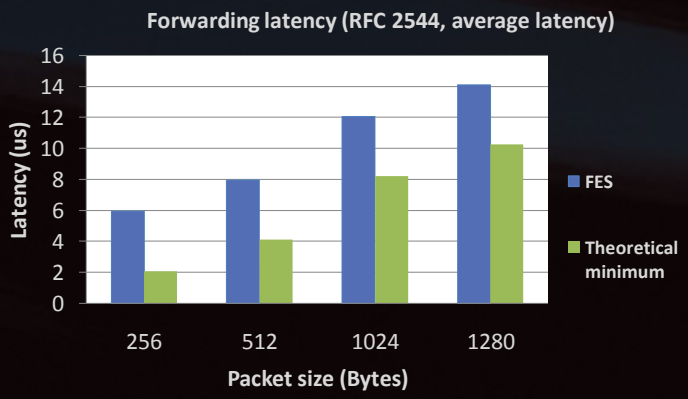
Packet forwarding takes place at wire-speed and the switching operation is non-blocking. These IP cores support the following interface options:

- MII
- GMII
- RMII
- RGMII

FES also supports MDIO interface for possible host CPU to access registers of FES and the registers of the PHY chips connected to FES. The optional host CPU can be used to manage the functionality of FES or to implement Spanning Tree Protocol (STP) or Rapid Spanning Tree Protocol (RSTP). The CPU port can be configured as a management port which enables the CPU to be able to send and receive any kinds of Ethernet frames to/from any other port. FES can also be used without a host CPU, the IP core can automatically poll the status of the connected PHY interface chips and adjust its interface speed accordingly.

Multi-Gigabit Forwarding Engine

The core of FES is a multi-gigabit forwarding engine capable of serving up to eight full-duplex gigabit Ethernet ports, thus forwarding eight gigabits of data every second. All the ports have four priority queues enabling four different priority levels. At congestion situation frames are discarded in WRED (Weighted Random Early Detection) fashion, which drops frames from low priority queues first, preserving the more important streams also during congestion. Using Store-and-Forward technique enables error-checking of the frames and eliminates the possibility of the switch forwarding broken frames, which is impossible for Cut-through type of switches. Forwarding latency is minimal, thanks to gigabit operation.



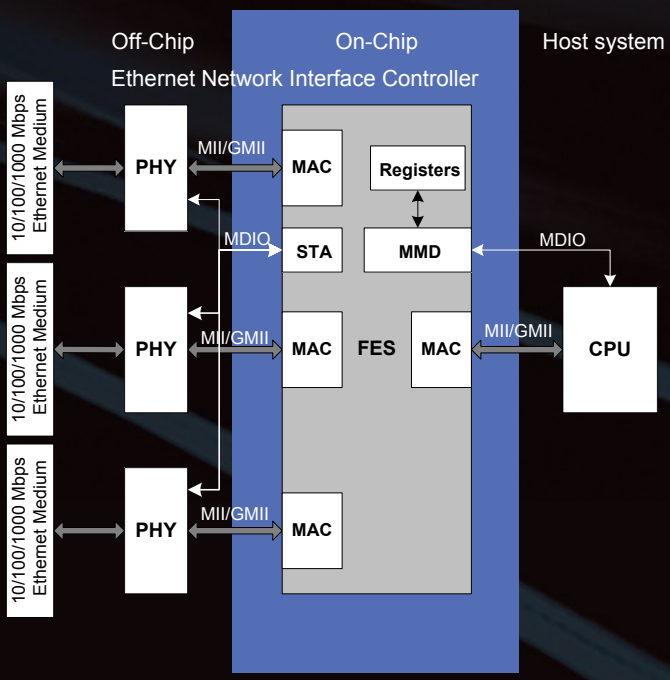
To preserve valuable FPGA internal memory resources the switch core includes advanced memory management functionality: frames are stored in centralized manner and in fragments of 512 bytes. This prevents small frames from consuming the same amount of memory as maximum sized frames. Also by not having fixed size per port queues prevents the currently empty queues from allocating memory that could be used by the other queues. 512 kbits of FPGA internal memory is reserved for output queues, which makes it possible to queue 42 to 128 Ethernet frames depending on their length.

Precision Time Protocol

Precision Time Protocol (PTP), defined in IEEE standard 1588, enables precise synchronization of device clocks in packet based networks. Devices are automatically synchronized to the most accurate clock in the network. The protocol supports system wide synchronization accuracy usually in sub microsecond range with minimal network and local clock computing resources. The protocol is used in applications such as test and measurement, power-line management, industrial automation and telecom applications.

FLEXIBILIS

PTP accuracy is based on an assumption that the delay in Ethernet is approximately constant and symmetric. Ethernet switches cause fluctuation to the packet delay, thus decreasing PTP synchronization accuracy. Transparent PTP switch functionality removes these problems and enables precise synchronization of clocks in switched Ethernet. When using Gigabit fiber Ethernet FES is able to achieve nanosecond class accuracy in clock transfer.



FES has been in use by Flexibilis customers since year 2007 and its compatibility has been tested in three ISPCS plug-fests.

Standard features

- Compatible with IEEE standard 802.1D ”Media Access Control (MAC) Bridges”
- Time and frequency synchronization using IEEE1588-2008 Precision Time Protocol
- End-to-end transparent switch functionality
- Triple-speed Full-Duplex operation on all ports
- Wire-speed packet forwarding
- Reliable Store-and-Forward operation with data integrity checking
- Ethernet packet filtering and priorization
- 4 priority queues for each port
- Weighted Random Early Detection (WRED) queue management
- 512 kbit internal memory for output queues
- Efficient internal memory management
- Management Ethernet port
- Rapid Spanning Tree Protocol implementation support
- Automatic polling of connected Ethernet PHY interface chips
- 2048 address MAC-table
- Automatic address learning and aging

Also available

- Evaluation package for LatticeECP3 PCI Express Solutions Board
- Open source IEEE 1588 PTP protocol stack implementation and Linux software for embedded environments
- Accelerated hardware test environment

Flexibilis Oy
Naulakatu 3
33100 Tampere
Finland
http://www.flexibilis.com/