syn1588®VIP Dual *High Performance*

Brief Data Sheet

Bringing Time in Line

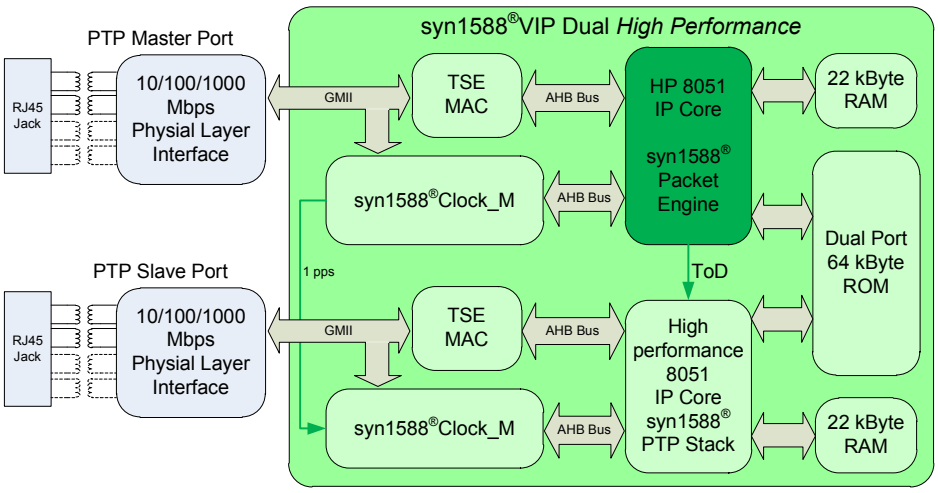
Version 1.1 – April 2011

Features

- 2 independent PTP ports with shared local oscillator
- High performance packet generation engine on one port
- Up to 10.000 packet/sec in master mode
- Configurable role per port
- Configurable profile per port
- 10/100/1000 Mbps Ethernet MAC, (IEEE802.3-2000)
- IEEE1588-2008 hardware timestamping
- 2 IEEE1588 hardware clocks
- IEEE1588-2008 Layer 2 compliant
- IEEE1588-2008 Layer 3 compliant (UDP, ARP, DHCP)
- Clocks accuracy better than 50 ns
- syn1588® PTP stack binary included (running on integrated 8-bit CPU core)
- Shared program ROM
- 2x 1 pps outputs
- 2x Frequency outputs
- 2x Event input
- In layer 3 mode each node may be controlled remotely via IEEE1588 management messages
- Optional analog PLL using VXCOs

Options

- Serial interface to external CPU upon request



syn1588® Versatile IP Dual *HP*-Fully integrated 2-port clock synchronization solution

The syn1588® VIP Dual *HP* SoC IP core offers unparalleled integration density combined with extremely high sync packets rates, providing the end user with a versatile 2-port PTP node. One port is equipped with a high performance packet generating engine enabling packets rates of up to 10,000 packets/sec (assuming Gbit connectivity). Each port may operate in any PTP role using either the default, the power, or the telecom profile. The combination of all necessary hard- and software module into one single chip enables a cost effective and highly integrated single chip dual port PTP solution. Only a single external Ethernet PHY for every port is required to create an IEEE1588 node.

Every port will generate an accurate high precision 1-pps signal together with a user programmable frequency output phase locked to the synchronized local clock of the respective port. Additionally, time stamps are generated in case an external event occurs on a dedicated pin.

Every port may be configured separately according to IEEE1588. The syn1588® VIP Dual *HP* supports a variety of possible implementation scenarios

- **Different Profiles:** One port may be run in slave mode being connected to an external multicast master, while the other port will run in unicast master mode supporting the telecom profile. Alternatively the second port may be operated in power profile using the peer-delay mechanism transmitting messages at a pre-defined rate.
- **Slave – *HP* Master:** In this preferred configuration one port is configured as a slave-only node attached to an external grand master thus maintaining the connection to an external network. The other port will run in master mode suppling the local network with accurate time information. The time information will be transferred internally between the two ports. In case the telecom profile is selected for the master mode port it may take advantage of the packet processing engine supplying a large number of unicast clients with message rate of up to 64 messages per client. The internal CPU will handle unicast negotiation without the need to generate sync packet at an overall rate of more than 1000 packets / sec.
- **GPS – Connectivity:** One port may be configured to accept NMEA formatted Time-of-Day data from a standard GPS timing receiver. In combination with a 1 pps input signal it will synchronize to this time refence subsequently acting as a PTP master on the respective port.

The syn1588® VIP is initially available on LatticeECP3 and LatticeECP2M FPGAs. As the IP is designed to be completely technology independent, it can be easily retargeted to other FPGAs or any ASIC technology.

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Technical Specifications	
Standards	IEEE802.3-2000 IEEE1588-2008
Supported functions	IEEE1588 hardware timestamping IEEE1588 hardware clock 1 one pulse per second output per port 1 synchronous frequency output per port 1 event timestamp input per port NMEA compatible data stream on serial interface Boundary Clock with fixed port assignment Profile selectable per port Serial Control interface
Operating temperature	N/A (depending on target technology)
Humidity	N/A
Driver support	N/A

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