Bringing Time in Line

syn1588®VIP

Brief Data Sheet

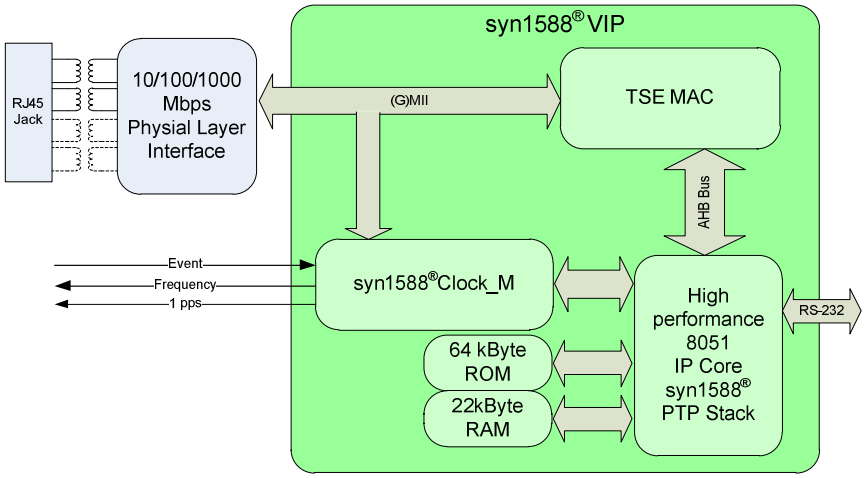
Version 1.6 – April 2011

Features

- 10/100/1000 Mbps Ethernet MAC included, compliant to IEEE802.3-2000
- IEEE1588-2008 hardware timestamping
- IEEE1588 hardware clock
- IEEE1588-2008 Layer 2 compliant.
- 1-step & 2-step master
- IEEE1588-2008 Layer 3 compliant (UDP, ARP, DHCP)
- Clock accuracy better than 50 ns
- syn1588® PTP stack running on integrated 8-bit CPU core
- 1 pps output
- Arbitrary frequency output
- Event input
- Node remotely controlled via IEEE1588 management messages (in layer 3 mode)
- Direct replacement for GPS receiver
- Grand Master operation with seamless link to external GPS timing receiver.
- Analog PLL using an external TCVCXO or OCVCXO
- Default, telecom and power profile supported
- Multicast & unicast PTP message supported

Options

- Interface to external CPU upon request



syn1588® Versatile IP - Fully integrated clock synchronization solution

The syn1588® VIP clock synchronization SoC IP Core enables a cost effective yet highly integrated single chip IEEE1588 solution. Only a single external Ethernet PHY is required to create a fully functional IEEE1588 node.

Due to its highly efficient PTP stack implementation the syn1588® VIP may be used is variety of different timing applications: It fully supports the default as well as the telecom, and power profile both in layer-2 or layer-3 communication mode.

The syn1588® VIP generates a highly accurate 1 pps signal together with a user programmable frequency output phase locked to the synchronized local clock. Additionally, time stamps are generated and stored in a local buffer memory in case an external event occurs at an input pin.

These digital IO signals in combination with the RS-232 interface make

The syn1588® VIP may assume the role of a GPS timing receiver in a system without the need for an external antenna: If connected to a PTP Grand Master it will switch to slave mode synchronizing its local clock to the master. Apart from a 1 pps signal it will generate an NMEA compatible data stream on the serial interface effectively acting as a GPS timing receiver.

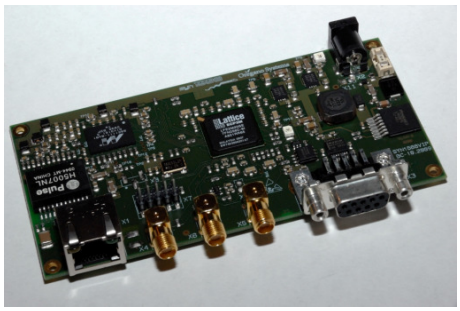
Equally well the syn1588®VIP may be attached directly to a GPS timing receiver via its event input and its serial interface. It will synchronize its local clock to the GPS time assuming the role of a grand master to the network it is attached to.

The syn1588® VIP is available as:

- IP core
- Single chip device
- Evaluation Board

The syn1588® VIP is initially available on LatticeECP3 and LatticeECP2M FPGAs. As the IP is designed to be completely technology independent, it can be easily retargeted to other Lattice FPGAs or any ASIC technology.

Additionally a fully functional reference board is available. Customers may receive all design data of this reference board enabling them to easily adapt this design to their specific needs.



Syn1588®VIP Evaluation Board

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Technical Specifications	
Standards	IEEE802.3-2000 IEEE1588-2008
Supported functions	IEEE1588 hardware timestamping IEEE1588 hardware clock 1 one pulse per second output 1 synchronous frequency output 1 event timestamp input NMEA compatible data stream on serial interface
Operating temperature	N/A (depending on target technology)
Humidity	N/A
Driver support	N/A

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