MachXO2 sysI/O User Guide

Technical Note

FPGA-TN-02158-2.4

March 2026

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Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
ASCII	American Standard Code for Information Interchange
BIDI/BIDIs	Bidirectional I/O
BLVDS	Bus Low-Voltage Differential Signalling
DDR	Double Date Rate
DRC	Design Rule Check
GPIO	General-Purpose Input/Output
GUI	Graphical User Interface
HDL	Hardware Description Language
HSTL	High-Speed Transceiver Logic
IBIS	I/O Buffer Information Specification
I/O	Input/Output
JTAG	Joint Test Action Group
LVDS	Low-Voltage Differential Signaling
LVPECL	Low-Voltage Positive Emitter-Coupled Logic
LVTTL	Low-Voltage Transistor-Transistor Logic
MIPI	Mobile Industry Processor Interface
MLVDS	Multipoint Low-Voltage Differential Signaling
PCI	Peripheral Component Interconnect
PIC	Programmable I/O Cell
PIO	Programmable I/O
PLD	Programmable Logic Device
SSTL	Stub Series Terminated Logic
TSALL	Tri-State All

1. Introduction

The MachXO2™ programmable logic device (PLD) family sysI/O™ buffers are designed to meet the needs of flexible I/O standards in today's fast-paced design world. The supported I/O standards range from single-ended I/O standards to differential I/O standards so that you can easily interface your designs to standard buses, memory devices, video applications and emerging standards. This technical note provides a description of the supported I/O standards and the banking scheme for the MachXO2 PLD family. The sysI/O architecture and the software usage are also discussed to provide a better understanding of the I/O functionality and placement rules.

2. sysI/O Buffer Overview

The basic building block of the MachXO2 sysI/O architecture is the Programmable I/O Cell (PIC) block. There are four PIC types in the MachXO2 device family. These include the basic PIC block, the memory PIC block for DDR memory support, the receiving PIC block with gearing, and the transmitting PIC block with gearing. The PIC blocks with gearing are used for video and high-speed applications and include a built-in control module for word alignment. The memory PIC block incorporates additional logic for managing DQS strobe signals and clock phase adjustments. The details of the memory PIC block and the gearing PIC block can be found in Implementing High-Speed Interfaces with MachXO2 Devices (FPGA-TN-02153).

All PIC types contains four programmable I/Os (PIOs), each consisting of a sysI/O buffer and an I/O logic block. A simplified sysI/O block diagram is shown in Figure 2.1. The I/O logic block includes input, output, and tri-state circuitry with registers, input delay cells, and control logic to support multiple operational modes. The sysI/O buffer determines compliance with supported I/O standards and provides features such as programmable hysteresis. Both the sysI/O buffer and I/O logic block are designed to optimized die area usage, enabling efficient bus interfacing, and pinout utilization.

Two adjacent PIOs can form a pair of complementary output drivers. In addition, PIOA and PIOB form the primary pair, while PIOC and PIOD form the alternate pair. The primary pair includes enhanced capabilities not available in the alternate pair. When configured for single-ended signaling, the sysI/O buffers of the PIC block operate equivalently.

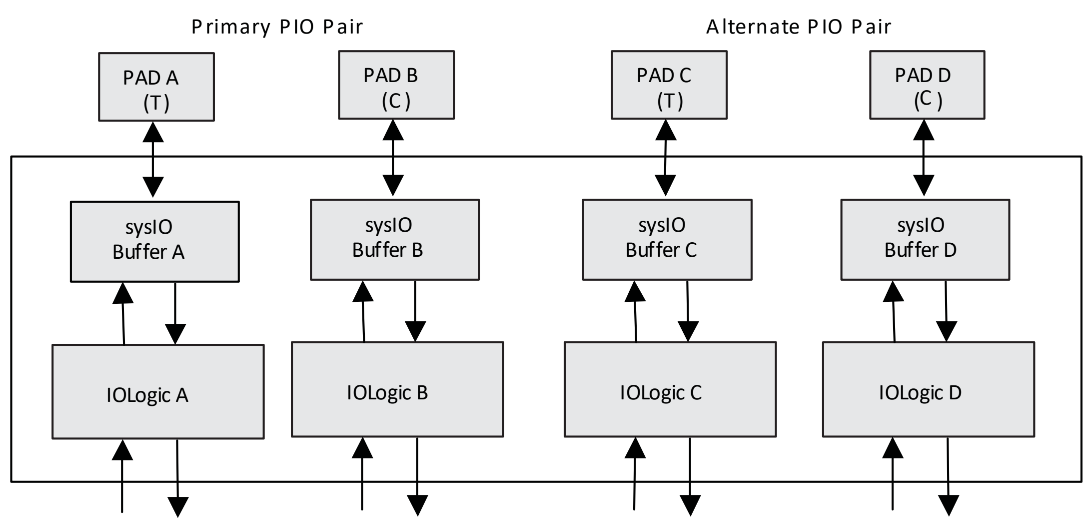


Figure 2.1. PIC Block Diagram

3. Supported sysI/O Standards

The Lattice MachXO2 sysI/O buffer supports both single-ended and differential standards. The single-ended standard can be further divided into internally ratioed standards such as LVCMOS, and externally referenced standards such as SSTL. The internally ratioed standards support individually configurable drive strength and bus maintenance circuits (weak pull-up, weak pull-down, or bus keeper).

There are two types of ratioed input buffers. One is connected to V_{CCIO} and the other is connected to V_{CC} (1.2 V). Each sysI/O buffer supports both buffers in parallel, and therefore provides an option to program any input buffer to be a 1.2 V ratioed input buffer regardless of the V_{CCIO} voltage.

All banks of the MachXO2 devices support true differential inputs, and emulated differential outputs using external resistors and the complementary LVCMOS outputs. The true-LVDS differential outputs and LVDS input termination are supported in specific banks as described in the sysI/O Banking Scheme section of this document.

Table 3.1. Supported Input Standards

Input Standard	V_{REF} (Nominal)	V_{CCIO}[1] (Nominal)
Single-Ended Interfaces		
LVTTL33	—	—
LVCMOS33	—	—
LVCMOS25	—	—
LVCMOS18	—	—
LVCMOS15	—	—
LVCMOS12	—	—
SSTL25 Class I, II	1.25	—
SSTL18 Class I, II	0.9	—
HSTL18 Class I, II	0.9	—
PCI33	—	3.3
Differential Interfaces		
LVDS25	—	—
LVPECL33	—	—
MLVDS25	—	—
BLVDS25	—	—
RSDS25	—	—
SSTL25 Differential	—	—
SSTL18D Differential	—	—
HSTL18D Differential	—	—
LVTTL / LVCMOS Differential	—	—
MIPI[2]	—	—

Notes:

1. If not specified, refer to mixed voltage support in the VCCIO Requirement for I/O Standards section.
2. This interface can be emulated with external resistors.

Table 3.2. Supported Output Standards

Output Standards	Drive (mA)	V_{CCIO} (Nominal)
Single-Ended Interfaces		
LVTTL33	4, 8, 12, 16, 24	3.3
LVCMOS33	4, 8, 12, 16, 24	3.3
LVCMOS25	4, 8, 12, 16	2.5
LVCMOS18	4, 8, 12	1.8
LVCMOS15	4, 8	1.5
LVCMOS12	2, 6	1.2
SSTL25 Class I	8	2.5
SSTL18 Class I	8	1.8
HSTL18 Class I	8	1.8
PCI33	24	3.3
Differential Interfaces		
LVDS25	3.5, 2.5, 2.0, 1.25	2.5, 3,3
LVPECL33	16	3.3
MLVDS25	16	2.5
BLVDS25	16	2.5
RSDS25	8	2.5
SSTL25 Differential	8	2.5
SSTL18D Differential	8	1.8
HSTL18D Differential	8	1.8
LVTTL33 Differential	4, 8, 12, 16, 24	3.3
LVCMOS33 Differential	4, 8, 12, 16, 24	3.3
LVCMOS25 Differential	4, 8, 12, 16	2.5
LVCMOS18 Differential	4, 8, 12	1.8
LVCMOS15 Differential	4, 8	1.5
LVCMOS12 Differential	2, 6	1.2
MIPI[1]	2	2.5

4. sysI/O Banking Scheme

The MachXO2 family has a non-homogeneous I/O banking structure. The MachXO2-256, MachXO2-640/U and MachXO2-1200 devices have four I/O banks each with one I/O bank per side. The MachXO2-1200U, MachXO2-2000/U, MachXO2-4000, and MachXO2-7000 devices have six I/O banks each, with one I/O bank on each of the top, bottom and right sides, and three banks on the left side.

The MachXO-640U, MachXO-1200/U, and higher-density devices support true LVDS differential outputs through the primary pairs in the top bank (bank 0). These devices also support 100 Ω differential input termination on every I/O pair on the bottom I/O bank. There is also a programmable PCI clamp available on the bottom I/O bank for these devices. For the *R1* version of the MachXO2 devices, the 100 Ω differential input termination is approximately 200 Ω. The *R1* version of the MachXO2 devices have an *R1* suffix at the end of the part number, for example, LCMXO2-1200ZE-1TG144CR1. For more details on the *R1* version to standard migration, refer to the Designing for Migration from MachXO2-1200-R1 to Standard (Non-R1) Devices (FPGA-AN-02012).

The MachXO2-256 and MachXO2-640 devices do not support true LVDS differential outputs, differential input termination, and PCI clamps in any banks (the MachXO2-640U I/O architecture is similar to the larger devices and supports the aforementioned features). Each of the I/O pins on all MachXO2 PLDs has a clamp feature which can be disabled or enabled. This clamp is similar to the PCI clamp but is not PCI compliant except in the bottom bank of the MachXO2-640U, MachXO2-1200/U and higher-density devices. When the CLAMP DIODE is ON, careful design consideration must be followed. For more information, refer to Appendix D.

The arrangements of the I/O banks are shown in Figure 4.1, Figure 4.2, and Figure 4.3. The DDR memory support in bank 1 is not available for devices in the wafer-level chip scale packages (WLCSP).

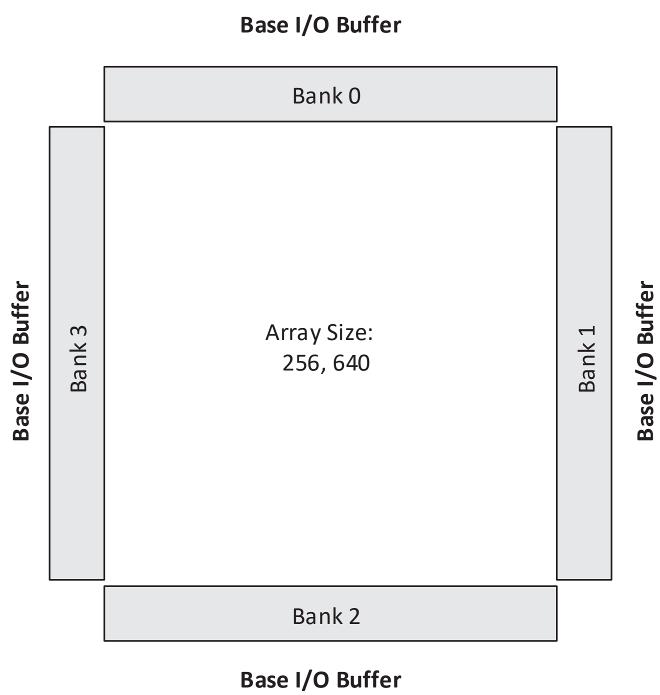


Figure 4.1. MachXO2-256 and MachXO2-640 I/O Banking Arrangement

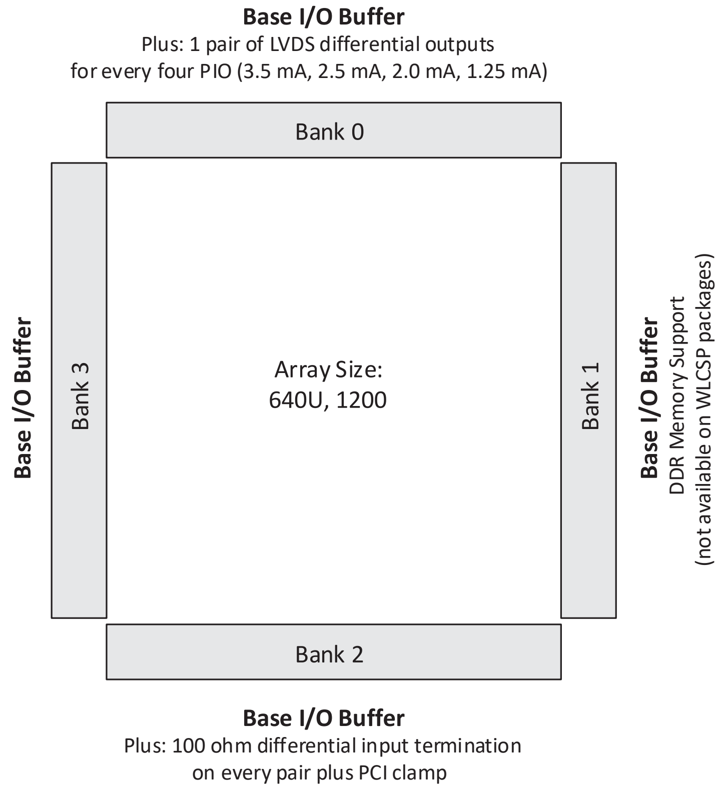


Figure 4.2. MachXO2-640U and MachXO2-1200 I/O Banking Arrangement

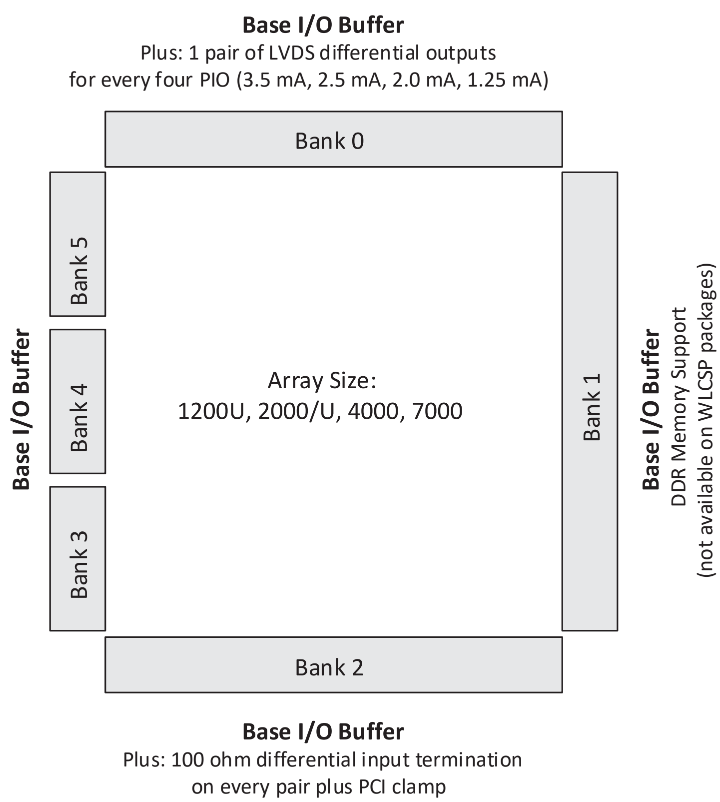


Figure 4.3. MachXO2-1200U, MachXO2-2000/U, MachXO2-4000, and MachXO2-7000 I/O Banking Arrangement

5. sysI/O Standards Supported by I/O Banks

All banks can support multiple I/O standards under the V_{CCIO} rules discussed above.

Table 5.1 and Table 5.2. summarize the I/O standards supported on various sides of the MachXO2 device.

Table 5.1. Single-Ended I/O Standards Supported on Various Sides

Standard	Top	Bottom	Left	Right
PCI33	—	Yes[1]	—	—
LVTTL33	Yes	Yes	Yes	Yes
LVCMOS33	Yes	Yes	Yes	Yes
LVCMOS25	Yes	Yes	Yes	Yes
LVCMOS18	Yes	Yes	Yes	Yes
LVCMOS15	Yes	Yes	Yes	Yes
LVCMOS12	Yes	Yes	Yes	Yes
SSTL25[2]	Yes	Yes	Yes	Yes
SSTL18[2]	Yes	Yes	Yes	Yes
HSTL18[2]	Yes	Yes	Yes	Yes

Notes:

1. PCI33 is supported at the bottom bank of MachXO2-640U, MachXO2-1200/U, MachXO2-2000/U, MachXO2-4000, and MachXO2-7000 devices.
2. SSTL Class II and HSTL Class II are supported as input only.

Table 5.2. Differential I/O Standards Supported on Various Sides

Standard	Top	Bottom	Left	Right
LVDS output	Yes[1]	—	—	—
LVPECL33E[2]	Yes	Yes	Yes	Yes
MLVDS25E[2]	Yes	Yes	Yes	Yes
BLVDS25E[2]	Yes	Yes	Yes	Yes
RSDS25E[2]	Yes	Yes	Yes	Yes
LVDS25E[2]	Yes	Yes	Yes	Yes
SSTL25D output	Yes	Yes	Yes	Yes
SSTL18D output	Yes	Yes	Yes	Yes
HSTL18D output	Yes	Yes	Yes	Yes
LVTTL33D output	Yes	Yes	Yes	Yes
LVCMOS33D output	Yes	Yes	Yes	Yes
LVCMOS25D output	Yes	Yes	Yes	Yes
LVCMOS18D output	Yes	Yes	Yes	Yes
LVCMOS15D output	Yes	Yes	Yes	Yes
LVCMOS12D output	Yes	Yes	Yes	Yes
LVDS input	Yes	Yes	Yes	Yes
LVPECL33 input	Yes	Yes	Yes	Yes
MLVDS25 input	Yes	Yes	Yes	Yes
BLVDS25 input	Yes	Yes	Yes	Yes
RSDS25 input	Yes	Yes	Yes	Yes
SSTL25D input	Yes	Yes	Yes	Yes
SSTL18D input	Yes	Yes	Yes	Yes
HSTL18D input	Yes	Yes	Yes	Yes
LVTTL33D input	Yes	Yes	Yes	Yes
LVCMOS33D input	Yes	Yes	Yes	Yes
LVCMOS25D input	Yes	Yes	Yes	Yes
LVCMOS18D input	Yes	Yes	Yes	Yes

Standard	Top	Bottom	Left	Right
LVCMOS15D input	Yes	Yes	Yes	Yes
LVCMOS12D input	Yes	Yes	Yes	Yes
MIPI	Yes	Yes	Yes	Yes

Notes:

1. True LVDS output is supported at the top bank of MachXO2-640U, MachXO2-1200/U, MachXO2-2000/U, MachXO2- 4000, and MachXO2-7000 devices.
2. Emulated output standards are denoted with a trailing ***E*** in the name of the standard.

6. Power Supply Requirements

The MachXO2 device family has a simplified power supply scheme for sysI/O buffers. The core power V_{CC} and the bank power V_{CCIO} are the two main power supplies. A MachXO2 device can be powered and operated with a single power supply by connecting V_{CC} and V_{CCIO} to nominal voltages of 1.2 V. The JTAG programming pins are powered by V_{CCIO} in bank 0 where the JTAG pins reside. All the user sysI/Os have a weak pull-down after power-up is complete and before the device configuration is done.

7. V_{CCIO} Requirement for I/O Standards

Each I/O bank of the MachXO2 device has a separate V_{CCIO} supply pin that can be connected to 1.2 V, 1.5 V, 1.8 V, 2.5 V or 3.3 V. This voltage is used to power the output I/O standard and source the drive strength for the output. In addition to this, the V_{CCIO} also powers the ratioed input buffers such as LVTTL, LVCMOS and PCI. This ensures that the threshold of the input buffers tracking the V_{CCIO} voltage level.

For LVCMOS I/O types, mixed input voltage support is allowed in each I/O bank as long as the V_{CCIO} requirement for the input or output I/O standard is the same, or when all inputs in the bank are within the over-drive or underdrive range as specified in Table 7.1 and Table 7.2. Two other options exist to further increase the input receiver flexibility. One is to configure an I/O to be a 1.2 V ratioed input buffer, regardless of the bank V_{CCIO} voltage. This is possible because the MachXO2 sysI/O buffer has two ratioed input buffers connected to V_{CCIO} and V_{CC} in parallel. The other option is to use the input reference voltage pin to set the input threshold for LVCMOS standards that are not covered by the V_{CCIO} of the bank.

Table 7.1. V_{CCIO} for Same Bank LVCMOS/LVTTL Input/Output Requirements[1]

I/O Type	Bank Restrictions
LVCMOS10R33[2, 3]	Inputs or BIDIs only require V_{CCIO} = 3.3 V and V_{REF} = 0.50 V. BIDIs additionally require Open-Drain output.
LVCMOS10R25[2, 3]	Inputs or BIDIs only require V_{CCIO} = 2.5 V and V_{REF} = 0.50 V. BIDIs additionally require Open-Drain output.
LVCMOS12	Outputs require V_{CCIO} = 1.2 V. Inputs available in all V_{CCIO} levels.
LVCMOS12R33[2, 3]	Inputs or BIDIs only, require V_{CCIO} = 3.3 V and V_{REF} = 0.60 V. BIDIs additionally require Open-Drain output.
LVCMOS12R25[2, 3]	Inputs or BIDIs only require V_{CCIO} = 2.5 V and V_{REF} = 0.60 V. BIDIs additionally require Open-Drain output.
LVCMOS15	Outputs require V_{CCIO} = 1.5 V. Inputs available in all V_{CCIO} levels.
LVCMOS15R33 [2, 3]	Inputs only require V_{CCIO} = 3.3 V and V_{REF} = 0.75 V.
LVCMOS15R25[2, 3]	Inputs only require V_{CCIO} = 2.5 V and V_{REF} = 0.75 V.
LVCMOS18	Outputs require V_{CCIO}= 1.8 V. Inputs require V_{CCIO} = 1.5 V, 1.8 V, 2.5 V, or 3.3 V.
LVCMOS18R33 [2, 3]	Inputs only require V_{CCIO} = 3.3 V and V_{REF} = 0.9 V.
LVCMOS18R25[2, 3]	Inputs only require V_{CCIO} = 2.5 V and V_{REF} = 0.9 V.
LVCMOS25	Outputs require V_{CCIO} = 2.5 V (Other V_{CCIO} voltages are also supported when the OPENDRAIN attribute is selected). Inputs require V_{CCIO} = 1.5 V, 1.8 V, 2.5 V, or 3.3 V.
LVCMOS25R33[2, 3]	Inputs only require V_{CCIO} = 3.3 V and V_{REF} = 1.25 V.
LVCMOS33	Outputs require V_{CCIO} = 3.3 V. Inputs require V_{CCIO} = 1.5 V, 1.8 V, 2.5 V, or 3.3 V.
LVTTL33	Outputs require V_{CCIO} = 3.3 V. Inputs require V_{CCIO} = 1.5 V, 1.8 V, 2.5 V, or 3.3 V.
PCI33	Inputs and outputs both require V_{CCIO}= 3.3 V.

Notes:

1. Certain I/O type and bank V_{CCIO} combinations may cause higher DC current. For more details refer to Table 7.2. Use the Power Calculator to get power estimation for I/O types.
2. The HYSTERESIS option and BUS KEEPER option are not available for these I/O types.
3. Since only one V_{REF} signal can be supported in each I/O bank, only one of these I/O standards can be used in each I/O bank.

Table 7.2. Mixed Voltage Support for LVCMOS and LVTTL I/O Types[8]

V_{CCIO}	Inputs						Outputs					
	1.0 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	1.0 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V
1.2 V	—	Yes	Yes[6]	—	—	—	—	Yes	—	—	—	—
1.5 V	—	Yes[1]	Yes	Yes[6]	Yes[6]	Yes[6]	—	—	Yes	—	—	—
1.8 V	—	Yes[1]	Yes[5]	Yes	Yes[6]	Yes[6]	—	—	—	Yes	—	—
2.5 V	Yes[1, 9]	Yes[1, 10]	Yes[2, 5, 7]	Yes[3, 5, 7]	Yes	Yes[6]	Yes[11]	Yes[11]	—	—	Yes	—
3.3 V	Yes[1, 9]	Yes[1, 10]	Yes[2, 5, 7]	Yes[3, 5, 7]	Yes[4, 5, 7]	Yes	Yes[11]	Yes[11]	—	—	—	Yes

Notes:

1. Leakage occurs if bus hold or weak pull-up is turned on.
2. This input standard can be supported using the ratioed input buffer in under-drive conditions or using the I/O types LVCMOS15R25 or LVCMOS15R33 with the referenced input buffer.
3. This input standard can be supported using the ratioed input buffer in under-drive conditions or using the I/O type LVCMOS18R25 or LVCMOS18R33 with the referenced input buffer.
4. This input standard can be supported using the ratioed input buffer in under-drive conditions or using the I/O type LVCMOS25R33 with the referenced input buffer.
5. Under-drive condition when using the ratioed input buffer and the input standard voltage is below V_{CCIO}
   a. Under-drive causes higher DC current when the IO is at logic high. It is recommended to use Power Calculator to estimate the power consumption under such condition.
   b. Hysteresis is not supported. In the Diamond software, HYSTERESIS must be set to NA.
   c. CLAMP is not supported. In the Diamond software, CLAMP must be set to OFF.
   d. IO termination is not supported. In the Diamond software, PULLMODE must be set to NONE.
6. Over-drive condition when using the ratioed input buffer and the input standard voltage is above V_{CCIO}.
   a. Hysteresis is not supported. In the Diamond software, HYSTERESIS must be set to NA.
   b. CLAMP is not supported. In the Diamond software, CLAMP must be set to OFF.
   c. IO termination is not supported. In the Diamond software, PULLMODE must be set to NONE.
7. Ratioed input buffer in under-drive conditions is preferred over referenced input buffer due to lower power requirement for the ratioed input buffer.
8. When using the ratioed input buffers in under-drive or over-drive conditions, the HYSTERESIS setting shall be NA, the CLAMP setting shall be OFF, and the UP and KEEPER PULLMODE settings are not supported.
9. This input standard can be supported using the I/O types LVCMOS10R25 or LVCMOS10R33 with the referenced input buffer.
10. This input standard can be supported using the ratioed input buffer in under-drive conditions or using the I/O types LVCMOS12R25 or LVCMOS12R33 with the referenced input buffer.
11. This output standard is supported as a Bidirectional open-drain buffer only. IO termination is not supported. In the Diamond software, OPENDRAIN must be set to ON, PULLMODE must be set to NONE, and CLAMP must be set to OFF.

For differential input standards, certain mixed voltage support is allowed in the architecture as shown in Table 7.3.

Table 7.3. Mixed Voltage Support for Differential Input Standards

V_{CCIO}	Differential Inputs					
	LVDS, LVPECL33, MLVDS25, BLVDS25, RSDS25	SSTL25D	SSTD18D, HSTL18D	LVTTL33D, LVCMOS33D	LVCMOS25D, LVCMOS15D, LVCMOS12D	LVCMOS18D
1.2 V	—	—	—	—	—	—
1.5 V	—	—	—	—	—	—
1.8 V	—	—	Yes	—	—	Yes
2.5 V	Yes	Yes	Yes	—	Yes	Yes
3.3 V	Yes	Yes	Yes	Yes	Yes	Yes

7.1. Input Reference Voltage

Each I/O bank supports one reference voltage (V_{REF}). Any I/O in the bank can be configured as the input reference voltage pin. This pin is a regular I/O if it is not used as reference voltage input. To support SSTL and HSTL inputs, the reference voltage is set to half of the V_{CCIO} level. The input reference voltage can also be generated internally from the V_{REF} generator. Again, there is one V_{REF} generator per bank and its programmable settings include OFF, 45% of V_{CCIO}, 50% of V_{CCIO}, and 55% of V_{CCIO}. Programming of the internal V_{REF} generator and the external V_{REF} pin cannot be set at the same time for a particular bank because there is only one V_{REF} bus per bank.

8. sysI/O Buffer Configuration

The MachXO2 devices have three types of general-purpose sysI/O buffer pairs to support a variety of single-ended and differential standards. Each sysI/O buffer pair is made of two PIO buffers. PIO A and B pads form the primary pair, and PIO C and D pads form the alternate pair. Pads A and C of the pair are considered the *true* pad, while pads B and D are considered the *comp* pad. The *true* pad is associated with the positive side of the differential signal, while the *comp* pad is associated with the negative side of the differential signal.

All the PIOs support programmable clamp and bus maintenance circuitry to allow a weak pull-up, a weak pull-down, or a weak bus keeper. The base sysI/O buffer pair is used on all sides of the smaller devices, and on the left and right sides of the MachXO2-640U, MachXO2-1200/U, MachXO2-2000/U, MachXO2-4000, and MachXO2-7000 devices. The LVDS sysI/O buffer pairs have additional LVDS output drivers in the primary PIO pairs. They are used on the top bank of the MachXO2-640U, MachXO2-1200/U, MachXO2-2000/U, MachXO2-4000, and MachXO2- 7000 devices. The bottom sysI/O buffer pairs have additional 100 Ω termination resistors between the *true* and *comp* pads. The bottom sysI/O buffer pairs also support PCI clamp. They are supported on the bottom I/O bank of the MachXO2-640U, MachXO2-1200/U, MachXO2-2000/U, MachXO2-4000, and MachXO2-7000 devices.

8.1. LVCMOS Buffer Configurations

The LVCMOS buffers are built on the base sysI/O buffer pairs. These LVCMOS buffers can be configured in a variety of modes to support common circuit design needs.

8.1.1. Bus Maintenance Circuit

Each pad has a weak pull-up, weak pull-down, and weak bus-keeper capability. These are selected with ON and OFF programmability. The pull-up and pull-down settings offer a fixed characteristic, which is useful in creating wired logic such as wired ORs. The bus-keeper option latches the signal in the last driven state, holding it at a valid level with minimal power dissipation. Input leakage can be minimized by turning off the bus maintenance circuitry. However, it is important to ensure that inputs are driven to a known state to avoid unnecessary power dissipation in the input buffer. The bus maintenance circuit is available for single-ended ratioed I/O standards.

8.1.2. Programmable Drive Strength

All single-ended drivers have programmable drive strength. This option can be set for each I/O independently. The drive strengths available for each I/O standard can be found in Table 9.1. The MachXO2 programmable drive architecture is guaranteed with minimum drive strength for each drive setting. The IBIS models provide details of output driving capability versus the output load. This information, together with the current per bank and the package thermal limit current, should be taken into consideration when selecting the drive strength.

8.1.3. Input Hysteresis

VIH is the trip point for a low-to-high transition and VIL is the trip point for a high-to-low transition, hysteresis voltage is the difference between VIH and VIL. Hysteresis is used to prevent several quick successive changes if the input signal contains some noise. For example, the noise could mean that you cross the trip point more than just once, which causes a glitch in the system.

All ratioed input receivers, except LVCMOS12, support input hysteresis. The input hysteresis for the LVCMOS33, LVCMOS25, LVCMOS18 and LVCMOS15 have two settings for flexibility. The ratioed input receivers have no input hysteresis when they are operated in under-drive or over-drive input conditions as shown in Table 7.1 and Table 7.2.

8.1.4. Programmable Slew Rate

The single-ended output buffer for each device I/O pin has programmable output slew rate control that can be configured for either low noise (SLEWRATE=SLOW) or high speed (SLEWRATE=FAST) performance. Each I/O pin has an individual slew rate control. This slew rate control affects both the rising edge and the falling edges. The rise and fall ramp rates for each I/O standard can be found in the device IBIS file for a given I/O configuration.

8.1.5. Tri-state and Open Drain Control

Each single-ended output driver has a separate tri-state control in addition to the global tri-state control for the device. The single-ended output drivers also support open drain operation on each I/O independently. The open drain output is typically pulled up externally and only the sink current specification is maintained.

8.1.6. PCI Support with PCI Clamp

The bottom sysI/O buffer pair supports an optional PCI clamp diode that may be programmed individually.

This is only supported at the bottom edge of MachXO2-640U, MachXO2-1200/U, MachXO2-2000/U, MachXO2- 4000, and MachXO2-7000 devices. The PCI clamp supports a larger clamping current than the programmable clamp available on all other sides of the devices.

8.1.7. Complementary Outputs

Each sysI/O buffer pair has a built-in complementary circuit that can optionally be driven by the complement of the data that drives the single-ended driver associated with the true pad. This allows a pair of single-ended drivers to be used to drive complementary outputs with the lowest possible skew between the signals.

8.2. Differential Buffer Configurations

The base sysI/O buffer pair supports differential input standards. Its complementary outputs support SSTL and HSTL differential output standards. The top and bottom edges of MachXO2-640U, MachXO2-1200/U, and higher-density devices support some additional functions over those supported by the base sysI/O buffer pairs.

8.2.1. Differential Receivers

All the sysI/O buffer pairs support differential input on all edges of the device. When a sysI/O buffer pair is configured as a differential receiver, the input hysteresis and the bus maintenance capabilities are disabled for the buffer.

8.2.2. On-Chip Input Termination

The MachXO2 device supports on-chip 100 Ω (nominal) input differential termination on the bottom edge of MachXO2-640U, MachXO2-1200/U, MachXO2-2000/U, MachXO2-4000, and MachXO2-7000 devices. The termination is available on all input PIO pairs of the bottom edge and is programmable.

8.2.3. Emulated Differential Outputs

All sysI/O buffer pairs support complementary outputs as described above. This feature can be used to drive complementary SSTL or HSTL signals as required for differential SSTL and HSTL standards. It can also be used together with off-chip resistor networks for emulating the differential output standards such as LVPECL, MLVDS, BLVDS, MIPI and RSDS differential standards. When a sysI/O buffer pair is configured as differential transmitter, the bus maintenance and open drain capabilities are disabled. All single-ended sysI/O buffers pairs in the MachXO2 family can support emulated differential output standards.

8.3. True Differential Output And Output Drive

The MachXO2-640U, MachXO2-1200/U, MachXO2-2000/U, MachXO2-4000, and MachXO2-7000 devices support true differential output drivers on the top edge of these devices. These true differential outputs are only available on the primary PIO pairs. The output driver has a fixed common mode of 1.2 V and a programmable drive current of 1.25 mA, 2.5 mA, 2.0 mA or 3.5 mA. Only one true LVDS differential drive setting is available at a time. All true LVDS differential drivers on the top edge must be programmed to have the same drive strength. The bank V_{CCIO} for true differential output can be 2.5 V or 3.3 V.

9. Software sysIO Attributes

The sysI/O attributes or primitives must be used in the Lattice development software to control the functions and capabilities of the sysI/O buffers. The sysI/O attributes or primitives can be specified in the HDL source code in the Lattice Diamond™ spreadsheet view GUI, or in the ASCII preference file (.lpf) directly. Appendices A, B, and C list examples of using such attributes in different environments. This section describes each of these attributes in detail.

9.1. HDL Attributes

All the attributes discussed in this section, except two, can be used in the HDL source code to direct the sysI/O buffer functionality.

9.1.1. IO_TYPE

This attribute is used to set the sysI/O standard for an I/O. The V_{CCIO} required to set these I/O standards are embedded in the attribute names. The bank V_{CCIO} attribute is used to specify the allowed V_{CCIO} combinations for each I/O type. Table 9.1 shows the valid I/O types for the MachXO2 family.

Table 9.1. Supported I/O Types

sysI/O Signaling Standard	IO_TYPE
LVDS 2.5 V	LVDS25
Emulated LVDS 2.5 V[1]	LVDS25E
RSDS	RSDS25
Emulated RSDS[1]	RSDS25E
Bus LVDS 2.5 V	BLVDS25
Emulated Bus LVDS 2.5 V[1]	BLVDS25E
MLVDS 2.5 V	MLVDS25
Emulated MLVDS 2.5 V[1]	MLVDS25E
LVPECL 3.3 V	LVPECL33
Emulated LVPECL 3.3 V[1]	LVPECL33E
SSTL 25 Class I	SSTL25_I
SSTL 25 Class II[2]	SSTL25_II
SSTL 25 Class I differential[3]	SSTL25D_I
SSTL 25 Class II differential[2, 3]	SSTL25D_II
SSTL 18 Class I	SSTL18_I
SSTL 18 Class II[2]	SSTL18_II
SSTL 18 Class I differential[3]	SSTL18D_I
SSTL 18 Class II differential[2, 3]	SSTL18D_II
HSTL 18 Class I	HSTL18_I
HSTL 18 Class II[2]	HSTL18_II
HSTL 18 Class I differential[3]	HSTL18D_I
HSTL 18 Class II differential[2,3]	HSTL18D_II
PCI 3.3 V	PCI33
LVTTL 3.3 V	LVTTL33
LVTTL 3.3 V differential[3]	LVTTL33D
LVCMOS 3.3 V	LVCMOS33
LVCMOS 3.3 V differential[3]	LVCMOS33D
LVCMOS 2.5 V (default)	LVCMOS25
LVCMOS 2.5 V differential[3]	LVCMOS25D
LVCMOS 2.5 V in a 3.3 V V_{CCIO} bank[4]	LVCMOS25R33
LVCMOS 1.8 V	LVCMOS18
LVCMOS 1.8 V differential[3]	LVCMOS18D

sysI/O Signaling Standard	IO_TYPE
LVCMOS 1.8 V in 3.3 V V_{CCIO} bank[4]	LVCMOS18R33
LVCMOS 1.8 V in 2.5 V V_{CCIO} bank[4]	LVCMOS18R25
LVCMOS 1.5 V	LVCMOS15
LVCMOS 1.5 V differential[3]	LVCMOS15D
LVCMOS 1.5 V in 3.3 V V_{CCIO} bank[4]	LVCMOS15R33
LVCMOS 1.5 V in 2.5 V V_{CCIO} bank[4]	LVCMOS15R25
LVCMOS 1.2 V	LVCMOS12
LVCMOS 1.2 V differential[3]	LVCMOS12D
LVCMOS 1.2 V in 3.3 V V_{CCIO} bank[5]	LVCMOS12R33
LVCMOS 1.2 V in 2.5 V V_{CCIO} bank[5]	LVCMOS12R25
LVCMOS 1.0 V in 3.3 V V_{CCIO} bank[5]	LVCMOS10R33
LVCMOS 1.0 V in 2.5 V V_{CCIO} bank[5]	LVCMOS10R25
MIPI	MIPI

Notes:

1. These differential output standards are emulated by using a complementary LVCMOS driver pair together with an external resistor pack.
2. Only input mode is supported. Output or bidirectional modes are not supported for these I/O types.
3. These differential standards are implemented by using a complementary LVCMOS driver pair.
4. These are input only and require V_{REF} to be set to certain value to allow the specified I/O types to be used.
5. These are input or bidirectional only and require V_{REF} to be set to certain value to allow the specified I/O types to be used.

9.1.2. DRIVE

The DRIVE strength attribute is available for the output and bidirectional I/O standards. The default drive value depends on the I/O standard used. Table 9.2. shows the supported drive strength for the single-ended I/O types under the designated V_{CCIO} conditions.

Table 9.2. Output Drive Capability for Ratioed sysI/O Standards

Drive Strength (mA)	I/O Type					
	LVCMOS12	LVCMOS15	LVCMOS18	LVCMOS25	LVCMOS33	LVTTL33
2	YES	—	—	—	—	—
4	—	YES	YES	YES	YES	YES
6	YES	—	—	—	—	—
8[1]	—	YES	YES	YES	YES	YES
12	—	—	YES	YES	YES	YES
16	—	—	—	YES	YES	YES
24	—	—	—	—	YES	YES

Note: Hardware Default (Erased) setting

9.1.3. DIFFDRIVE

The DIFFDRIVE strength attribute is available for true LVDS output standard. All true LVDS differential drivers on the top edge must be programmed to have the same drive strength. The DIFFDRIVE value is listed in the DRIVE column of the Design Planner since this value is only valid for LVDS25 outputs.

Values: 1.25, 2.0, 2.5, 3.5, NA

Software Default: 3.5

Hardware Default (Erased): NA

9.1.4. PULLMODE

The PULLMODE option can be enabled or disabled independently for each I/O. When the user selects OPENDRAIN= ON, the PULLMODE for the output standard is default to NONE. If using the LVCMOS I/O type in an under-drive or over-drive mode, the UP and KEEPER settings are not supported. The FAILSAFE option is available only for MLVDS25E bi-directional mode.

Values: UP, DOWN, NONE, KEEPER, FAILSAFE

Software Default: DOWN for LVTTL, LVCMOS, and PCI; all others NONE

Hardware Default (Erased): Down

9.1.5. CLAMP

The CLAMP option can be enabled or disabled independently for each I/O. The available settings on the bottom edge of MachXO2-640U, MachXO2-1200/U, MachXO2-2000/U, MachXO2-4000, and MachXO2-7000 devices is PCI or OFF. All other I/O have ON or OFF settings for this attribute.

Values: OFF, ON, PCI

Default value of CLAMP for OUTPUT: OFF

Default value of CLAMP for INPUT: ON if V_{CCIO} is same or higher as I/O standard

Default value of CLAMP for INPUT: OFF if V_{CCIO} is less than I/O standard

When the CLAMP DIODE is ON, careful design consideration must be followed. For more information see Appendix D.

9.1.6. HYSTERESIS

The ratioed input buffers have two input hysteresis settings. The HYSTERESIS option can be used to change the amount of hysteresis for the LVTTL and LVCMOS input and bidirectional I/O standards, except for the LVCMOS12 inputs. The LVCMOS12 inputs do not support HYSTERESIS.

The LVCMOS25R33, LVCMOS18R25, LVCMOS18R33, LVCMOS15R25, LVCMOS15R33, LVCMOS12R33, LVCMOS12R25, LVCMOS10R33, and LVCMOS10R25 input types do not support HYSTERESIS. The HYSTERESIS option for each of the input pins can be set independently when it is supported for the I/O type.

Values: SMALL, LARGE, NA

Software Default: SMALL

Hardware Default (Erased): with very small hysteresis (0 to 60 mV)

9.1.7. V_{REF}

The V_{REF} option is enabled for single-ended SSTL and HSTL inputs and the referenced LVMCOS input buffers. The referenced LVMCOS input buffers are specified by choosing the I/O type as LVCMOS25R33, LVCMOS18R25, LVCMOS18R33, LVCMOS15R25, LVCMOS15R33, LVCMOS12R33, LVCMOS12R25, LVCMOS10R33, or LVCMOS10R25. The default value of NA applies for all I/O types that do not use a V_{REF} signal.

The V_{REF} defaults to external V_{REF} pin for the single-ended SSTL/HSTL inputs, LVCMOS25R33, LVCMOS18R25, LVCMOS18R33, LVCMOS15R25, LVCMOS15R33, LVCMOS12R33, LVCMOS12R25, LVCMOS10R33, or LVCMOS10R25 inputs. The user may enter a VREF_NAME value in the *V_{REF} Location* pop-up window of the spreadsheet view of the Lattice Diamond software. In doing so, the software presents the VREF_NAME as an available value in addition to the I45, I50 and I55 values in the V_{REF} column of the Port Assignments tab of the Lattice Diamond Spreadsheet View. A pin location specified by the VREF_NAME value is used as the V_{REF} driver for that I/O bank. VREF_NAME is only necessary if the user wants to specify a pin to be used as an external V_{REF} pin. Otherwise, the software automatically assigns a pin for the V_{REF} signal. There is only one V_{REF} pin or internal V_{REF} driver per I/O bank. Only one of the V_{REF} driver settings chosen from I45, I50, I55 or VREF1_LOAD can be used in each I/O bank. This attribute can be set in the software GUI or in the ASCII preference file.

Values: OFF, I45, I50, I55, VREF_NAME

Software Default: NA

Hardware Default (Erased): OFF

9.1.8. OPENDRAIN

The OPENDRAIN option is available for all LVTTL and LVCMOS output and bidirectional I/O standards. Each sysI/O can be assigned independently to be open drain. When the OPENDRAIN attribute is used, the PULLMODE must be NONE and the CLAMP must be OFF.

Values: OFF, ON

Software Default: OFF

Hardware Default (Erased): OFF

9.1.9. SLEWRATE

Each I/O pin has an individual slew rate control. This allows the designer to specify slew rate control on a pin-by-pin basis for outputs and bidirectional I/O pins. This is not a valid attribute for inputs or true differential outputs.

Values: FAST, SLOW, NA

Software Default: SLOW

Hardware Default (Erased): SLOW

9.1.10. DIFFRESISTOR

The bottom side I/O pins support on-chip differential input termination resistors on the MachXO2-640U, MachXO2-1200/U, MachXO2-2000/U, MachXO2-4000, and MachXO2-7000 devices. The termination resistor is available for both the primary pair and the alternate pair of a sysI/O. The values supported are zero (OFF) or 100 Ω.

Values: OFF, 100

Software Default: OFF

Hardware Default (Erased): OFF

9.1.11. DIN/DOUT

The DIN/DOUT option is available for each I/O and can be configured independently. An input register is used for the input if the DIN attribute is assigned. Similarly, the software assigns an output register when the DOUT attribute is specified. By default, the software automatically assigns DIN or DOUT to input or output registers if possible.

9.1.12. LOC

This attribute specifies the site location for the component after the mapping process. When attached to multiple components, it indicates that these blocks are to be mapped together in the specified site. It specifies the PIC site for the pad when it is assigned to a pad. The LOC attribute can be attached to components that end up on an I/O cell, clocks, and internal flip-flops, but it should not be attached to a combinational logic that ends up on a logic cell; doing so could fail to generate a locate preference. The LOC attribute overrides register ordering.

9.1.13. Bank V_{CCIO}

This attribute is necessary to verify the valid I/O types for a bank, to determine which input buffer to use, and to set the correct drive strength for the applicable I/O types. Since the I/O bank information is not required at the HDL level, this attribute is available through either the Lattice Diamond software Spreadsheet View or in the ASCII preference file. Values: AUTO, 3.3, 2.5, 1.8, 1.5, 1.2. Software Default: AUTO.

9.2. sysI/O Primitives

There are many sysI/O primitives in the software library. A few are selected to be discussed in this section because some sysI/O capabilities can only be utilized through instantiating the primitives in the HDL source code.

9.2.1. Tri-State All (TSALL)

The MachXO2 device supports the TSALL function that is used to enable or disable the tristate control to all the output buffers. The user can choose to assign any general purpose I/O pin to control the TSALL function since there is no dedicated TSALL pin. The TSALL primitive must be instantiated in the source code in order to enable the TSALL function. The input of the primitive can be assigned to an input pin or to an internal signal.

The value of TSALL=1 can tri-state all outputs but the outputs are under individual OE control when TSALL=0.

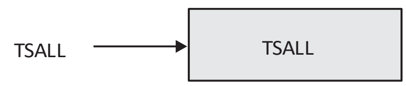


Figure 9.1. TSALL Primitive

9.2.2. Fixed Data Delay (DELAYE)

This primitive supports up to 32 steps of static delay for all sysI/O buffers in all banks of a MachXO2 device. Refer to the Dynamic Data Delay (DELAYD) section for the delay step values. Although users can choose USER_DEFINED mode to set input delay, this primitive is primarily used by pre-defined source synchronous interfaces as described in the Implementing High-Speed Interfaces with MachXO2 Devices (FPGA-TN-02153).

Figure 9.2. DELAYE Primitive and Associated Attributes

Table 9.3.Output Drive Capability for Ratioed sysI/O Standards

Attribute	Description	Value	Software Default
DEL_MODE	Fixed delay value depending on interface or user-defined delay values	SCLK_ZEROHOLD ECLK_ALIGNED ECLK_CENTERED SCLK_ALIGNED SCLK_CENTERED USER_DEFINED	USER_DEFINED
DEL_VALUE	User-defined value	DELAY0…DELAY31	DELAY0

9.2.3. Dynamic Data Delay (DELAYD)

This primitive supports dynamic delay for the sysI/O buffers in the bottom bank (Bank 2) of the MachXO2-640U, MachXO2-1200/U, and larger devices. The 5-bit inputs can be controlled by user logic to modify the delay during the device operation. The delay step for each DELAY varies based on the device used. For example (for HC/HE devices), DELAY1 = 50 ps, DELAY5 = 250 ps.

	HC/HE	ZE
DELAY	50 ps	100 ps

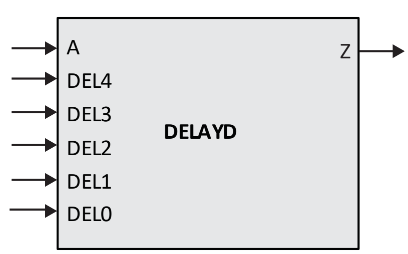


Figure 9.3. DELAYD Primitive

10. Design Consideration and Usage

This section summarizes the MachXO2 design rules and considerations that have been discussed in detail in the previous sections. Table 7.2 lists the miscellaneous I/O features on each side of a MachXO2 device.

10.1. sysI/O Buffer Features Common to All MachXO2 Devices

- All banks support true differential inputs.
- All banks support emulated differential outputs using external resistors and complementary LVCMOS outputs. Emulated differential output buffers are supported on both primary and alternate pairs.
- All banks have programmable I/O clamps but they are not PCI compliant clamps.
- All banks support weak pull-up, pull-down, and bus-keeper (bus hold latch) settings on each I/O independently.
- VCCIO voltage levels, together with the selected I/O types, determine the characteristics of an I/O, such as the pull mode, hysteresis, clamp behavior, and drive strength, supported in a bank. Multiple input standards can be supported in a bank through under-drive or over-drive conditions. Only one alternative input standard can be supported through the bank VREF setting (for example, LVCMOS25R33 requires VREF to be 1.25 V in a 3.3 V VCCIO bank). Each bank also supports 1.2 V inputs regardless of the VCCIO setting of the bank.
- Each bank supports one VCCIO signal.
- Each bank supports one VREF signal, whether it is from an external pin or from the internal VREF generator.

10.2. sysI/O Buffer Rules Specific to MachXO2-256 and MachXO2-640 Devices

- Does not support true differential output buffers.
- Does not support internal 100 Ω differential input terminations.
- Does not support PCI clamps.

10.3. sysI/O Buffer Rules Specific to MachXO2-640U, MachXO2-1200/U, MachXO2-2000/U, MachXO2-4000, and MachXO2-7000 Devices

- Only Bank 0 (top side) supports true differential output buffers with programmable drive strengths. Only the primary pair supports true differential output buffers.
- Only Bank 2 (bottom side) supports internal 100 Ω differential input terminations.
- Only Bank 2 (bottom side) supports PCI compliant clamps.

Table 10.1. Miscellaneous I/O Features on Each Device Edge

Feature	Top	Bottom	Left	Right
100 Ω Differential Resister	—	Yes[1]	—	—
Hot Socket	Yes	Yes	Yes	Yes
Clamp[3]	Yes	Yes	Yes	Yes
PCI Compliant Clamp	—	Yes[1]	—	—
Weak Pull-up[3]	Yes	Yes	Yes	Yes
Weak Pull-down[2]	Yes	Yes	Yes	Yes
Bus Keeper[3]	Yes	Yes	Yes	Yes
Input Hysteresis[3]	Yes	Yes	Yes	Yes
Slew Rate Control	Yes	Yes	Yes	Yes
Open Drain	Yes	Yes	Yes	Yes

Notes:

1. Supported by MachXO2-640U, MachXO2-1200/U, MachXO2-2000/U, MachXO2-4000, and MachXO2-7000 devices.
2. Software default setting.
3. I/O characteristic under special conditions.
    - HYSTERESIS option is not available for LVCMOS12.
    - HYSTERESIS option and BUS KEEPER option are not available for referenced input standards.
    - When using the ratioed input buffers in under-drive or over-drive conditions, the HYSTERESIS setting shall be NA. The CLAMP setting shall be OFF. The UP and KEEPER PULLMODE settings are not supported.
    - HYSTERESIS and the bus maintenance capabilities are disabled for differential receivers.

Appendix A. sysI/O HDL Attributes

The sysI/O attributes can be used directly in the HDL source codes. This section provides a list of sysI/O attributes supported by the MachXO2 PLD family. The correct syntax and examples for the Synplify® synthesis tool are provided here for reference.

A.1. Attributes in VHDL Language

This section lists syntax and examples for the sysI/O attributes in VHDL.

Syntax

Table A.1. VHDL Attribute Syntax

Attribute	Syntax
IO_TYPE	attribute IO_TYPE: string; attribute IO_TYPE of Pinname: signal is “IO_TYPE Value”;
DRIVE	attribute DRIVE: string; attribute DRIVE of Pinname: signal is “Drive Value”;
DIFFDRIVE	attribute DRIVE: string; attribute DRIVE of Pinname: signal is “Diffdrive Value”;
DIFFRESISTOR	attribute DIFFRESISTOR: string; attribute DIFFRESISTOR of Pinname: signal is “DIFFRESISTOR Value”;
CLAMP	attribute CLAMP: string; attribute CLAMP of Pinname: signal is “Clamp Value”;
HYSTERESIS	attribute HYSTERESIS: string; attribute HYSTERESIS OF Pinname: signal is “Hysteresis Value”;
V_{REF}	NA
PULLMODE	attribute PULLMODE: string; attribute PULLMODE of Pinname: signal is “Pullmode Value”;
OPENDRAIN	attribute OPENDRAIN: string; attribute OPENDRAIN of Pinname: signal is “OpenDrain Value”;
SLOWSLEW	attribute PULLMODE: string; attribute PULLMODE of Pinname: signal is “Slewrate Value”;
DIN	attribute DIN: string; attribute DIN of Pinname: signal is “value “;
DOUT	attribute DOUT: string; attribute DOUT of Pinname: signal is “value “;
LOC	attribute LOC: string; attribute LOC of Pinname: signal is “Pin locations”;
BANK V_{CCIO}	NA

Examples

IO_TYPE

```
--***Attribute Declaration***
ATTRIBUTE IO_TYPE: string;
--***IO_TYPE assignment for I/O Pin***
ATTRIBUTE IO_TYPE OF portA: SIGNAL IS "PCI33";
ATTRIBUTE IO_TYPE OF portB: SIGNAL IS "LVCMOS33";
ATTRIBUTE IO_TYPE OF portC: SIGNAL IS "SSTL18_I";
ATTRIBUTE IO_TYPE OF portD: SIGNAL IS "LVDS25";
```

DRIVE

```
--***Attribute Declaration***
ATTRIBUTE DRIVE: string;
--***DRIVE assignment for I/O Pin***
ATTRIBUTE DRIVE OF portB: SIGNAL IS “8”;
```

DIFFDRIVE

```
--***Attribute Declaration***
ATTRIBUTE DIFFDRIVE: string;
--*** DIFFDRIVE assignment for I/O Pin***
ATTRIBUTE DIFFDRIVE OF portD: SIGNAL IS “2.0”;
```

DIFFRESISTOR

```
--***Attribute Declaration***
ATTRIBUTE DIFFRESISTOR: string;
--*** DIFFRESISTOR assignment for I/O Pin***
ATTRIBUTE DIFFRESISTOR OF portD: SIGNAL IS "100";
```

CLAMP

```
--***Attribute Declaration***
ATTRIBUTE CLAMP: string;
--*** CLAMP assignment for I/O Pin***
ATTRIBUTE CLAMP OF portA: SIGNAL IS “PCI33”;
```

HYSTERESIS

```
--***Attribute Declaration***
ATTRIBUTE HYSTERESIS: string;
--*** HYSTERESIS assignment for Input Pin***
ATTRIBUTE HYSTERESIS OF portA: SIGNAL IS " LARGE ";
```

PULLMODE

```
--***Attribute Declaration***
ATTRIBUTE PULLMODE : string;
--***PULLMODE assignment for I/O Pin***
ATTRIBUTE PULLMODE OF portA: SIGNAL IS “DOWN”;
ATTRIBUTE PULLMODE OF portB: SIGNAL IS “UP”;
```

OPENDRAIN

```
--***Attribute Declaration***
ATTRIBUTE OPENDRAIN: string;
--***Open Drain assignment for I/O Pin***
ATTRIBUTE OPENDRAIN OF portB: SIGNAL IS “ON”;
```

SLEWRATE

```
--***Attribute Declaration***
ATTRIBUTE SLEWRATE : string;
--*** SLEWRATE assignment for I/O Pin***
ATTRIBUTE SLEWRATE OF portB: SIGNAL IS “FAST”;
```

DIN/DOUT

```
--***Attribute Declaration***
ATTRIBUTE din : string; ATTRIBUTE dout : string;
--*** din/dout assignment for I/O Pin***
ATTRIBUTE din OF input_vector: SIGNAL IS “TRUE “;
ATTRIBUTE dout OF output_vector: SIGNAL IS “TRUE “;
```

LOC

```
--***Attribute Declaration***
ATTRIBUTE LOC : string;
--*** LOC assignment for I/O Pin***
ATTRIBUTE LOC OF input_vector: SIGNAL IS “E3,B3,C3 “;
```

A.2. Attributes in Verilog Language

This section lists syntax and examples for the sysI/O attributes in Verilog.

Syntax

Table A.2. Verilog Attribute Syntax

Attribute	Syntax
IO_TYPE	PinType PinName /* synthesis IO_Type=”IO_Type Value”*/;
DRIVE	PinType PinName /* synthesis DRIVE=”Drive Value”*/;
DIFFDRIVE	PinType PinName /* synthesis DIFFDRIVE =” DIFFDRIVE Value”*/;
DIFFRESISTOR	PinType PinName /* synthesis DIFFRESISTOR =” DIFFRESISTOR Value”*/;
CLAMP	PinType PinName /* synthesis CLAMP =” Clamp Value”*/;
HYSTERESIS	PinType PinName /*synthesis HYSTERESIS = “Hysteresis Value” */;
V_{REF}	N/A
PULLMODE	PinType PinName /* synthesis PULLMODE=”Pullmode Value”*/;
OPENDRAIN	PinType PinName /* synthesis OPENDRAIN =”OpenDrain Value”*/;
SLOWSLEW	PinType PinName /* synthesis SLEWRATE=”Slewrate Value”*/;
DIN	PinType PinName /* synthesis DIN= “value” */;
DOUT	PinType PinName /* synthesis DOUT= “value” */;
LOC	PinType PinName /* synthesis LOC=”pin_locations “*/;
Bank V_{CCIO}	N/A

Examples

//IO_TYPE, PULLMODE, SLEWRATE and DRIVE assignment

```
output portB /*synthesis IO_TYPE=”LVCMOS33”
PULLMODE =”UP” SLEWRATE =”FAST” DRIVE =”20”*/;
output portC /*synthesis IO_TYPE=”LVDS25” */;
```

//DIFFDRIVE

```
output portD /* synthesis IO_TYPE="LVDS25" DIFFDRIVE="2.0"*/;
```

//DIFFRESISTOR

```
output [4:0] portA /* synthesis IO_TYPE="LVDS25" DIFFRESISTOR ="100"*/;
```

//CLAMP

```
output portA /*synthesis IO_TYPE=”PCI33” CLAMP =”PCI” */;
```

//HYSTERESIS

```
input mypin /* synthesis HYSTERESIS = “LARGE” */;
```

//OPENDRAIN

```
output portA /*synthesis OPENDRAIN =”ON”*/;
```

// DIN Place the flip-flops near the load input

```
input load /* synthesis din=”” TRUE */;
```

// DOUT Place the flip-flops near the outload output

```
output outload /* synthesis dout=”TRUE” */;
```

//LOC pin location

```
input [3:0] DATA0 /* synthesis loc=”E3,B1,F3”*/;
```

//LOC Register pin location

```
reg data_in_ch1_buf_reg3 /* synthesis loc=”R10C16” */;
```

//LOC Vectored internal bus

```
reg [3:0] data_in_ch1_reg /*synthesis loc =”R10C16,R10C15,R10C14,R10C9” */;
```

Appendix B. sysI/O Attributes Using the Spreadsheet View

The sysI/O buffer attributes can be assigned using the **Spreadsheet View** available in the Lattice Diamond design tool. The attributes that are not available as HDL attributes, such as V_{REF} and Bank V_{CCIO}, are available in the Spreadsheet View GUI.

The **Port Assignment** tab lists all the ports in a design and all the available sysI/O attributes as preferences. Click on each of these cells for a list of all the valid I/O preferences for that port. Each column takes precedence over the next. Therefore, when a particular **IO_TYPE** is chosen, the columns for the **DRIVE**, **PULLMODE**, **SLEWRATE** and other attributes list the valid combinations for that IO_TYPE. Pin locations can be locked using the Pin column of the **Port Assignment** tab. Right-clicking on a cell lists all the available pin locations. The **Spreadsheet View** can run a DRC check to check for incorrect sysI/O attribute assignments.

All the preferences assigned using the **Spreadsheet View** are written into the logical preference file (.lpf).

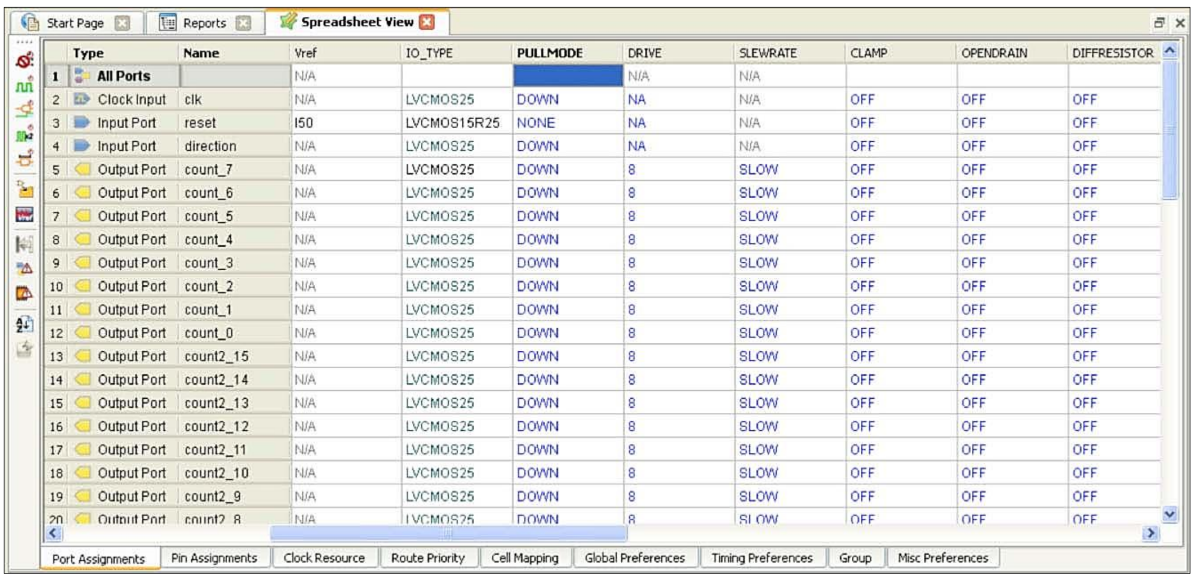


Figure B.1. Port Assignment Tab of Spreadsheet View

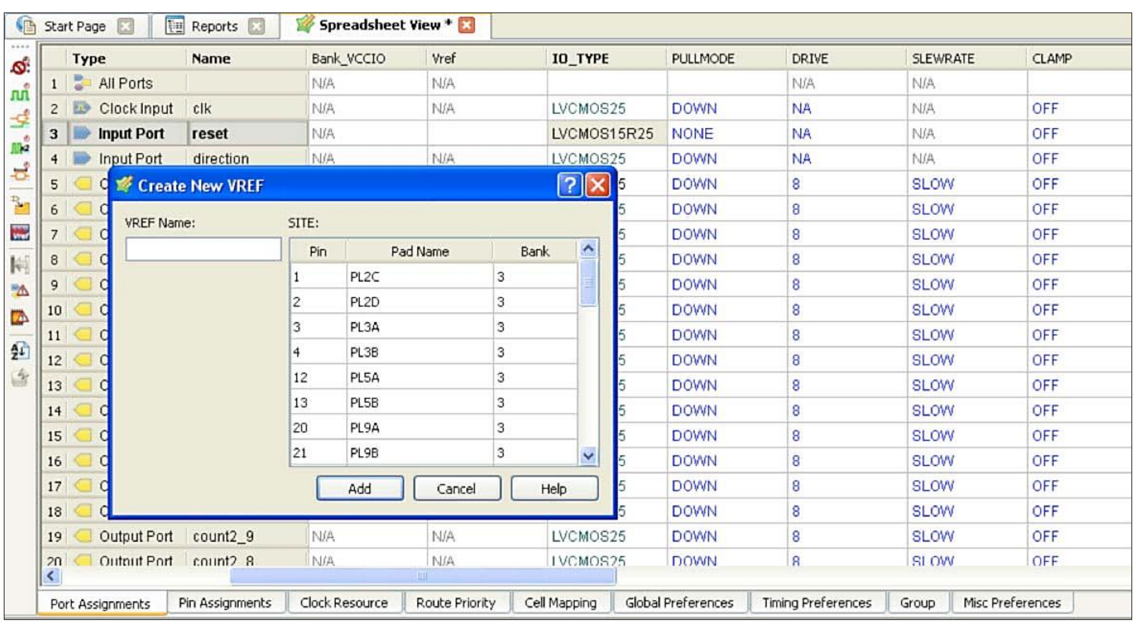


Figure B.2. V_{REF} Name and Location Pop-up Window of the Spreadsheet View

B.1. V_{REF} Assignment in the Spreadsheet View

The V_{REF} attribute can be assigned in the **Spreadsheet View** by clicking on the V_{REF} Location button on the left hand side. It is required to use this button only if a specific location for the V_{REF} driver is desired. Otherwise, the software assigns the V_{REF} driver signal to any location that does not violate the sysI/O bank rules. When the VREF_NAME is assigned to a specific pin, the software lists VREF_NAME in the V_{REF} column of the **Port Assignments** tab. Both VREF_NAME and pin location are reflected in the V_{REF} column of the Pin Attribute sheet.

B.2. Bank V_{CCIO} Setting in the Spreadsheet View

Bank V_{CCIO} is editable in the **Global Preference** tab of the **Spreadsheet View**. The value of the Bank V_{CCIO} can be chosen by the users to determine the value of V_{CCIO} of a specific bank.

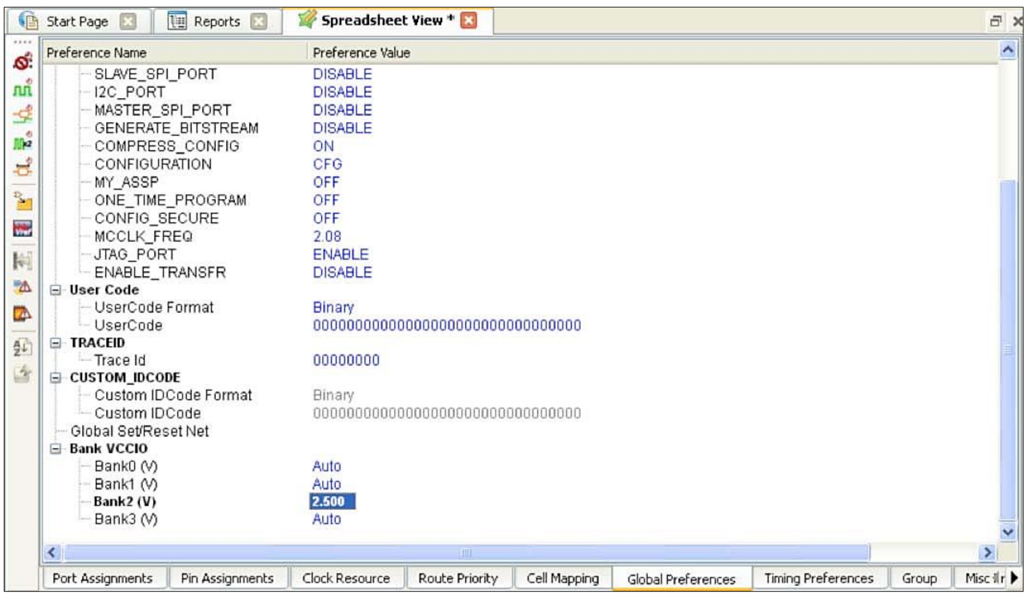


Figure B.3. Bank V_{CCIO} in Global Preference Tab

Appendix C. sysI/O Attributes Using Preference File (ASCII File)

You can enter sysI/O attributes directly in the preference (.lpf) file as sysI/O buffer preferences. The LPF file is a post-synthesis FPGA constraint file that stores logical preferences that have been created or modified in the Spreadsheet View or directly in a text editor. It also contains logical preferences originating in the HDL source. Modifying the Spreadsheet View in the Lattice Diamond software can automatically update the content of the LPF file and vice versa. The settings in the Spreadsheet View are reflected in the preference file once they are saved. Details of the supported preferences and their corresponding syntax can be found in the Lattice Diamond Help System.

Appendix D. Issue: GPIO Input Prevents Powering Down the FPGA

For ZC/HC devices where the design involves V_{CC} and bank V_{CCIOx} voltages that are the same, either 3.3 V or 2.5 V, and they are connected together, careful design consideration must be followed. This is to avoid the FPGA not fully powering down and operating in an undefined state.

Note: Chip failures can occur when the datasheet input current limits are exceeded.

D.1. GPIO Input Current Leakage Pathway

The FPGA is powered on, with the bitstream program input CLAMPs on.
While the FPGA powers down, the external circuit continues to drive input pins.
As the FPGA V_{CC} and V_{CCIOx} voltage drops, the GPIO input pins allow external devices to drive reverse current into the FPGA through the on-CLAMPs ,and this current appears at the V_{CCIOx} pins which are connected to V_{CC} and keeping the V_{CC} voltage high enough for the input CLAMPs to remain active.

Other devices besides the FPGA, can be connected to the V_{CC} rail, with each device drawing current from the FPGA. As a result, the FPGA can pass enough reverse current to cause internal burnouts or failures to occur quickly or gradually, depending on the overcurrent of each pin and the number of pins involved.

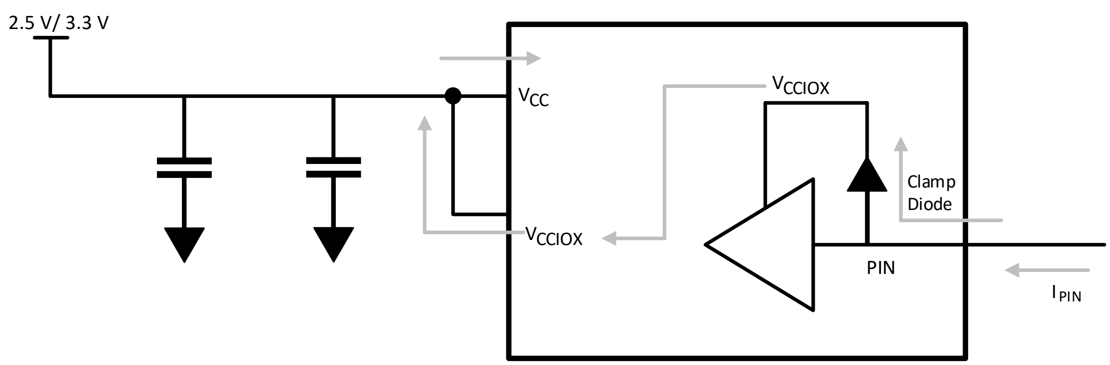


Figure D.1. Potential Current Path for Powered Down FPGA with Driven Input

D.2. Workarounds

Workaround 1
Turn off any external devices connected to the FPGA that are operating ≥ 2.5 V at the same time as FPGA.

Workaround 2
Configure the Lattice Diamond software to keep GPIO CLAMPs OFF in the bitstream when CLAMPs are not required.

Workaround 3

- Ensure that external circuits do not exceed the datasheet I/O pad current limits for banks operating at 2.5 V or higher.
- In each bank, the current should not exceed n × 8 mA. Where n represents the number of I/O pads in between two consecutive power pins. See below scenarios.
    - V_{CCIO} – I/O_1 – I/O_2 – I/O_x – V_{CCIO}
    - GND – I/O_1 – I/O_2 – I/O_x – GND
    - V_{CCIO} – I/O_1 – I/O_2 – I/O_x – GND
- The I/O groupings can be found in the pin tables generated by the Lattice Diamond software.

Example: Limit the pin current by connecting a series resistor to an FPGA GPIO input.

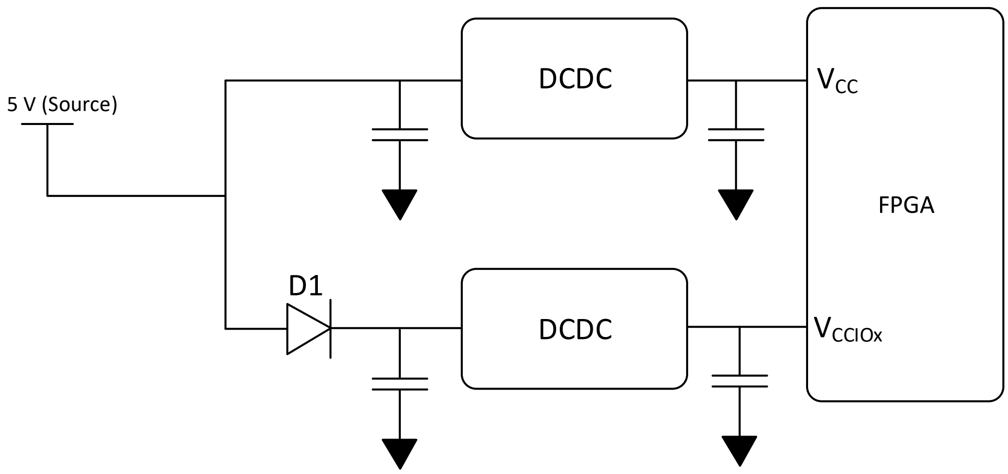
Most non-high-speed designs work well with a 200 Ω to 1 kΩ series resistor.

$$Math: R \times C \times 2\,Tau = Trise\,/\,Tfall$$

$$200\,\Omega\ series\ resistor\ at\ GPIO\ input \times 10\,pF\ etch\ and\ pin\ capacitance \times 2\,Tau = 4ns\ Trise\,/\,Tfall$$

Workaround 4

For V_{CCIO}, use a separate voltage regulator with a diode (D1) connecting the voltage source to the input.



References

- MachXO2 web page
- Implementing High-Speed Interfaces with MachXO2 Devices (FPGA-TN-02153)
- Designing for Migration from MachXO2-1200-R1 to Standard (Non-R1) Devices (FPGA-AN-02012)
- Lattice Diamond FPGA design software
- Lattice Insights for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/en/Support/AnswerDatabase.

Revision History

Revision 2.4, March 2026

Section	Change Summary
All	• Updated the document title to *MachXO2 sysI/O User Guide*. • Minor editorial fixes.
Disclaimer	Updated section contents.
Abbreviation in This Document	Added this section.
sysI/O Banking Scheme	Added a write-up to emphasize the need for careful design consideration when the CLAMP DIODE is ON. Added reference to Appendix D for detailed guidelines.
Software sysIO Attributes	Added a write-up to emphasize the need for careful design consideration when the CLAMP DIODE is ON. Added reference to Appendix D for detailed guidelines under the HDL Attribute – CLAMP section.
Appendix D. Issue: GPIO Input Prevents Powering Down the FPGA	Added this section.
References	Added this section.

Revision 2.3, December 2022

Section	Change Summary
Disclaimers	Updated this section.
sysI/O Buffer Overview	Updated the Bank Restrictions for the LVCMOS25 I/O Type In Table 7.1. V_{CCIO} for Same Bank LVCMOS/LVTTL Input/Output Requirements[1].
Technical Support Assistance	Updated this section.

Revision 2.2, November 2019

Section	Change Summary
All	• Changed document number from TN1202 to FPGA-TN-02158. • Updated document template.
Disclaimers	Added this section.

Revision 2.1, September 2016

Section	Change Summary
VCCIO Requirement for I/O Standards	• Updated Table 7.1., V_{CCIO} for Same Bank LVCMOS/LVTTL Input/Output Requirements. • Updated Table 7.2., Mixed Voltage Support for LVCMOS and LVTTL I/O Types.
sysI/O Buffer Configuration	Under Programmable Drive Strength, the reference to V/I curves in the data was changed to IBIS models.
Software sysI/O Attributes	• Added standards and footnote to Table 9.1., Supported I/O Types. • Modified CLAMP values. • Under Fixed Data Delay (DELAYE), the reference to DS1035, MachXO2 Family Data Sheet was changed to Dynamic Data Delay section.
HYSTERESIS	Updated this section. Added I/O types.
VREF	Updated this section. Added I/O types.
Dynamic Data Delay (DELAYD)	Updated this section. Modified description and added table to represent data.

Revision 2.0, April 2015

Section	Change Summary
Supported sysI/O Standards	Updated this section to add MIPI information • Supported sysI/O Standards. Updated Table 3.1., Supported Input Standards and Table 3.2., Supported Output Standards.
sysI/O Standards Supported by I/O Banks	Updated this section to add MIPI information • sysI/O Standards Supported by I/O Banks. Updated Table 5.2., Differential I/O Standards Supported on Various Sides
Software sysI/O Attributes	Updated this section to add MIPI information • Software sysI/O Attributes. Updated Table 9.1., Supported I/O Types.
Input Hysteresis	Updated this section. Added information.
Emulated Differential Outputs	Updated this section. Added MIPI to examples of output standards.
Technical Support Assistance	Updated this section.

Revision 1.9, August 2014

Section	Change Summary
VCCIO Requirement for I/O Standards	Updated Table 7.2., Mixed Voltage Support for LVCMOS and LVTTL I/O Types. Revised data on V_{CCIO} 1.2 V.

Revision 1.8, July 2014

Section	Change Summary
HDL Attributes	Updated this section. Indicated Software Default and Hardware Default (Erased) settings.
Software sysI/O Attributes	Updated Table 9.2., Output Drive Capability for Ratioed sysI/O Standards. Added note.

Revision 1.7, October 2013

Section	Change Summary
Software sysI/O Attributes	Changed I/O_TYPE to IO_TYPE.

Revision 1.6, August 2013

Section	Change Summary
VCCIO Requirement for I/O Standards	Updated Mixed Voltage Support for LVCMOS and LVTTL I/O Types table.
Technical Support Assistance	Updated Technical Support Assistance information.

Revision 1.5, March 2013

Section	Change Summary
VCCIO Requirement for I/O Standards	Updated footnotes in the Mixed Voltage Support for LVCMOS and LVTTL I/O Types table.
sysI/O Buffer Configuration	Added information on LVCMOS Buffer Configurations – Programmable Slew Rate.

Revision 1.4, February 2012

Section	Change Summary
All	• Updated document with new corporate logo • Document status changed from Preliminary to Final.

Revision 1.3, July 2011

Section	Change Summary
sysI/O Banking Scheme	Updated sysI/O Banking Scheme text section with information on migrating from MachXO2-1200-R1 to Standard (non-R1) devices.

Revision 1.2, April 2011

Section	Change Summary
All	Updated for Lattice Diamond design software.

Revision 1.1, January 2011

Section	Change Summary
All	Updated for ultra-high I/O ("U") devices.

Revision 1.0, November 2010

Section	Change Summary
All	Initial release.

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