LOW COST BOARD LAYOUT TECHNIQUES FOR DESIGNING WITH PLDS IN BGA PACKAGES

A Lattice Semiconductor White Paper

July 2010

Lattice Semiconductor
5555 Northeast Moore Ct.
Hillsboro, Oregon 97124 USA
Telephone: (503) 268-8000
www.latticesemi.com

Overview of BGA Packages

The need to respond to changing market standards and compressed time to market windows has led to the widespread use of programmable logic devices (PLDs) in board and system design. PLDs offer inherent time-to-market and design flexibility advantages over application specific integrated circuits (ASICs) and application specific standard products (ASSPs). In many product categories, such as handheld devices, PLDs have found acceptance due to new product architectures that reduce power consumption, new packaging options and lower unit cost. Typical PLD applications include power up sequencing, voltage level translation, timing control, interface bridging, I/O expansion and discrete logic functions.

The increasing complexity of system requirements has driven the need to increase the logic density and I/O pins of PLDs. As a result, the Ball Grid Array (BGA) has become the package of choice for PLDs. BGA options such as chip scale BGA, fine pitch BGA and chip array BGA have largely replaced most quad flat package (QFP) options on most PLDs. BGAs are popular with system designers primarily due to their higher I/O density, which substantially improves the ratio between pin count and board area. BGA packages are also ideal for space-constrained applications, since they have smaller package sizes compared to QFP packages. There can also be savings in both area and in the height of the package itself. Other key advantages of BGAs include improved heat dissipation, better misalignment tolerance, robust package construction and proven assembly processes.

The Challenge for System Designers

As PLDs have evolved, BGA packages have followed a trend of increasing pin counts and shrinking pin pitch. Pin pitch or solder ball pitch refers to the distance between the centers of two adjacent pins or solder balls. Pin pitch has a major impact on the routing of I/O from the PLD. This trend towards higher pin counts and shrinking pin pitch creates a significant challenge for system designers, who must use more aggressive design rules, advanced stackup and via technology to meet design requirements. Together, these factors increase the cost of the PCB significantly. This whitepaper

examines techniques system designers can use to lower board cost when designing with PLDs in BGA packages.

Factors That Impact PCB Fabrication Cost

PCB fabrication cost is a key consideration for many electronics products. Various factors such as PCB layer count, choice of stackup and via technology, design rules and routing techniques impact the cost of the PCB.

PCB Layer Count

PCB layer count is one of the major factors in PCB cost. The term "BGA breakout" refers to fanout and escape routing to the perimeter of the device, prior to general routing of the PCB. BGA breakout is the most significant contributor to the number of PCB layers. PCB layer count can be minimized by selecting the appropriate BGA breakout scheme, stackup models, and via technologies. Most PLD vendors provide BGA breakout tips to assist in board design and layout. These tips can help optimize PCB fabrication and lower the cost.

Stackup and Via Models

The choice of stackup and via models has the greatest impact on reducing layer count and PCB fabrication cost. There are two main types of stack up technologies – FR-4 Laminated and High Density Interconnect (HDI). FR-4 Laminated stackups are used for larger designs, such as those for computer motherboards. HDI is preferred for space-constrained applications, such as handhelds.

Via, or plated through holes, are used in multi-layer PCBs to transfer signals from one layer to another. There are four main types of via: through, blind, buried (or embedded), and micro.

Through via provides a connection between the top and bottom layer of a PCB. A blind via provides a connection from the top or bottom layer to an inner PCB layer. An embedded, or buried, via provides a connection between inner PCB layers. Micro via are minute holes drilled by a laser to generate the electrical connection between the layers in a multilayer circuit board. Micro vias are used with HDI circuit boards.

Typically, PCB fabrication costs are lowest for laminated stackup boards with through vias, and are highest for HDI stackup boards with micro vias. The PCB fabrication costs of laminated stackup boards with blind or buried vias are higher than those of laminated stackup boards with through vias, and they are lower than those of HDI stackup boards with micro vias. There are several new technologies whereby the via is filled with epoxy and covered in soldermask, which also adds to the board cost.

Design Rules

Design rules impact both fabrication yields and performance. When more aggressive design rules are used, they tend to drive up fabrication costs. Two examples of design rules are shown below. These design rule examples are for a Lattice MachXO PLD in a 8x8 mm, 0.5 mm pitch, 132-ball csBGA package (LCMXO640-M132/MN132). In each example, the MachXO PLD is placed into a 4-layer stackup fabrication scenario. Notice that the design rules in Example 1 are more aggressive than those in Example 2. Consequently, a PCB designed to meet the design rules of the first example will cost more than a PCB designed to meet the design rules of the second example.

Example 1

Specification	mm	mils
Trace Width/Space	0.085/0.085	3.3/3.3
Ball Pad	0.23	9
Ball Mask	0.38	15
Escape Via Pad	0.40	16
Escape Via Drill	0.15	6
Escape Via Mask	0.50	20
Plane Antipad Space	0.50	20
Thermal Relief	0.50	20

Example 2

Specification	mm	mils
Trace Width/Space	0.10/0.10	4/4
Ball Pad	0.23	9
Ball Mask	0.38	15
Escape Via Pad	0.40	16
Escape Via Drill	0.15	6
Escape Via Mask	NA	
Plane Antipad Space	0.55	22
Thermal Relief	0.50	20

Most PLD vendors provide design rules and package layout examples, such as those shown in the following tables. These are helpful for lowering fabrication cost and are supported by most PCB fabricators.

	Pitch 0.4 mm ucBGA	Pitch 0.5 mm csBGA	Pitch 0.8 mm caBGA
SMD Pad Recommendations			
Optimum Solder Land Diameter	0.25	0.40	0.50
Solder Land Diameter Range	0.20 – 0.25	0.25 – 0.40	0.4 – 0.60
Optimum Solder Mask Opening	0.20	0.25	0.40
Solder Mask Opening Range	0.18 – 0.22	0.20 – 0.30	0.35 – 0.50
NSMD Pad Recommendations			
Optimum Solder Land Diameter	0.16	0.23	0.35
Solder Land Diameter Range	0.14-0.18	0.20-0.30	0.35-0.50
Optimum Solder Mask Opening	0.22	0.35	0.45
Solder Mask Opening Range	0.20-0.25	0.30-0.40	0.45-0.55

Table 1: Pad Recommendations for Different Pin Pitch Packages from Lattice Semiconductor

Package	Example #	Pitch (mm)	Signal/ Power Layers	Trace/ Width-Space (mm)	Ball Pad (mm)	Ball Mask (mm)	Via Pad (mm)	Via Drill (mm)
MN64	1	0.5	6	.100/.100	.23	.33	.30	.125
UMN64	1	0.4	6	.100/.100	.18	.28	.25	.10
MN100	1	0.5	4	.085/.085	.23	.38	.45	.20
	2	0.5	4	.100/.100	.23	.38	.45	.20
MN132	1	0.5	4	.085/.085	.23	.38	.40	.15
	2	0.5	4	.100/.100	.23	.38	.40	.15
MN144	1	0.5	6	.100/.100	.23	.33	.30	.125
	2	0.5	4	.100/.100	.23	.38	.30	.125
BN256	1	0.8	6	.100/.100	.35	.50	.40	.125
	2	0.8	4	.100/.100	.35	.50	.40	.15

Table 2: Summary of Package Layout Examples for MachXO and ispMACH 4000ZE Devices from Lattice Semiconductor

Routing Techniques

Fanout via patterns have the most significant effect on the number of layers used for the breakout, once appropriate choices have been made for the stackup, via models and design rules. The following techniques can help reduce cost:

Push perimeter fanouts to allow more routing on the same layer. When using BGAs with a pin pitch less than 0.8 mm, push the fanout vias for the first two rows of pins around the perimeter and away from the BGA. Pushing them far enough will allow routing the next two rows of pins on the same layer. This will help reduce PCB layers and fabrication cost.

Use north, south, east, and west (NSEW) or layer biased routing to enable more efficiency. When only two to four layers are available for routing a BGA, escaping in all directions (also referred to as NSEW routing) on each layer makes sense due to the extreme route density. However, when more than four layers are available, applying a layer biased concept, where the escape routes obey the layer bias, enables more efficient routing.

Apply quadrant dog-bone to increase route density. When escaping in all directions on a layer, it helps if escape routes and via patterns (also referred to as dog-bone) are in different directions for different quadrants. This is an effective way to increase route density. The following figure shows an example of quadrant dog-bone routing.

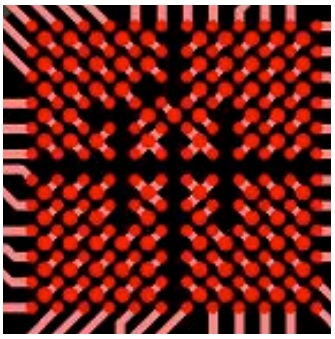

Figure 1 - Example of Quadrant Dog-Bone Style Fanouts for ispMACH 4000ZE in a 7x7 Mm, 0.5 Mm Pitch, 144-Ball CsBGA Package (LC4256ZE-MN144)

Notice how quadrant dog-bone routing opens up additional routing channels in the center row and column. This space can be used for routing additional signals. On the side of the board, the column and row channel is a convenient place to add capacitors and pull-up resistors. Quadrant dog-bone routing has lower cost and runs less risk of soldering problems compared to via-in-pad.

Use via-in-pad to provide space for escape routing. Use of via-in-pad can open up space between pads for escape routing of other signals. As the name implies, a through via is added in the center of BGA ball pads. Figure 2 illustrates this technique.

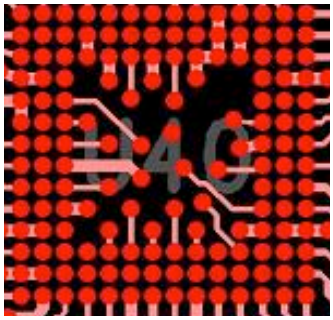

Figure 2 - Example of Via-In-Pad Use for Escape Routing of a MachXO PLD in a 8x8 Mm, 0.5 Mm Pitch, 132-Ball CsBGA Package (LCMXO640-M132/MN132)

Three rows of BGA ball pads are shown. The middle row has via-in-pad. This technique is most useful when the mount layer is either a power or a ground layer, because it allows a continuous power or ground plane under the BGA. When using via-in-pad, one must remember that there is less room for capacitors and resistors on the opposite side of the board, under the BGA, due to fanout and escape routing from the vias.

Align blind vias to increase route density. When blind vias are used, aligning blind vias in columns and rows is a very effective way to increase the route density. It is most effective with high-pin-count BGAs, and when escaping the device is the primary contributor to the layer count.

Use micro vias with HDI stackup to reduce layer count. Micro vias are inextricably linked to HDI stackup. Using micro vias in an HDI stackup is essential to reduce layer count.

Summary

As the ball pitch becomes smaller with each new BGA generation, new PCB fabrication techniques and signal via types are being developed to handle the increased complexity. By reviewing the PLD device package ball density and pitch, I/O signal requirements of the application, and the manufacturing constraints of the PCB fabrication facility, system designers can better weigh the tradeoffs among design decisions. Most PLD vendors provide PCB layout tips and BGA breakout examples on

their websites. System designers can leverage this information to optimize the cost of the PCB.

###