Delta-Sigma ADC

October 2009 **Reference Design RD1063**

Introduction

The Delta-Sigma ADC reference design targets the implementation of an analog-to-digital converter in a Lattice PLD. The design can be implemented with few PLD resources and is flexible enough to meet a variety of application requirements. The Delta-Sigma ADC is an excellent choice for monitoring the various sensors and power rails in a system.

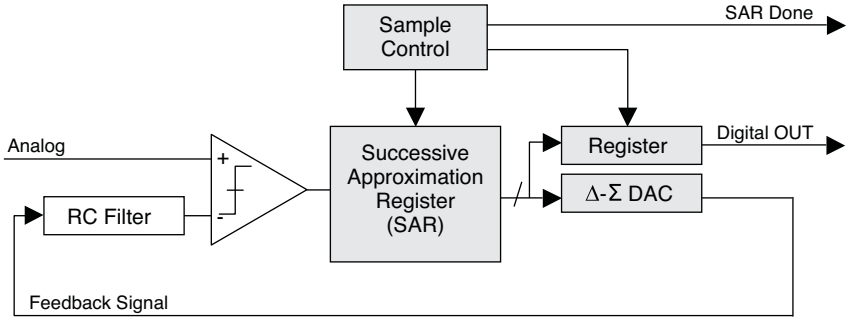
Features

- Parameterized Bit Precision
- Adjustable Sampling Frequency

Overview

The Delta-Sigma ADC is implemented using an analog comparator, low-pass RC filter, Successive Approximation Register (SAR) technique and a Delta-Sigma DAC. An analog input signal is tracked and converted to a digital value. Users are able to enter parameter values to define the bit precision and sampling rates of the ADC.

Figure 1. ADC Functional Block Diagram



In Figure 1, the following logic blocks are implemented in the PLD:

- Successive Approximation Register
- Delta-Sigma DAC
- Sample Control
- Output Register
- SAR Done Flag

Parameter Descriptions

Table 1. Parameter Descriptions

Parameter Name	Description
ADC_WIDTH	This parameter defines the width of the ADC.
DAC_SET_WIDTH	This parameter defines the register width for holding the count of SAR updates during successive approximation. A 4-bit register will accommodate SAR updates for an ADC up to 16 bits wide.
DAC_SETTLE_TIME	This parameter defines the time for the DAC output (output of the RC low-pass filter) to settle. Settle Time = (Clock Period) x 2^(DAC_SETTLE_TIME)
DAC_WIDTH	This parameter defines the width of the DAC. The converter precision is calculated based on the value of this parameter.

Signal Descriptions

Table 2. Signal Descriptions

Signal Name	Direction	Description
clk	Input	ADC operating clock signal
rstn	Input	ADC active low reset signal
analog_cmp	Input	Data received from the output of the analog comparator
analog_out	Output	DAC 1-bit digital output signal to the analog RC filter
digital_out	Output	Digital representation of the analog signal that is converted by the ADC. Bus width is defined by the ADC_WIDTH parameter [ADC_WIDTH-1:0].
sar_done	Output	Active high flag, indicating the digital output value of the ADC is valid.

Successive Approximation Register (SAR)

The SAR function block has a critical role in the architecture of this ADC. It is responsible for approximating the voltage level of the analog input signal and evaluating its approximation by monitoring the output of the analog comparator.

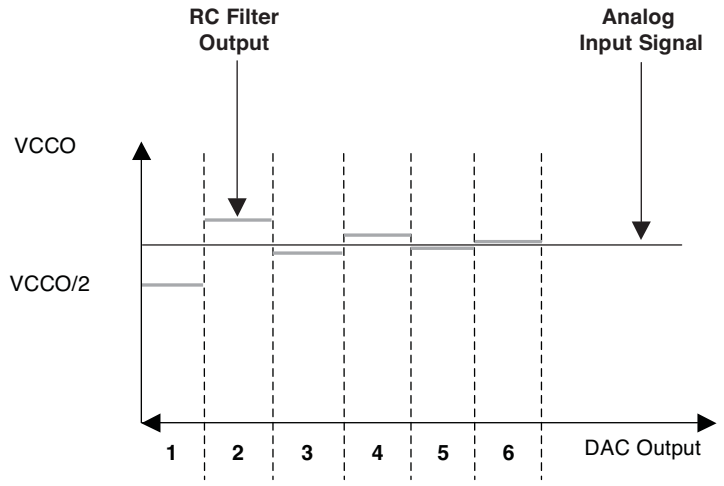
SAR begins the operation by providing a digital value to the DAC, representing half of the VCCO level. MSB is set high and all less significant bits are low. After the output of the RC low-pass filter has settled, SAR will evaluate the output of the analog comparator. If the output of the analog comparator is logic high, then SAR will set the next most significant bit high to force the output of the RC filter to a higher level. If the output of the analog comparator is logic low, then SAR will set the most significant bit low and the next most significant bit high to force the output of the RC filter to a lower level. This procedure is executed until the LSB is updated by SAR approximations. At the end of the procedure, SAR has approximated the analog input signal with half the LSB accuracy.

Figure 2 illustrates the SAR approximation for a 6-bit ADC. It takes six successive approximations to approximate the analog input signal with half the LSB accuracy.

The SAR must complete all six approximations in order to achieve one sample of the analog input signal.

The sampling frequency of the ADC is defined by the time it takes the RC low-pass filter to settle, the number of SAR approximations and the operating clock frequency. The relationship of these variables is expressed by a formula later in the document.

Figure 2. Successive Approximation



Note: VCCO = Voltage level of the VCCIO bank of the PLD.

Delta-Sigma DAC

The function of the Delta-Sigma DAC is to receive a digital value from SAR and output a train of pulses to the RC low-pass filter. The digital value is represented by the average density of the pulses. The function is achieved by calculating the difference (delta) between the DAC output and DAC input digital values. A second adder is used to integrate (sigma) the differences calculated by the delta adder.

The voltage increments, V_i, that can be generated by the DAC are calculated by the following formula:

V_i = VCCO / 2^(DAC_WIDTH)

As an example, for an 8-bit DAC and VCCO = 3.3V, the volt increment V_i is 12.89mV.

Continuing with the 8-bit DAC example, the tables below show the relationship between the DAC digital input value and the 1-bit digital output characteristics.

Table 3. Increasing DAC Digital Input

DAC Digital Input	DAC Output Frequency	DAC Output Duty Cycle
128	clk / 2	1/2
192	clk / 4	3/4
224	clk / 8	7/8
240	clk / 16	15/16
248	clk / 32	31/32
252	clk / 64	63/64
254	clk / 128	127/128
255	clk / 256	255/256

Note: clk = ADC operating clock signal.

Table 4. Decreasing DAC Digital Input

DAC Digital Input	DAC Output Frequency	DAC Output Duty Cycle
128	clk / 2	1/2
64	clk / 4	1/4
32	clk / 8	1/8
16	clk / 16	1/16
8	clk / 32	1/32
4	clk / 64	1/64
2	clk / 128	1/128
1	clk / 256	1/256

Note: clk = ADC operating clock signal.

The highest DAC Output Frequency is for DAC Digital Input of 128, which is half the VCCO value. The lowest DAC Output Frequency is for DAC Digital Input of 1 or 255, which are one V_i from the DC values of ground or VCCO respectively.

The DAC Output Frequency and Duty Cycle are required for calculating the settling time of the RC low-pass filter. The longest settling time will occur when DAC Digital Input is half the VCCO.

Sampling Frequency

The sampling frequency is adjustable to meet the needs of specific applications. The sampling frequency is calculated by the following formula:

Sampling Frequency = (clk) / (2^(DAC_SETTLE_TIME) x ADC_WIDTH)

Where:

clk = ADC operating clock signal
DAC_SETTLE_TIME value must be set to guarantee the RC filter has settled
ADC_WIDTH value defines the width of the converter

RC Filter Design

The main design consideration when selecting the resistor and capacitor values are the voltage ripple and settling time.

The voltage ripple at the output of the low-pass filter must be lower then 1/2 V_i. SAR approximates the analog input signal with half the LSB accuracy, or half V_i. The RC values can be calculated by the following formula:

$1/2\ V_i = 1 / (1+2 \times \Pi \times F_{DAC} \times RC)$

Voltage ripple will decrease by choosing relatively high RC values. However, there is a trade-off between lower voltage ripple and settling time. High RC values will cause long settling time. The settling time is modeled by the fundamental current-voltage relationship of the capacitor:

$V_N = V_O + 1/C \int i dt$

Where:

i = Current flow through the capacitor
dt = Time delta
C = Capacitor value
V_O = Output Voltage of RC network
V_N = Next Output Voltage of RC network

Substituting current with voltage/resistance ratio and dt with ΔT_{ON} and ΔT_{OFF}, the two equations needed to model the settling time are:

$V_N = V_O + ((V_{DAC} – V_O) / (RC)) \times \Delta T_{ON}$ for V_{DAC} = VCCO

$V_N = V_O + ((V_{DAC} – V_O) / (RC)) \times \Delta T_{OFF}$ for V_{DAC} = 0V

Where:

V_{DAC} = DAC 1 bit digital output signal (VCCO or 0V)
ΔT_{ON} = Time frame V_{DAC} = VCCO
ΔT_{OFF} = Time frame V_{DAC} = 0V
VCCO = Voltage level of the VCCIO bank of the PLD

The longest settling time will occur when the DAC Digital Input is half the VCCO. To model the longest settle time, use F_{DAC} = clk / 2 and half the duty cycle.

Implementation

Table 5. Performance and Resource Utilization[1]

Device	Speed Grade	Utilization	f_{MAX} (MHz)	I/Os	Architecture Resources
MachXO™[2]	-5	59 LUTs	148	13	N/A

1. The parameter settings for this implementation include: ADC_WIDTH = 8, DAC_SET_WIDTH = 4, and DAC_SETTLE_TIME = 8.
2. Performance and utilization characteristics are generated using LCMXO2280C-5FT256C, with ispLEVER 7.2 SP2 software. When using this design in a different device, density, speed, or grade, performance and utilization may vary.

Technical Support Assistance

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Revision History

Date	Version	Change Summary
October 2009	01.0	Initial release.