Linking or Selecting Scan Ports with BSCAN2

Application Note

FPGA-AN-02013-1.1

January 2022

Disclaimers

Lattice makes no warranty, representation, or guarantee regarding the accuracy of information contained in this document or the suitability of its products for any particular purpose. All information herein is provided AS IS, with all faults and associated risk the responsibility entirely of the Buyer. Buyer shall not rely on any data and performance specifications or parameters provided herein. Products sold by Lattice have been subject to limited testing and it is the Buyer's responsibility to independently determine the suitability of any products and to test and verify the same. No Lattice products should be used in conjunction with mission- or safety-critical or any other application in which the failure of Lattice's product could create a situation where personal injury, death, severe property or environmental damage may occur. The information provided in this document is proprietary to Lattice Semiconductor, and Lattice reserves the right to make any changes to the information in this document or to any products at any time without notice.

Contents

1. Introduction 4
2. Demo Setup Using Lattice Evaluation Boards 4
3. Programming the Devices 6
4. Demo Steps 6
References 11
Technical Support Assistance 12
Revision History 13

Figures

Figure 2.1. Breaking Up a Single Chain for Board Diagnosis 4
Figure 2.2. BSCAN2 Demo Setup 5
Figure 3.1. JTAG Pin Connections for Programming and BSCAN2 Controller 6
Figure 4.1. ispLEVER Project Structure 7

1. Introduction

Boundary scan is often used to check the interconnects of components on PCBs, monitor pin states or test logic status within a design. It is essentially a probeless technique that allows hardware testing through JTAG commands. The IEEE standard 1149.1 is a boundary testing standard which addresses the hardware and software of the boundary scan logic. Lattice FPGA and CPLD devices support boundary scan cells in their I/Os and therefore are compliant to the IEEE 1149.1 standard. The boundary scan cells in the I/O cells are only active when the device is in test mode. The boundary scan cells have no effect during normal device operation.

A single boundary chain connecting devices in serial, known as a daisy chain, is often sufficient for a simple PCB. A failure on the daisy chain only affects one PCB and usually can be isolated and repaired. In complex systems with multiple boards, a single daisy chain that links all the boards in serial is not effective. A failure on one PCB could render the entire system to be non-testable. There is a great need to perform tests and diagnoses on complex systems in a more efficient and cost effective manner. Designers are looking for solutions to break up big boundary scan chains or merge smaller boundary scan chains based on the IEEE 1149.1 standard. Lattice has provided two reference designs, RD1001, BSCAN1 - Multiple Scan Port Addressable Buffer and RD1002, BSCAN2 - Multiple Scan Port Linker, to address the needs of dynamically linking multiple scan ports or selecting a particular scan port. This document uses BSCAN2 (RD1002) to demonstrate the flexibility of using parallel boundary scan chains for complex system test.

2. Demo Setup Using Lattice Evaluation Boards

Figure 2.1. illustrates the concept of multi-chain capability. A single boundary scan chain can be broken into multiple chains by device type, programming requirements or diagnostic methods. In this demo, a mixed-signal board is placed in a separate chain from the digital board. An 8-port Boundary Scan Port Linker (BSCAN2) is the controller for the local scan ports (LSPs).

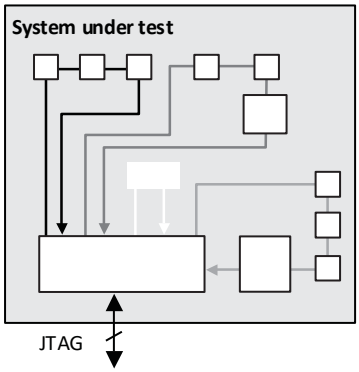


Figure 2.1. Breaking Up a Single Chain for Board Diagnosis

The demo uses three Lattice evaluation boards. The MachXO™ Control Evaluation Board features a MachXO2280 device and is used as the BSCAN2 controller. The MachXO Starter Evaluation Board and the ispPAC®-POWR1220AT8 Evaluation Board are connected to the local scan ports, port2 (LSP2) and port7 (LSP7) respectively. The demo user interface is accessed through the Lattice ispVM™ System programming software. A download cable is used to connect the ispVM System software to the MachXO Control Evaluation Board. Figure 2.2. shows the connection of the boards.

The prototype space of the MachXO Control Evaluation Board is used for the LSP ports. As shown in Figure 2.2., the LSP2 uses the M7, T8, T6 and T4 pin locations for the MSPTDI_2, MSPTDO_2, MSPTMS_2, and MSPTCK_2 signals espectively. The same arrangement exists for the LSP7 and the JTAG port of BSCAN2. Two ribbon cables, shown in Figure 2.2., connect the LSPs on the MachXO Control Evaluation Board to the JTAG ports of the devices on the two other boards. The common ground among the boards is established through the ribbon cable. The MachXO Control Evaluation Board programming is done through the FTUSB cable, while the BSCAN2 controller uses EzUSB for controlling the LSPs. It is important to provide Vcc and GND for the BSCAN2's JTAG port in order for the ispVM System software to recognize the JTAG port.

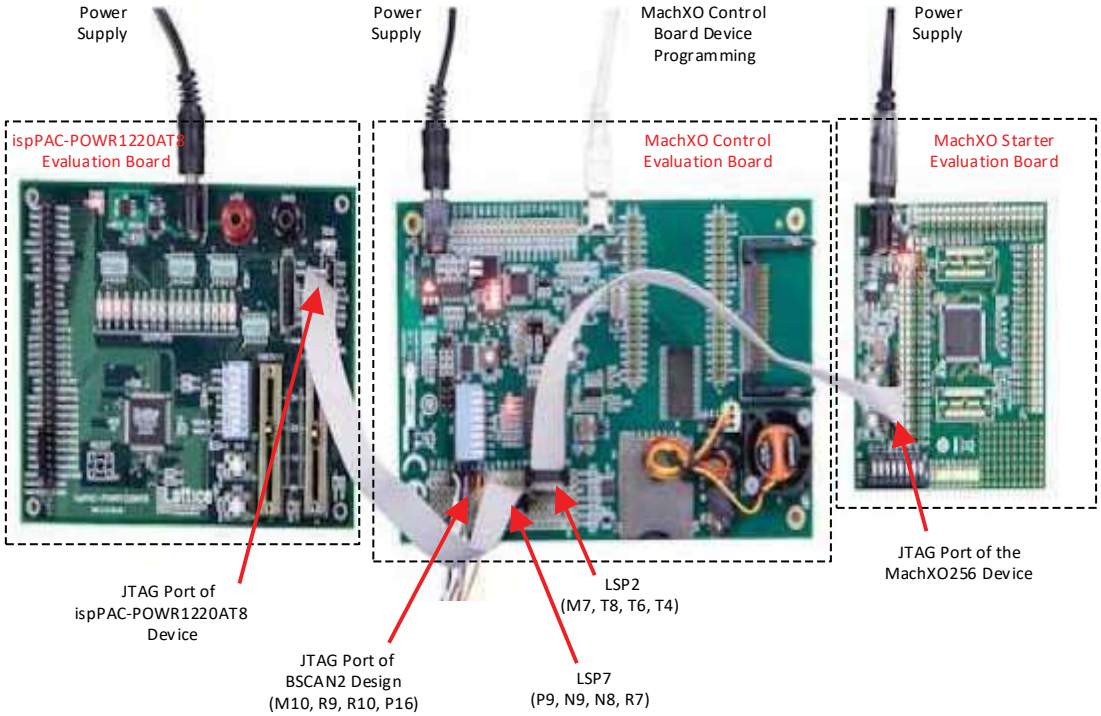


Figure 2.2. BSCAN2 Demo Setup

3. Programming the Devices

The programming of Lattice devices is through the built-in JTAG port on the device. Users can use a USB or parallel download cable to program the devices on the board. With some planning, the board that hosts the BSCAN2 controller can switch between the JTAG port and the without moving the programming header, as shown in Figure 3.1. The jumper on the TMS line isolates the TMS signal during device programming.

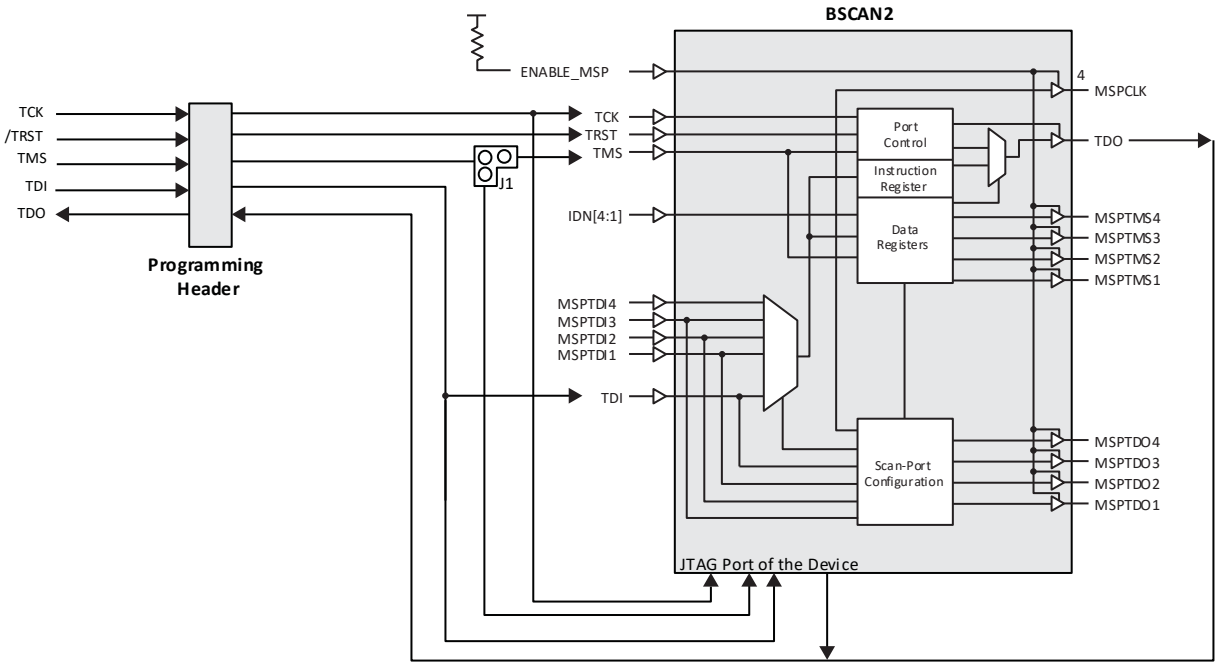


Figure 3.1. JTAG Pin Connections for Programming and BSCAN2 Controller

4. Demo Steps

Once the boards are connected as shown in Figure 2.2., the user needs to compile the BSCAN2 design for the MachXO Control Evaluation Board with LSP2, LSP7 and the JTAG port for the BSCAN2 pins defined. These pin locations must match the desired prototype locations on the MachXO Control Evaluation Board. Figure 4.1. shows the ispLEVER® window for a successful compilation, where top_linker is a lower-level ngo file for the BSCAN2 design.

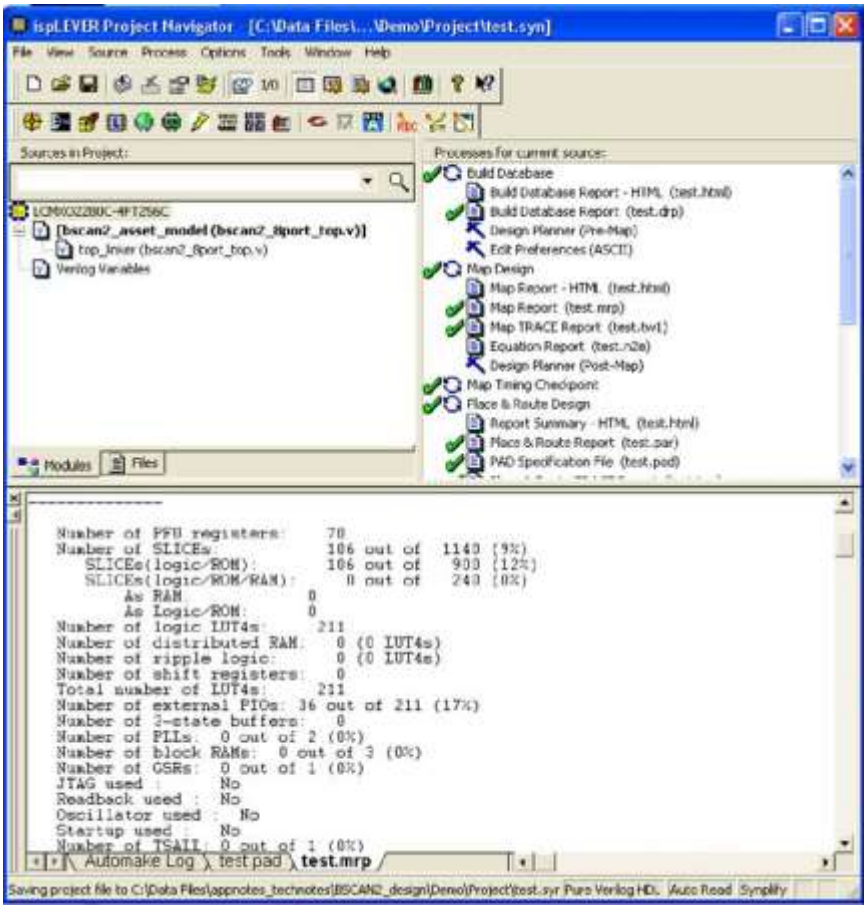
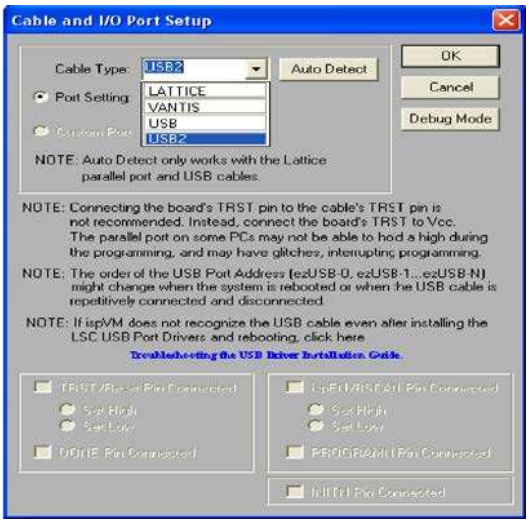


Figure 4.1. ispLEVER Project Structure

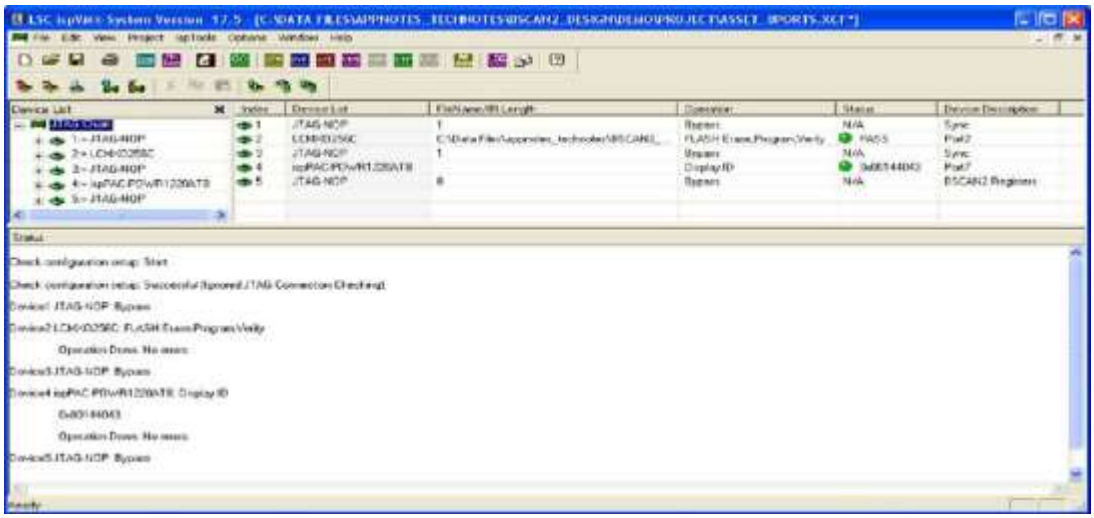
Follow these steps to complete the demo:

1. Power up all the boards by connecting them to the appropriate power supplies.
2. Bring up the ispVM software. Go to the Options menu and choose Cable and I/O Port Setup to select the USB port. Use the USB2/FTUSB cable to program the MachXO2280 device on the MachXO Control Evaluation Board.

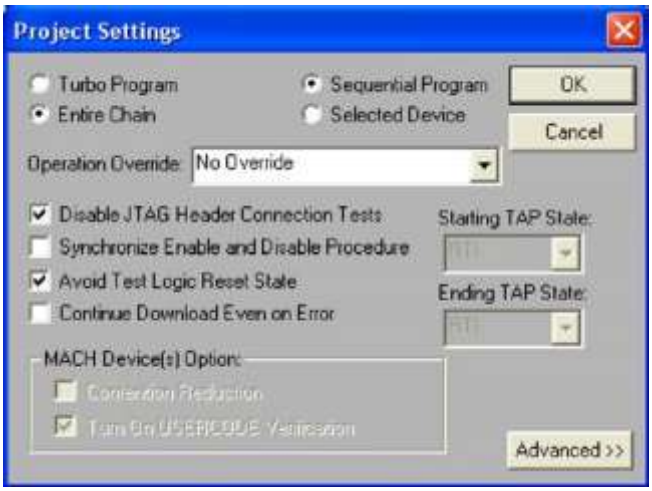


3. Use the **Scan** button to scan the MachXO Control Evaluation Board. The LCMXO2280 device will show up in the ispVM window. Select the BSCAN2 JEDEC file from the ispLEVER project directory and run **Flash Erase, Program, Verify** to program the device.

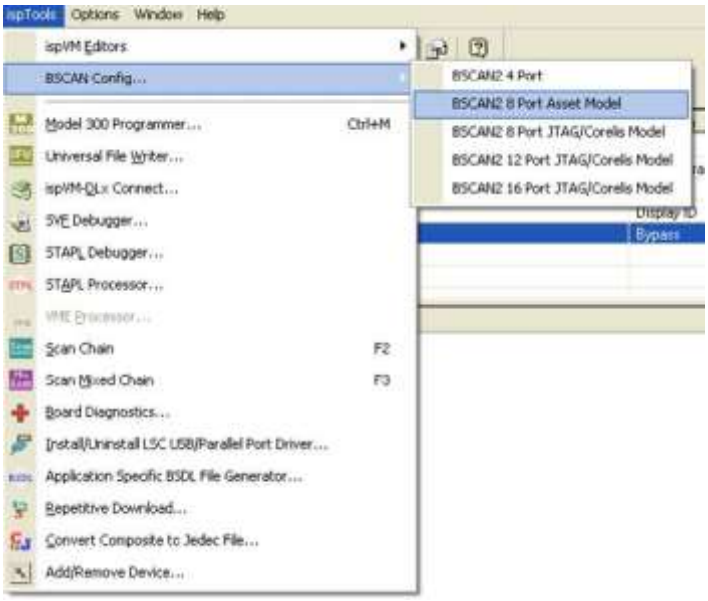
4. Now the MachXO device on the MachXO Control Evaluation Board becomes the BSCAN2 Controller. Switch the download cable port from USB2/FTUSB to USB/EzUSB using the ispVM Cable and I/O Port Setup menu.
5. The flywires of the EzUSB cable must be connected to the JTAG port of the BSCAN2 controller. In this case, they are M10, R9, R10, and P16 for signals TDI, TDO, TMS and TCK on the prototype area. The Vcc and GND must be provided to the flywires as well.
6. Start a new window in ispVM, and manually create a BSCAN2 chain that connects the active LSP ports. Select the operation for each LSP port. There is a JTAG-NOP sync bit associated with each active LSP port. An ASSET model is used in this demo. If the JTAG model is used, an 8-bit register must be inserted between LSP4 and LSP5.



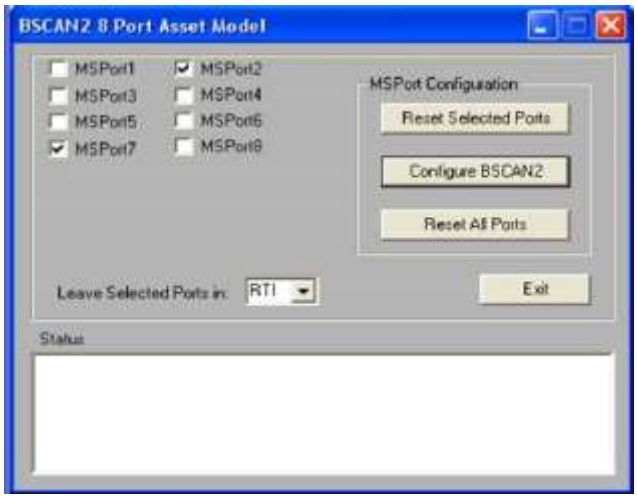
7. Before starting to run any operation, make sure **Disable JTAG Header Connection Test** and **Avoid Test Logic Reset State** are checked in the **Project Settings**. Then save the BSCAN2 chain as a configuration file (.xcf file).



8. The BSCAN2 ports have to be configured. Go to the **ispTools** menu, select **BSCAN Config** and then select **BSCAN2 8 Port Asset Model**. This demo can also be done with the BSCAN2 4 Port Model, provided the appropriate top_linker ngo file is used during BSCAN2 JEDEC file generation.



9. An Asset Model window will pop up. The user can select which LSP ports will be included in the chain by checking the appropriate selection boxes. In this demo, LSP2 and LSP7 are the active ports. In a real system, users can easily link more than two ports at a time. Click the **RESET Selected Ports** button, and then the **Configure BSCAN2** button.



10. Now the BSCAN2 chain is ready to run the specified operation for each port. Return to the main ispVM window and click the Go button. The operations for each LSP chain should be completed successfully.

The BSCAN2 feature in the ispVM System software can run all the operation modes that ispVM supports. It is a convenient tool for breaking up large daisy chains to isolate a non-functioning device or simply to separate the devices according to their programming needs.

References

- Multiple Scan Port Linker (FPGA-RD-02106)
- Using Multiple Boundary Scan Port Linker (BSCAN2) (FPGA-AN-02017)

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.1, January 2022

Section	Change Summary
All	• Changed document number from AN8083 to FPGA-AN-02013. • Updated document template.
Disclaimers	Added this section.

Revision 1.0, October 2009

Section	Change Summary
All	Initial release.

www.latticesemi.com