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## **LatticeSC SERDES Eye/Backplane Demo Design**

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**User's Guide**

Revision 4.0  
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### 1. Introduction

This document provides technical information and instructions on using the LatticeSC SERDES Eye/Backplane Demo Design. The demo has been designed to demonstrate the performance of the LatticeSC flexiPCS SERDES IO at 3.125 Gbps. The document provides a circuit description as well as instructions for running the demo on the LatticeSC Communications Platform evaluation board.

In addition to this user's guide the SERDES Eye/Backplane Demo comes with the following:

- Verilog source code for the FPGA design
- Bitstream (in format of \*.bit)
- ORCAstra Plug-in GUI

Hardware requirement for this loop back application test design:

- LatticeSC Communications Platform evaluation board with LatticeSC 900-pin SC25 device
- Power module
- PC w/ORCAstra -PC not provided
- 156.25 MHz onboard oscillator for flexiPCS QUAD 360
- Clock Generator instrument for flexiPCS QUAD 3E0 –Instrument not provided
- Customer Backplane w/SMAs- Not provided
- Pair of DC Blocks –not provided
- Eye viewing instrument (DCA, SDA etc.)- Not provided
- Cables- only one pair of 10in. SMA cable is provided
- Six 50-ohm to ground SMA terminations for the unused output SERDES channels of a flexiPCS quad. The assumption is that only one differential channel of a QUAD would be used for any specific demo.

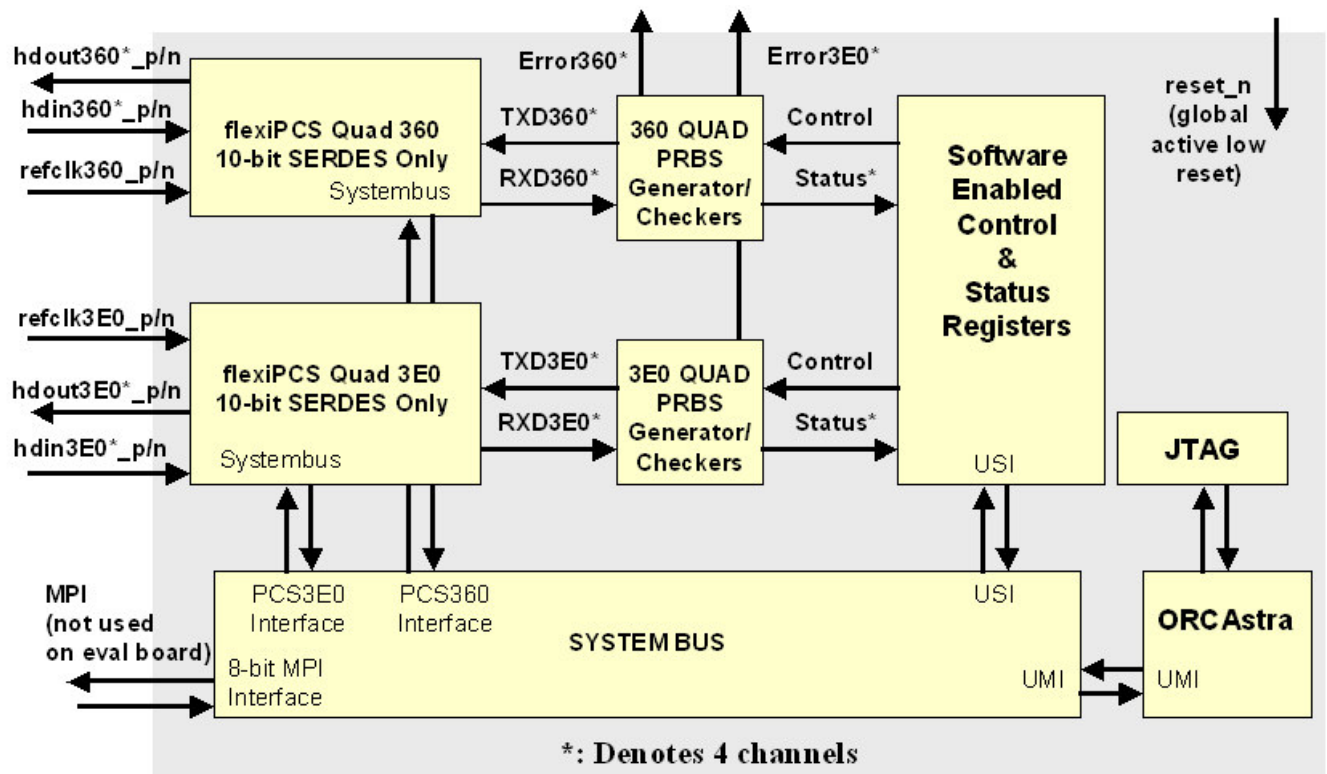
The next few sections cover:

- A design overview of the SERDES Eye/Backplane Demo.
- A description of the Communications Platform evaluation board setup for the demo.
- A design IO signal description.
- Downloading the SERDES Eye Demo bitstream.
- A description of the ORCA-stra GUI environment used with the Design.
- Running Typical Backplane Demos.
- Alternate Reference Clock Setting.

## 2. SERDES Eye/Backplane Demo Design Overview

A block diagram of the FPGA IO Demo design is provided in Figure 1.

Figure 1. SERDES Eye/Backplane Demo Design



The basic concept of the design is a quad-based PRBS Generator/checker that transmits 4 channels of parallel data to a flexiPCS quad. In turn, the flexiPCS SERDES channels serialize the data in the transmit direction, and de-serialize it in the receive direction. The serial data stream can be:

- Looped back via a cable on the evaluation board, or
- Sent to a DCA or SDA for eye viewing.

In both cases, a backplane of variable length can be included in the serial path.

For this demo, both flexiPCS quads PCS360 and PCS3E0 are used. These have been generated in 10-bit SERDES only mode, at 3.2 Gbps per channel (actual demo rate is 3.125Gbps or equivalent).

## 2.1. Clock Sources

Each of FlexiPCS quad 360 and 3E0 is clocked by its own reference clock (refpclk360 or refpclk3E0). The reference clock's frequency is 312.5MHZ (or equivalent). Internally to each flexiPCS, the reference clock is used to create 312.5MHZ receive and transmit clocks. The 312.5 MHZ transmit and receive clocks clock transmit (TXD) and receive (RXD) interfaces respectively for both the flexiPCS and corresponding PRBS Generator/Checker logic. Since RXD and TXD busses are 10bit-wide, the data bandwidth is 3.125 Gbps (based on a 312.5MHZ reference clock).

## 2.2. PRBS Generator/Checker QUAD

There are 2 PRBS Generator/Checker QUAD blocks in the demo design. The first is associated with flexiPCS Quad 360 and the second with flexiPCS Quad 3E0.

Each PRBS generator/checker QUAD has the following characteristics:

- 4 channels in 10-bit SERDES Only Mode
- 1 PRBS Generator ( $2^7$  and  $2^{31}$ ) transmitting to all 4 TXD channels
- 1 PRBS Checker ( $2^7$  and  $2^{31}$ ) per channel (4 checkers total per QUAD)
- Control/Status interface to user registers.
- 1 Error Counter per checker (4 total per QUAD) connected to a user register for monitoring.
- 1 real time Error signal indicator per checker (4 total per QUAD) connected to a primary output buffer.

The System Bus controls the user registers via the User Slave Interface (USI).

The System Bus is controlled in turn either via an MPI interface (not supported on evaluation board) or the ORCAstra interface via JTAG.

### 2.2.1. PRBS Generator/Checker QUAD ORCAstra GUI

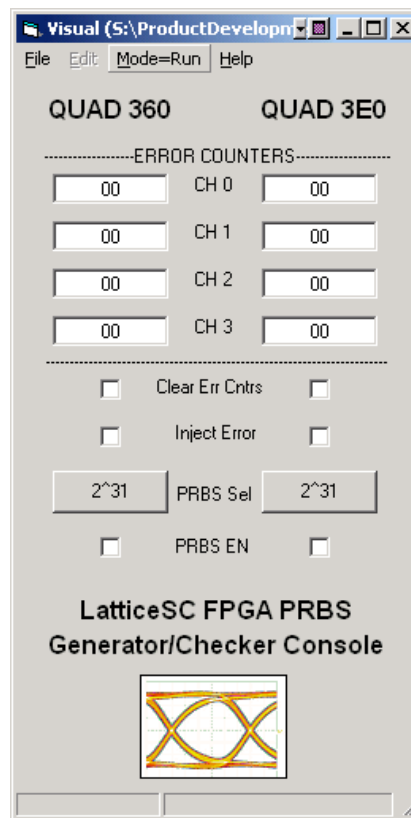
This demo utilizes a visual window plug-in to the base ORCAstra installation. To open this visual window, complete the following steps.

1. Open ORCAstra and select CustomProgrammability->Visual Window. An empty window will appear.
2. Select File->Open. Browse to the directory where you have installed the SERDES Eye Demo directory, then to ORCAstra Plug-ins. Select EyeDemo.vis and click Open. Figure 2 provides a screen capture of this window.

At this point, make sure that the Continuous Polling check box is selected in the main ORCAstra window.

As shown in Figure 2, the control and status elements are identical for both the 360 and 3E0 PRBS Generator/Checker Quad. The following is a description of each of these elements.

Figure 2. PRBS Generator/Checker QUAD ORCAstra Plug-in Visual Window



**PRBS EN:** When checked, it enables both the transmission of PRBS data from the generator, and the detection of errors by the checkers of a quad. When this button is unchecked, the PRBS ERROR counters in the visual window stop incrementing, and the real time output PRBS Error signal indicators (see Figure 1 and Table 3) remain low.

**2<sup>31</sup>/2<sup>7</sup> Button Selection:** This button allows the selection of either 2<sup>7</sup> or 2<sup>31</sup> PRBS generation and checking.

**Error Counters:** There are 4 hexadecimal error counters per quad, corresponding to the 4 channel checkers in a quad. Each error counter increments every time a single error is detected at the checker. Each counter is only 8-bit wide, so the maximum count reached is hFF. When the counter reaches hFF, it does not roll back to zero unless the Clear Error Counters button is checked. A counter will not increment when PRBS EN is not checked.

**Clear Error Counters:** When checked, it asynchronously clears the content of all 4 channel PRBS checker Error Counters.

**Inject Error:** The design injects a single incorrect DATA word in the transmitted PRBS data every time a positive edge occurs on the register bit associated with the **Inject Error** check box. So, an incorrect DATA word is inserted every time the **Inject Error** box is unchecked then checked. **PRBS EN** has to be checked for this error injection feature to work. Note that a single incorrect DATA word received by a channel checker will correspond to 2 increments in the checker's error counter. This is related to the behavior of the PRBS checker soft IP in the FPGA: Every time the checker receives data word A, it

compares it against the current expected word value, and data A becomes the seed for the next expected PRBS data word. So, if data A is incorrect, the PRBS errors counter increments once. When correct DATA word B is received after DATA A, the checker's expected value computed based on incorrect DATA A is also incorrect, and does not match DATA B. So the error counter increments once again for a total of 2 increments per incorrect DATA word.

## 2.2.2. PRBS Generator/Checker USI register map

The user registers for both 360 and 3E0 PRBS generator/checker Quad are defined as per Table 1. All register addresses are in hex. Also note that register address h00800 (not shown in Table 1) is a read only register that contains the version number of the design.

**Table 1. User Slave Interface Register Map**

GUI OPTION	QUAD 360 FPGA registers				QUAD 3E0 FPGA registers				Description
	ch0	ch1	ch2	ch3	ch0	ch1	ch2	ch3	
PRBS SELECT	08000, bit 0				08100, bit 0				0=2 <sup>7</sup> -1 1=2 <sup>31</sup> -1
PRBS EN	08000, bit 1				08100, bit 1				0=disable 1=enable
PRBS ERR CNT	08001, bits [0:7]	08002, bits [0:7]	08003, bits [0:7]	08004, bits [0:7]	08101, bits [0:7]	08102, bits [0:7]	08103, bits [0:7]	08104, bits [0:7]	Count up to FF. Clear on read
Inject error	08000, bit 2				08100, bit 2				0=don't inject 1=inject continuously
Clear Error Counters	08000, bit 3				08100, bit 3				0=don't Clear 1=Clear

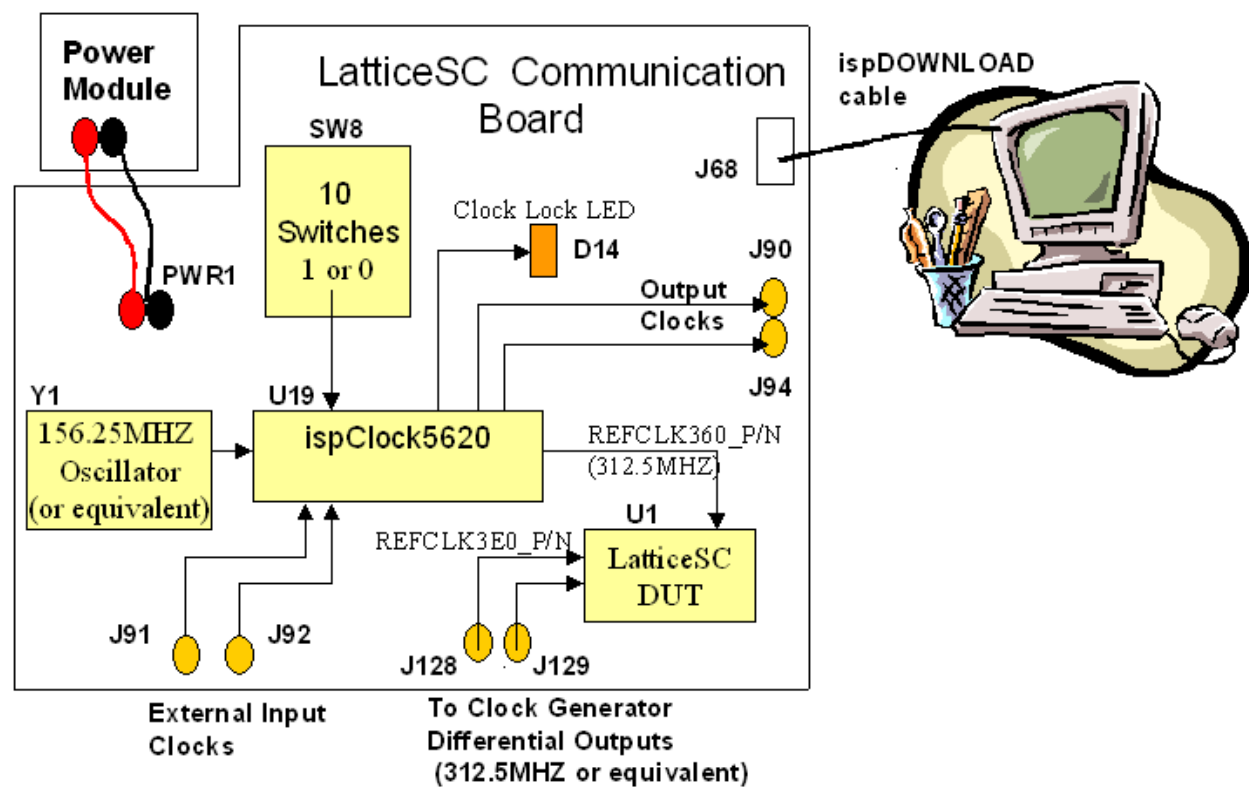
### 3. Communication Platform Board Setup

There are two evaluations that can be done using the SERDES Eye/Backplane Demo design. The first demo is to loop the PRBS data back to the LatticeSC and check the data. The second demo is to evaluate the CML eye diagram of the high-speed data signal to a DCA (or SDA). The following setups assume the following.

1. ispVM is installed on a PC (if the bitstream is to be loaded via the ispVM tool).
2. ORCAstra is installed on a PC.
3. A 156.25MHz Oscillator is plugged into Y1.
4. ispDOWNLOAD cable connected to the USB port of the PC and to the ispVM JTAG Connector on the board. A HW-USB-1A is included with the board delivery.
5. Power is applied to the board via the provided power supply.

Figure 3 shows the power supply, ispVM and the reference clock setup for both 360 and 3E0 flexiPCS quads.

Figure 3. LatticeSC Communication Platform Board Setup





### 3.1. Clocking Scheme for 360 flexiPCS

The 360 flexiPCS quad reference clock is generated from the ispClock5620 module (U19). This requires that a 156.25MHZ (or equivalent) clock oscillator be inserted in Y1 and that the SW8 properly configure the ispClock5620. This requires that the SW8 switch module be configured as per Table 2. This configuration ensures the following:

- The source clock to the ispClock5620 module is from the Y1 oscillator. It is possible to source the input clock from external SMA inputs (J91 and J92). This configuration requires that switch 5 of SW8 be in the ON position. **Note that while facing the board with the Lattice logo in the top right position, any switch on SW8 in ON if it is in the left (0V) position, and OFF when it is in the right position (3.3V).**
- The ispClock5620 module is selecting program 1 from its flash RAM. All ispClock5620 modules come pre-configured with several programs. Program 1 allows the source clock from Y1 to be multiplied by 2 and the creation of 312.5MHZ differential clocks at its outputs. This is the source of the refclk360\_p/n differential reference clock to the 360 flexiPCS quad.

In normal operation, LED D14 should glow to indicate that the ispClock5620 module PLL is locked to its clock input. Flipping switch 2 to the ON position resets the Lock (D14 turns off). Switching it back to the OFF position should allow D14 to turn on as lock occurs again.

The differential outputs of the ispClock5620 module can be observed at the J90 and J94 SMA pins.

For more information on how to program the ispClock5620 module, please refer to the LatticeSC Communications Platform evaluation board user's guide.

**Table 2. SW8 switches configuration**

SWITCH	POSITION	Function
1	OFF	
2	OFF	Resets Internal PLL lock when in ON position.
3	OFF	
4	OFF	
5	OFF	Selects Oscillator clock inputs in this position. Selects J91 and J92 SMA clock inputs in ON position.
6	OFF	
7	OFF	
8	OFF	Switches 8 and 9 select program 1 in current positions.
9	ON	
10	OFF	Selects internal PLL in current position. Bypasses PLL in ON position.

### 3.2. Clocking Scheme for 3E0 flexiPCS

The 3E0 flexiPCS quad differential reference clock is generated from an external clock generator. The external 312.5 MHZ clock is connected to the board via SMA J128 and J129. The recommended levels for the differential clock source are 1.2V High and 0.8V Low.

#### 4. SERDES Eye/Backplane Demo Design Signal Descriptions

Table 3 lists all the SERDES Eye/Backplane Demo Design signals that are connected on the LatticeSC Communication Platform Board.

**Table 3. Signal Descriptions**

Signal		Lattice Communication Platform Board	Description
Name	Type	Connection	
General Signals			
reset_n	I	SW2 Push Button	FPGA Global active low reset
JTAG Signals			
tck	I	To on-board JTAG logic	JTAG Pins
tdi	I		
tdo	O		
tms	I		
PRBS Error Signals for 360 QUAD			
Error360_0	O	Jumper pins 5 and 6 on J152 to see RED LED D36 light when errors occur	PRBS Error indicator for channel 0. Will not light if PRBS EN in Visual GUI is unchecked.
Error360_1	O	Jumper pins 8 and 9 on J152 to see RED LED D37 light when errors occur	PRBS Error indicator for channel 1. Will not light if PRBS EN in Visual GUI is unchecked.
Error360_2	O	Jumper pins 11 and 12 on J152 to see RED LED D38 light when errors occur	PRBS Error indicator for channel 2. Will not light if PRBS EN in Visual GUI is unchecked.
Error360_3	O	Jumper pins 14 and 15 on J152 to see RED LED D39 light when errors occur	PRBS Error indicator for channel 3. Will not light if PRBS EN in Visual GUI is unchecked.
PRBS Error Signals for 3E0 QUAD			
Error3E0_0	O	Jumper pins 17 and 18 on J152 to see YELLOW LED D40 light when errors occur	PRBS Error indicator for channel 0. Will not light if PRBS EN in Visual GUI is unchecked.
Error3E0_1	O	Jumper pins 20 and 21 on J152 to see YELLOW LED D41 light when errors occur	PRBS Error indicator for channel 1. Will not light if PRBS EN in Visual GUI is unchecked.
Error3E0_2	O	Jumper pins 23 and 24 on J152 to see YELLOW LED D42 light when errors occur	PRBS Error indicator for channel 2. Will not light if PRBS EN in Visual GUI is unchecked.
Error3E0_3	O	Jumper pins 26 and 27 on J152 to see YELLOW LED D43 light when errors occur	PRBS Error indicator for channel 3. Will not light if PRBS EN in Visual GUI is unchecked.

FlexiPCS QUAD 360			
refclk360n/refclk360p	I	Sourced from U19	Differential input reference clock
hdin360p_0/ hdin360n_0	I	SMA J103 and J105	Channel 0 Differential High Speed SERDES inputs
hdin360p_1/ hdin360n_1	I	SMA J106 and J108	Channel 1 Differential High Speed SERDES inputs
hdin360p_2/ hdin360n_2	I	SMA J110 and J112	Channel 2 Differential High Speed SERDES inputs
hdin360p_3/ hdin360n_3	I	SMA J114 and J116	Channel 3 Differential High Speed SERDES inputs
hdout360p_0/ hdout360n_0	I	SMA J104 and J102	Channel 0 Differential High Speed SERDES outputs
hdout360p_1/ hdout360n_1	I	SMA J107 and J109	Channel 1 Differential High Speed SERDES outputs
hdout360p_2/ hdout360n_2	I	SMA J111 and J113	Channel 2 Differential High Speed SERDES outputs
hdout360p_3/ hdout360n_3	I	SMA J115 and J117	Channel 3 Differential High Speed SERDES outputs
FlexiPCS QUAD 3E0			
refclk3E0n/refclk3E0p	I	SMA J128 and J129	Differential input reference clock
hdin3E0p_0/ hdin3E0n_0	I	SMA J118 and J120	Channel 0 Differential High Speed SERDES inputs
hdin3E0p_1/ hdin3E0n_1	I	SMA J122 and J124	Channel 1 Differential High Speed SERDES inputs
hdin3E0p_2/ hdin3E0n_2	I	SMA J126 and J130	Channel 2 Differential High Speed SERDES inputs
hdin3E0p_3/ hdin3E0n_3	I	SMA J132 and J135	Channel 3 Differential High Speed SERDES inputs
hdout3E0p_0/ hdout3E0n_0	I	SMA J119 and J121	Channel 0 Differential High Speed SERDES outputs
hdout3E0p_1/ hdout3E0n_1	I	SMA J123 and J125	Channel 1 Differential High Speed SERDES outputs
hdout3E0p_2/ hdout3E0n_2	I	SMA J127 and J131	Channel 2 Differential High Speed SERDES outputs
hdout3E0p_3/ hdout3E0n_3	I	SMA J133 and J136	Channel 3 Differential High Speed SERDES outputs

## 5. Settings of Jumpers and Switches

Table 4 below lists the jumpers, switches, connectors and indicators on the LatticeSC Communications Platform Evaluation Board, and indicates the proper setting or output for each item.

**Table 4. Settings for Jumpers, Switches, Connectors and Indicators**

Name	Loc on Dwg ①	Loc on Bd ②	Description	③	Setting
BAN1	2-C2	12-11	Bench Input – 3.3 V		(open)
BAN2	2-C3	11-18	Bench Input – 5 V		(open)
BAN3	2-C2	23-05	Bench Input - Gnd		(open)
BAN4	2-C3	05-18	Bench Input - Gnd		(open)
D1	2-D4	61-29	Power Rail- 1.0/1.2 V		“On”
D2	2-D3	67-29	Power Rail- 1.5 V		“On”
D3	2-D3	36-29	Power Rail- 1.8 V		“On”
D4	2-D3	29-29	Power Rail- 2.5 V		“On”
D5	2-D3	40-29	Power Rail-3.3 V		“On”
D6	2-D4	52-29	Power Rail- 1.2 V		“On”
D7	2-B1	28-13	Input Power- 5 V		“On”
D8	2-B1	28-07	Input Power- 3.3 V		“On”
D9	10-D5	21-51	INITN		④
D10	10-D5	23-51	DONE		⑤
D13	10-D4	21-78	TDI Activity		⑥
D14	11-B5	20-38	IspCLOCK LOCK #1		See Section 3.1
D15	11-B2	33-41	IspCLOCK LOCK #2		“Off”
D16	13-B3	81-41	RXSIGALM		“Off”
D17	13-B3	81-40	ALM_INT		“Off”
D18	13-B2	81-39	TXALM_INT		“Off”
D19	13-B2	81-38	RXALM_INT		“Off”
D20	13-B2	81-37	RXPOWALM		“Off”
D21	13-B2	81-36	MODBIASALM		“Off”
D22	13-B2	81-35	LSPOWALM		“Off”
D23	13-B2	81-34	LSTEMPALM		“Off”
D24	13-B2	81-33	LSBIASALM		“Off”
D25	13-B2	81-32	TXFIFOERR		“Off”
D26	13-B2	81-31	RXLOCKERR		“Off”
D27	13-B2	81-30	TXLOCKERR		“Off”
D29	14-B3	71-33	Analog 5 V		“On”
D30	14-B3	71-32	Analog 3.3 V		“On”
D31	14-B3	71-31	Digital 3.3 V		“On”
D32	14-B3	71-30	Analog Neg 5 V		“On”
D33	14-B3	71-29	Digital Neg 5 V		“On”
D34	14-B4	71-34	1.8 V		“On”
D35	18-D3	57-37	User I/O #1		—
D36	18-D2	56-37	User I/O #2		—
D37	18-D2	55-37	User I/O #3		—
D38	18-D1	54-37	User I/O #4		—
D39	18-D1	53-37	User I/O #5		—
D40	18-D3	52-37	User I/O #6		—
D41	18-D2	51-37	User I/O #7		—
D42	18-D2	50-37	User I/O #8		—
D43	18-D1	49-37	User I/O #9		—

# LatticeSC SERDES Eye/Backplane Demo Design

Name	Loc on Dwg ①	Loc on Bd ②	Description	③	Setting
D44	18-D1	48-37	User I/O #10		—
D45	18-C3	47-37	User I/O #11		—
D46	18-C2	46-37	User I/O #12		—
D47	18-C2	45-37	User I/O #13		—
D48	18-C1	44-37	User I/O #14		—
D49	18-C1	43-37	User I/O #15		—
D50	18-C3	42-37	User I/O #16		—
D51	18-C2	41-37	User I/O #17		—
D52	18-C2	40-37	User I/O #18		—
D53	18-C1	39-37	User I/O #19		—
D54	18-C1	38-37	User I/O #20		—
D55	18-B3	37-37	User I/O #21		—
D56	18-B2	36-37	User I/O #22		—
D57	18-B2	35-37	User I/O #23		—
D58	18-B1	34-37	User I/O #24		—
J1	2-B5	02-30	Power Manager Interface		(open)
J2	2-B4	42-50	Power Manager Config		2-3, 5-6, 8-9, 11-12, 14-15, 17-18, 20-21, 23-24, 26-27, 29-30, 92-93, 95-96, 98-99, 101-102, 104- 105, 107-108
J3	2-A2	56-79	Chip Cooler		(open)
J8	3-D4	61-12	Voltage Reg – 1.0/1.2 V		(open)
J9	3-D3	52-12	Voltage Reg – 1.2 V		(open)
J10	3-C4	61-13	Voltage Reg – 1.0/1.2 V Resistor Sel		2-3
J15	3-B3	12-21	Voltage Reg – 2.5 V		(open)
J16	3-B4	69-12	Voltage Reg – 1.5 V		(open)
J21	3-A3	44-12	Voltage Reg – 3.3 V		(open)
J22	3-A4	38-12	Voltage Reg – 1.8 V		(open)
J23	7-A4	91-36	VCC12 Select		1-2
J26	4-D5	83-30	SerDes Supplies – VDDIB		2-3
J27	4-D4	88-30	SerDes Supplies – VDDOB		2-3
J28	4-C2	91-30	SerDes Supplies – VDDAX25		1-2
J29	4-B5	91-22	SerDes Supplies – VDDRX		1-2
J30	4-B4	88-22	SerDes Supplies – VDDTX		1-2
J31	4-B2	83-22	SerDes Supplies – VDDP		1-2
J32	6-D3	35-77	Select VCCIO1		3-4
J44	7-D3	88-36	Select VCC_AUX		1-2
J46	7-B4	61-73	Select VCCJ		1-2
J48	8-D5	93-16	Shutdown Right		2-3
J49	8-D1	93-10	Shutdown Left		2-3
J50	8-C2	93-12	Select VTT Left		3-4
J52	8-C4	93-21	Select VTT Right		3-4
J56	8-B5	88-16	Shutdown Bottom		2-3
J59	8-A4	88-21	Select VTT Bottom		3-4
J63	10-D3	21-75	Daisy Chain		1-2
J64	10-D3	19-73	JTAG Daisy Chain		(open)

# LatticeSC SERDES Eye/Backplane Demo Design

Name	Loc on Dwg ①	Loc on Bd ②	Description	③	Setting
J68	10-D3	19-77	IspVM Cable Connector	✓	See section 3
J73	10-B3	32-65	DAT_OUT Select		(open)
J74	10-C3	32-64	PCM_CLK Select		(open)
J76	10-C1	25-58	PCM Connector		(open)
J78	10-B2	20-59	CPU_CS Select		(open)
J80	10-B2	20-60	CPU_CS1 Select		(open)
J81	10-B3	35-65	Temp Sense		(open)
J98	11-A2	21-42	IspCLOCK Cable Connector		(open)
J102	12-D4	17-97	SMA- A_HDOUTN0_L		See section 8
J103	12-D5	07-92	SMA- A_HDINP0_L		See section 8
J104	12-D4	12-97	SMA- A_HDOUTP0_L		See section 8
J105	12-D5	12-92	SMA- A_HDINN0_L		See section 8
J106	12-D5	22-92	SMA- A_HDINP1_L		See section 8
J107	12-D4	27-97	SMA- A_HDOUTP1_L		See section 8
J108	12-C5	17-92	SMA- A_HDINN1_L		See section 8
J109	12-C4	22-97	SMA- A_HDOUTN1_L		See section 8
J110	12-C5	27-92	SMA- A_HDINP2_L		See section 8
J111	12-C4	32-97	SMA- A_HDOUTP2_L		See section 8
J112	12-C5	32-92	SMA- A_HDINN2_L		See section 8
J113	12-C4	37-97	SMA- A_HDOUTN2_L		See section 8
J114	12-C5	42-92	SMA- A_HDINP3_L		See section 8
J115	12-C4	47-97	SMA- A_HDOUTP3_L		See section 8
J116	12-C5	37-92	SMA- A_HDINN3_L		See section 8
J117	12-C4	42-97	SMA- A_HDOUTN3_L		See section 8
J118	12-C5	92-92	SMA- A_HDINP0_R		See section 8
J119	12-C4	87-97	SMA- A_HDOUTP0_R		See section 8
J120	12-C5	87-92	SMA- A_HDINN0_R		See section 8
J121	12-C4	82-97	SMA- A_HDOUTN0_R		See section 8
J122	12-B5	77-92	SMA- A_HDINP1_R		See section 8
J123	12-B4	62-97	SMA- A_HDOUTP1_R		See section 8
J124	12-B5	82-92	SMA- A_HDINN1_R		See section 8
J125	12-B4	77-97	SMA- A_HDOUTN1_R		See section 8
J126	12-B5	62-92	SMA- A_HDINP2_R		See section 8
J127	12-B4	67-97	SMA- A_HDOUTP2_R		See section 8
J128	12-B3	65-71	SMA- A_REFCLKN_R		See section 8
J129	12-B3	65-76	SMA- A_REFCLKP_R		See section 8
J130	12-B5	67-92	SMA- A_HDINN2_R		See section 8
J131	12-B4	62-97	SMA- A_HDOUTN2_R		See section 8
J132	12-B5	57-92	SMA- A_HDINP3_R		See section 8
J133	12-B4	52-97	SMA- A_HDOUTP3_R		See section 8
J134	12-B3	61-76	SMA- A_RXREFCLKP_R		(open)
J135	12-B5	62-92	SMA- A_HDINN3_R		See section 8
J136	12-B4	57-97	SMA- A_HDOUTN3_R		See section 8
J137	12-B3	61-71	SMA- A_RXREFCLKN_R		(open)
J138	13-D5	79-41	Input Buffer VREF Select		1-3, 2-4
J139	13-C4	70-45	MSA Analog Inputs		(open)
J140	14-C4	86-45	MSA Header		(open)
J141	14-A5	72-22	MSA Power		(open)
J147	15-B4	79-20	MC VREF Select		1-3, 2-4
J148	16-B3	31-58	Shutdown MC VTT		2-3
J149	17-A5	32-74	LVDS Output Buffer CM Adj		1-3, 2-4

Name	Loc on Dwg ①	Loc on Bd ②	Description	③	Setting
J152	18-B4	45-42	Test Header		⑦
J153	18-B5	66-47	SMA- LVDS_INN		(open)
J154	18-B5	66-43	SMA- LVDS_INP		(open)
J161	18-A4	66-55	SMA- PLL Input LRC_PLLC		(open)
J162	18-A4	66-63	SMA- PLL Input LRC_PLLT		(open)
J163	18-A4	66-51	SMA- DLL Input LRC_DLLC		(open)
J164	18-A4	66-59	SMA- DLL Input LRC_DLLT		(open)
J165	18-A3	59-51	SMA- 50_OHM_2		(open)
J166	18-A3	59-55	SMA- 50_OHM_1		(open)
J167	18-A2	59-43	SMA- 50_OHM_4		(open)
J168	18-A2	59-47	SMA- 50_OHM_3		(open)
J181	18-B5	59-59	SMA- LVDS_OUTN		(open)
J182	18-B5	59-63	SMA- LVDS_OUTP		(open)
PWR1	2-D1	00-12	Power Connector	✓	See Section 3
SW1	2-D2	08-11	Power Switch	✓	Right (on)
SW2	10-C5	20-44	FPGA Reset		(Momentary)
SW3	10-C5	23-44	PROGRAM		(Momentary)
SW4	10-B5	26-50	FPGA LSRN		(Momentary)
SW5	10-A5	26-46	FPGA LSR		(Momentary)
SW6	10-A2	26-52	FPGA Mode Select	✓	"1010"
SW7	11-B3	28-44	IspCLOCK Controls #1		All Off
SW8	11-B5	13-44	IspCLOCK Controls #2	✓	See Section 3.1
SW9	13-B3	76-38	MSA Control #1		All Off
SW10	13-B2	75-25	RX_Reset		(Momentary)
SW11	13-B3	76-35	MSA Control #2		All Off
SW12	13-B2	80-25	TX_Reset		(Momentary)
SW13	13-A3	76-32	MSA Control #3		All Off
SW14	18-D5	36-44	Test Control #1		App. specific
SW15	18-D5	40-44	Test Control #2		App. specific
SW16	18-D5	44-44	Test Control #3		App. specific
SW17	18-C5	48-44	Test Control #4		App. specific
SW18	18-C5	52-44	Test Control #5		App. specific
SW19	18-C5	56-44	Test Control #6		App. specific
SW20	10-B4	62-79	Flash Select		"00100001"
TB1	2-D4	99-15	Terminal Block Power Input		(open)
TB2	2-C4	99-32	Terminal Block Power Input		(open)
TB4	14-A4	87-00	Terminal Block MSA Ext Pwr Input		(open)

**Notes:**

- ① The "Loc on Dwg" column specifies the component's location on the schematic, in page and sector form.
- ② The "Loc on Bd" column specifies the component's location on the board, in the form xx-yy. With the board oriented such that the Lattice logo is upright, xx specifies the x-position, where 00 is the left edge and 99 is the right edge, and yy specifies the y-position, where 00 is the bottom edge and 99 is the top edge.
- ③ When checked, the settings differ from the default settings.
- ④ INITN illuminates when the LatticeSC device is reset or a configuration error occurs.
- ⑤ DONE illuminates when the LatticeSC device is properly configured.
- ⑥ TDI flashes when there is activity on the JTAG interface.
- ⑦ The default configuration for J152 places 24 jumpers connecting the middle and lower pins (e.g., 1-2, 4-5, etc.), so that the 24 LEDs are each tied to a user I/O pin.

## 6. Loading the LatticeSC SERDES Eye/Backplane Demo bitstream

There are two ways to download the SERDES demo bitstream:

- Via the via the pre-loaded SPI Flash bitstream
- Via ispVM, using the provided bitstream file.

### 6.1. Loading the bitstream via the pre-loaded SPI Flash

The LatticeSC 900-BGA Communications Platform Evaluation Board is shipped with three pre-configured demonstration designs available via the SPI Flash.

Included in the pre-programmed Flash, are a board startup design, SERDES evaluation design, and the FPGA IO evaluation design. The Flash has been programmed in a manner that allows the user to sequence between designs by toggling the PROGRAMN pushbutton (SW3 on the board).

The SPI Flash has been shipped with the WRITE PROTECTION enabled via a DIP-switch setting.

At power up the board startup design is loaded, the second design is the SERDES Eye Demo evaluation, and the third design is the FPGA IO design. It will sequence back to the board startup design if PROGRAMN is toggled while the third design is loaded.

**To summarize, pressing the PROGRAMN button once after power-up should load the SERDES eye Demo design.**

The JTAG USERCODE can be displayed with ispVM, which can indicate the current programmed design.

Design	Binary ID
START UP DESIGN	00000000000000000000000000000001
SERDES EYE DEMO	00000000000000000000000000000010
FPGA IO	00000000000000000000000000000011

### 6.2. Loading the bitstream with ispVM

Follow these steps to load the provided SERDES eye demo bitstream file with ispVM:

NOTE: Since the ORCA-stra GUI and ispVM both share the on-board JTAG interface, one should always make sure that the Continuous Polling check box in ORCAstra (see Figure 4) is unchecked prior to loading a bitstream via ispVM.

1. Make sure the ispDOWNLOAD cable is connected to board (J68) and PC.
2. Start the Lattice ispVM Program.
3. Click on the "Scan" icon.
4. In the new window (New Scan Configuration Setup), Double-Click on the FileName/IR-Length entry of the first row, then select LFSC3GA25E. A Device Information window should pop-up.
5. Make sure that Operation is set to Fast Program and Device Access Options is set to JTAG 1532 Mode.
6. Click on the Browse button. Browse to the directory where you have installed the SERDES Eye Demo directory, then to Serdes\Bitstreams\.
7. Select comm\_sc25\_serdes\_demo\_4.bit and click Open.
8. Click OK in the Device Information window.
9. Click on the GO green button in the ispVM window.
10. The download process should start. When it is done, the ispVM New Scan Configuration Setup window should indicate a PASS in the status column of the first row.
11. Also make sure the D10 DONE LED on the board is lit.



## 7. Running a Demo with the ORCAstra PCS View

This section describes the use of the PCS view of the ORCAstra GUI to interactively change flexiPCS SERDES buffer characteristics.

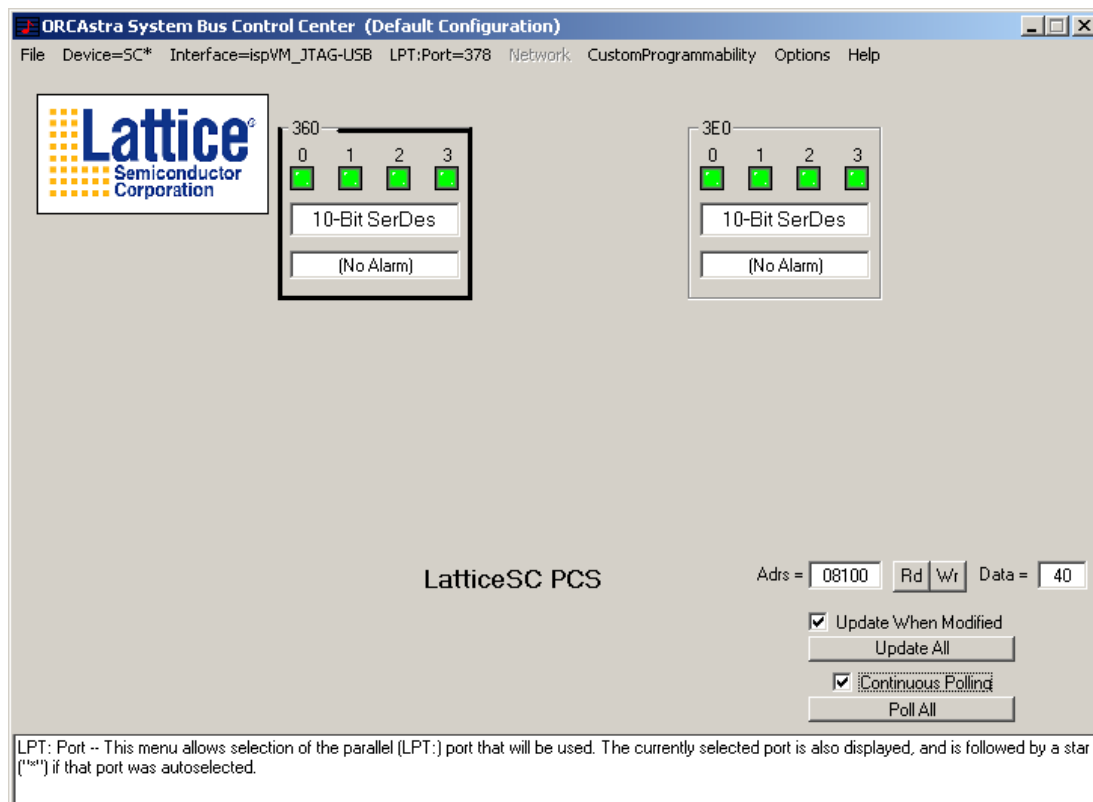
### 7.1. Selecting the flexiPCS views in ORCAstra

Assuming the LatticeSC SERDES Eye/Backplane Demo bitstream has been loaded:

1. Start an ORCAstra session.
2. In The ORCAstra GUI, select Interface->ispVM JTAG USB Interface.
3. In The ORCAstra GUI, select Device->Auto Device Detect/Select. ORCAstra should detect the latticeSC device. Click OK in the device detection window.
4. In The ORCAstra GUI, select Device->Lattice SC PCS.

At this point, the resulting GUI should look as in Figure 4. The Figure shows how ORCAstra recognizes that both flexiPCS 360 and 3E0 are active and configured in 10-Bit SERDES-only mode. The Design's PRBS Visual Window can now also be invoked as described in the PRBS Generator/Checker ORCAstra GUI section.

**Figure 4. Lattice PCS ORCAstra View**



## 7.2. Configuring SERDES Buffer Options in ORCAstra

The following steps result in the Visual Window shown in Figure 5.

1. Select either the 360 or 3E0 frame in Figure 4
2. In the 10-Bits SerDes Only View, select the following Tabs:
  - Power, Resets & Alarms
  - SerDes Buffer Options
  - Clocking

**Figure 5. 10-Bit SerDes Only View**

**PCS 360**

Power, Resets & Alarms << SerDes Buffer Options << Clocking << Diagnostics >>

360

### 10-Bit SerDes Only

0 1 2 3 Enable  
Low-Speed Data (<500 Mbps)

a b c d e i f g h j  
10-bit Word Value  
10-bit Word Value NOT  
10-bit Word Mask

Code Octet HGF-EDCBA abcdei-fghj abcdei-fghj

Power, Resets and Alarms <<

0 1 2 3 Quad  
Power-Up  
TX Datapath Reset  
RX Datapath Reset  
SERDES Reset  
Loss of PLL Lock  
Loss of Ext. REFCLK Signal  
Loss of Ext. RXREFCLK Signal

0 1 2 3  
HDIN LOS LO Threshold  
HDIN LOS HI Threshold  
CDR Loss of Lock to Data  
LOS Threshold  
LO = 100 mV p-p, HI = 175 mV p-p

SerDes Buffer Options <<

Channel 0	Channel 1	Channel 2	Channel 3
<b>Transmit</b>		<b>Receive</b>	
000 = 00% 00 = default 00 = 50 Ohm		0 = +6 dB 0 = AC 00 = 50 Ohm	
Pre-Emphasis Amplitude Termination		Equalization Coupling Termination	
<b>RefClk</b>			
0 = AC Coupling		0 = AC RX Coupling	

Clocking <<

00 = Single external source for TX and RX  
Reference Clock Source

00 = 20X or 16X  
REFCLK Multiplier

0 1 2 3  
TX Half Rate  
RX Half Rate

Caution: LatticeSC designs are optimized for a specific REFCLK clock rate at the time of compilation, and will tolerate only small deviations at execution time.

### 7.2.1. Power, Reset and Alarms View

This view allows the user to identify which channels (or the entire QUAD), are powered down or reset. Also, the High and Low Thresholds for LOS can be set here. Finally, loss of lock or signal for PLL and SERDES input data and reference clocks are also displayed. In normal operation, only the Green LEDs should be glowing (Continuous Polling should be checked in main ORCAstra window).

### 7.2.2. Clocking View

This view allows the user to identify the clocking mode (source of reference clock, reference clock multiplication, and whether a channel is in full or half rate).

### 7.2.3. SerDes Buffer Options View

This is the most relevant View for the SERDES Eye/Backplane Demo design, as it allows controlling the characteristics of output, input, and reference clock buffers.

**TX Buffer Pre-emphasis:** can be 0, 16, 32, 64, 80, or 48%.

**TX Buffer Amplitude Offset (from 1000mV):** can be 0, -12, -25, or 12%.

**TX Buffer Termination:** can be 50, 75, or 5K ohms.

**RX Buffer Equalization:** can be 0, +6 or +12 db.

**RX DC Coupling:** Couples the inputs SERDES buffers to 5pf internally.

**RX Buffer Termination:** can be 50, 60, 75, or 2K ohms.

**RefClk DC Coupling:** Couples the reference clock buffers to 5pf internally.

**RX RefClk DC Coupling:** Couples the RX reference clock buffers to 5pf internally.

## 8. Typical Backplane Demo Applications

As mentioned earlier, the serial data stream can be:

- Looped back via a cable on the evaluation board, or
- Sent to a DCA or SDA for eye viewing.

FlexiPCS quad 360 and 3E0 SERDES outputs can be sent to both a DCA (requires external trigger input) and an SDA for eye viewing.

The following sections describe both applications.

### 8.1. SERDES Eye/Backplane Demo

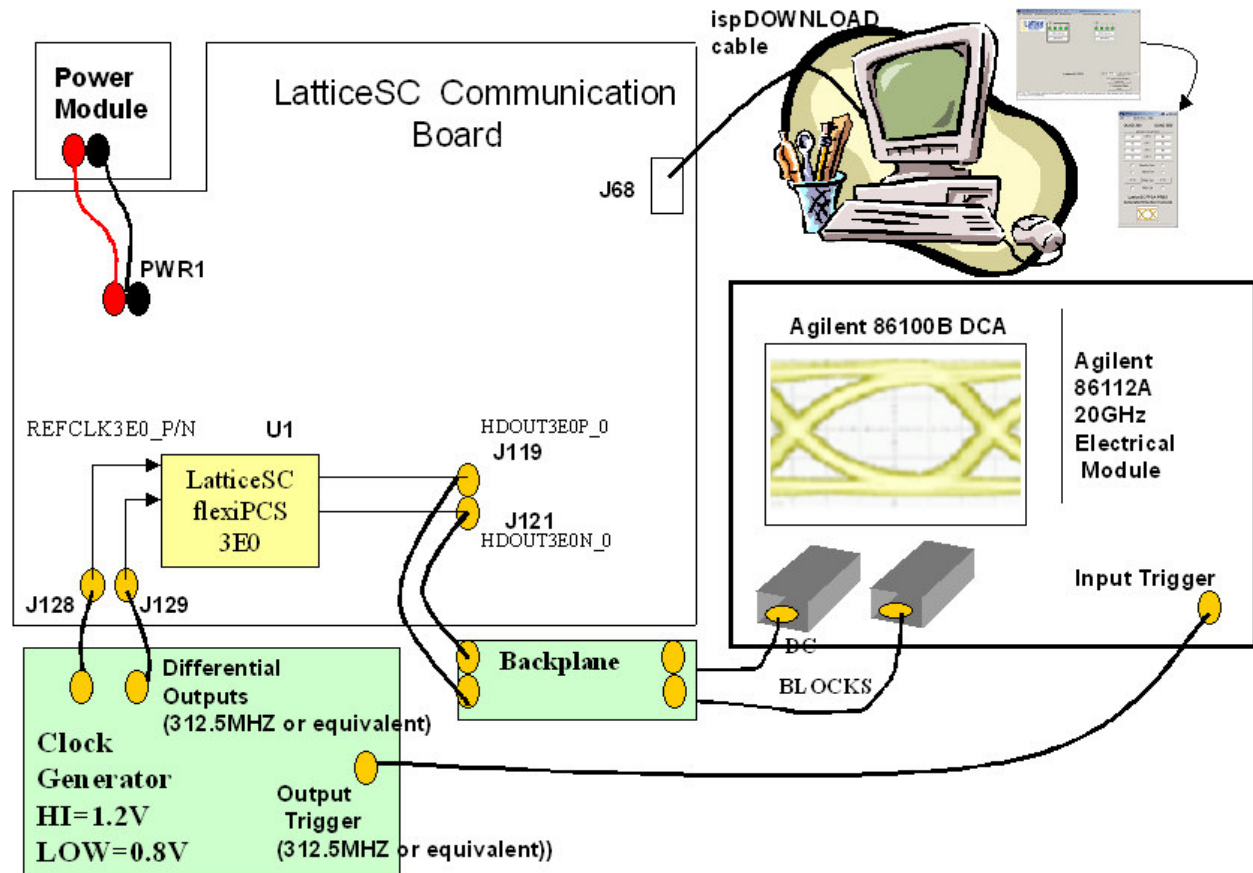
As mentioned earlier, an eye demo can be performed with either an SDA or DCA instrument. DCA instruments provide a much higher degree of precision eye viewing than SDA instruments. DCA instruments require an external trigger.

The following sections illustrate a DCA eye viewing demonstration with flexiPCS 3E0 and an SDA eye demo demonstration with flexiPCS 360.

### 8.1.1. DCA Eye Demo with flexiPCS quad 3E0

A typical DCA SERDES Eye/Backplane Demo application with flexiPCS 3E0 is illustrated in Figure 6.

Figure 6. Typical DCA SERDES backplane Eye Demo on flexiPCS QUAD 3E0



The setup is as follows:

- External clock generator applies differential clock inputs to refclk3E0\_n/p (J128 and J129).
- The external clock frequency is 312.5MHz (or equivalent).
- The external clock levels (per terminal) are VHI=1.2V, VLO=0.8V.
- The external clock generator applies an output trigger to the DCA input trigger.
- Channel 0's high speed outputs (J119 and J121) are connected via high-speed SMA cables to SMA terminals on the backplane.
- The other terminals on the backplane are connected to DC blocks (directly connected to the DCA input terminals) via high-speed SMA cables.
- Tie the 50-ohm to ground SMA terminations to SERDES outputs of channels 1, 2 and 3.

The following steps describe the demo sequence:

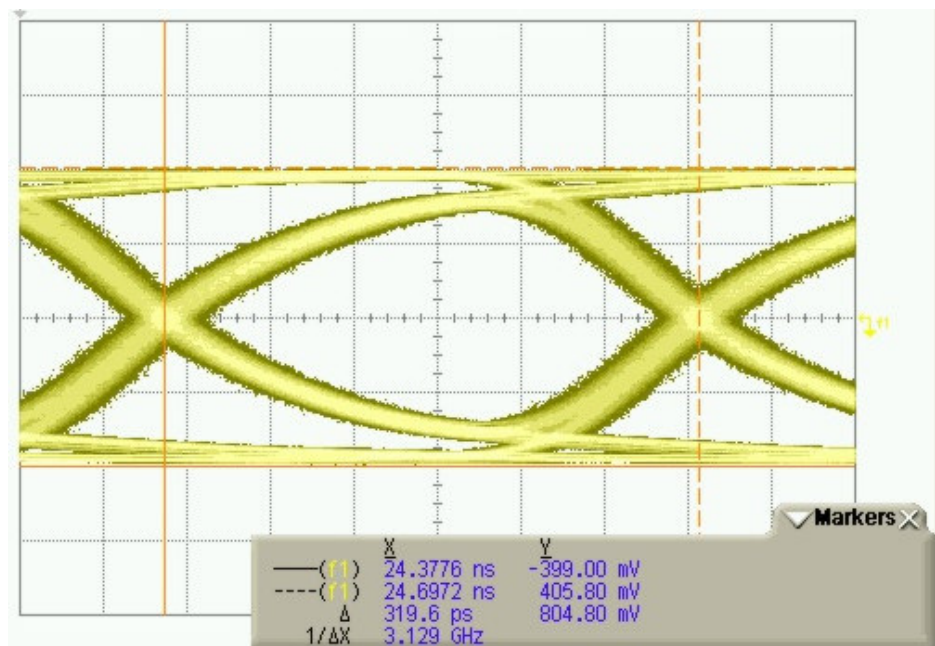
1. Make sure power is supplied to the Communication Platform evaluation board.
2. Load the LatticeSC SERDES Eye/Backplane Demo bitstream.
3. Make sure the external clock generator's outputs are toggling.
4. Start an ORCAstra session.
5. In The ORCAstra GUI, select Interface->ispVM JTAG USB Interface.
6. In The ORCAstra GUI, select Device->Lattice SC PCS. You should now get Figure 4.

7. Open ORCAstra and select CustomProgrammability->Visual Window. An empty window will appear.
8. Select File->Open and select the ORCAstra Plug-ins\EyeDemo.vis file provided with the demo. Figure 2 provides a screen capture of this window. This is the PRBS Generator/Checker QUAD ORCAstra Plug-in Visual Window.
9. Make sure the Continuous Polling box is checked in the main window.
10. In the PRBS visual window, select  $2^7$  or  $2^{31}$  for QUAD 3E0.
11. In the PRBS visual window, check the PRBS EN box for QUAD 3E0.

At this point, a PRBS eye should appear on the DCA screen. As a reference point, Figure 7 illustrates a 3.125Gbps differential eye obtained after the above steps were performed ( $2^7$  PRBS mode) with the SERDES output SMAS (J119 and J121) connected directly to the DC blocks (**no backplane**).

In a typical back-plane application, the SERDES Buffer Options View of flexiPCS in ORCAstra (Figure 5) allows real-time modification of output buffer characteristics, as different backplane lengths are utilized to maintain a clean SERDES Eye Diagram at the DCA input. Invoking this Visual window is described in the Configuring SERDES Buffer Options in the ORCAstra section of this document. Make sure flexiPCS 3E0 is first selected from the main ORCAstra window. Changes to the eye of Figure 7 can be observed once any of the TX buffer options (amplitude, pre-emphasis, coupling) are changed.

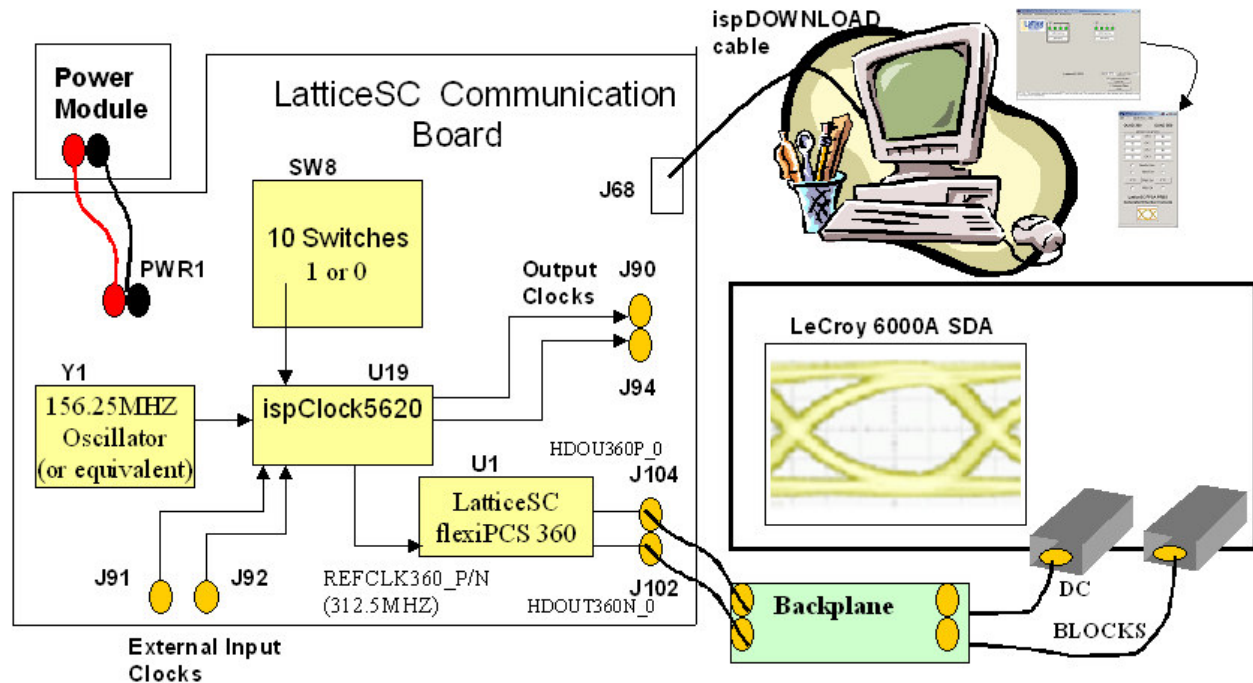
**Figure 7. DCA Differential Eye Diagram with flexiPCS QUAD 3E0 and no backplane**



### 8.1.2. SDA Eye Demo with flexiPCS quad 360

A typical SDA SERDES Eye/Backplane Demo application with flexiPCS 360 is illustrated in Figure 8.

Figure 8. Typical SDA SERDES backplane Eye Demo on flexiPCS QUAD 360



The setup is as follows:

- Clock setup for QUAD 360 as described in the Clocking Scheme for 360 flexiPCS section of this document.
- Channel 0's high speed outputs (J104 and J102) are connected via high-speed SMA cables to SMA terminals on the backplane.
- The other terminals on the backplane are connected to DC blocks (directly connected to the SDA input terminals) via high-speed SMA cables.
- Tie the 50-ohm to ground SMA terminations to SERDES outputs of channels 1, 2 and 3

If looking at an eye with a DCA instrument, then either SMA J90 or J94 can be used as the trigger to the DCA trigger input.



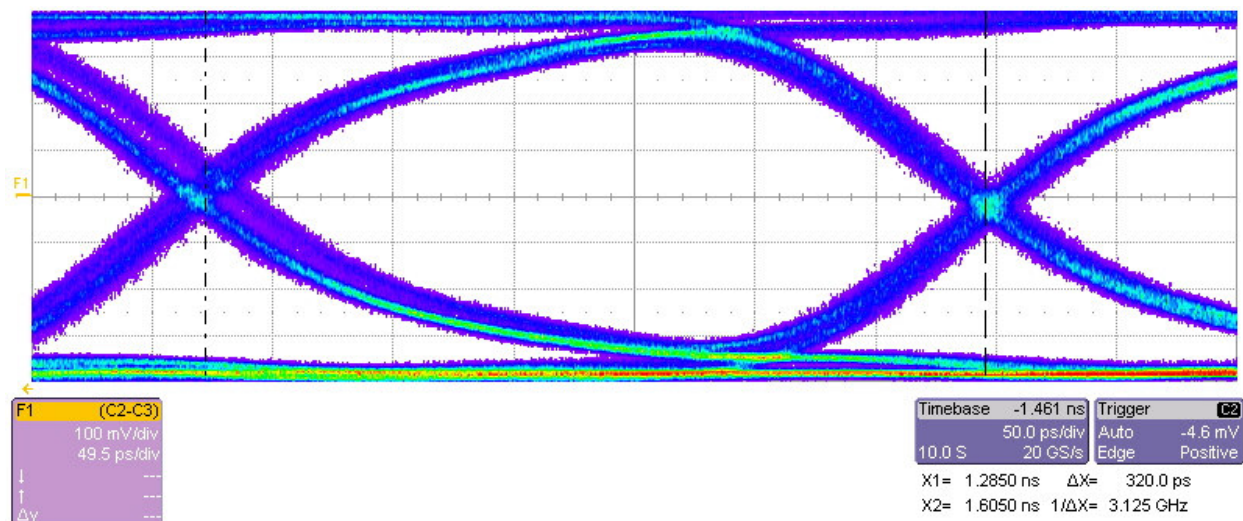
The following steps describe the demo sequence:

1. Make sure power is supplied to the Communication Platform evaluation board.
2. Load the LatticeSC SERDES Eye/Backplane Demo bitstream.
3. Make sure the D14 LED is glowing to indicate that the ispClock5620 module is locked
4. Start an ORCAstra session.
5. In The ORCAstra GUI, select Interface->ispVM JTAG USB Interface.
6. In The ORCAstra GUI, select Device->Lattice SC PCS. You should now get Figure 4.
7. Open ORCAstra and select CustomProgrammability->Visual Window. An empty window will appear.
8. Select File->Open and select the ORCAstra Plug-ins\EyeDemo.vis file provided with the demo. Figure 2 provides a screen capture of this window. This is the PRBS Generator/Checker QUAD ORCAstra Plug-in Visual Window.
9. Make sure the Continuous Polling box is checked in the main window.
10. In the PRBS visual window, select  $2^7$  or  $2^{31}$  for QUAD 360.
11. In the PRBS visual window, check the PRBS EN box for QUAD 360.

At this point, a PRBS eye should appear on the SDA screen. As a reference point, Figure 9 illustrates a 3.125Gbps differential eye obtained after the above steps were performed ( $2^7$  PRBS mode) with the SERDES output SMAS (J104 and J102) connected directly to the DC blocks (**no backplane**). A LeCroy setup file is available at Misc\lecroy6000A.iss. This file contains the configuration options used with the SDA to obtain the SDA eye. Note that the differential inputs to the SDA were fed to the C2 and C3 terminals.

In a typical back-plane application, the SERDES Buffer Options View of flexiPCS in ORCAstra (Figure 5) allows real-time tweaking of output buffer characteristics, as different backplane lengths are utilized to maintain a clean SERDES Eye Diagram at the SDA input. Invoking this Visual window is described in the Configuring SERDES Buffer Options in ORCAstra section of this document. Make sure flexiPCS 360 is first selected from the main ORCAstra window. Changes to the eye of Figure 9 can be appreciated if any of the TX buffer options (amplitude, pre-emphasis, coupling) are changed.

**Figure 9. SDA Differential Eye Diagram with flexiPCS QUAD 360 and no backplane**



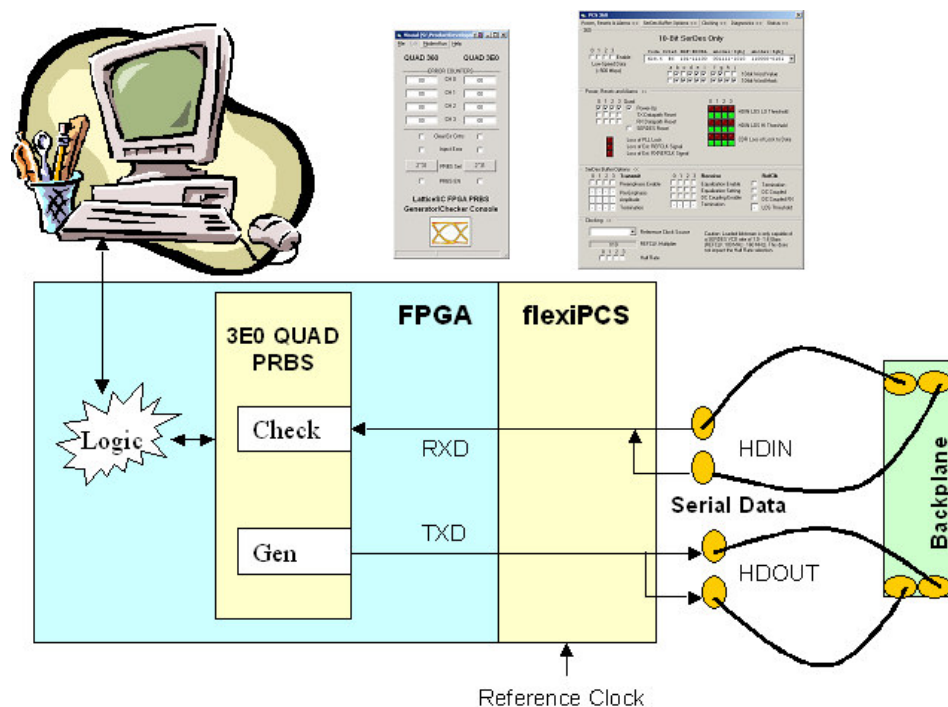
## 8.2. PRBS Loopback Demo

In a typical PRBS back-plane loopback application:

- The FPGA PRBS Generator is used to transmit data from the FPGA to the flexiPCS TXD ports on a given channel
- The flexiPCS SERDES HDOUT pins are connected to a backplane through SMA cables.
- The other backplane terminals connect to the flexiPCS HDIN channel inputs through SMA cables.
- The flexiPCS RXD ports then feed the recovered data to the FPGA PRBS QUAD checker.

This type of application is illustrated in Figure 10. This setup applies to either flexiPCS 360 or 3E0.

**Figure 10. Typical PRBS Loopback Application**



This application can make use of the PRBS Generator/Checker QUAD ORCAstra Plug-in Visual Window from Figure 2 and the SerDes Buffer Options ORCAstra View (see Figure 5). While looping PRBS data on any given channel the first window is used to verify error-free PRBS data is received, while the second window is used to tweak output and input buffer options (as different backplane lengths are used).



The following steps describe how to run through a typical  $2^{31}$  PRBS loopback demo on channel 0 of flexiPCS quad 360. The assumption is that the HDIN and HDOUT SMA (P, N) pairs are (J103, J105) and (J104, J102) respectively.

1. Load the LatticeSC SERDES Eye/Backplane Demo bitstream.
2. Make sure power is supplied to the Communication Platform evaluation board.
3. Make sure the external clock generator's outputs are toggling.
4. Make sure the D14 LED is glowing to indicate that the ispClock5620 module is locked.
5. Start an ORCAstra session.
6. In The ORCAstra GUI, select Interface->ispVM JTAG USB Interface.
7. In The ORCAstra GUI, select Device->Lattice SC PCS. You should now get Figure 4.
8. Open ORCAstra and select CustomProgrammability->Visual Window. An empty window will appear.
9. Select File->Open and select the ORCAstra Plug-ins\EyeDemo.vis file provided with the demo. Figure 2 provides a screen capture of this window. This is the PRBS Generator/Checker QUAD ORCAstra Plug-in Visual Window.
10. Select the 360 frame in Figure 4
11. In the 10-Bits SerDes Only View (Figure 5), open the following Tabs:
  - Power, Resets & Alarms
  - SerDes Buffer Options
12. Make sure the Continuous Polling box is checked in the main window.
13. In the PRBS visual window, select  $2^{31}$  for QUAD 360.
14. In the PRBS visual window, check the PRBS EN box for QUAD 360.
15. Clear the Error counter by checking and un-checking the Clear Error Counters check box for QUAD 360. Check the PRBS RED LED D36 on the board for channel 0 errors (see Table 3 for a complete list of error LEDs).
  - i. If the error count remains at zero after clearing, and LED D36 remains off, then the channel 0 checker is receiving error-free data. Check the Power, Resets & Alarms section of the 10-Bits SerDes Only View (Figure 5) to make sure no RED QUAD or channel 0 alarms are on.
  - ii. If the QUAD 360 channel 0's error counter does not remain at 0, and the D36 LED flickers (flicker will not be observable if errors occur at a slow rate).
    1. Verify that the Power, Reset and Alarm view of Figure 5 does not show any PLL loss of lock or reference clock loss of sync. If any of these alarms are on, then verify that the Y1 oscillator is properly working, and that the SW8 switches are properly set. Also try to reset the ispClock5620 lock by flipping switch number 2 of SW8 away from position 2 (D14 turns off). Switching it back to position 2 should allow D14 to turn on as ispClock5620 locks again to the input clock.
    2. Try modifying some of the input and output buffer settings in the SerDes Buffer Options section (TX pre-emphasis, TX amplitude, RX equalization...).
    3. Restart step 15.

## 9. Alternate Reference Clock Setting

The demonstrations described in the previous sections use differential clocks of 312.5MHZ to drive the flexiPCS reference clock inputs. This mode, where the data rate (3.125Gbps) is ten times the reference clocks frequency (312.5MHZ) is referred to as X10 mode.

Another supported mode is the X20 mode, whereby a 156.25MHZ reference clock frequency can be used to run at a 3.125Gbps data rate.

Even though X20 mode requires a lower reference clock frequency source than X10 mode, it nevertheless introduces more output jitter (to HDOUT\* pins) than X10 mode.

This section describes the modifications needed to run both 360 and 3E0 flexiPCS QUAD in X20 mode.

### 9.1. flexiPCS 3E0 Modifications

As shown in Figure 6, the reference clock inputs are driven directly from SMA J128 and J129 from the frequency generator. The following modifications are needed to run in X20 mode:

1. Change the frequency generator clock frequency from 312.5MHZ to 156.25MHZ.
2. Change the flexiPCS 3E0 PLL clock multiplier setting from X10 (default setting in bitstream) to X20. This requires changing the value of flexiPCS register h3E028 from 50 to 40. Entering an address of 3e028 and a data of 40 in the address and data fields of Figure 4, and pressing the Wr button accomplishes this.

### 9.2. flexiPCS 360 Modifications

As shown in Figure 8, since both the frequency oscillator and SMA J91 and J92 are already assumed to be providing a 156.25MHZ frequency, the following modifications are needed to run in X20 mode:

1. Bypass the ispCLOCK5620 PLL by allowing its inputs to directly drive its outputs. This provides the required 156.25MHZ frequency to the flexiPCS 360 QUAD. In order to achieve this, flip switches 8, 9 and 10 of SW8 to the ON position (see Table 2).
2. Change the flexiPCS 360 PLL clock multiplier setting from X10 (default setting in bitstream) to X20. This requires changing the value of flexiPCS register h36028 from 50 to 40. Entering an address of 36028 and a data of 40 in the address and data fields of Figure 4, and pressing the Wr button accomplishes this.

## 10. Reference Information

The following documents provide more information:

- *ispLEVER® Software User Manual*
- *LatticeSC Family flexiPCS Data Sheet*
- *LatticeSC Communications Platform Evaluation Board User's Guide*
- *ORCAstra™ System Bus control Panel User's Manual*

## 11. Technical Support Assistance

Hotline: 1-800-LATTICE (North America)  
+1-408-826-6002 (Outside North America)

e-mail: [techsupport@latticesemi.com](mailto:techsupport@latticesemi.com)

Internet: [www.latticesemi.com](http://www.latticesemi.com)