SYN1588®Clock_M IP-CORE

SYN1588® enabled IEEE 1588 compliant clock synchronization

The SYN1588®Clock_M IP-core provides highly accurate clock synchronization compliant to the IEEE 1588 standard 2002 and 2008. It contains a high resolution, high accuracy hardware clock which uses a 96-bit wide adder based clock architecture allowing supporting input clock frequencies in the range of 10 – 200 MHz. Furthermore the SYN1588®Clock_M comprises an MII-Scanner unit, which scans all Ethernet traffic in search for IEEE1588 synchronization packets. Upon detection of any such packet it draws a 96-bit wide time stamp from the local clock any copies it together with status and identification data into a so-called time-stamp FIFO.

The core is connected one of the system's Ethernet MII ports (according to IEEE 802.3 clause 22) and via a 32bit wide AHB bus interface to a local CPU as show in figure 1.

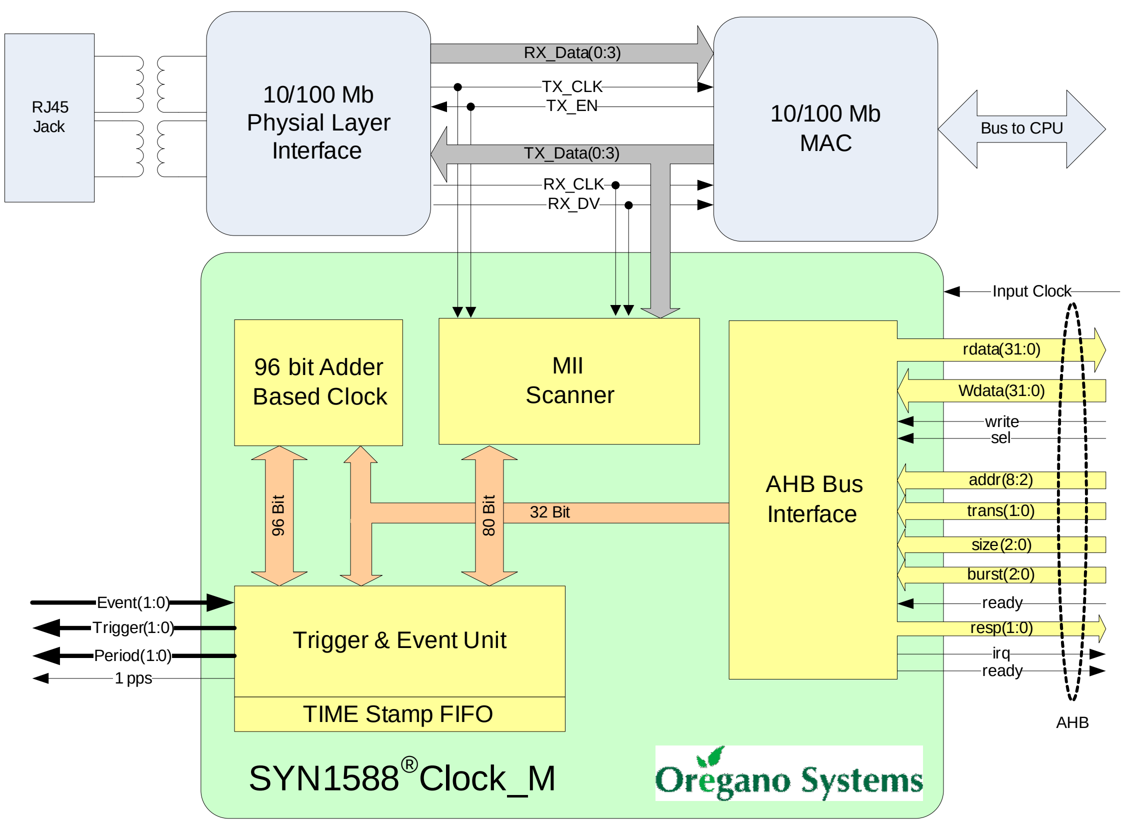

Figure 1: SYN1588®Clock_M block diagram

The Oregano System's SYN1588®Clock_M is intended to be integrated as a part of a larger FPGA design which may be attached to an external CPU as sown in figure 2. This solution requires both a MAC IP-core and a bus controller interface e.g. a PCI-controller to be added to the design. Both these cells are available from Oregano Systems upon request as ready to use add-ons to the SYN1588®Clock_M cell.

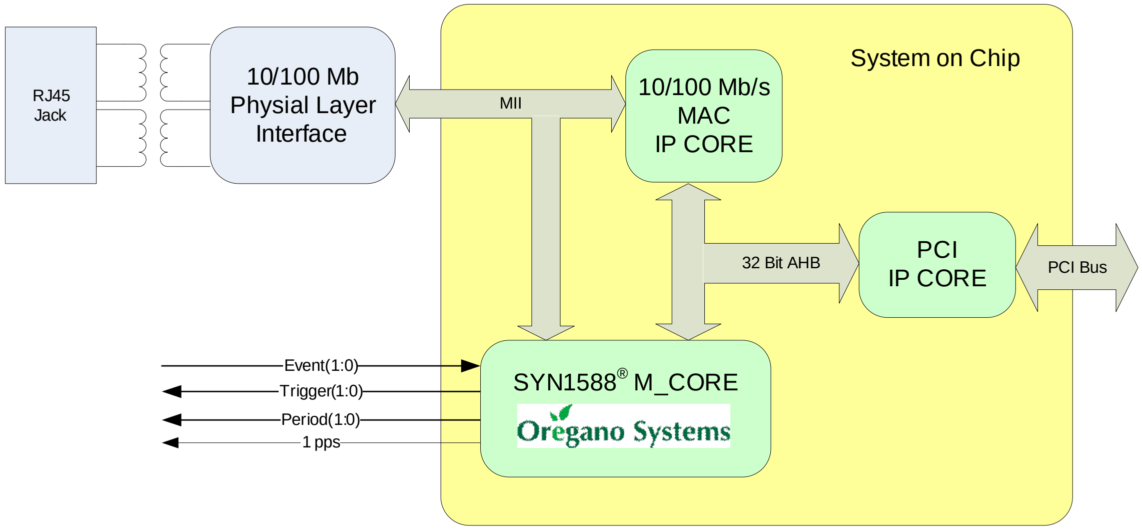

Figure 2: Block diagram of a typical Embedded System

Another system level option would be to build a complete SoC module capable of clock synchronization on its own and delivering synchronized time information by means of a 1pps signal or a phase locked frequency. Such a system is shown in figure 3, where the MICO32 core is suggested as a target CPU. This 32-bit core offered by LATTICE Semiconductor under GPL-like license conditions is suitable to run the drivers and the PTP-stack to operate as a fully functional IEEE1588 node.

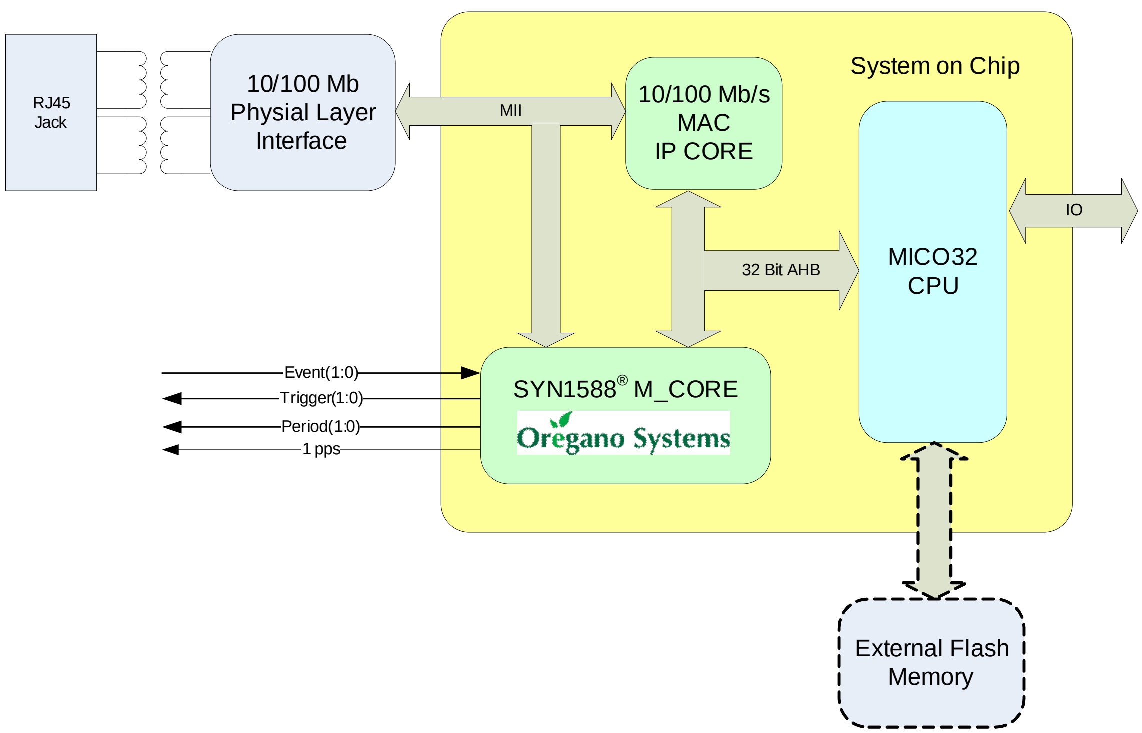

Figure 3: Block Diagram of a System on Chip

For layer 2 synchronization according to IEEE1588 (2008) please contact Oregano Systems

Features

- Seamless integration in SoCs
- The core is completely synchronous to the system clock
- All registers of the core operate with the rising edge of the system clock
- The clock time format is compatible to the IEEE1588 standard (2002 & 2008)
- Supports 10/100 Mbit/s half & full duplex modes
- RMII Interface option available upon request
- 32-bit fully compliant AHB-Bus Interface
  - operating at 66 MHz (XP family) or 150 MHz (XP2 family)
- 1 pps output
- 2 period timer outputs allowing generating user configurable output frequencies with a period ranging from 14,000 sec down to 100 nsec.
- 2 event inputs which draw a time stamp and store it in the time stamp FIFO upon polarity changes of the input pin.
- Events may be processed at a burst rate of 5 MHz. The sustained event rate processing capabilities are dependent on the performance of the host processor.
- 2 trigger output signals which may be used to generate a signal transition at a given point in time.
- All event, period, and trigger signals are strictly synchronous to the internal high accuracy clock.
- Coded in VHDL
- Delivered with test bench, 100% code coverage guaranteed
- Optional support of GPS timing receivers
- Delivered with PTP Version 1.0 and version 2.0 stack (Linux or Windows®)
- Layer 2 synchronization according to IEE1588 (2008) upon request

Resource utilization

Device	Slices	LUT4s	Registers	SysMEM EBRs	fMAX (MHz)
XP	2178	2866	1941	2	75
XP2	2069	2834	1941	2	125

For evaluation and licensing terms contact: www.oregano.at