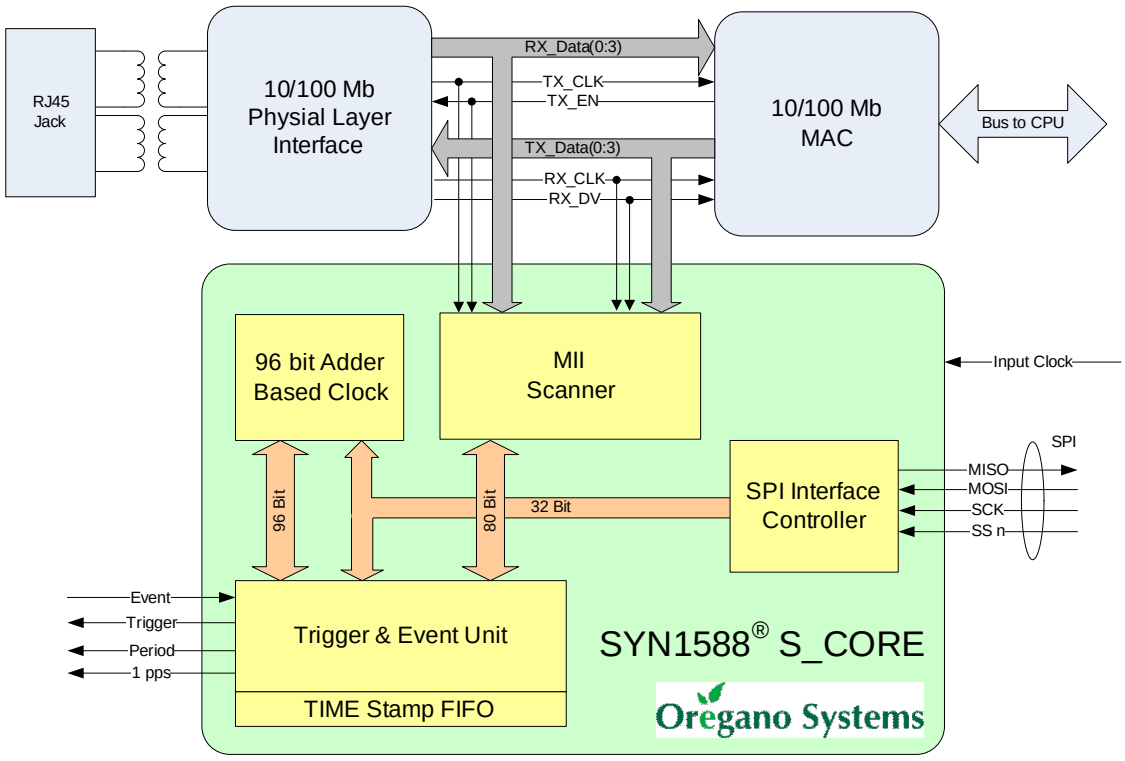
SYN1588®Clock_S IP-CORE

SYN1588® enabled IEEE 1588 compliant clock synchronization

The SYN1588®Clock_S IP-core provides highly accurate clock synchronization compliant to the IEEE 1588 standard version 1.0 and 2.0. It provides a high resolution, high accuracy hardware clock which uses a 96-bit wide adder based clock architecture allowing supporting input clock frequencies in the range of 10 – 200 MHz. Furthermore the SYN1588®Clock_S comprises an MII-Scanner unit, which scans all Ethernet traffic in search for IEEE1588 synchronization packets. Upon detection of any such packet it draws a 96-bit wide time stamp from the local clock any copies it together with status and identification data into a so-called time-stamp FIFO.

The core is connected to the system's Ethernet MII port (according to IEEE 802.3 clause 22) and an SPI port of the host processor of the node as shown in the following figure.



The Oregano System's SYN1588®Clock_S is intended to be used in embedded systems with stringent requirements on both space and costs. It easily fits into the smallest members of both the LATTICE XP and XP2 families as a single chip addition to existing designs

Features

- Small footprint and small I/O count
- The core is completely synchronous to the system clock
- All registers of the core operate with the rising edge of the system clock
- The clock time format is compatible to the IEEE1588 standard
- Supports 10/100 Mbit/s half & full duplex modes
- RMII Interface option available upon request
- Supports SPI cascade and independent slave mode
- SPI data rates up to 20 Mbit/sec
- 16-bit SPI data transfers
- 32 bit interface to the internal SPI controller
- 1 pps output
- 1 period timer output allowing to generate user configurable output frequencies with a period ranging from 14,000 sec down to 200 nsec.
- 1 event input which draws a time stamp and stores it in the time stamp FIFO upon polarity changes of the input pin.
- Events may be processed at a burst rate of 1 MHz. The sustained event rate is dependent on the performance of the host processor.
- 1 trigger output signal which may be used to generate a signal transition at a given point in time
- All event, period, and trigger signals are strictly synchronous to the internal high accuracy clock.
- Coded in VHDL
- Delivered with test bench, 100% code coverage guaranteed
- Optional support of GPS timing receivers
- Delivered with PTP Version 1.0 and version 2.0 stack (Linux or Windows®)

Resource utilization

Device	Slices	LUT4s	Registers	SysMEM EBRs	fMAX (MHz)
XP	1668	1954	1726	4	75
XP2	1552	1968	1591	4	125

For evaluation and licensing terms contact: www.oregano.at