LatticeSC/M Hardware Checklist

June 2008 Technical Note TN1167

Introduction

When designing complex hardware using the LatticeSC™ or LatticeSCM™ FPGAs, designers must be attentive to critical hardware configuration requirements. This technical note steps through these critical hardware implementation items relative to the LatticeSC/M device. The document will not provide detailed step-by-step instructions but will give a high-level summary checklist to assist in the design process.

The device family consists of FPGA LUT densities ranging from 15K to115K. This technical note assumes that the reader is familiar with the LatticeSC/M device features as described in the LatticeSC/M Family Data Sheet. The data sheet includes the functional specification for the device. Topics covered in the data sheet include but are not limited to the following:

- High-level functional overview
- Pinouts and packaging information
- Signal descriptions
- Device-specific information about peripherals and registers
- Electrical specifications

Please refer to the data sheets for the device-specific details.

- DS1004 - LatticeSC/M Family Data Sheet
- DS1005 - LatticeSC/M flexiPCS™ Data Sheet

The critical hardware areas covered in this technical note are:

- Power supplies as they relate to the LatticeSC/M supply rails and how to connect them to the PCB and the associated system
- Configuration mode selection for proper power-up behavior
- Device I/O interface and critical signals

Please refer to the following technical notes for detailed recommendations.

- TN1114 - Electrical Recommendations for Lattice SERDES
- TN1088 - LatticeSC PURESPEED™ I/O Usage Guide
- TN1080 - LatticeSC sysCONFIG™ Usage Guide

Power Supplies

All power supplies including V_{CC}, V_{CC12}, $V_{CCIO1-7}$, V_{CCJ} and V_{CCAUX} (SERDES power supplies excluded) determine the LatticeSC/M internal power good condition. These supplies need to be at a valid and stable level before the device can become operational. Table 1 shows the power supplies and the appropriate voltage levels for each supply.

Table 1. LatticeSC/M FPGA Power Supplies

Supply	Voltage (Nominal Value)	Description
VCC	1.0V to 1.2V	FPGA core power supply.
VCC12	1.2V	Power supply for PLL and analog SERDES blocks. Should be isolated and "clean" from excessive noise.
VCCIO1-7	1.2V to 3.3V[1]	I/O power supply. Seven general purpose I/O banks and each bank has its own supply V_{CCIO0} to V_{CCIO7}. V_{CCIO1} is used in conjunction with the pins dedicated and shared with device configuration.
V_{CCAUX}	2.5V	Independent I/O power supply
VCCJ	1.8V to 3.3V	JTAG power supply for the TAP controller port.

1. Banks 1, 4, and 5 can be 3.3V. Banks 2, 3, 6, and 7 can only be used with 2.5V maximum power supplies.

The LatticeSC/M FPGA has a power-up reset state machine that depends on various power supplies. A power-up reset counter will begin to count after all of the approximate conditions are met:

- V_{CC} reaches 0.5V or above
- V_{CC12} reaches 0.5V or above
- V_{CCAUX} reaches 1.0V or above
- $V_{CCIO[1:7]}$ reaches 0.5V or above
- V_{CCJ} reaches 0.5V or above

Configuration of the device will not proceed until the last power supply has reached its minimum operating voltage.

LatticeSCM SERDES/PCS Power Supplies

Supplies dedicated to the operation of the SERDES/PCS include V_{CC12}, V_{DDAX25}, V_{DDIB} and V_{DDOB}. All V_{CC12} and V_{DDAX25} supply pins must always be powered to the recommended operating voltage range regardless of the SERDES use. V_{DDAX25} can be connected to the standard FPGA 2.5V power supplies since the noise levels of these supplies are not critical. V_{CC12} should always be provided a noise-free power supply. V_{DDIB} and V_{DDOB} can be left floating for unused SERDES channels. Unused channel outputs are tri-stated, with approximately 10 K-ohm internal resistor connecting between the differential output pair.

When using the SERDES with 1.5V V_{DDIB} or V_{DDOB}, the SERDES should not be left in a steady state condition with the 1.5V power applied and the V_{CC12} 1.2V power not applied. Both the 1.2V and the 1.5V power should be applied to the SERDES at nominally the same time. The normal variation in ramp-up times of power supplies and voltage regulators is not a concern.

It is very important that the V_{CC12} supply be low-noise and isolated from heavily loaded switching supplies. Please refer to technical note TN1114, *Electrical Recommendations for Lattice SERDES*.

Power Supply Sequencing

To prevent high power supply and input pin currents, each V_{CC}, V_{CC12}, V_{CCAUX}, $V_{CCIO[1:7]}$ and V_{CCJ} power supplies must have a monotonic ramp up time of 75 ms or less to reach its minimum operating voltage. V_{CC}, V_{CC12}, V_{CCAUX}, $V_{CCIO[1:7]}$ and V_{CCJ} power supplies can ramp up in any order, with no restriction on the time between them. However, the ramp time for each must be 75 ms or less. Additional supply requirements need consideration for V_{CC}, V_{CC12}, V_{CCIO}, and V_{CCAUX}.

Additional Requirement for V_{CC} and V_{CC12}

V_{CC12} must always be higher than V_{CC}. This condition must be maintained at ALL times, including during power-up and power-down. Note that for 1.2V only operation, it is advisable to source both of these supplies from the same power supply.

Additional Requirement for V_{CCIO} and V_{CCAUX}

If any V_{CCIO} is 1.2/1.5/1.8V, then V_{CCAUX} MUST be applied before them. If any V_{CCIO} is 1.2/1.5/1.8V and is powered up before V_{CCAUX}, then when V_{CCAUX} is powered up, it may drag V_{CCIO} up with it as it crosses through the V_{CCIO} value.

Power Estimate

Once the LatticeSC/M device density, package and logic implementation is decided, power estimation for the system environment should be determined based on the Power Calculator provided as part of the ispLEVER® design tool. When estimating power, the designer should keep two goals in mind:

1. Power supply budgeting should be based on the maximum DC and AC current for the given system's environmental conditions.
2. The ability for the system environment and LatticeSC/M device packaging to be able to support the specified maximum operating junction temperature.

By determining these two criteria, LatticeSC/M power requirements are taken into consideration early in the design phase.

Configuration Considerations

The LatticeSC includes provisions to program the FPGA via a JTAG interface or though several modes utilizing the sysCONFIG port. The JTAG port includes a 4-pin interface. The interface requires the following PCB considerations.

Table 2. JTAG Pin Recommendations

JTAG Pin	PCB Recommendation
TDI	10K-ohm Pullup to V_{CCJ}
TMS	10K-ohm Pullup to V_{CCJ}
TDO	10K-ohm Pullup to V_{CCJ}
TCK	10K-ohm Pull-down

Using other programming modes requires the use of the MODE[3:0] input pins. For JTAG, the MODE pins are not used. The MODE[3:0] pins include weak internal pull-ups. It is recommended that 5-10K external resistors be used when using the sysCONFIG modes. Pull-up resistors should be connected to V_{CCIO1}.

The use of external resistors is always needed if the configuration signals are being used to handshake to other devices. Recommended 5 to 10K-ohm pull-up resistors to V_{CCIO1} should be used on the following pins.

Table 3. Pull-up Recommendations for Configuration Pins

PROGRAMN
PINITN
PRESETN
PRDCFGN
MPIIRQN

I/O Pin Assignments

The V_{CC12} provides a quiet supply for the internal PLLs and critical SERDES blocks. For the best jitter performance, careful pin assignment will keep noisy I/O pins away from "sensitive" pins. The leading cause of PCB-related SERDES crosstalk is related to FPGA outputs located in close proximity to the sensitive SERDES power supplies. These supplies require cautious board layout to insure noise immunity to the switching noise generated

by FPGA outputs. Guidelines are provided to build quiet filtered supplies for the V_{CC12}, however robust PCB layout is required to insure that noise does not infiltrate into these analog supplies.

Although coupling has been reduced in the device packages of the LatticeSC devices where little crosstalk is generated, the PCB board can cause significant noise injection from any I/O pin adjacent to SERDES data, reference clock, and power pins as well as other critical I/O pins such as clock signals. Technical note TN1114, *Electrical Recommendations for Lattice SERDES*, provides detailed guidelines for optimizing the hardware to reduce the likelihood of crosstalk to the analog supplies.

LVDS Pin Assignments

True LVDS outputs are available on 50% of the I/O pins on the left and right sides of the device. The left- and right-side I/O banks are banks 2, 3, 6 and 7. When using the LVDS outputs, only the A and B pads of an I/O cell can be used. Note that differential drivers are not supported in Banks 1, 4 and 5.

LVDS inputs are available on any A and B or C and D pad of all I/O cells around the device. The LatticeSC device allows two types of differential termination. The first is a single resistor across the differential inputs. The second is a center-tapped system where each input is terminated to the on-chip termination bus V_{CMT}. The V_{CMT} bus is DC-coupled through an internal capacitor to ground.

If a differential driver is configured in a bank, one pin in that bank becomes a DIFFR pin. This DIFFR pin must be connected to ground via an external 1K +/-1% ohm resistor.

Differential drivers have user selectable internal or external bias. The dedicated V_{REF1} pin for the bank connects external bias. External bias for differential buffers is needed for applications that requires tighter than standard output common mode range. Since a bank can have only one external bias circuit for differential drivers, LVDS and RSDS differential outputs can be mixed in a bank but not with HYPT (HyperTransport™).

HSTL and SSTL Pin Assignments

These externally referenced I/O standards require an external reference voltage. The V_{REF} pin(s) should get high priority when assigning pins on the PCB. Each bank can support up to two separate V_{REF} voltages, V_{REF1} and V_{REF2}, set the threshold for the referenced input buffers. In the LatticeSC/M devices, any I/O pin in a bank can also be configured to be a dedicated reference voltage supply pin however the predefined V_{REF} pins provide the best case. Each I/O is individually configurable based on the bank's supply and reference voltages.

In addition, there are dedicated Terminating Supply (V_{TT}) pins to be used as terminating voltage for one of the two ways to perform parallel terminations. These V_{TT} pins are available in banks 2 to 7, these pins are not available in some packages. Unused V_{TT} pins should be connected to GND if the internal or external V_{CMT} function is not used in the bank. If the internal or external V_{CMT} function for differential input termination is used, the V_{TT} pins should be unconnected and allowed to float.

A calibration resistor is used to compensate output drivers. A 1K-ohm +/-1% resistor connected between the XRES pin and PCB ground is needed.

SERDES Pin Considerations

REFCLK Inputs

A recommended 100-ohm differential termination resistance is required at the input to the SERDES REFCLK inputs. The resistor should be as close to the device as possible.

RESP

The SERDES requires external bias generation utilizing a 4.02K-ohm resistor. Depending on the device package, this resistor will be connected between the RESP pin and PCB ground or between RESP and another dedicated RESPN pin. Refer to the LatticeSC/M Family Data Sheet for specific details.

Table 4. Hardware Checklist

	Item	OK	NA
1	**FPGA Power Supplies**		
1.1	V_{CC} core @ 1.0V -1.2V +/-5%		
1.2	V_{CC12} @ 1.2V +/-5%		
1.2.1	V_{CC12} “quiet” and isolated		
1.3	All V_{CCIO} 1.2V to 3.3V (3.3V Banks 1, 4, 5, only)		
1.4	V_{CCJ} 1.2V to 3.3V		
1.5	FPGA power supply sequencing/ramping		
1.6	Power estimate		
1.7	1K-ohm +/-1% pull-down on XRES pin		
2	**SERDES Power Supplies**		
2.1	V_{CC12} “quiet” and isolated; all V_{CC12} supply pins must be connected to a voltage supply		
2.2	V_{DDAX25} connected to 2.5V source (whether SERDES is used or not used)		
2.3	V_{DDIB} and V_{DDOB} connected for USED SERDES channels		
3	**Configuration**		
3.1	Pull-ups and pull-downs on configuration specific pins		
3.2	V_{CCIO1} bank voltage matches sysCONFIG peripheral devices such as SPI Flash		
4	**SERDES**		
4.1	RESP 4.02K-ohm +/-1% external bias resistors connected		
4.2	100-ohm differential resistor across REFCLKP and REFCLKN for used channels		
5	**Special Pin Assignments**		
5.1	1K-ohm +/-1% pull-down resistors on DIFFR for differential drivers		
5.2	V_{REF} assignments followed for single-ended HSTL or SSTL inputs		
5.3	V_{TT} pins		
5.3.1	V_{TT} needed for parallel termination connected to termination power supply		
5.3.2	V_{TT} is shared with V_{CMT} for differential receiver termination and should float or connect to external capacitor		

Technical Support Assistance

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Revision History

Date	Version	Change Summary
August 2007	01.0	Initial release.
June 2008	01.1	Modified description for item 2.1 in the Hardware Checklist table.

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