



W65C02SRTL: 8-Bit 65xx Microprocessor

The W65C02SRTL Soft Core from The Western Design Center is a general purpose 8-bit Microprocessor Core. The core was designed to emulate the available W65C02S GDSII Hard Core. This characteristic makes the soft core ideal in FPGA prototyping systems for ASIC designs that will use the hard core, while remaining flexible for strictly FPGA designs.

Implementation Results

The following are typical performance and utilization results.

LatticeXP	Device LUT-4s	Registers	Slices	SLICES	External I/Os	Speed (fmax, MHz)
LFXP10C4F-5	1876	356	1148	0	46	42
LatticeXP2	Device LUT-4s	Registers	Slices	SLICES	External I/Os	Speed (fmax, MHz)
LFXP2-17E-5QFP208	1936	347	1135	0	46	42

Features

- 8-bit Data Bus
- 16-bit address bus provides access to 65,536 bytes of memory space
- 69 Instructions
- 212 Operation Codes (OpCodes)
- 16 Addressing Modes
- Vector Pull (VPB) output indicates when interrupt vectors are being addressed
- WAit-for-Interrupt (WAI) and SToP (STP) instructions reduce power consumption, decrease interrupt latency and enable synchronization with external events
- Variable length instruction set enables smaller code optimization over fixed length instruction set processors. This also results in lower power consumption.



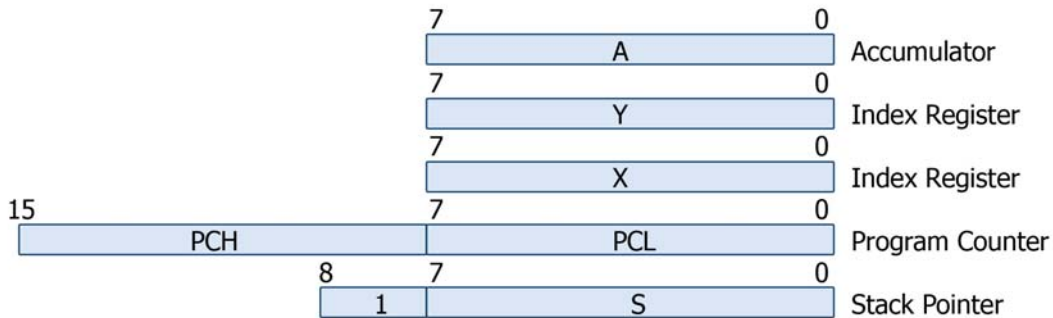
Development Tools

WDC supports the 65xx brand microprocessor technology with an ANSI Standard C compiler tool suite that includes the Terbium Integrated Development Environment (TIDE). In addition to integration of WDC development tool suite TIDE also provides debugger features with unlimited software breakpoints for in-circuit debug through the TIDE port embedded monitor.

Available Development Tools:

- TIDE
- ISO/ANSI Standard C Compiler
- Assembler
- Linker
- Librarian
- Object Inspector
- Symbol Tool

Microprocessor Programming Model



Processor Status Register (P) Coding

