FPGA
Libraries Manual

For Use With
ORCA 2002, and ispLEVER 2.0 and higher

Technical Support Line: 1-800-LATTICE or 408-826-6002 (international)

FPGA Libraries Manual
ispLEVER

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FPGA LIBRARIES MANUAL

OVERVIEW

We support several libraries used in designing FPGAs with ORCA in a number of CAE synthesis, schematic capture, and simulation platforms. (Please see the ORCA documentation on your CAE interface kit for specific support.) These libraries are the main front-end design libraries for the Series 4, Series 3 and ORCA 2CA/2TA/2TB families of FPGAs for both 3V and 5V devices. This manual also includes Lattice FPGA elements.

To help build a specific application, the library contains a number of logic elements that offer flexibility and efficiency when used with the ORCA architecture. In addition to these components, you can enter any SCUBA module-compliant component (symbol) you create in Module/IP Manager (or SCUBA command line) and any physical macros you create in EPIC. See the appropriate topic in the online help system.

Note

Throughout this document when ORCA PFUs are referred to collectively, they are called logic cells.

This manual contains descriptions of all available symbols (macros). Note that in the body of the manual, elements are listed in alphanumeric order. Clicking on the hyperlinked library name below will take you to the appropriate table of functional grouping of all the elements. Refer to the next section about Series 3+ library elements.

- FPGA MACRO LIBRARY LatticeSC
- FPGA MACRO LIBRARY MachXO
- FPGA MACRO LIBRARY LatticeXP and LatticeEC/ECP-DSP
- ORCA MACRO LIBRARY SERIES 4
- ORCA MACRO LIBRARY SERIES 3
- ORCA MACRO LIBRARY 2CA/2TA/2TB

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SPECIAL NOTE ABOUT LatticeSC, LatticeXP, and LatticeEC LIBRARY ELEMENTS

We strongly recommend that you generate most LatticeSC, LatticeXP, and LatticeEC elements using Module/IP Manager in ispLEVER's Project Navigator. Please refer to application notes or technical support for third-party synthesis/simulation vendor support.

Memory Port Definitions

This section shows port descriptions for LatticeSC | XP | EC devices.

Single Port RAM Port Definitions

Single Port RAM	
Port Name	*Description*
CE	Clock Enable
AD[x:x]	Address Bus Port
DI[x:x]	Input Data Port
DO[x:x]	Output Data Port
WE	Write Enable
CS[x:x]	Chip Select
RST	Reset
CLK	Clock

Dual Port RAM Port Definitions

Dual Port RAM	
Port Name	*Description*
CEA, CEB	Clock Enables for Port CLKA and CLKB
CLKA, CLKB	Clock for PortA and PortB
RSTA, RSTB	Reset for PortA and PortB
WEA, WEB	Write enable port A and port B
CSA[x:x], CSB[x:x]	3 Chip Selects for each port
DIA[x:x], DIB[x:x]	Input Data port A and port B
ADA[x:x], ADB[x:x]	Address Bus port A and port B
DOA[x:x], DOB[x:x]	Output Data port A and port B

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Pseudo Dual Port RAM Port Definitions

Pseudo-Dual Port RAM	
Port Name	*Description*
WCE	Write Clock Enable
RCLK	Read Clock
WCLK	Write Clock
RST	Reset
RCE	Read Clock Enable
WE	Write Enable
RD[x:x]	Read Data (up to 18)
WD[x:x]	Write Data (up to 18)

FIFO Port Definitions

FIFO	
Port Name	*Description*
FF	Full Flag
AFF	Almost Full Flag
EF	Empty Flag
AEF	Almost Empty Flag
FULLI, CSW[x:x]	Full Flag In (slave in width casc) & CS
EMPTYI, CSR[x:x]	Empty Flag In (slave in width casc) & CS
RST	FIFO Reset
RPRST	FIFO Read Pointer Reset
DI	Input Data
DO	Output Data
WE / RE	Write Enable / Read Enable

ROM Port Definitions

ROM	
Port Name	*Description*
CLOCK	Clock
CLOCKEN	Clock Enable
AD	Address Bus
DO	Output Data

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SPECIAL NOTE ABOUT SERIES 4 LIBRARY ELEMENTS

We strongly recommend that you generate most Series 4 elements using Module/IP Manager in ispLEVER's Project Navigator. As indicated in the chart, you *cannot* generate MUX81, PFUMX41, ORCALUT6, ILVDS, OLVDS, BMW6, OBW6, IODDR, IOSR2, IOSR4, HIODDR, HIOSR2, and HIOSR4 in Module/IP Manager. Many of these elements are generated by synthesis tools or they must otherwise be instantiated in the netlist.

Series 4 library elements are supported for Verilog and VHDL. There are no Viewlogic/ EDIF library elements for Series 4 available. Refer to applicable sections in this guide for more details on these new Series 4 elements.

Please note that in the Series 4 FIFO element FF2X512X9, the values for the INHIBITMODE0 and INHIBITMODE1 must either both be "TRUE" or "FALSE" to be valid. The Series 4 elements listed in the table below are supported in ORCA 2002 and ispLEVER 2.0 and higher:

Series 4 Element ORCA Module Support

Element Name	Description	SCUBA Module
BR512X18	512-Word by18-Bit 4-Port Block RAM	✓
BR1024X18	1024-Word by18-Bit 4-Port Block RAM	✓
CAM2X256X16	2X256X16 Content Addressable Memory	✓
CMULT16	8-Bit or 16-Bit Constant Multiplier	✓
MULT8X8	8-Bit by 8-Bit Multiplier	✓
FF512X18	512-Word by 18-Bit FIFO	✓
FF256X36	256-Word by 36-Bit FIFO	✓
FF2X512X9*	2 512-Word by 9-Bit FIFOs	✓
MUX81	8 to 1 Multiplexor	
PFUMX41	4-Input Multiplexor within the PFU	
ULIM	System Bus User Logic Interface (Master)	✓

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Series 4 Element ORCA Module Support

Element Name	Description	SCUBA Module
ULIS	System Bus User Logic Interface (Slave)	✓
SBR512X18	512-Word by18-Bit System Bus RAM	✓
SBR1024X18	1024-Word by 18-Bit System Bus RAM	✓
ORCALUT6	6-Input Look-up Table	
ILVDS	LVDS Input Buffer	
OLVDS	LVDS Output Buffer	
BMW6	BiDirectional Buffer	
OBW6	Output Tri-state Buffer	
IODDR	Input/Output DDR	
IOSR2	Input/Output 2-Bit Shift Register	
IOSR4	Input/Output 4-Bit Shift Register	
HIODDR	High-speed Input/Output DDR	
HIOSR2	High-speed Input/Output 2-Bit Shift Register	
HIOSR4	High-speed Input/Output 4-Bit Shift Register	
PLL1	Programmable Clock Manager (Phase Locked Loop) — Top-right and bottom-left dedicated PLL used for clock conditioning at 1.544 MHz and 2.048 MHz	✓
PLL2	Programmable Clock Manager (Phase Locked Loop) — Top-left and bottom-right dedicated PLL used for clock conditioning at 155.52 MHz	✓
PPLL	Programmable Clock Manager (Programmable general purpose Phase Locked Loop)	✓

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Series 4 Element ORCA Module Support

Element Name	Description	SCUBA Module
HPPLL	High Frequency Programmable Clock Manager (Programmable general purpose Phase Locked Loop)	✓
OSR2X2	Output Dual 2-Bit Shift Register	
HOSR2X2	High Speed Output Dual 2-Bit Shift Register	

Migrating from Series 3 to Series 4 Designs

The Series 4 software has been designed to provide maximum compatibility for migration from Series 3 designs to Series 4 devices. Migration should involve minimum conversion effort for most customer designs.

To ensure optimal results, observe the following conditions when migrating from Series 3 designs:

- When re-targeting Series 3 designs to Series 4, make sure that the *.edn* file does *not* have the LIBRARY property set to or3c00.
- Do not run the Series 4 mapper with a Series 3 *.ngd* file.
- Series 3 macros cannot be used in Series 4 designs.
- If LVTTL input buffers were used (e.g., in the IBT input buffer element), place a LEVELMODE=LVTTL attribute on output buffers to preserve buffer compatibility.

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SPECIAL NOTE ABOUT SERIES 3+ LIBRARY ELEMENTS

This section is for legacy users only. This enhanced Series 3+ architecture was the pilot architecture for FPSCs and is no longer offered.

The current version of ispLEVER does not include a separate library for the Series 3+ architecture. The Series 3+ cells are a part of the ORCA 3 library. Four buffers are available to interface to the FPSC Technology in Series 3+. If you use these cells, you are automatically in the Series 3+ architecture.

Series 3+ Library Elements

INTRBUF	ASB/FPGA interface cell that gets mapped to the bottom row of PICs. Unconnected inputs should be pulled down. Inputs: ASBI, TOASB,TOASBM1,TOASBM2,TOASBM3; Outputs: FRASB,ASBO,ASBM10,ASBM20,ASBM30;
INTRBUFS	ASB/FPGA interface cell that gets mapped to the bottom row of PICs. Delayed input buffer, unconnected inputs should be pulled down. Inputs: ASBI,TOASB,TOASBM1,TOASBM2,TOASBM3 Outputs: FRASB,ASBO,ASBM10,ASBM20,ASBM30;
TOASBCK	Buffer used to route clocks from FPGA to ASB along clock spine. Inputs: CLKTOASB; Outputs: ASBCK0;
FRASBCK	Buffer used to route clocks rom ASB to FPGA along clock spine. Inputs: ASBCKI; Outputs: CKFRASB;

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SPECIAL NOTE ABOUT BUFFERS AND PCI

The Series 3 5V architecture (ORCA 3C) supports both TTL and CMOS levels for input and bidirectional buffers for designs.

The Series 3 3.3V architecture (ORCA 3T) supports only CMOS levels for input or bidirectional buffers. You can program each input buffer or bidirectional buffer site to be 3.3V PCI compliant or 5V tolerant/5V PCI compliant.

To obtain a 3.3V PCI compliant buffer, install a CMOS level buffer in your design. To obtain a 5V tolerant/5V PCI compliant buffer, install a TTL level buffer in your design. The default buffer upon powerup for the unused sites is 5V tolerant/5V PCI compliant. Please consult the ORCA Macro Library Series 3 I/O Cells section on page 91 for the appropriate buffer required.

SPECIAL NOTE ABOUT 3C RAM/ROM AND GSR

For simulation with a 3C RAM or ROM cell, you must instantiate a GSR in your netlist, and pulse the GSR high to low at the beginning of the simulation.

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NAMING CONVENTIONS

The table shows the convention for naming all of the sequential elements. Each cell is identified using up to seven characters.

Table 5-1. **Flip-Flop/Latch Naming Conventions (name = abcdef)**

a=	F - Static implementation
b=	D - D type flip-flop
	J - J/K type flip-flop
	L - Cells contain a positive select front end (loadable)
	N - Cells contain a negative select front end (loadable)
	S - R-S type flip-flop
	T - Toggle type flip-flop
c=	Value - Number of clocks
d=	This parameter identifies the enable capability
	S - No enable input
	P - Positive-level enable
	N - Negative-level enable
e=	This parameter identifies the clock capability
	1 - Positive-level sense (latch)
	2 - Negative edge-triggered (flip-flop)
	3 - Positive edge-triggered (flip-flop)
	5 - Negative-level sense (latch)

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f=	A - No clear or preset inputs
	B - Positive-level asynchronous preset
	D - Positive-level asynchronous clear
	I - Positive-level synchronous clear
	J - Positive-level synchronous preset
	X - Standard library element where GSR asynchronously clears or presets the flip-flop depending upon the function of the local clear or preset. If no local clear or preset is present (f=A), then GSR clears the register element.
	Y - Element is preset using GSR rather than cleared
	Z - Element not compatible with similar elements available in the standard cell library

Example

FD1P3BX is a single clock positive edge-triggered static D-type flip-flop with a positive-level enable, and a positive-level asynchronous preset.

FD1P3BX
a = F Static cell
b = D D type
c = 1 Single clock
d = P Positive-level enable
e = 3 Positive edge-triggered
f = B Positive-level asynchronous preset

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Illegal Names and Characters

When creating designs for ORCA from schematic or synthesis, please observe the following rules:

- Component, net, site, or instance names should be unique and independent of case. For example, if a net in a design is named “d0”, then you cannot have an instance of AND2 named “D0”.
- Component, net, site, or instance names cannot be any ORCA or Neoprim cell name.
- Component, net, site, or instance names cannot be GND, PWR, VSS, VDD, GSR, GSRNET, TSALL, TSALLNET, etc.
- Component, net, site, or instance names cannot contain preference keywords such as DIN, DOUT, SITE, COMP, etc.
- Component, net, site, or instance names cannot contain names starting with 0–9, /, \, +, –, and other special characters.
- Component, net, site, or instance names cannot be named using VHDL or Verilog keywords such as IN, OUT, INOUT, etc.

Pin Order and Numbering

Note the following about pin order and numbering used throughout this manual:

- Pin order can be represented in either ascending or descending order numerically, for example, either A(0:7) or A(7:0) can be ascribed to pin groupings in a given element.
- *Least significant bits* (LSBs) on an element are always determined by the lowest integer value (usually zero) expressed in a pin name input or output in a pin grouping just as *most significant bits* (MSBs) are always determined by the highest integer value.

  For example, out of the pin group containing pins A0, A1, A2, and A3, A0 is the LSB and A3 is the MSB. The LSB or MSB is not affected by the order in which pins are numbered (i.e., whether or not they are in ascending or descending order).

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CELL SUPPORT MATRIXES

On each library element page description there is a cell matrix support box in the top right corner. This support box shows in what architectures the current element is supported. This is necessary because many elements are forward compatible with new architectures.

The cell support matrix does not show to what architecture the current element belongs. For this information, go to the contents pages for the architecture of interest and look for allowable elements. New elements per architecture and distinguished by their own cell support matrix box.

The following is an example of an element supported in all architectures:

Example Cell Support Matrix

ORCA Series/Lattice FPGA							
2	3	4	SC	XP	EC	ECP	MX
✓	✓	✓	✓	✓	✓	✓	✓

Key:

Abbreviation	Device Family
2	ORCA Series 2
3	ORCA Series 3
4	ORCA Series 4
SC	LatticeSC
XP	LatticeXP
EC	LatticeEC/LatticeECP-DSP
ECP	LatticeECP-DSP (DSP Blocks Only)
MX	MachXO

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CELL AREA ESTIMATES

Each cell of the ORCA library contains a cell area estimate in terms of PLC utilization. This was obtained using the following guidelines and should only be used as an estimation. To get an accurate PLC count, the design must be mapped in ORCA.

- We have assumed that a PLC is made up of four 4 input LUTs and 4 sequential elements. Thus there are 8 total elements in a PLC used for this calculation. One flipflop in the ORCA library would use 1/8 of a PLC or 0.125. One 2-input gate would also use 1/8 of a PLC or 0.125. An adder (FADD4) would use all the LUTs or 0.5 of a PLC, but the remaining 0.5 left in the PLC could only be used as sequential elements. Please note this limitation.
- Other limitations with these numbers relate to the ORCA FPGA architecture. Suppose a design uses four flipflops, each with a different clock. The total area would be 4 x (0.125) = 0.5 PLCs. One would assume that the flipflops would fit into one PLC that contains four sequential elements. The *actual* area would be four PLCs reported from ORCA, since four different clocks require four different PLCs to implement the logic.
- For another example, assume two AND2 gates for a total area of 2 x 0.125 = 0.250 of a PLC. ORCA may optimize this logic into a single 4-input LUT for a savings of 0.125 of a PLC.

The numbers contained in this manual are not absolute and should only be used as relative estimates. ORCA reports whole numbers of PLCs, so it is difficult to compare these partial numbers with the values reported from ORCA. The numbers will vary greatly depending upon the design being implemented.

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FPGA MACRO LIBRARY MachXO

This listing includes compatible ORCA library elements in addition to new MachXO-specfiic elements. This chapter contains the following sections:

- Logic Gates
- Comparators
- Adders/Subtracters
- Multipliers
- Counters
- Flip-Flops
- Latches
- Memory
- MachXO-Specific Memory
- Multiplexers
- I/O Cells
- Special Cells

Logic Gates

AND2	2 Input AND Gate
AND3	3 Input AND Gate
AND4	4 Input AND Gate
AND5	5 Input AND Gate
ND2	2 Input NAND Gate
ND3	3 Input NAND Gate
ND4	4 Input NAND Gate
ND5	5 Input NAND Gate
OR2	2 Input OR Gate

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OR3	3 Input OR Gate
OR4	4 Input OR Gate
OR5	5 Input OR Gate
NR2	2 Input NOR Gate
NR3	3 Input NOR Gate
NR4	4 Input NOR Gate
NR5	5 Input NOR Gate
XNOR2	2 Input Exclusive NOR Gate
XNOR3	3 Input Exclusive NOR Gate
XNOR4	4 Input Exclusive NOR Gate
XNOR5	5 Input Exclusive NOR Gate
XOR2	2 Input Exclusive OR Gate
XOR3	3 Input Exclusive OR Gate
XOR4	4 Input Exclusive OR Gate
XOR5	5 Input Exclusive OR Gate
XOR11	11 Input Exclusive OR Gate
XOR21	21 Input Exclusive OR Gate

Miscellaneous Logic

INV	Inverter
VHI	Logic High Generator
VLO	Logic Low Generator

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Comparators

AGEB2	“A” Greater Than Or Equal To “B” (2 bit)
ALEB2	“A” Less Than Or Equal To “B” (2 bit)
ANEB2	“A” Not Equal To “B” (2 bit)

Adders/Subtracters

FADD2	2 Bit Fast Adder
FSUB2	2 Bit Fast Subtracter (two’s complement)
FADSU2	2 Bit Fast Adder/Subtracter (two’s complement)

Multipliers

MULT2	2x2 Multiplier

Counters

CB2	Combinational Logic for 2-Bit Bidirectional Counter using Look-Up Table
CU2	Combinational Logic for 2 Bit Up Counter using Look-Up Table
CD2	Combinational Logic for 2 Bit Down Counter using Look-Up Table

Flip-Flops

FD1P3AX	Positive Edge Triggered D Flip-Flop with Positive Level Enable, GSR used for Clear
FD1P3AY	Positive Edge Triggered D Flip-Flop with Positive Level Enable, GSR used for Preset

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FD1P3BX	Positive Edge Triggered D Flip-Flop with Positive Level Enable and Positive Level Asynchronous Preset
FD1P3DX	Positive Edge Triggered D Flip-Flop with Positive Level Enable and Positive Level Asynchronous Clear
FD1P3IX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Clear and Positive Level Enable (Clear overrides Enable)
FD1P3JX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Preset and Positive Level Enable (Preset overrides Enable)
FD1S3AX	Positive Edge Triggered D Flip-Flop, GSR Used for Clear
FD1S3AY	Positive Edge Triggered D Flip-Flop, GSR Used for Preset
FD1S3BX	Positive Edge Triggered D Flip-Flop with Positive Level Asynchronous Preset
FD1S3DX	Positive Edge Triggered D Flip-Flop with Positive Level Asynchronous Clear
FD1S3IX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Clear
FD1S3JX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Preset
FL1P3AY	Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, Positive Level Data Select, and Positive Level Enable, GSR used for Preset
FL1P3AZ	Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, Positive Level Data Select, and Positive Level Enable, GSR used for Clear
FL1P3BX	Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, Positive Level Data Select, Positive Level Asynchronous Preset, and Positive Level Enable

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FL1P3DX	Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, Positive Level Data Select, Positive Level Asynchronous Clear, and Positive Level Enable
FL1P3IY	Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, Positive Level Data Select, Positive Level Synchronous Clear, and Positive Level Enable (Clear overrides Enable)
FL1P3JY	Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, Positive Level Data Select, Positive Level Synchronous Preset, and Positive Level Enable (Preset overrides Enable)
FL1S3AX	Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, GSR used for Clear
FL1S3AY	Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, GSR used for Preset

Latches

FD1S1A	Positive Level Data Latch with GSR Used for Clear
FD1S1AY	Positive Level Data Latch with GSR Used for Preset
FD1S1B	Positive Level Data Latch with Positive Level Asynchronous Preset
FD1S1D	Positive Level Data Latch with Positive Level Asynchronous Clear
FD1S1I	Positive Level Data Latch with Positive Level Synchronous Clear
FD1S1J	Positive Level Data Latch with Positive Level Synchronous Preset
FL1S1A	Positive Level Loadable Latch with Positive Select and GSR Used for Clear
FL1S1AY	Positive Level Loadable Latch with Positive Select and GSR Used for Preset
FL1S1B	Positive Level Loadable Latch with Positive Select and Positive Level Asynchronous Preset

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FL1S1D	Positive Level Loadable Latch with Positive Select and Positive Level Asynchronous Clear
FL1S1I	Positive Level Loadable Latch with Positive Select and Positive Level Synchronous Clear
FL1S1J	Positive Level Loadable Latch with Positive Select and Positive Level Synchronous Preset

Memory

ROM16X1	16 Word by 1 bit read-only memory
ROM32X1	32 Word by 1 bit read-only memory
ROM64X1	64 Word by 1 bit read-only memory
ROM128X1	128 Word by 1 bit read-only memory
ROM256X1	256 Word by 1 bit read-only memory

MachXO-Specific Memory

DP8KB	8K Dual Port Block RAM
DPR16X2B	16 Word by 2 Dual Port RAM (within PFU)
PDP8KB	8K Pseudo Dual Port Block RAM
SP8KB	8 Word by 8 Bit Single Port Block RAM
SPR16X2B	16 Word by 2 Bit Positive Edge Triggered Write Synchronous Single Port RAM Memory with Positive Write Enable and Positive Write Port Enable (1-Slice)

Multiplexers

MUX161	16 to 1 Mux

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MUX321	32 to 1 Mux
MUX21	2 to 1 Mux
MUX41	4 to 1 Mux
MUX81	8 to 1 Mux

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I/O Cells

Input Buffers

IB	Input Buffer
IBPD	Input Buffer with Pull-down
IBPU	Input Buffer with Pull-up
ILVDS	LVDS Input Buffer

Output Buffers

OB	Output Tristate Buffer
OBW	Output Buffer with Tristate
OBZ	Output Buffer with Tristate
OBZPD	Output Buffer with Tristate and Pull-down
OBZPU	Output Buffer with Tristate and Pull-up
OLVDS	LVDS Output Buffer

Bidirectional Buffers

BB	CMOS Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate – BiDirectional
BBPD	CMOS Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate – BiDirectional and Pull-down
BBPU	CMOS Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate – BiDirectional and Pull-up
BBW	CMOS Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate – BiDirectional in keepermode

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Special Cells

Miscellaneous

OSCC	Internal Oscillator
RDBK	Readback Controller
STRTUP	Startup Controller
GSR	Global Set/Reset
L6MUX21	LUT-6 2 to 1 Multiplexer
PFUMX	2-Input Mux within the PFU, C0 used for Selection with Positive Select
PUR	Power Up Set/Reset
GOE	Global Ouput Enable
TBUF	Internal Buffer with Tristate

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FPGA MACRO LIBRARY LatticeXP and LatticeEC/ECP-DSP

This listing includes compatible ORCA library elements in addition to new LatticeXP and related LatticeEC/ECP-DSP family specfiic elements. This chapter contains the following sections:

- Logic Gates
- Comparators
- Adders/Subtracters
- Counters
- Flip-Flops
- Latches
- Memory
- LatticeXP and LatticeEC-Specific Memory
- LatticeECP DSP Block
- Multipliers (Not DSP)
- Multiplexers
- I/O Cells
- PIC Cells
- Special Cells

Logic Gates

AND2	2 Input AND Gate
AND3	3 Input AND Gate
AND4	4 Input AND Gate
AND5	5 Input AND Gate
ND2	2 Input NAND Gate
ND3	3 Input NAND Gate
ND4	4 Input NAND Gate

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ND5	5 Input NAND Gate
OR2	2 Input OR Gate
OR3	3 Input OR Gate
OR4	4 Input OR Gate
OR5	5 Input OR Gate
NR2	2 Input NOR Gate
NR3	3 Input NOR Gate
NR4	4 Input NOR Gate
NR5	5 Input NOR Gate
XNOR2	2 Input Exclusive NOR Gate
XNOR3	3 Input Exclusive NOR Gate
XNOR4	4 Input Exclusive NOR Gate
XNOR5	5 Input Exclusive NOR Gate
XOR2	2 Input Exclusive OR Gate
XOR3	3 Input Exclusive OR Gate
XOR4	4 Input Exclusive OR Gate
XOR5	5 Input Exclusive OR Gate

Miscellaneous Logic

INV	Inverter
VHI	Logic High Generator
VLO	Logic Low Generator

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Comparators

AGEB2	“A” Greater Than Or Equal To “B” (2 bit)
AGEB4	“A” Greater Than Or Equal To “B” (4 bit)
AGEB8	“A” Greater Than Or Equal To “B” (8 bit)
ALEB2	“A” Less Than Or Equal To “B” (2 bit)
ALEB4	“A” Less Than Or Equal To “B” (4 bit)
ALEB8	“A” Less Than Or Equal To “B” (8 bit)
ANEB2	“A” Not Equal To “B” (2 bit)
ANEB4	“A” Not Equal To “B” (4 bit)
ANEB8	“A” Not Equal To “B” (8 bit)

Adders/Subtracters

FADD2	2 Bit Fast Adder
FADD4	4 Bit Fast Adder
FADD8	8 Bit Fast Adder
FSUB2	4 Bit Fast Subtracter (two’s complement)
FSUB4	4 Bit Fast Subtracter (two’s complement)
FSUB8	8 Bit Fast Subtracter (two’s complement)
FADSU2	2 Bit Fast Adder/Subtracter (two’s complement)
FADSU4	4 Bit Fast Adder/Subtracter (two’s complement)
FADSU8	8 Bit Fast Adder/Subtracter (two’s complement)

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Counters

CU2	Combinational Logic for 2 Bit Up Counter using Look-Up Table
CU4	Combinational Logic for 4 Bit Up Counter using Look-Up Table
CU4P3BX	4 Bit Positive Edge Triggered Fast Up Counter with Positive Clock Enable and Positive Asynchronous Preset
CU4P3DX	4 Bit Positive Edge Triggered Fast Up Counter with Positive Clock Enable and Positive Asynchronous Clear
CU4P3IX	4 Bit Positive Edge Triggered Fast Up Counter with Positive Clock Enable and Positive Synchronous Clear
CU4P3JX	4 Bit Positive Edge Triggered Fast Up Counter with Positive Clock Enable and Positive Synchronous Preset
CU8P3BX	8 Bit Positive Edge Triggered Fast Up Counter with Positive Clock Enable and Positive Asynchronous Preset
CU8P3DX	8 Bit Positive Edge Triggered Fast Up Counter with Positive Clock Enable and Positive Asynchronous Clear
CU8P3IX	8 Bit Positive Edge Triggered Fast Up Counter with Positive Clock Enable and Positive Synchronous Clear
CU8P3JX	8 Bit Positive Edge Triggered Fast Up Counter with Positive Clock Enable and Positive Synchronous Preset
CB2	LatticeXP based counter
CD2	Combinational Logic for 2 Bit Down Counter using Look-Up Table
CD4	Combinational Logic for 4 Bit Down Counter using Look-Up Table
CD4P3BX	4 Bit Positive Edge Triggered Fast Down Counter with Positive Clock Enable and Positive Asynchronous Preset
CD4P3DX	4 Bit Positive Edge Triggered Fast Down Counter with Positive Clock Enable and Positive Asynchronous Clear

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CD4P3IX	4 Bit Positive Edge Triggered Fast Down Counter with Positive Clock Enable and Positive Synchronous Clear
CD4P3JX	4 Bit Positive Edge Triggered Fast Down Counter with Positive Clock Enable and Positive Synchronous Preset
CD8	LatticeXP based counter
CD8	8 Bit Positive Edge Triggered Fast Down Counter with Positive Clock Enable and Positive Asynchronous Preset
CD8P3DX	8 Bit Positive Edge Triggered Fast Down Counter with Positive Clock Enable and Positive Asynchronous Clear
CD8P3IX	8 Bit Positive Edge Triggered Fast Down Counter with Positive Clock Enable and Positive Synchronous Clear
CD8P3JX	8 Bit Positive Edge Triggered Fast Down Counter with Positive Clock Enable and Positive Synchronous Preset

Flip-Flops

FD1P3AX	Positive Edge Triggered D Flip-Flop with Positive Level Enable, GSR used for Clear
FD1P3AY	Positive Edge Triggered D Flip-Flop with Positive Level Enable, GSR used for Preset
FD1P3BX	Positive Edge Triggered D Flip-Flop with Positive Level Enable and Positive Level Asynchronous Preset
FD1P3DX	Positive Edge Triggered D Flip-Flop with Positive Level Enable and Positive Level Asynchronous Clear
FD1P3IX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Clear and Positive Level Enable (Clear overrides Enable)
FD1P3JX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Preset and Positive Level Enable (Preset overrides Enable)

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FD1S3AX	Positive Edge Triggered D Flip-Flop, GSR Used for Clear
FD1S3AY	Positive Edge Triggered D Flip-Flop, GSR Used for Preset
FD1S3BX	Positive Edge Triggered D Flip-Flop with Positive Level Asynchronous Preset
FD1S3DX	Positive Edge Triggered D Flip-Flop with Positive Level Asynchronous Clear
FD1S3IX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Clear
FD1S3JX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Preset

Latches

FD1S1A	Positive Level Data Latch with GSR Used for Clear
FD1S1AY	Positive Level Data Latch with GSR Used for Preset
FD1S1B	Positive Level Data Latch with Positive Level Asynchronous Preset
FD1S1D	Positive Level Data Latch with Positive Level Asynchronous Clear
FD1S1I	Positive Level Data Latch with Positive Level Synchronous Clear
FD1S1J	Positive Level Data Latch with Positive Level Synchronous Preset

Memory

Read-Only Memory

ROM16X1	16 Word by 1 Bit Read-Only Memory
ROM32X1	32 Word by 1 Bit Read-Only Memory

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ROM64X1	64 Word by 1 Bit Read-Only Memory
ROM128X1	128 Word by 1 Bit Read-Only Memory
ROM256X1	256 Word by 1 Bit Read-Only Memory

LatticeXP and LatticeEC-Specific Memory

DP8KA	8K Dual Port Block RAM
DPR16X2B	16 Word by 2 Dual Port RAM (within PFU)
PDP8KA	8K Pseudo Dual Port Block RAM
SP8KA	8K Single Port Block RAM
SPR16X2B	16 Word by 2 Single Port RAM (within PFU)

LatticeECP DSP Block

MULT18X18	ECP 18X18 DSP Multiplier
MULT18X18ADDSUB	ECP 18X18 DSP Adder/Subtractor
MULT18X18ADDSUBSUM	ECP 18X18 DSP Adder/Subtractor/Sum
MULT18X18MAC	ECP 18X18 DSP MAC
MULT36X36	ECP 36X36 DSP Multiplier
MULT9X9	ECP 9X9 DSP Multiplier
MULT9X9ADDSUB	ECP 9X9 DSP Adder/Subtractor
MULT9X9ADDSUBSUM	ECP 9X9 DSP Adder/Subtractor/Sum

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MULT9X9MAC	ECP 9X9 DSP MAC

Multipliers (Not DSP)

MULT2	2X2 Multiplier

Multiplexers

DCS	Dynamic Clock Selection Multiplexer
L6MUX21	2 to 1 Mux
MUX161	16 to 1 Mux in PFU
MUX321	32 to 1 Mux
MUX21	2 to 1 Mux
MUX41	4 to 1 Mux
MUX81	8 to 1 Mux
PFUMX	PFU Mux
PFUMX41	4 to 1 Mux

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I/O Cells

Input Buffers

IB	CMOS Input Buffer
IBM	CMOS Input Buffer
IBMPD	CMOS Input Buffer with Pull-down
IBMPDS	CMOS Input Buffer with Pull-down and Delay
IBMPU	CMOS Input Buffer with Pull-up
IBMPUS	CMOS Input Buffer with Pull-up and Delay
IBMS	CMOS Input Buffer with Delay

Output Buffers

OB	Output Buffer
OBZ	6mA Sink 3mA Source Sinklim Output Buffer
OBZPD	12mA Sink 6mA Source Slewlim Output Buffer
OBZPU	12mA Sink 6mA Source Fast Output Buffer
OBW	6mA Sink 3mA Source Sinklim Output Buffer with Tristate

Bidirectional Buffers

BB	CMOS Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate – BiDirectional
BBPD	CMOS Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate and Pull-down – BiDirectional

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BBPU	CMOS Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate and Pull-up – BiDirectional
BBW	CMOS Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate – BiDirectional in keepermode

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PIC Cells

PIC Flip-Flops (Input)

IFS1P3BX	Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Asynchronous Preset, and System Clock (used in input PIC area only)
IFS1P3DX	Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Asynchronous Clear, and System Clock (used in input PIC area only)
IFS1P3IX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Clear, Positive Level Enable, and System Clock (Clear overrides Enable) (used in input PIC area only)
IFS1P3JX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Preset, Positive Level Enable, and System Clock (Preset overrides Enable) (used in input PIC area only)

PIC Flip-Flops (Output)

OFE1P3BX	Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Asynchronous Preset, and Express Clock (used in output PIC area only)
OFE1P3DX	Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Asynchronous Clear, and Express Clock (used in output PIC area only)
OFE1P3IX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Clear, Positive Level Enable (Clear overrides Enable), and Express Clock (used in output PIC area only)
OFE1P3JX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Preset, Positive Level Enable (Preset overrides Enable), and Express Clock (used in output PIC area only)

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OFS1P3BX	Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Asynchronous Preset, and System Clock (used in output PIC area only)
OFS1P3DX	Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Asynchronous Clear, and System Clock (used in output PIC area only)
OFS1P3IX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Clear, Positive Level Enable (Clear overrides Enable), and System Clock (used in output PIC area only)
OFS1P3JX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Preset, Positive Level Enable (Preset overrides Enable), and System Clock (used in output PIC area only)

PIC Latches (Input)

IFS1P1B	Positive Level Latch with Positive Level Enable and Positve Level Asynchronous Preset
IFS1P1D	Positive Level Latch with Positive Level Enable and Positive Asynchronous Clear
IFS1P1I	Positive Level Latch with Positive Level Enable and Positive Asynchronous Clear
IFS1P1J	Positive Level Latch with Positive Level Enable and Positive Level Asynchronous Preset
IFS1S1B	Positive Level Data Latch with Positive Level Asynchronous Preset and System Clock (used in input PIC area only)
IFS1S1D	Positive Level Data Latch with Positive Level Asynchronous Clear and System Clock (used in input PIC area only)
IFS1S1I	Positive Level Data Latch with Positive Level Synchronous Clear and System Clock (used in input PIC area only)
IFS1S1J	Positive Level Data Latch with Positive Level Synchronous Preset and System Clock (used in input PIC area only)

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Special Cells

Clock/PLL

DCS	Dynamic Clock Selection Multiplexer
EPLLB	Enhanced PLL
EHXPLLB	Enhanced High Performance with Dynamic Input Delay Control PLL

Dual Data Rate Cells

DQSBUFB	DDR DQS Buffer used as DDR memory DQS generator
DQSDLL	DLL used as DDR memory DQS DLL
IDDRXB	DDRX Input Cell
ODDRXB	ODDR Output Cell

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FPGA MACRO LIBRARY LatticeSC

This listing includes compatible ORCA library elements in addition to new LatticeSC-specfiic elements. This chapter contains the following sections:

- Logic Gates
  - → Miscellaneous Logic
- Comparators
- Adders/Subtracters
- Counters
- Flip-Flops
- Latches
- Memory
- LatticeSC-Specific Memory
- Multiplexers
- I/O Cells
  - → Input Buffers
  - → Output Buffers
  - → Bidirectional Buffers
- PIC Cells
  - → PIC Flip-Flops (Input)
  - → PIC Flip-Flops (Output)
  - → PIC Flip-Flops (Latched)
  - → PIC Latches (Input)
  - → PIC Shift Registers and DDR
- Special Cells

Logic Gates

AND2	2 Input AND Gate
AND3	3 Input AND Gate

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AND4	4 Input AND Gate
AND5	5 Input AND Gate
ND2	2 Input NAND Gate
ND3	3 Input NAND Gate
ND4	4 Input NAND Gate
ND5	5 Input NAND Gate
OR2	2 Input OR Gate
OR3	3 Input OR Gate
OR4	4 Input OR Gate
OR5	5 Input OR Gate
NR2	2 Input NOR Gate
NR3	3 Input NOR Gate
NR4	4 Input NOR Gate
NR5	5 Input NOR Gate
XNOR2	2 Input Exclusive NOR Gate
XNOR3	3 Input Exclusive NOR Gate
XNOR4	4 Input Exclusive NOR Gate
XNOR5	5 Input Exclusive NOR Gate
XOR2	2 Input Exclusive OR Gate
XOR3	3 Input Exclusive OR Gate
XOR4	4 Input Exclusive OR Gate
XOR5	5 Input Exclusive OR Gate

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XOR11	11 Input Exclusive OR Gate
XOR21	21 Input Exclusive OR Gate

Miscellaneous Logic

INV	Inverter
VHI	Logic High Generator
VLO	Logic Low Generator

Comparators

AGEB2	“A” Greater Than Or Equal To “B” (2 bit)
ALEB2	“A” Less Than Or Equal To “B” (2 bit)
ANEB2	“A” Not Equal To “B” (2 bit)

Adders/Subtracters

FADD2	2 Bit Fast Adder
FSUB2	2 Bit Fast Subtracter (two’s complement)

Counters

CB2	Combinational Logic for 2-Bit Bidirectional Counter using Look-Up Table
CB4	Combinational Logic for 4 Bit Bidirectional Counter using Look-Up Table
CU2	Combinational Logic for 2 Bit Up Counter using Look-Up Table
CD2	Combinational Logic for 2 Bit Down Counter using Look-Up Table

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Loadable Counters

LU2P3AX	2 Bit Positive Edge Triggered Loadable Up Counter with Positive Clock Enable, GSR Used for Clear
LU2P3AY	2 Bit Positive Edge Triggered Loadable Up Counter with Positive Clock Enable, GSR Used for Preset
LU2P3BX	2 Bit Positive Edge Triggered Loadable Up Counter with Positive Clock Enable and Positive Level Asynchronous Preset
LU2P3DX	2 Bit Positive Edge Triggered Loadable Up Counter with Positive Clock Enable and Positive Level Asynchronous Clear
LU2P3IX	2 Bit Positive Edge Triggered Loadable Up Counter with Positive Clock Enable and Positive Level Synchronous Clear (Clear overrides Enable)
LU2P3JX	2 Bit Positive Edge Triggered Loadable Up Counter with Positive Clock Enable and Positive Level Synchronous Preset (Preset overrides Enable)
LU4P3AX	4 Bit Positive Edge Triggered Loadable Up Counter with Positive Clock Enable, GSR Used for Clear
LU4P3AY	4 Bit Positive Edge Triggered Loadable Up Counter with Positive Clock Enable, GSR Used for Preset
LU4P3BX	4 Bit Positive Edge Triggered Loadable Up Counter with Positive Clock Enable and Positive Level Asynchronous Preset
LU4P3DX	4 Bit Positive Edge Triggered Loadable Up Counter with Positive Clock Enable and Positive Level Asynchronous Clear
LU4P3IX	4 Bit Positive Edge Triggered Loadable Up Counter with Positive Clock Enable and Positive Level Synchronous Clear (Clear overrides Enable)
LU4P3JX	4 Bit Positive Edge Triggered Loadable Up Counter with Positive Clock Enable and Positive Level Synchronous Preset (Preset overrides Enable)

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LD2P3AX	2 Bit Positive Edge Triggered Loadable Down Counter with Positive Clock Enable, GSR Used for Clear
LD2P3AY	2 Bit Positive Edge Triggered Loadable Down Counter with Positive Clock Enable, GSR Used for Preset
LD2P3BX	2 Bit Positive Edge Triggered Loadable Down Counter with Positive Clock Enable and Positive Level Asynchronous Preset
LD2P3DX	2 Bit Positive Edge Triggered Loadable Down Counter with Positive Clock Enable and Positive Level Asynchronous Clear
LD2P3IX	2 Bit Positive Edge Triggered Loadable Down Counter with Positive Clock Enable and Positive Level Synchronous Clear (Clear overrides Enable)
LD2P3JX	2 Bit Positive Edge Triggered Loadable Down Counter with Positive Clock Enable and Positive Level Synchronous Preset (Preset overrides Enable)
LD4P3AX	4 Bit Positive Edge Triggered Loadable Down Counter with Positive Clock Enable, GSR Used for Clear
LD4P3AY	4 Bit Positive Edge Triggered Loadable Down Counter with Positive Clock Enable, GSR Used for Preset
LD4P3BX	4 Bit Positive Edge Triggered Loadable Down Counter with Positive Clock Enable and Positive Level Asynchronous Preset
LD4P3DX	4 Bit Positive Edge Triggered Loadable Down Counter with Positive Clock Enable and Positive Level Asynchronous Clear
LD4P3IX	4 Bit Positive Edge Triggered Loadable Down Counter with Positive Clock Enable and Positive Level Synchronous Clear (Clear overrides Enable)
LD4P3JX	4 Bit Positive Edge Triggered Loadable Down Counter with Positive Clock Enable and Positive Level Synchronous Preset (Preset overrides Enable)
LB2P3AX	2 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable, GSR Used for Clear

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LB2P3AY	2 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable, GSR Used for Preset
LB2P3BX	2 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable and Positive Level Asynchronous Preset
LB2P3DX	2 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable and Positive Level Asynchronous Clear
LB2P3IX	2 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable and Positive Level Synchronous Clear (Clear overrides Enable)
LB2P3JX	2 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable and Positive Level Synchronous Preset (Preset overrides Enable)
LB4P3AX	4 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable, GSR Used for Clear
LB4P3AY	4 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable, GSR Used for Preset
LB4P3BX	4 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable and Positive Level Asynchronous Preset
LB4P3DX	4 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable and Positive Level Asynchronous Clear
LB4P3IX	4 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable and Positive Level Synchronous Clear (Clear overrides Enable)
LB4P3JX	4 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable and Positive Level Synchronous Preset (Preset overrides Enable)

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Flip-Flops

FD1P3AX	Positive Edge Triggered D Flip-Flop with Positive Level Enable, GSR used for Clear
FD1P3AY	Positive Edge Triggered D Flip-Flop with Positive Level Enable, GSR used for Preset
FD1P3BX	Positive Edge Triggered D Flip-Flop with Positive Level Enable and Positive Level Asynchronous Preset
FD1P3DX	Positive Edge Triggered D Flip-Flop with Positive Level Enable and Positive Level Asynchronous Clear
FD1P3IX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Clear and Positive Level Enable (Clear overrides Enable)
FD1P3JX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Preset and Positive Level Enable (Preset overrides Enable)
FD1S3AX	Positive Edge Triggered D Flip-Flop, GSR Used for Clear
FD1S3AY	Positive Edge Triggered D Flip-Flop, GSR Used for Preset
FD1S3BX	Positive Edge Triggered D Flip-Flop with Positive Level Asynchronous Preset
FD1S3DX	Positive Edge Triggered D Flip-Flop with Positive Level Asynchronous Clear
FD1S3IX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Clear
FD1S3JX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Preset
FL1P3AY	Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, Positive Level Data Select, and Positive Level Enable, GSR used for Preset

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FL1P3AZ	Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, Positive Level Data Select, and Positive Level Enable, GSR used for Clear
FL1P3BX	Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, Positive Level Data Select, Positive Level Asynchronous Preset, and Positive Level Enable
FL1P3DX	Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, Positive Level Data Select, Positive Level Asynchronous Clear, and Positive Level Enable
FL1P3IY	Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, Positive Level Data Select, Positive Level Synchronous Clear, and Positive Level Enable (Clear overrides Enable)
FL1P3JY	Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, Positive Level Data Select, Positive Level Synchronous Preset, and Positive Level Enable (Preset overrides Enable)
FL1S3AX	Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, GSR used for Clear
FL1S3AY	Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, GSR used for Preset

Latches

FD1S1A	Positive Level Data Latch with GSR Used for Clear
FD1S1AY	Positive Level Data Latch with GSR Used for Preset
FD1S1B	Positive Level Data Latch with Positive Level Asynchronous Preset
FD1S1D	Positive Level Data Latch with Positive Level Asynchronous Clear
FD1S1I	Positive Level Data Latch with Positive Level Synchronous Clear
FD1S1J	Positive Level Data Latch with Positive Level Synchronous Preset
FL1S1A	Positive Level Loadable Latch with Positive Select and GSR Used for Clear

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FL1S1AY	Positive Level Loadable Latch with Positive Select and GSR Used for Preset
FL1S1B	Positive Level Loadable Latch with Positive Select and Positive Level Asynchronous Preset
FL1S1D	Positive Level Loadable Latch with Positive Select and Positive Level Asynchronous Clear
FL1S1I	Positive Level Loadable Latch with Positive Select and Positive Level Synchronous Clear
FL1S1J	Positive Level Loadable Latch with Positive Select and Positive Level Synchronous Preset

Memory

ROM16X1	16 Word by 1 bit read-only memory
ROM32X1	32 Word by 1 bit read-only memory
ROM32X4	32 Word by 4 bit read-only memory
ROM64X1	64 Word by 1 bit read-only memory
ROM128X1	128 Word by 1 bit read-only memory
ROM256X1	256 Word by 1 bit read-only memory

LatticeSC-Specific Memory

DP16KA	16K Dual Port Block RAM
DPR16X2	16 Word by 2 Dual Port RAM (within PFU)
FIFO16KA	16K FIFO
PDP16KA	16K Pseudo Dual Port Block RAM
SP16KA	16 Word by 16 Bit Single Port Block RAM

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SPR16X2	16 Word by 2 Single Port RAM (within PFU)

Multiplexers

MUX161	16 to 1 Mux
MUX321	32 to 1 Mux
MUX21	2 to 1 Mux
MUX41	4 to 1 Mux
MUX81	8 to 1 Mux

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I/O Cells

Input Buffers

IB	Input Buffer
IBPD	Input Buffer with Pull-down
IBPU	Input Buffer with Pull-up
ILVDS	LVDS Input Buffer

Output Buffers

OB	Output Tristate Buffer
OBW	Output Buffer with Tristate
OBZ	Output Buffer with Tristate
OBZPD	Output Buffer with Tristate and Pull-down
OBZPU	Output Buffer with Tristate and Pull-up
OLVDS	LVDS Output Buffer

Bidirectional Buffers

BB	CMOS Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate – BiDirectional
BBPD	CMOS Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate – BiDirectional and Pull-down
BBPU	CMOS Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate – BiDirectional and Pull-up
BBW	CMOS Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate – BiDirectional in keepermode

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PIC Cells

PIC Flip-Flops (Input)

IFS1P3BX	Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Asynchronous Preset, and System Clock (used in input PIC area only)
IFS1P3DX	Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Asynchronous Clear, and System Clock (used in input PIC area only)
IFS1P3IX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Clear, Positive Level Enable, and System Clock (Clear overrides Enable) (used in input PIC area only)
IFS1P3JX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Preset, Positive Level Enable, and System Clock (Preset overrides Enable) (used in input PIC area only)

PIC Flip-Flops (Output)

OFE1P3BX	Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Asynchronous Preset, and Express Clock (used in output PIC area only)
OFE1P3DX	Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Asynchronous Clear, and Express Clock (used in output PIC area only)
OFE1P3IX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Clear, Positive Level Enable (Clear overrides Enable), and Express Clock (used in output PIC area only)
OFE1P3JX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Preset, Positive Level Enable (Preset overrides Enable), and Express Clock (used in output PIC area only)

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OFS1P3BX	Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Asynchronous Preset, and System Clock (used in output PIC area only)
OFS1P3DX	Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Asynchronous Clear, and System Clock (used in output PIC area only)
OFS1P3IX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Clear, Positive Level Enable (Clear overrides Enable), and System Clock (used in output PIC area only)
OFS1P3JX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Preset, Positive Level Enable (Preset overrides Enable), and System Clock (used in output PIC area only)

PIC Flip-Flops (Latched)

ILF2P3BX	Negative Level Express Clocked (ECLK) Latch, Feeding Positive Edge Triggered System Clocked (SCLK) Flip-Flop, and Positive Level Asynchronous Preset (used in input PIC area only)
ILF2P3DX	Negative Level Express Clocked (ECLK) Latch, Feeding Positive Edge Triggered System Clocked (SCLK) Flip-Flop, and Positive Level Asynchronous Clear (used in input PIC area only)
ILF2P3IX	Negative Level Express Clocked (ECLK) Latch, Feeding Positive Edge Triggered System Clocked (SCLK) Flip-Flop, and Positive Level Synchronous Clear (Clear overrides Enable) (used in input PIC area only)
ILF2P3JX	Negative Level Express Clocked (ECLK) Latch, Feeding Positive Edge Triggered System Clocked (SCLK) Flip-Flop, and Positive Level Synchronous Preset (Preset overrides Enable) (used in input PIC area only)

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PIC Latches (Input)

IFS1S1B	Positive Level Data Latch with Positive Level Asynchronous Preset and System Clock (used in input PIC area only)
IFS1S1D	Positive Level Data Latch with Positive Level Asynchronous Clear and System Clock (used in input PIC area only)
IFS1S1I	Positive Level Data Latch with Positive Level Synchronous Clear and System Clock (used in input PIC area only)
IFS1S1J	Positive Level Data Latch with Positive Level Synchronous Preset and System Clock (used in input PIC area only)

PIC Shift Registers and DDR

IDDRA	Input DDR
IDDRXA	Input DDR
IDDRX1A	Input DDR
IDDRX2A	Input DDR
IDDRX4A	Input DDR
ISRX1A	Input 1-Bit Shift Register
ISRX2A	Input 2-Bit Shift Register
ISRX4A	Input 4-Bit Shift Register
OSRX1A	Output 1-Bit Shift Register
OSRX2A	Output 2-Bit Shift Register
OSRX4A	Output 4-Bit Shift Register
ODDRA	Output DDR
ODDRXA	Output DDR

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ODDRX2A	Output DDR
ODDRX4A	Output DDR

Special Cells

Clock Manager/PLL/DLL

CIDDLLA	Clock Injection Delay Removal
CIMDLLA	Clock Injection Match
CLKCNTL	Clock Controller
EHXPLLA	Enhanced High Performance with Dynamic Input Delay Control PLL
SDCDLLA	Single Delay Cell DLL
TRDLLA	Time Reference Delay

Miscellaneous

JTAGA	JTAG — Logic Control Circuit
OSCA	Internal Oscillator
CLKDET	Clock Detect
CLKDIV	Clock Divider
DELAY	Delay
DCS	Dynamic Clock Selection Multiplexer
RDBK	Readback Controller
STRTUP	Startup Controller
GSR	Global Set/Reset

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SGSR	Synchronous Release Global Set/Reset Interface
L6MUX21	LUT-6 2 to 1 Multiplexer
PFUMX	2-Input Mux within the PFU, C0 used for Selection with Positive Select
TSALL	Global Tristate Interface
PUR	Power Up Set/Reset

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ORCA MACRO LIBRARY SERIES 4

This chapter contains the following sections:

- Logic Gates
- Comparators
- Adders/Subtracters
- Counters
- Flip-Flops
- Latches
- Memory
- 4E-Specific Memory (Block RAM Functions)
- Multiplexers
- Multipliers
- I/O Cells
- PIC Cells
- Special Cells
- FPSC Elements

Logic Gates

AND2	2 Input AND Gate
AND3	3 Input AND Gate
AND4	4 Input AND Gate
AND5	5 Input AND Gate
ND2	2 Input NAND Gate
ND3	3 Input NAND Gate
ND4	4 Input NAND Gate

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ND5	5 Input NAND Gate
OR2	2 Input OR Gate
OR3	3 Input OR Gate
OR4	4 Input OR Gate
OR5	5 Input OR Gate
NR2	2 Input NOR Gate
NR3	3 Input NOR Gate
NR4	4 Input NOR Gate
NR5	5 Input NOR Gate
XNOR2	2 Input Exclusive NOR Gate
XNOR3	3 Input Exclusive NOR Gate
XNOR4	4 Input Exclusive NOR Gate
XNOR5	5 Input Exclusive NOR Gate
XOR2	2 Input Exclusive OR Gate
XOR3	3 Input Exclusive OR Gate
XOR4	4 Input Exclusive OR Gate
XOR5	5 Input Exclusive OR Gate
XOR11	11 Input Exclusive OR Gate
XOR21	21 Input Exclusive OR Gate

Miscellaneous Logic

INV	Inverter

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VHI	Logic High Generator
VLO	Logic Low Generator

Comparators

AGEB4	“A” Greater Than Or Equal To “B” (4 bit)
AGEB8	“A” Greater Than Or Equal To “B” (8 bit)
ALEB4	“A” Less Than Or Equal To “B” (4 bit)
ALEB8	“A” Less Than Or Equal To “B” (8 bit)
ANEB4	“A” Not Equal To “B” (4 bit)
ANEB8	“A” Not Equal To “B” (8 bit)

Adders/Subtracters

FADD4	4 Bit Fast Adder
FADD4O	4 Bit Fast Adder with Overflow
FADD8	8 Bit Fast Adder
FADD8O	8 Bit Fast Adder with Overflow
FSUB4	4 Bit Fast Subtracter (two’s complement)
FSUB4O	4 Bit Fast Subtracter (two’s complement) with Overflow
FSUB8	8 Bit Fast Subtracter (two’s complement)
FSUB8O	8 Bit Fast Subtracter (two’s complement) with Overflow
FADSU4	4 Bit Fast Adder/Subtracter (two’s complement)

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FADSU4O	4 Bit Fast Adder/Subtracter (two's complement) with Overflow
FADSU8	8 Bit Fast Adder/Subtracter (two's complement)
FADSU8O	8 Bit Fast Adder/Subtracter (two's complement) with Overflow

Counters

CU4	Combinational Logic for 4 Bit Up Counter using Look-Up Table
CU4P3BX	4 Bit Positive Edge Triggered Fast Up Counter with Positive Clock Enable and Positive Asynchronous Preset
CU4P3DX	4 Bit Positive Edge Triggered Fast Up Counter with Positive Clock Enable and Positive Asynchronous Clear
CU4P3IX	4 Bit Positive Edge Triggered Fast Up Counter with Positive Clock Enable and Positive Synchronous Clear
CU4P3JX	4 Bit Positive Edge Triggered Fast Up Counter with Positive Clock Enable and Positive Synchronous Preset
CU8P3BX	8 Bit Positive Edge Triggered Fast Up Counter with Positive Clock Enable and Positive Asynchronous Preset
CU8P3DX	8 Bit Positive Edge Triggered Fast Up Counter with Positive Clock Enable and Positive Asynchronous Clear
CU8P3IX	8 Bit Positive Edge Triggered Fast Up Counter with Positive Clock Enable and Positive Synchronous Clear
CU8P3JX	8 Bit Positive Edge Triggered Fast Up Counter with Positive Clock Enable and Positive Synchronous Preset
CD4	Combinational Logic for 4 Bit Down Counter using Look-Up Table
CD4P3BX	4 Bit Positive Edge Triggered Fast Down Counter with Positive Clock Enable and Positive Asynchronous Preset
CD4P3DX	4 Bit Positive Edge Triggered Fast Down Counter with Positive Clock Enable and Positive Asynchronous Clear

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CD4P3IX	4 Bit Positive Edge Triggered Fast Down Counter with Positive Clock Enable and Positive Synchronous Clear
CD4P3JX	4 Bit Positive Edge Triggered Fast Down Counter with Positive Clock Enable and Positive Synchronous Preset
CD8	8 Bit Positive Edge Triggered Fast Down Counter with Positive Clock Enable and Positive Asynchronous Preset
CD8P3DX	8 Bit Positive Edge Triggered Fast Down Counter with Positive Clock Enable and Positive Asynchronous Clear
CD8P3IX	8 Bit Positive Edge Triggered Fast Down Counter with Positive Clock Enable and Positive Synchronous Clear
CD8P3JX	8 Bit Positive Edge Triggered Fast Down Counter with Positive Clock Enable and Positive Synchronous Preset
CB4	Combinational Logic for 4 Bit Bidirectional Counter using Look-Up Table
CB4P3BX	4 Bit Positive Edge Triggered Bidirectional Counter with Positive Clock Enable and Positive Asynchronous Preset
CB4P3DX	4 Bit Positive Edge Triggered Bidirectional Counter with Positive Clock Enable and Positive Asynchronous Clear
CB4P3IX	4 Bit Positive Edge Triggered Bidirectional Counter with Positive Clock Enable and Positive Synchronous Clear
CB4P3JX	4 Bit Positive Edge Triggered Bidirectional Counter with Positive Clock Enable and Positive Synchronous Preset
CB8P3BX	8 Bit Positive Edge Triggered Bidirectional Counter with Positive Clock Enable and Positive Asynchronous Preset
CB8P3DX	8 Bit Positive Edge Triggered Bidirectional Counter with Positive Clock Enable and Positive Asynchronous Clear
CB8P3IX	8 Bit Positive Edge Triggered Bidirectional Counter with Positive Clock Enable and Positive Synchronous Clear

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CB8P3JX	8 Bit Positive Edge Triggered Bidirectional Counter with Positive Clock Enable and Positive Synchronous Preset
DEC4	Combinational Logic for 4 Bit Down Counter using Look-Up Table
DEC8	Combinational Logic for 8 Bit Down Counter using Look-Up Table
INC4	Combinational Logic for 4 Bit Up Counter using Look-Up Table
INC8	Combinational Logic for 8 Bit Up Counter using Look-Up Table
INCDEC4	Combinational Logic for 4 Bit Bidirectional Counter using Look-Up Table
INCDEC8	Combinational Logic for 8 Bit Bidirectional Counter using Look-Up Table

Loadable Counters

LU4P3AX	4 Bit Positive Edge Triggered Loadable Up Counter with Positive Clock Enable, GSR Used for Clear
LU4P3AY	4 Bit Positive Edge Triggered Loadable Up Counter with Positive Clock Enable, GSR Used for Preset
LU4P3BX	4 Bit Positive Edge Triggered Loadable Up Counter with Positive Clock Enable and Positive Level Asynchronous Preset
LU4P3DX	4 Bit Positive Edge Triggered Loadable Up Counter with Positive Clock Enable and Positive Level Asynchronous Clear
LU4P3IX	4 Bit Positive Edge Triggered Loadable Up Counter with Positive Clock Enable and Positive Level Synchronous Clear (Clear overrides Enable)
LU4P3JX	4 Bit Positive Edge Triggered Loadable Up Counter with Positive Clock Enable and Positive Level Synchronous Preset (Preset overrides Enable)
LU8P3BX	8 Bit Positive Edge Triggered Loadable Up Counter with Positive Clock Enable and Positive Level Asynchronous Preset

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LU8P3DX	8 Bit Positive Edge Triggered Loadable Up Counter with Positive Clock Enable and Positive Level Asynchronous Clear
LU8P3IX	8 Bit Positive Edge Triggered Loadable Up Counter with Positive Clock Enable and Positive Level Synchronous Clear (Clear overrides Enable)
LU8P3JX	8 Bit Positive Edge Triggered Loadable Up Counter with Positive Clock Enable and Positive Level Synchronous Preset (Preset overrides Enable)
LD4P3AX	4 Bit Positive Edge Triggered Loadable Down Counter with Positive Clock Enable, GSR Used for Clear
LD4P3AY	4 Bit Positive Edge Triggered Loadable Down Counter with Positive Clock Enable, GSR Used for Preset
LD4P3BX	4 Bit Positive Edge Triggered Loadable Down Counter with Positive Clock Enable and Positive Level Asynchronous Preset
LD4P3DX	4 Bit Positive Edge Triggered Loadable Down Counter with Positive Clock Enable and Positive Level Asynchronous Clear
LD4P3IX	4 Bit Positive Edge Triggered Loadable Down Counter with Positive Clock Enable and Positive Level Synchronous Clear (Clear overrides Enable)
LD4P3JX	4 Bit Positive Edge Triggered Loadable Down Counter with Positive Clock Enable and Positive Level Synchronous Preset (Preset overrides Enable)
LD8P3BX	8 Bit Positive Edge Triggered Loadable Down Counter with Positive Clock Enable and Positive Level Asynchronous Preset
LD8P3DX	8 Bit Positive Edge Triggered Loadable Down Counter with Positive Clock Enable and Positive Level Asynchronous Clear
LD8P3IX	8 Bit Positive Edge Triggered Loadable Down Counter with Positive Clock Enable and Positive Level Synchronous Clear (Clear overrides Enable)

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LD8P3JX	8 Bit Positive Edge Triggered Loadable Down Counter with Positive Clock Enable and Positive Level Synchronous Preset (Preset overrides Enable)
LB4P3AX	4 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable, GSR Used for Clear
LB4P3AY	4 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable, GSR Used for Preset
LB4P3BX	4 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable and Positive Level Asynchronous Preset
LB4P3DX	4 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable and Positive Level Asynchronous Clear
LB4P3IX	4 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable and Positive Level Synchronous Clear (Clear overrides Enable)
LB4P3JX	4 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable and Positive Level Synchronous Preset (Preset overrides Enable)
LB8P3BX	8 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable and Positive Level Asynchronous Preset
LB8P3DX	8 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable and Positive Level Asynchronous Clear
LB8P3IX	8 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable and Positive Level Synchronous Clear (Clear overrides Enable)
LB8P3JX	8 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable and Positive Level Synchronous Preset (Preset overrides Enable)

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Flip-Flops

FD1P3AX	Positive Edge Triggered D Flip-Flop with Positive Level Enable, GSR used for Clear
FD1P3AY	Positive Edge Triggered D Flip-Flop with Positive Level Enable, GSR used for Preset
FD1P3BX	Positive Edge Triggered D Flip-Flop with Positive Level Enable and Positive Level Asynchronous Preset
FD1P3DX	Positive Edge Triggered D Flip-Flop with Positive Level Enable and Positive Level Asynchronous Clear
FD1P3IX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Clear and Positive Level Enable (Clear overrides Enable)
FD1P3IZ	Positive Edge Triggered D Flip-Flop with Positive Level Enable and Positive Level Synchronous Clear
FD1P3JX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Preset and Positive Level Enable (Preset overrides Enable)
FD1P3JZ	Positive Edge Triggered D Flip-Flop with Positive Level Enable and Positive Level Synchronous Preset
FD1S3AX	Positive Edge Triggered D Flip-Flop, GSR Used for Clear
FD1S3AY	Positive Edge Triggered D Flip-Flop, GSR Used for Preset
FD1S3BX	Positive Edge Triggered D Flip-Flop with Positive Level Asynchronous Preset
FD1S3DX	Positive Edge Triggered D Flip-Flop with Positive Level Asynchronous Clear
FD1S3IX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Clear

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FD1S3JX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Preset
FL1P3AY	Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, Positive Level Data Select, and Positive Level Enable, GSR used for Preset
FL1P3AZ	Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, Positive Level Data Select, and Positive Level Enable, GSR used for Clear
FL1P3BX	Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, Positive Level Data Select, Positive Level Asynchronous Preset, and Positive Level Enable
FL1P3DX	Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, Positive Level Data Select, Positive Level Asynchronous Clear, and Positive Level Enable
FL1P3IY	Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, Positive Level Data Select, Positive Level Synchronous Clear, and Positive Level Enable (Clear overrides Enable)
FL1P3IZ	Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, Positive Level Data Select, Positive Level Synchronous Clear, and Positive Level Enable
FL1P3JY	Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, Positive Level Data Select, Positive Level Synchronous Preset, and Positive Level Enable (Preset overrides Enable)
FL1P3JZ	Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, Positive Level Data Select, Positive Level Asynchronous Preset, and Positive Level Enable
FL1S3AX	Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, GSR used for Clear
FL1S3AY	Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, GSR used for Preset

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Latches

FD1S1A	Positive Level Data Latch with GSR Used for Clear
FD1S1AY	Positive Level Data Latch with GSR Used for Preset
FD1S1B	Positive Level Data Latch with Positive Level Asynchronous Preset
FD1S1D	Positive Level Data Latch with Positive Level Asynchronous Clear
FD1S1I	Positive Level Data Latch with Positive Level Synchronous Clear
FD1S1J	Positive Level Data Latch with Positive Level Synchronous Preset
FL1S1A	Positive Level Loadable Latch with Positive Select and GSR Used for Clear
FL1S1AY	Positive Level Loadable Latch with Positive Select and GSR Used for Preset
FL1S1B	Positive Level Loadable Latch with Positive Select and Positive Level Asynchronous Preset
FL1S1D	Positive Level Loadable Latch with Positive Select and Positive Level Asynchronous Clear
FL1S1I	Positive Level Loadable Latch with Positive Select and Positive Level Synchronous Clear
FL1S1J	Positive Level Loadable Latch with Positive Select and Positive Level Synchronous Preset

Memory

DCE32X4	32 Word by 2 Bit Negative Edge Triggered Write Synchronous Dual Port Memory with Positive Write Enable and Two Positive Write Port Enables
RCE32X4	32 Word by 4 Bit Negative Edge Triggered Write Synchronous Single Port Memory with Positive Write Enable and Two Positive Write Port Enables

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ROM16X1	16 word by 1 bit read-only memory
ROM32X1	32 word by 1 bit read-only memory
ROM32X4	32 Word by 4 Bit Positive Edge Triggered Read-Only Memory with Registered Data Outputs

4E-Specific Memory (Block RAM Functions)

BR512X18	512 Word by18 Bit 4 Port Block RAM
BR1024X18	1024 Word by18 Bit 4 Port Block RAM
CAM2X256X16	2X256X16 Content Addressable Memory
CMULT16	8 Bit or 16 Bit Constant Multiplier
FF512X18	512 Word by 18 Bit FIFO
FF256X36	256 Word by 36 Bit FIFO
FF1024X9	1024 Word by 9 Bit FIFO
FF2X512X9	2 512 Word by 9 Bit FIFOs
MULT8X8	8 Bit by 8 Bit Multiplier
SBR512X18	512 Word by18 Bit System Bus RAM
SBR1024X18	1024 Word by 18 Bit System Bus RAM
ULIM	System Bus User Logic Interface (Master)
ULIS	System Bus User Logic Interface (Slave)

Multiplexers

MUX21	2 to 1 Mux
MUX21E	2 to 1 Mux with Enable

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MUX41	4 to 1 Mux
MUX41E	4 to 1 Mux with Enable
MUX81	8 to 1 Mux
PFUMX41	4 to 1 PFU Mux

Multipliers

FMULT41	4 X 1 Fast Multiplier
FMULT81	8 X 1 Fast Multiplier

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I/O Cells

Input Buffers

IBM	CMOS Input Buffer
IBMS	CMOS Input Buffer with Delay
IBMPD	CMOS Input Buffer with Pull-down
IBMPDS	CMOS Input Buffer with Pull-down and Delay
IBMPU	CMOS Input Buffer with Pull-up
IBMPUS	CMOS Input Buffer with Pull-up and Delay
IBT	TTL Input Buffer
IBTS	TTL Input Buffer with Delay
IBTPD	TTL Input Buffer with Pull-down
IBTPDS	TTL Input Buffer with Pull-down and Delay
IBTPU	TTL Input Buffer with Pull-up
IBTPUS	TTL Input Buffer with Pull-up and Delay
ILVDS	LVDS Input Buffer

Output Buffers

OBW6	Output Tri-state Buffer
OB6	6mA Sink 3mA Source Sinklim Output Buffer
OB12	12mA Sink 6mA Source Slewlim Output Buffer
OB12F	12mA Sink 6mA Source Fast Output Buffer
OBZ6	6mA Sink 3mA Source Sinklim Output Buffer with Tristate

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OBZ6PD	6mA Sink 3mA Source Sinklim Output Buffer with Tristate and Pull-down
OBZ6PU	6mA Sink 3mA Source Sinklim Output Buffer with Tristate and Pull-up
OBZ12	12mA Sink 6mA Source Slewlim Output Buffer with Tristate
OBZ12PD	12mA Sink 6mA Source Slewlim Output Buffer with Tristate and Pull-down
OBZ12PU	12mA Sink 6mA Source Slewlim Output Buffer with Tristate and Pull-up
OBZ12F	12mA Sink 6mA Source Fast Output Buffer with Tristate
OBZ12FPD	12mA Sink 6mA Source Fast Output Buffer with Tristate and Pull-down
OBZ12FPU	12mA Sink 6mA Source Fast Output Buffer with Tristate and Pull-up
OLVDS	LVDS Output Buffer

Bidirectional Buffers

BMW6	BiDirectional Buffer
BMZ6	CMOS Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate – BiDirectional
BMZ6PD	CMOS Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate and Pull-down – BiDirectional
BMZ6PU	CMOS Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate and Pull-up – BiDirectional
BMZ12	CMOS Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate – BiDirectional
BMZ12PD	CMOS Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate and Pull-down – BiDirectional

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BMZ12PU	CMOS Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate and Pull-up –BiDirectional
BMZ12F	CMOS Input 12mA Sink 6mA Source Fast Output Buffer with Tristate – BiDirectional
BMZ12FPD	CMOS Input 12mA Sink 6mA Source Fast Output Buffer with Tristate and Pull-down – BiDirectional
BMZ12FPU	CMOS Input 12mA Sink 6mA Source Fast Output Buffer with Tristate and Pull-up – BiDirectional
BTZ6	TTL Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate – BiDirectional
BTZ6PD	TTL Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate and Pull-down – BiDirectional
BTZ6PU	TTL Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate and Pull-up – BiDirectional
BTZ12	TTL Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate – BiDirectional
BTZ12PD	TTL Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate and Pull-down – BiDirectional
BTZ12PU	TTL Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate and Pull-up– BiDirectional
BTZ12F	TTL Input 12mA Sink 6mA Source Fast Output Buffer with Tristate – BiDirectional
BTZ12FPD	TTL Input 12mA Sink 6mA Source Fast Output Buffer with Tristate and Pull-down – BiDirectional
BTZ12FPU	TTL Input 12mA Sink 6mA Source Fast Output Buffer with Tristate and Pull-up – BiDirectional

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Bidirectional Buffers With Delayed Input

BMS6	CMOS Delayed Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate – BiDirectional
BMS6PD	CMOS Delayed Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate and Pull-down – BiDirectional
BMS6PU	CMOS Delayed Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate and Pull-up – BiDirectional
BMS12	CMOS Delayed Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate – BiDirectional
BMS12PD	CMOS Delayed Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate and Pull-down – BiDirectional
BMS12PU	CMOS Delayed Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate and Pull-up – BiDirectional
BMS12F	CMOS Delayed Input 12mA Sink 6mA Source Fast Output Buffer with Tristate – BiDirectional
BMS12FPD	CMOS Delayed Input 12mA Sink 6mA Source Fast Output Buffer with Tristate and Pull-down – BiDirectional
BMS12FPU	CMOS Delayed Input 12mA Sink 6mA Source Fast Output Buffer with Tristate and Pull-up – BiDirectional
BTS6	TTL Delayed Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate – BiDirectional
BTS6PD	TTL Delayed Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate and Pull-down – BiDirectional
BTS6PU	TTL Delayed Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate and Pull-up – BiDirectional
BTS12	TTL Delayed Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate – BiDirectional

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BTS12PD	TTL Delayed Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate and Pull-down – BiDirectional
BTS12PU	TTL Delayed Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate and Pull-up – BiDirectional
BTS12F	TTL Delayed Input 12mA Sink 6mA Source Fast Output Buffer with Tristate – BiDirectional
BTS12FPD	TTL Delayed Input 12mA Sink 6mA Source Fast Output Buffer with Tristate and Pull-down – BiDirectional
BTS12FPU	TTL Delayed Input 12mA Sink 6mA Source Fast Output Buffer with Tristate and Pull-up – BiDirectional

PIC Cells

PIC Gates

OEAND2	2 Input AND Gate with Express Clock (used in PIC area only)
OEND2	2 Input NAND Gate with Express Clock (used in PIC area only)
OENR2	2 Input NOR Gate with Express Clock (used in PIC area only)
OEOR2	2 Input OR Gate with Express Clock (used in PIC area only)
OEXNOR2	2 Input Exclusive NOR Gate with Express Clock (used in PIC area only)
OEXOR2	2 Input Exclusive OR Gate with Express Clock (used in PIC area only)
OSAND2	2 Input AND Gate with System Clock (used in PIC area only)
OSND2	2 Input NAND Gate with System Clock (used in PIC area only)
OSNR2	2 Input NOR Gate with System Clock (used in PIC area only)
OSOR2	2 Input OR Gate with System Clock (used in PIC area only)

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OSXNOR2	2 Input Exclusive NOR Gate with System Clock (used in PIC area only)
OSXOR2	2 Input Exclusive OR Gate with System Clock (used in PIC area only)

PIC Multiplexers

OEMUX21	2 to 1 Mux with Express Clock (used in PIC area only)
OSMUX21	2 to 1 Mux with System Clock (used in PIC area only)

PIC Flip-Flops (Input)

IFS1P3BX	Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Asynchronous Preset, and System Clock (used in input PIC area only)
IFS1P3DX	Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Asynchronous Clear, and System Clock (used in input PIC area only)
IFS1P3IX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Clear, Positive Level Enable, and System Clock (Clear overrides Enable) (used in input PIC area only)
IFS1P3IZ	Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Synchronous Clear, and System Clock (used in input PIC area only)
IFS1P3JX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Preset, Positive Level Enable, and System Clock (Preset overrides Enable) (used in input PIC area only)
IFS1P3JZ	Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Synchronous Preset, and System Clock (used in input PIC area only)

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PIC Flip-Flops (Output)

OFE1P3BX	Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Asynchronous Preset, and Express Clock (used in output PIC area only)
OFE1P3DX	Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Asynchronous Clear, and Express Clock (used in output PIC area only)
OFE1P3IX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Clear, Positive Level Enable (Clear overrides Enable), and Express Clock (used in output PIC area only)
OFE1P3IZ	Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Synchronous Clear, and Express Clock (used in output PIC area only)
OFE1P3JX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Preset, Positive Level Enable (Preset overrides Enable), and Express Clock (used in output PIC area only)
OFE1P3JZ	Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Synchronous Preset, and Express Clock (used in output PIC area only)
OFS1P3BX	Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Asynchronous Preset, and System Clock (used in output PIC area only)
OFS1P3DX	Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Asynchronous Clear, and System Clock (used in output PIC area only)
OFS1P3IX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Clear, Positive Level Enable (Clear overrides Enable), and System Clock (used in output PIC area only)
OFS1P3IZ	Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Synchronous Clear, and System Clock (used in output PIC area only)

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OFS1P3JX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Preset, Positive Level Enable (Preset overrides Enable), and System Clock (used in output PIC area only)
OFS1P3JZ	Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Synchronous Preset, and System Clock (used in output PIC area only)

PIC Flip-Flops (Latched)

ILF2P3BX	Negative Level Express Clocked (ECLK) Latch, Feeding Positive Edge Triggered System Clocked (SCLK) Flip-Flop, and Positive Level Asynchronous Preset (used in input PIC area only)
ILF2P3DX	Negative Level Express Clocked (ECLK) Latch, Feeding Positive Edge Triggered System Clocked (SCLK) Flip-Flop, and Positive Level Asynchronous Clear (used in input PIC area only)
ILF2P3IX	Negative Level Express Clocked (ECLK) Latch, Feeding Positive Edge Triggered System Clocked (SCLK) Flip-Flop, and Positive Level Synchronous Clear (Clear overrides Enable) (used in input PIC area only)
ILF2P3IZ	Negative Level Express Clocked (ECLK) Latch, Feeding Positive Edge Triggered System Clocked (SCLK) Flip-Flop, and Positive Level Synchronous Clear (used in input PIC area only)
ILF2P3JX	Negative Level Express Clocked (ECLK) Latch, Feeding Positive Edge Triggered System Clocked (SCLK) Flip-Flop, and Positive Level Synchronous Preset (Preset overrides Enable) (used in input PIC area only)
ILF2P3JZ	Negative Level Express Clocked (ECLK) Latch, Feeding Positive Edge Triggered System Clocked (SCLK) Flip-Flop, and Positive Level Synchronous Preset (used in input PIC area only)

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PIC Latches (Input)

IFS1S1B	Positive Level Data Latch with Positive Level Asynchronous Preset and System Clock (used in input PIC area only)
IFS1S1D	Positive Level Data Latch with Positive Level Asynchronous Clear and System Clock (used in input PIC area only)
IFS1S1I	Positive Level Data Latch with Positive Level Synchronous Clear and System Clock (used in input PIC area only)
IFS1S1J	Positive Level Data Latch with Positive Level Synchronous Preset and System Clock (used in input PIC area only)

PIC Latches (Output)

OFE1S1B	Output Positive Level Data Latch with Positive Level Asynchronous Preset and Express Clock (used in output PIC area only)
OFE1S1D	Output Positive Level Data Latch with Positive Level Asynchronous Preset and Express Clock (used in output PIC area only)
OFE1S1I	Output Positive Level Data Latch with Positive Level Asynchronous Preset and Express Clock (used in output PIC area only)
OFE1S1J	Output Positive Level Data Latch with Positive Level Asynchronous Preset and Express Clock (used in output PIC area only)
OFS1S1B	Output Positive Level Data Latch with Positive Level Asynchronous Preset and System Clock (used in output PIC area only)
OFS1S1D	Output Positive Level Data Latch with Positive Level Asynchronous Preset and System Clock (used in output PIC area only)
OFS1S1I	Output Positive Level Data Latch with Positive Level Asynchronous Preset and System Clock (used in output PIC area only)
OFS1S1J	Output Positive Level Data Latch with Positive Level Asynchronous Preset and System Clock (used in output PIC area only)

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PIC Shift Registers and DDR

HIODDR	High-speed Input/Output DDR
HIOSR2	High-speed Input/Output 2 Bit Shift Register
HIOSR4	High-speed Input/Output 4 Bit Shift Register
HOSR2X2	High-speed Output Dual 2 Bit Shift Register
NOTE: The above high-speed elements use an edge clock. You must pass the property INTERFACE:FASTINPUT to the input pads driving these elements and also address the special requirement of the clock source with this property on pad C.	
IDDR	Input DDR
IODDR	Input/Output DDR
IOSR2	Input/Output 2 Bit Shift Register
IOSR4	Input/Output 4 Bit Shift Register
OSR2X2	Output Dual 2 Bit Shift Register

Special Cells

Miscellaneous

BNDSCAN	Boundary Scan — Logic Control Circuit
OSCIL	Internal Oscillator
PFUMX41	4 Input Mux within the PFU
READBK	Readback Controller
STRTUP	Startup Controller
GSR	Global Set/Reset
TSALL	Global Tristate Interface

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PUR	Power Up Set/Reset

Clock Manager

DLL1XB	Programmable Clock Manager (Delay Locked Loop) — Bottom
DLL1XT	Programmable Clock Manager (Delay Locked Loop) — Top
DLLPDB	Programmable Clock Manager (Programmable Delay, Delay Locked Loop) — Bottom
DLLPDT	Programmable Clock Manager (Programmable Delay, Delay Locked Loop) — Top
HPPLL	High Frequency Programmable Clock Manager (Programmable general purpose Phase Locked Loop)
PLL1	Programmable Clock Manager (Phase Locked Loop) — Top-right and bottom-left dedicated PLL used for clock conditioning at 1.544 MHz and 2.048 MHz
PLL2	Programmable Clock Manager (Phase Locked Loop) — Top-left and bottom-right dedicated PLL used for clock conditioning at 155.52 MHz
PLLB	Programmable Clock Manager (Phase Locked Loop) — Bottom
PLLT	Programmable Clock Manager (Phase Locked Loop) — Top
PCMB	Programmable Clock Manager – Bottom
PCMBUFB	Programmable Clock Manager In Bypass Mode – Bottom
PCMBUFT	Programmable Clock Manager In Bypass Mode – Top
PCMT	Programmable Clock Manager – Top
PPLL	Programmable Clock Manager (Programmable general purpose Phase Locked Loop)

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SLIC Gates

SAND2	2 Input AND Gate (used in SLIC area only)
SAND4	4 Input AND Gate (used in SLIC area only)
SAND6	6 Input AND Gate (used in SLIC area only)
SAND8	8 Input AND Gate (used in SLIC area only)
SAND10	10 Input AND Gate (used in SLIC area only)
SOR2	2 Input OR Gate (used in SLIC area only)
SOR4	4 Input OR Gate (used in SLIC area only)
SOR6	6 Input OR Gate (used in SLIC area only)
SOR8	8 Input OR Gate (used in SLIC area only)
SOR10	10 Input OR Gate (used in SLIC area only)
SAOI42	AND Array to OR Inverted (used in SLIC area only)
SAOI44	AND Array to OR Inverted (used in SLIC area only)
SAOI442	AND Array to OR Inverted (used in SLIC area only)

SLIC Buffers

TBUF	Internal Buffer with Tristate (used in SLIC area only)
TIBUF	Internal Buffer with Inverted Tristate (used in SLIC area only)

9th Flip-Flop

CFD1P3BX	Positive Edge Triggered D Flip-Flop with Positive Level Enable and Positive Level Asynchronous Preset (mapped to 9th Flip-Flop in the PLC only)

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CFD1P3DX	Positive Edge Triggered D Flip-Flop with Positive Level Enable and Positive Level Asynchronous Clear (mapped to 9th Flip-Flop in the PLC only)
CFD1P3IX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Clear and Positive Level Enable (Clear overrides Enable) (mapped to 9th Flip-Flop in the PLC only)
CFD1P3IZ	Positive Edge Triggered D Flip-Flop with Positive Level Enable and Positive Level Synchronous Clear (mapped to 9th Flip-Flop in the PLC only)
CFD1P3JX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Preset and Positive Level Enable (Preset overrides Enable) (mapped to 9th Flip-Flop in the PLC only)
CFD1P3JZ	Positive Edge Triggered D Flip-Flop with Positive Level Enable and Positive Level Synchronous Preset (mapped to 9th Flip-Flop in the PLC only)

FPSC Elements

INTRBUF	ASB/FPGA interface cell that gets mapped to the bottom row of PICs. Unconnected inputs should be pulled down.
IINTRBUFS	ASB/FPGA interface cell that gets mapped to the bottom row of PICs. Delayed input buffer, unconnected inputs should be pulled down.
ITOASBCK	Buffer used to route clocks from FPGA to ASB along clock spine.
IFRASBCK	Buffer used to route clocks from ASB to FPGA along clock spine.

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ORCA MACRO LIBRARY SERIES 3

This chapter contains the following sections:

- Logic Gates
- Counters
- Flip-Flops
- Latches
- Memory
- Multiplexers
- I/O Cells
- PIC Cells
- Special Cells
- Series 3+ Elements

Logic Gates

AND2	2 Input AND Gate
AND3	3 Input AND Gate
AND4	4 Input AND Gate
AND5	5 Input AND Gate
ND2	2 Input NAND Gate
ND3	3 Input NAND Gate
ND4	4 Input NAND Gate
ND5	5 Input NAND Gate
OR2	2 Input OR Gate
OR3	3 Input OR Gate

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OR4	4 Input OR Gate
OR5	5 Input OR Gate
NR2	2 Input NOR Gate
NR3	3 Input NOR Gate
NR4	4 Input NOR Gate
NR5	5 Input NOR Gate
XNOR2	2 Input Exclusive NOR Gate
XNOR3	3 Input Exclusive NOR Gate
XNOR4	4 Input Exclusive NOR Gate
XNOR5	5 Input Exclusive NOR Gate
XOR2	2 Input Exclusive OR Gate
XOR3	3 Input Exclusive OR Gate
XOR4	4 Input Exclusive OR Gate
XOR5	5 Input Exclusive OR Gate
XOR11	11 Input Exclusive OR Gate
XOR21	21 Input Exclusive OR Gate

Miscellaneous Logic

INV	Inverter
VHI	Logic High Generator
VLO	Logic Low Generator

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Comparators

AGEB4	“A” Greater Than Or Equal To “B” (4 bit)
AGEB8	“A” Greater Than Or Equal To “B” (8 bit)
ALEB4	“A” Less Than Or Equal To “B” (4 bit)
ALEB8	“A” Less Than Or Equal To “B” (8 bit)
ANEB4	“A” Not Equal To “B” (4 bit)
ANEB8	“A” Not Equal To “B” (8 bit)

Adders/Subtracters

FADD4	4 Bit Fast Adder
FADD4O	4 Bit Fast Adder with Overflow
FADD8	8 Bit Fast Adder
FADD8O	8 Bit Fast Adder with Overflow
FSUB4	4 Bit Fast Subtracter (two’s complement)
FSUB4O	4 Bit Fast Subtracter (two’s complement) with Overflow
FSUB8	8 Bit Fast Subtracter (two’s complement)
FSUB8O	8 Bit Fast Subtracter (two’s complement) with Overflow
FADSU4	4 Bit Fast Adder/Subtracter (two’s complement)
FADSU4O	4 Bit Fast Adder/Subtracter (two’s complement) with Overflow
FADSU8	8 Bit Fast Adder/Subtracter (two’s complement)
FADSU8O	8 Bit Fast Adder/Subtracter (two’s complement) with Overflow

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Multipliers

FMULT41	4 X 1 Fast Multiplier
FMULT81	8 X 1 Fast Multiplier

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Counters

CU4	Combinational Logic for 4 Bit Up Counter using Look-Up Table
CU4P3BX	4 Bit Positive Edge Triggered Fast Up Counter with Positive Clock Enable and Positive Asynchronous Preset
CU4P3DX	4 Bit Positive Edge Triggered Fast Up Counter with Positive Clock Enable and Positive Asynchronous Clear
CU4P3IX	4 Bit Positive Edge Triggered Fast Up Counter with Positive Clock Enable and Positive Synchronous Clear
CU4P3JX	4 Bit Positive Edge Triggered Fast Up Counter with Positive Clock Enable and Positive Synchronous Preset
CU8P3BX	8 Bit Positive Edge Triggered Fast Up Counter with Positive Clock Enable and Positive Asynchronous Preset
CU8P3DX	8 Bit Positive Edge Triggered Fast Up Counter with Positive Clock Enable and Positive Asynchronous Clear
CU8P3IX	8 Bit Positive Edge Triggered Fast Up Counter with Positive Clock Enable and Positive Synchronous Clear
CU8P3JX	8 Bit Positive Edge Triggered Fast Up Counter with Positive Clock Enable and Positive Synchronous Preset
CD4	Combinational Logic for 4 Bit Down Counter using Look-Up Table
CD4P3BX	4 Bit Positive Edge Triggered Fast Down Counter with Positive Clock Enable and Positive Asynchronous Preset
CD4P3DX	4 Bit Positive Edge Triggered Fast Down Counter with Positive Clock Enable and Positive Asynchronous Clear
CD4P3IX	4 Bit Positive Edge Triggered Fast Down Counter with Positive Clock Enable and Positive Synchronous Clear
CD4P3JX	4 Bit Positive Edge Triggered Fast Down Counter with Positive Clock Enable and Positive Synchronous Preset

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CD8	8 Bit Positive Edge Triggered Fast Down Counter with Positive Clock Enable and Positive Asynchronous Preset
CD8P3DX	8 Bit Positive Edge Triggered Fast Down Counter with Positive Clock Enable and Positive Asynchronous Clear
CD8P3IX	8 Bit Positive Edge Triggered Fast Down Counter with Positive Clock Enable and Positive Synchronous Clear
CD8P3JX	8 Bit Positive Edge Triggered Fast Down Counter with Positive Clock Enable and Positive Synchronous Preset
CB4	Combinational Logic for 4 Bit Bidirectional Counter using Look-Up Table
CB4P3BX	4 Bit Positive Edge Triggered Bidirectional Counter with Positive Clock Enable and Positive Asynchronous Preset
CB4P3DX	4 Bit Positive Edge Triggered Bidirectional Counter with Positive Clock Enable and Positive Asynchronous Clear
CB4P3IX	4 Bit Positive Edge Triggered Bidirectional Counter with Positive Clock Enable and Positive Synchronous Clear
CB4P3JX	4 Bit Positive Edge Triggered Bidirectional Counter with Positive Clock Enable and Positive Synchronous Preset
CB8P3BX	8 Bit Positive Edge Triggered Bidirectional Counter with Positive Clock Enable and Positive Asynchronous Preset
CB8P3DX	8 Bit Positive Edge Triggered Bidirectional Counter with Positive Clock Enable and Positive Asynchronous Clear
CB8P3IX	8 Bit Positive Edge Triggered Bidirectional Counter with Positive Clock Enable and Positive Synchronous Clear
CB8P3JX	8 Bit Positive Edge Triggered Bidirectional Counter with Positive Clock Enable and Positive Synchronous Preset
DEC4	Combinational Logic for 4 Bit Down Counter using Look-Up Table
DEC8	Combinational Logic for 8 Bit Down Counter using Look-Up Table

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INC4	Combinational Logic for 4 Bit Up Counter using Look-Up Table
INC8	Combinational Logic for 8 Bit Up Counter using Look-Up Table
INCDEC4	Combinational Logic for 4 Bit Bidirectional Counter using Look-Up Table
INCDEC8	Combinational Logic for 8 Bit Bidirectional Counter using Look-Up Table

Loadable Counters

LU4P3AX	4 Bit Positive Edge Triggered Loadable Up Counter with Positive Clock Enable, GSR Used for Clear
LU4P3AY	4 Bit Positive Edge Triggered Loadable Up Counter with Positive Clock Enable, GSR Used for Preset
LU4P3BX	4 Bit Positive Edge Triggered Loadable Up Counter with Positive Clock Enable and Positive Level Asynchronous Preset
LU4P3DX	4 Bit Positive Edge Triggered Loadable Up Counter with Positive Clock Enable and Positive Level Asynchronous Clear
LU4P3IX	4 Bit Positive Edge Triggered Loadable Up Counter with Positive Clock Enable and Positive Level Synchronous Clear (Clear overrides Enable)
LU4P3JX	4 Bit Positive Edge Triggered Loadable Up Counter with Positive Clock Enable and Positive Level Synchronous Preset (Preset overrides Enable)
LU8P3BX	8 Bit Positive Edge Triggered Loadable Up Counter with Positive Clock Enable and Positive Level Asynchronous Preset
LU8P3DX	8 Bit Positive Edge Triggered Loadable Up Counter with Positive Clock Enable and Positive Level Asynchronous Clear
LU8P3IX	8 Bit Positive Edge Triggered Loadable Up Counter with Positive Clock Enable and Positive Level Synchronous Clear (Clear overrides Enable)

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LU8P3JX	8 Bit Positive Edge Triggered Loadable Up Counter with Positive Clock Enable and Positive Level Synchronous Preset (Preset overrides Enable)
LD4P3AX	4 Bit Positive Edge Triggered Loadable Down Counter with Positive Clock Enable, GSR Used for Clear
LD4P3AY	4 Bit Positive Edge Triggered Loadable Down Counter with Positive Clock Enable, GSR Used for Preset
LD4P3BX	4 Bit Positive Edge Triggered Loadable Down Counter with Positive Clock Enable and Positive Level Asynchronous Preset
LD4P3DX	4 Bit Positive Edge Triggered Loadable Down Counter with Positive Clock Enable and Positive Level Asynchronous Clear
LD4P3IX	4 Bit Positive Edge Triggered Loadable Down Counter with Positive Clock Enable and Positive Level Synchronous Clear (Clear overrides Enable)
LD4P3JX	4 Bit Positive Edge Triggered Loadable Down Counter with Positive Clock Enable and Positive Level Synchronous Preset (Preset overrides Enable)
LD8P3BX	8 Bit Positive Edge Triggered Loadable Down Counter with Positive Clock Enable and Positive Level Asynchronous Preset
LD8P3DX	8 Bit Positive Edge Triggered Loadable Down Counter with Positive Clock Enable and Positive Level Asynchronous Clear
LD8P3IX	8 Bit Positive Edge Triggered Loadable Down Counter with Positive Clock Enable and Positive Level Synchronous Clear (Clear overrides Enable)
LD8P3JX	8 Bit Positive Edge Triggered Loadable Down Counter with Positive Clock Enable and Positive Level Synchronous Preset (Preset overrides Enable)
LB4P3AX	4 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable, GSR Used for Clear

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LB4P3AY	4 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable, GSR Used for Preset
LB4P3BX	4 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable and Positive Level Asynchronous Preset
LB4P3DX	4 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable and Positive Level Asynchronous Clear
LB4P3IX	4 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable and Positive Level Synchronous Clear (Clear overrides Enable)
LB4P3JX	4 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable and Positive Level Synchronous Preset (Preset overrides Enable)
LB8P3BX	8 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable and Positive Level Asynchronous Preset
LB8P3DX	8 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable and Positive Level Asynchronous Clear
LB8P3IX	8 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable and Positive Level Synchronous Clear (Clear overrides Enable)
LB8P3JX	8 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable and Positive Level Synchronous Preset (Preset overrides Enable)

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Flip-Flops

FD1P3AX	Positive Edge Triggered D Flip-Flop with Positive Level Enable, GSR used for Clear
FD1P3AY	Positive Edge Triggered D Flip-Flop with Positive Level Enable, GSR used for Preset
FD1P3BX	Positive Edge Triggered D Flip-Flop with Positive Level Enable and Positive Level Asynchronous Preset
FD1P3DX	Positive Edge Triggered D Flip-Flop with Positive Level Enable and Positive Level Asynchronous Clear
FD1P3IX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Clear and Positive Level Enable (Clear overrides Enable)
FD1P3IZ	Positive Edge Triggered D Flip-Flop with Positive Level Enable and Positive Level Synchronous Clear
FD1P3JX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Preset and Positive Level Enable (Preset overrides Enable)
FD1P3JZ	Positive Edge Triggered D Flip-Flop with Positive Level Enable and Positive Level Synchronous Preset
FD1S3AX	Positive Edge Triggered D Flip-Flop, GSR Used for Clear
FD1S3AY	Positive Edge Triggered D Flip-Flop, GSR Used for Preset
FD1S3BX	Positive Edge Triggered D Flip-Flop with Positive Level Asynchronous Preset
FD1S3DX	Positive Edge Triggered D Flip-Flop with Positive Level Asynchronous Clear
FD1S3IX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Clear

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FD1S3JX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Preset
FL1P3AY	Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, Positive Level Data Select, and Positive Level Enable, GSR used for Preset
FL1P3AZ	Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, Positive Level Data Select, and Positive Level Enable, GSR used for Clear
FL1P3BX	Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, Positive Level Data Select, Positive Level Asynchronous Preset, and Positive Level Enable
FL1P3DX	Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, Positive Level Data Select, Positive Level Asynchronous Clear, and Positive Level Enable
FL1P3IY	Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, Positive Level Data Select, Positive Level Synchronous Clear, and Positive Level Enable (Clear overrides Enable)
FL1P3IZ	Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, Positive Level Data Select, Positive Level Synchronous Clear, and Positive Level Enable
FL1P3JY	Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, Positive Level Data Select, Positive Level Synchronous Preset, and Positive Level Enable (Preset overrides Enable)
FL1P3JZ	Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, Positive Level Data Select, Positive Level Asynchronous Preset, and Positive Level Enable
FL1S3AX	Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, GSR used for Clear
FL1S3AY	Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, GSR used for Preset

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Latches

FD1S1A	Positive Level Data Latch with GSR Used for Clear
FD1S1AY	Positive Level Data Latch with GSR Used for Preset
FD1S1B	Positive Level Data Latch with Positive Level Asynchronous Preset
FD1S1D	Positive Level Data Latch with Positive Level Asynchronous Clear
FD1S1I	Positive Level Data Latch with Positive Level Synchronous Clear
FD1S1J	Positive Level Data Latch with Positive Level Synchronous Preset
FL1S1A	Positive Level Loadable Latch with Positive Select and GSR Used for Clear
FL1S1AY	Positive Level Loadable Latch with Positive Select and GSR Used for Preset
FL1S1B	Positive Level Loadable Latch with Positive Select and Positive Level Asynchronous Preset
FL1S1D	Positive Level Loadable Latch with Positive Select and Positive Level Asynchronous Clear
FL1S1I	Positive Level Loadable Latch with Positive Select and Positive Level Synchronous Clear
FL1S1J	Positive Level Loadable Latch with Positive Select and Positive Level Synchronous Preset

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Memory

DCE32X4	32 Word by 2 Bit Negative Edge Triggered Write Synchronous Dual Port Memory with Positive Write Enable and Two Positive Write Port Enables
RCE32X4	32 Word by 4 Bit Negative Edge Triggered Write Synchronous Single Port Memory with Positive Write Enable and Two Positive Write Port Enables
ROM16X1	16 word by 1 bit read-only memory
ROM32X1	32 word by 1 bit read-only memory
ROM32X4	32 Word by 4 Bit Positive Edge Triggered Read-Only Memory with Registered Data Outputs

Multiplexers

MUX21	2 to 1 Mux
MUX21E	2 to 1 Mux with Enable
MUX41	4 to 1 Mux
MUX41E	4 to 1 Mux with Enable

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I/O Cells

Input Buffers

IBM	CMOS Input Buffer
IBMS	CMOS Input Buffer with Delay
IBMPD	CMOS Input Buffer with Pull-down
IBMPDS	CMOS Input Buffer with Pull-down and Delay
IBMPU	CMOS Input Buffer with Pull-up
IBMPUS	CMOS Input Buffer with Pull-up and Delay
IBT	TTL Input Buffer
IBTS	TTL Input Buffer with Delay
IBTPD	TTL Input Buffer with Pull-down
IBTPDS	TTL Input Buffer with Pull-down and Delay
IBTPU	TTL Input Buffer with Pull-up
IBTPUS	TTL Input Buffer with Pull-up and Delay

Output Buffers

OB6	6mA Sink 3mA Source Sinklim Output Buffer
OB12	12mA Sink 6mA Source Slewlim Output Buffer
OB12F	12mA Sink 6mA Source Fast Output Buffer
OBZ6	6mA Sink 3mA Source Sinklim Output Buffer with Tristate
OBZ6PD	6mA Sink 3mA Source Sinklim Output Buffer with Tristate and Pull-down

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OBZ6PU	6mA Sink 3mA Source Sinklim Output Buffer with Tristate and Pull-up
OBZ12	12mA Sink 6mA Source Slewlim Output Buffer with Tristate
OBZ12PD	12mA Sink 6mA Source Slewlim Output Buffer with Tristate and Pull-down
OBZ12PU	12mA Sink 6mA Source Slewlim Output Buffer with Tristate and Pull-up
OBZ12F	12mA Sink 6mA Source Fast Output Buffer with Tristate
OBZ12FPD	12mA Sink 6mA Source Fast Output Buffer with Tristate and Pull-down
OBZ12FPU	12mA Sink 6mA Source Fast Output Buffer with Tristate and Pull-up

Bidirectional Buffers

BMZ6	CMOS Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate – BiDirectional
BMZ6PD	CMOS Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate and Pull-down – BiDirectional
BMZ6PU	CMOS Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate and Pull-up – BiDirectional
BMZ12	CMOS Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate – BiDirectional
BMZ12PD	CMOS Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate and Pull-down – BiDirectional
BMZ12PU	CMOS Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate and Pull-up –BiDirectional
BMZ12F	CMOS Input 12mA Sink 6mA Source Fast Output Buffer with Tristate – BiDirectional

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BMZ12FPD	CMOS Input 12mA Sink 6mA Source Fast Output Buffer with Tristate and Pull-down – BiDirectional
BMZ12FPU	CMOS Input 12mA Sink 6mA Source Fast Output Buffer with Tristate and Pull-up – BiDirectional
BTZ6	TTL Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate – BiDirectional
BTZ6PD	TTL Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate and Pull-down – BiDirectional
BTZ6PU	TTL Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate and Pull-up – BiDirectional
BTZ12	TTL Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate – BiDirectional
BTZ12PD	TTL Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate and Pull-down – BiDirectional
BTZ12PU	TTL Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate and Pull-up– BiDirectional
BTZ12F	TTL Input 12mA Sink 6mA Source Fast Output Buffer with Tristate – BiDirectional
BTZ12FPD	TTL Input 12mA Sink 6mA Source Fast Output Buffer with Tristate and Pull-down – BiDirectional
BTZ12FPU	TTL Input 12mA Sink 6mA Source Fast Output Buffer with Tristate and Pull-up – BiDirectional

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Bidirectional Buffers With Delayed Input

BMS6	CMOS Delayed Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate – BiDirectional
BMS6PD	CMOS Delayed Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate and Pull-down – BiDirectional
BMS6PU	CMOS Delayed Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate and Pull-up – BiDirectional
BMS12	CMOS Delayed Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate – BiDirectional
BMS12PD	CMOS Delayed Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate and Pull-down – BiDirectional
BMS12PU	CMOS Delayed Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate and Pull-up – BiDirectional
BMS12F	CMOS Delayed Input 12mA Sink 6mA Source Fast Output Buffer with Tristate – BiDirectional
BMS12FPD	CMOS Delayed Input 12mA Sink 6mA Source Fast Output Buffer with Tristate and Pull-down – BiDirectional
BMS12FPU	CMOS Delayed Input 12mA Sink 6mA Source Fast Output Buffer with Tristate and Pull-up – BiDirectional
BTS6	TTL Delayed Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate – BiDirectional
BTS6PD	TTL Delayed Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate and Pull-down – BiDirectional
BTS6PU	TTL Delayed Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate and Pull-up – BiDirectional
BTS12	TTL Delayed Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate – BiDirectional

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BTS12PD	TTL Delayed Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate and Pull-down – BiDirectional
BTS12PU	TTL Delayed Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate and Pull-up – BiDirectional
BTS12F	TTL Delayed Input 12mA Sink 6mA Source Fast Output Buffer with Tristate – BiDirectional
BTS12FPD	TTL Delayed Input 12mA Sink 6mA Source Fast Output Buffer with Tristate and Pull-down – BiDirectional
BTS12FPU	TTL Delayed Input 12mA Sink 6mA Source Fast Output Buffer with Tristate and Pull-up – BiDirectional

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PIC Cells

PIC Gates

OEAND2	2 Input AND Gate with Express Clock (used in PIC area only)
OEND2	2 Input NAND Gate with Express Clock (used in PIC area only)
OENR2	2 Input NOR Gate with Express Clock (used in PIC area only)
OEOR2	2 Input OR Gate with Express Clock (used in PIC area only)
OEXNOR2	2 Input Exclusive NOR Gate with Express Clock (used in PIC area only)
OEXOR2	2 Input Exclusive OR Gate with Express Clock (used in PIC area only)
OSAND2	2 Input AND Gate with System Clock (used in PIC area only)
OSND2	2 Input NAND Gate with System Clock (used in PIC area only)
OSNR2	2 Input NOR Gate with System Clock (used in PIC area only)
OSOR2	2 Input OR Gate with System Clock (used in PIC area only)
OSXNOR2	2 Input Exclusive NOR Gate with System Clock (used in PIC area only)
OSXOR2	2 Input Exclusive OR Gate with System Clock (used in PIC area only)

PIC Multiplexers

OEMUX21	2 to 1 Mux with Express Clock (used in PIC area only)
OSMUX21	2 to 1 Mux with System Clock (used in PIC area only)

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PIC Flip-Flops (Input)

IFS1P3BX	Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Asynchronous Preset, and System Clock (used in input PIC area only)
IFS1P3DX	Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Asynchronous Clear, and System Clock (used in input PIC area only)
IFS1P3IX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Clear, Positive Level Enable, and System Clock (Clear overrides Enable) (used in input PIC area only)
IFS1P3IZ	Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Synchronous Clear, and System Clock (used in input PIC area only)
IFS1P3JX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Preset, Positive Level Enable, and System Clock (Preset overrides Enable) (used in input PIC area only)
IFS1P3JZ	Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Synchronous Preset, and System Clock (used in input PIC area only)

PIC Flip-Flops (Output)

OFE1P3BX	Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Asynchronous Preset, and Express Clock (used in output PIC area only)
OFE1P3DX	Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Asynchronous Clear, and Express Clock (used in output PIC area only)
OFE1P3IX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Clear, Positive Level Enable (Clear overrides Enable), and Express Clock (used in output PIC area only)

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OFE1P3IZ	Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Synchronous Clear, and Express Clock (used in output PIC area only)
OFE1P3JX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Preset, Positive Level Enable (Preset overrides Enable), and Express Clock (used in output PIC area only)
OFE1P3JZ	Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Synchronous Preset, and Express Clock (used in output PIC area only)
OFS1P3BX	Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Asynchronous Preset, and System Clock (used in output PIC area only)
OFS1P3DX	Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Asynchronous Clear, and System Clock (used in output PIC area only)
OFS1P3IX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Clear, Positive Level Enable (Clear overrides Enable), and System Clock (used in output PIC area only)
OFS1P3IZ	Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Synchronous Clear, and System Clock (used in output PIC area only)
X = Don’t careOFS1P3JX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Preset, Positive Level Enable (Preset overrides Enable), and System Clock (used in output PIC area only)
OFS1P3JZ	Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Synchronous Preset, and System Clock (used in output PIC area only)

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PIC Flip-Flops (Latched)

ILF2P3BX	Negative Level Express Clocked (ECLK) Latch, Feeding Positive Edge Triggered System Clocked (SCLK) Flip-Flop, and Positive Level Asynchronous Preset (used in input PIC area only)
ILF2P3DX	Negative Level Express Clocked (ECLK) Latch, Feeding Positive Edge Triggered System Clocked (SCLK) Flip-Flop, and Positive Level Asynchronous Clear (used in input PIC area only)
ILF2P3IX	Negative Level Express Clocked (ECLK) Latch, Feeding Positive Edge Triggered System Clocked (SCLK) Flip-Flop, and Positive Level Synchronous Clear (Clear overrides Enable) (used in input PIC area only)
ILF2P3IZ	Negative Level Express Clocked (ECLK) Latch, Feeding Positive Edge Triggered System Clocked (SCLK) Flip-Flop, and Positive Level Synchronous Clear (used in input PIC area only)
ILF2P3JX	Negative Level Express Clocked (ECLK) Latch, Feeding Positive Edge Triggered System Clocked (SCLK) Flip-Flop, and Positive Level Synchronous Preset (Preset overrides Enable) (used in input PIC area only)
ILF2P3JZ	Negative Level Express Clocked (ECLK) Latch, Feeding Positive Edge Triggered System Clocked (SCLK) Flip-Flop, and Positive Level Synchronous Preset (used in input PIC area only)

PIC Latches (Input)

IFS1S1B	Positive Level Data Latch with Positive Level Asynchronous Preset and System Clock (used in input PIC area only)
IFS1S1D	Positive Level Data Latch with Positive Level Asynchronous Clear and System Clock (used in input PIC area only)
IFS1S1I	Positive Level Data Latch with Positive Level Synchronous Clear and System Clock (used in input PIC area only)

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IFS1S1J	Positive Level Data Latch with Positive Level Synchronous Preset and System Clock (used in input PIC area only)

PIC Latches (Output)

OFE1S1B	Output Positive Level Data Latch with Positive Level Asynchronous Preset and Express Clock (used in output PIC area only)
OFE1S1D	Output Positive Level Data Latch with Positive Level Asynchronous Preset and Express Clock (used in output PIC area only)
OFE1S1I	Output Positive Level Data Latch with Positive Level Asynchronous Preset and Express Clock (used in output PIC area only)
OFE1S1J	Output Positive Level Data Latch with Positive Level Asynchronous Preset and Express Clock (used in output PIC area only)
OFS1S1B	Output Positive Level Data Latch with Positive Level Asynchronous Preset and System Clock (used in output PIC area only)
OFS1S1D	Output Positive Level Data Latch with Positive Level Asynchronous Preset and System Clock (used in output PIC area only)
OFS1S1I	Output Positive Level Data Latch with Positive Level Asynchronous Preset and System Clock (used in output PIC area only)
OFS1S1J	Output Positive Level Data Latch with Positive Level Asynchronous Preset and System Clock (used in output PIC area only)

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Special Cells

Miscellaneous

BNDSCAN	Boundary Scan — Logic Control Circuit
OSCIL	Internal Oscillator
PFUMX41	2 Input Mux within the PFU, CO used for Selection with Positive Select
READBK	Readback Controller
STRTUP	Startup Controller
GSR	Global Set/Reset
TSALL	Global Tristate Interface
PUR	Power Up Set/Reset

Clocking

CLKCNTLB	Clock Control/Shutoff (in LOW state) – Bottom Mid Site
CLKCNTLL	Clock Control/Shutoff (in LOW state) – Left Mid Site
CLKCNTLR	Clock Control/Shutoff (in LOW state) – Right Mid Site
CLKCNTLT	Clock Control/Shutoff (in LOW state) – Top Mid Site
CLKCNTHB	Clock Control/Shutoff (in HIGH state) – Bottom Mid Site
CLKCNTHL	Clock Control/Shutoff (in HIGH state) – Left Mid Site
CLKCNTHR	Clock Control/Shutoff (in HIGH state) – Right Mid Site
CLKCNTHT	Clock Control/Shutoff (in HIGH state) – Top Mid Site

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Clock Manager

DLL1XB	Programmable Clock Manager (Delay Locked Loop) — Bottom
DLL1XT	Programmable Clock Manager (Delay Locked Loop) — Top
DLLPDB	Programmable Clock Manager (Programmable Delay, Delay Locked Loop) — Bottom
DLLPDT	Programmable Clock Manager (Programmable Delay, Delay Locked Loop) — Top
PLLB	Programmable Clock Manager (Phase Locked Loop) — Bottom
PLLT	Programmable Clock Manager (Phase Locked Loop) — Top
PLLDFB	Programmable Clock Manager (Phase Locked Loop) — Dedicated Feedback Bottom
PLLDFT	Programmable Clock Manager (Phase Locked Loop) — Dedicated Feedback Top
PCMB	Programmable Clock Manager – Bottom
PCMT	Programmable Clock Manager – Top
PCMBUFB	Programmable Clock Manager In Bypass Mode – Bottom
PCMBUFT	Programmable Clock Manager In Bypass Mode – Top

Microprocessor Interface

MPI960 Interface	8-Bit Interface to the Intel i960 Microprocessor
MPIPPC Interface	8-Bit Interface to the PowerPC Microprocessor

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SLIC Gates

SAND2	2 Input AND Gate (used in SLIC area only)
SAND4	4 Input AND Gate (used in SLIC area only)
SAND6	6 Input AND Gate (used in SLIC area only)
SAND8	8 Input AND Gate (used in SLIC area only)
SAND10	10 Input AND Gate (used in SLIC area only)
SOR2	2 Input OR Gate (used in SLIC area only)
SOR4	4 Input OR Gate (used in SLIC area only)
SOR6	6 Input OR Gate (used in SLIC area only)
SOR8	8 Input OR Gate (used in SLIC area only)
SOR10	10 Input OR Gate (used in SLIC area only)
SAOI42	AND Array to OR Inverted (used in SLIC area only)
SAOI44	AND Array to OR Inverted (used in SLIC area only)
SAOI442	AND Array to OR Inverted (used in SLIC area only)

SLIC Buffers

TBUF	Internal Buffer with Tristate (used in SLIC area only)
TIBUF	Internal Buffer with Inverted Tristate (used in SLIC area only)

9th Flip-Flop

CFD1P3BX	Positive Edge Triggered D Flip-Flop with Positive Level Enable and Positive Level Asynchronous Preset (mapped to 9th Flip-Flop in the PLC only)

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CFD1P3DX	Positive Edge Triggered D Flip-Flop with Positive Level Enable and Positive Level Asynchronous Clear (mapped to 9th Flip-Flop in the PLC only)
CFD1P3IX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Clear and Positive Level Enable (Clear overrides Enable) (mapped to 9th Flip-Flop in the PLC only)
CFD1P3IZ	Positive Edge Triggered D Flip-Flop with Positive Level Enable and Positive Level Synchronous Clear (mapped to 9th Flip-Flop in the PLC only)
CFD1P3JX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Preset and Positive Level Enable (Preset overrides Enable) (mapped to 9th Flip-Flop in the PLC only)
CFD1P3JZ	Positive Edge Triggered D Flip-Flop with Positive Level Enable and Positive Level Synchronous Preset (mapped to 9th Flip-Flop in the PLC only)

Series 3+ Elements

INTRBUF	ASB/FPGA interface cell that gets mapped to the bottom row of PICs. Unconnected inputs should be pulled down.
IINTRBUFS	ASB/FPGA interface cell that gets mapped to the bottom row of PICs. Delayed input buffer, unconnected inputs should be pulled down.
ITOASBCK	Buffer used to route clocks from FPGA to ASB along clock spine.
IFRASBCK	Buffer used to route clocks from ASB to FPGA along clock spine.

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ORCA MACRO LIBRARY 2CA/2TA/2TB

This chapter contains the following sections:

- Logic Gates
- Counters
- Pads
- Buffers
- Latches
- Flip-Flops
- Multiplexers/Demultiplexers
- Registers
- Memory
- Special Elements

Logic Gates

AND2 AND2Bx	2 Input AND Gates with x Inputs Inverting
AND3 AND3Bx	3 Input AND Gates with x Inputs Inverting
AND4 AND4Bx	4 Input AND Gates with x Inputs Inverting
AND5 AND5Bx	5 Input AND Gates with x Inputs Inverting
AND6	6 Input AND Gate
ND2 ND2Bx	2 Input NAND Gates with x Inputs Inverting
ND3 ND3Bx	3 Input NAND Gates with x Inputs Inverting

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ND4 ND4Bx	4 Input NAND Gates with x Inputs Inverting
ND5 ND5Bx	5 Input NAND Gates with x Inputs Inverting
ND6	6 Input NAND Gate
OR2 OR2Bx	2 Input OR Gates with x Inputs Inverting
OR3 OR3Bx	3 Input OR Gates with x Inputs Inverting
OR4 OR4Bx	4 Input OR Gates with x Inputs Inverting
OR5 OR5Bx	5 Input OR Gates with x Inputs Inverting
OR6	6 Input OR Gate
NR2 NR2Bx	2 Input NOR Gates with x Inputs Inverting
NR3 NR3Bx	3 Input NOR Gates with x Inputs Inverting
NR4 NR4Bx	4 Input NOR Gates with x Inputs Inverting
NR5 NR5Bx	5 Input NOR Gates with x Inputs Inverting
NR6	6 Input NOR Gate
XOR2	2 Input Exclusive OR Gate
XOR3	3 Input Exclusive OR Gate
XOR4	4 Input Exclusive OR Gate
XOR5	5 Input Exclusive OR Gate

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XOR6	6 Input Exclusive OR Gate
XNOR2	2 Input Exclusive NOR Gate
XNOR3	3 InputExclusive NOR Gate
XNOR4	4 Input Exclusive NOR Gate
XNOR5	5 Input Exclusive NOR Gate
XNOR6	6 Input Exclusive NOR Gate

Invert Gates

AOIxxxx	AND Array to OR Inverted
OAIxxxx	OR Array to AND Inverted

Miscellaneous Logic

INV	Inverter
INRB	Inverter (Standard Cell equivalent)
VLO	Logic Low Generator
VHI	Logic High Generator
COMP	2 Bit Equality Comparator
COMP4	4 Bit Equality Comparator
LTGT	Less Than or Greater Than
AGEB4	“A” Greater Than Or Equal To “B”
ANEB4	“A” Not Equal To “B”

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Special Logic

ADD	1 Bit Adder
FADD4	4 Bit Fast Adder
FADD4O	4 Bit Fast Adder with Overflow
SUB	1 Bit Subtracter (two's complement)
FSUB4	4 Bit Fast Subtracter (two's complement)
FSUB4O	4 Bit Fast Subtracter (two's complement) with Overflow
ADSU	1 Bit Adder/Subtracter (two's complement)
FADSU4	4 Bit Fast Adder/Subtracter (two's complement)
FADSU4O	4 Bit Fast Adder/Subtracter (two's complement) with Overflow
FAC4P3D	4 Bit Fast Accumulator with Positive Level Enable and Positive Level Asynchronous Clear
FMULT4	4 X 4 Multiplier
FMULT41	4 X 1 Fast Multiplier
PFUND	3 Input NAND Element within the PFU
PFUND0	2 Input NAND Element within the PFU
PFUXR	3 Input XOR Element within the PFU
PFUXR0	2 Input XOR Element within the PFU

Counters

CU4P3BX	4 Bit Positive Edge Triggered Fast Up Counter with Positive Clock Enable and Positive Asynchronous Preset

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CU4P3DX	4 Bit Positive Edge Triggered Fast Up Counter with Positive Clock Enable and Positive Asynchronous Clear
CU4P3IX	4 Bit Positive Edge Triggered Fast Up Counter with Positive Clock Enable and Positive Synchronous Clear
CU4P3JX	4 Bit Positive Edge Triggered Fast Up Counter with Positive Clock Enable and Positive Synchronous Preset
CD4P3BX	4 Bit Positive Edge Triggered Fast Down Counter with Positive Clock Enable and Positive Asynchronous Preset
CD4P3DX	4 Bit Positive Edge Triggered Fast Down Counter with Positive Clock Enable and Positive Asynchronous Clear
CD4P3IX	4 Bit Positive Edge Triggered Fast Down Counter with Positive Clock Enable and Positive Synchronous Clear
CD4P3JX	4 Bit Positive Edge Triggered Fast Down Counter with Positive Clock Enable and Positive Synchronous Preset
CB4P3BX	4 Bit Positive Edge Triggered Bidirectional Counter with Positive Clock Enable and Positive Asynchronous Preset
CB4P3DX	4 Bit Positive Edge Triggered Bidirectional Counter with Positive Clock Enable and Positive Asynchronous Clear
CB4P3IX	4 Bit Positive Edge Triggered Bidirectional Counter with Positive Clock Enable and Positive Synchronous Clear
CB4P3JX	4 Bit Positive Edge Triggered Bidirectional Counter with Positive Clock Enable and Positive Synchronous Preset
CU4	Combinational Logic for 4 Bit Up Counter using Look Up Table
CD4	Combinational Logic for 4 Bit Down Counter using Look Up Table
CB4	Combinational Logic for 4 Bit Bidirectional Counter using Look Up Table
LU4P3AX	4 Bit Positive Edge Triggered Loadable Up Counter with Positive Clock Enable, GSR Used for Clear

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LU4P3AY	4 Bit Positive Edge Triggered Loadable Up Counter with Positive Clock Enable, GSR Used for Preset
LD4P3AX	4 Bit Positive Edge Triggered Loadable Down Counter with Positive Clock Enable, GSR Used for Clear
LD4P3AY	4 Bit Positive Edge Triggered Loadable Down Counter with Positive Clock Enable, GSR Used for Preset
LB4P3AX	4 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable, GSR Used for Clear
LB4P3AY	4 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable, GSR Used for Preset

Pads

IPAD	Input PAD
OPAD	Output PAD
BPAD	Bi Directional PAD

Buffers

Input Buffers

IBM	CMOS Input Buffer
IBMS	CMOS Input Buffer with Delay
IBMPD	CMOS Input Buffer with Pull down
IBMPDS	CMOS Input Buffer with Pull down and Delay
IBMPU	CMOS Input Buffer with Pull up
IBMPUS	CMOS Input Buffer with Pull up and Delay

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IBT	TTL Input Buffer
IBTS	TTL Input Buffer with Delay
IBTPD	TTL Input Buffer with Pull down
IBTPDS	TTL Input Buffer with Pull down and Delay
IBTPU	TTL Input Buffer with Pull up
IBTPUS	TTL Input Buffer with Pull up and Delay

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Output Buffers

OB12	12mA Sink 6mA Source Slewlim Output Buffer
OB12F	12mA Sink 6mA Source Fast Output Buffer
OB6	6mA Sink 3mA Source Sinklim Output Buffer
OBZ12	12mA Sink 6mA Source Slewlim Output Buffer with Tristate
OBZ12F	12mA Sink 6mA Source Fast Output Buffer with Tristate
OBZ6	6mA Sink 3mA Source Sinklim Output Buffer with Tristate
OBZ12PU	12mA Sink 6mA Source Slewlim Output Buffer with Tristate and Pull up
OBZ12FPU	12mA Sink 6mA Source Fast Output Buffer with Tristate and Pull up
OBZ6PU	6mA Sink 3mA Source Sinklim Output Buffer with Tristate and Pull up
OBZ12PD	12mA Sink 6mA Source Slewlim Output Buffer with Tristate and Pull down
OBZ12FPD	12mA Sink 6mA Source Fast Output Buffer with Tristate and Pull down
OBZ6PD	6mA Sink 3mA Source Sinklim Output Buffer with Tristate and Pull down

Bidirectional Buffers

BMZ12	CMOS Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate – BiDirectional
BMZ12F	CMOS Input 12mA Sink 6mA Source Fast Output Buffer with Tristate – BiDirectional
BMZ6	CMOS Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate – BiDirectional

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BMZ12PU	CMOS Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate and Pull up –BiDirectional
BMZ12FPU	CMOS Input 12mA Sink 6mA Source Fast Output Buffer with Tristate and Pull up – BiDirectional
BMZ6PU	CMOS Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate and Pull up – BiDirectional
BMZ12PD	CMOS Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate and Pull down – BiDirectional
BMZ12FPD	CMOS Input 12mA Sink 6mA Source Fast Output Buffer with Tristate and Pull down – BiDirectional
BMZ6PD	CMOS Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate and Pull down – BiDirectional
BTZ12	TTL Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate – BiDirectional
BTZ12F	TTL Input 12mA Sink 6mA Source Fast Output Buffer with Tristate – BiDirectional
BTZ6	TTL Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate – BiDirectional
BTZ12PU	TTL Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate and Pull up– BiDirectional
BTZ12FPU	TTL Input 12mA Sink 6mA Source Fast Output Buffer with Tristate and Pull up – BiDirectional
BTZ6PU	TTL Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate and Pull up – BiDirectional
BTZ12PD	TTL Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate and Pull down – BiDirectional
BTZ12FPD	TTL Input 12mA Sink 6mA Source Fast Output Buffer with Tristate and Pull down – BiDirectional

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BTZ6PD	TTL Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate and Pull down – BiDirectional

Bidirectional Buffers With Delayed Input

BMS6	CMOS Delayed Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate – BiDirectional
BMS6PD	CMOS Delayed Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate and Pull-down – BiDirectional
BMS6PU	CMOS Delayed Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate and Pull-up – BiDirectional
BMS12	CMOS Delayed Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate – BiDirectional
BMS12PD	CMOS Delayed Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate and Pull-down – BiDirectional
BMS12PU	CMOS Delayed Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate and Pull-up – BiDirectional
BMS12F	CMOS Delayed Input 12mA Sink 6mA Source Fast Output Buffer with Tristate – BiDirectional
BMS12FPD	CMOS Delayed Input 12mA Sink 6mA Source Fast Output Buffer with Tristate and Pull-down – BiDirectional
BMS12FPU	CMOS Delayed Input 12mA Sink 6mA Source Fast Output Buffer with Tristate and Pull-up – BiDirectional
BTS6	TTL Delayed Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate – BiDirectional
BTS6PD	TTL Delayed Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate and Pull-down – BiDirectional
BTS6PU	TTL Delayed Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate and Pull-up – BiDirectional

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BTS12	TTL Delayed Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate – BiDirectional
BTS12PD	TTL Delayed Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate and Pull-down – BiDirectional
BTS12PU	TTL Delayed Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate and Pull-up – BiDirectional
BTS12F	TTL Delayed Input 12mA Sink 6mA Source Fast Output Buffer with Tristate – BiDirectional
BTS12FPD	TTL Delayed Input 12mA Sink 6mA Source Fast Output Buffer with Tristate and Pull-down – BiDirectional
BTS12FPU	TTL Delayed Input 12mA Sink 6mA Source Fast Output Buffer with Tristate and Pull-up – BiDirectional

Miscellaneous Buffers

TBUF	Internal Buffer with Tristate
TIBUF	Internal Buffer with Inverted Tristate

Latches

FD1S1A	Positive Level Data Latch with GSR Used for Clear
FD1S1AY	Positive Level Data Latch with GSR Used for Preset
FD1S1B	Positive Level Data Latch with Positive Level Asynchronous Preset
FD1S1D	Positive Level Data Latch with Positive Level Asynchronous Clear
FD1S1I	Positive Level Data Latch with Positive Level Synchronous Clear
FD1S1J	Positive Level Data Latch with Positive Level Synchronous Preset
FL1S1A	Positive Level Loadable Latch with Positive Select and GSR Used for Clear

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FL1S1AY	Positive Level Loadable Latch with Positive Select and GSR Used for Preset
FS1S1A	Positive Level R/S Latch and GSR Used for Clear

Flip-Flops

FD1P3AX	Positive Edge Triggered D Flip-Flop with Positive Level Enable, GSR used for Clear
FD1P3AY	Positive Edge Triggered D Flip-Flop with Positive Level Enable, GSR used for Preset
FD1P3BX	Positive Edge Triggered D Flip-Flop with Positive Level Enable and Positive Level Asynchronous Preset
FD1P3DX	Positive Edge Triggered D Flip-Flop with Positive Level Enable and Positive Level Asynchronous Clear
FD1P3IX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Clear and Positive Level Enable (Clear overrides Enable)
FD1P3IZ	Positive Edge Triggered D Flip-Flop with Positive Level Enable and Positive Level Synchronous Clear
FD1P3JX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Preset and Positive Level Enable (Preset overrides Enable)
FD1P3JZ	Positive Edge Triggered D Flip-Flop with Positive Level Enable and Positive Level Synchronous Preset
FD1S3AX	Positive Edge Triggered D Flip-Flop, GSR Used for Clear
FD1S3AY	Positive Edge Triggered D Flip-Flop, GSR Used for Preset
FD1S3BX	Positive Edge Triggered D Flip-Flop with Positive Level Asynchronous Preset

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FD1S3DX	Positive Edge Triggered D Flip-Flop with Positive Level Asynchronous Clear
FD1S3IX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Clear
FD1S3JX	Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Preset
FJ1S3AX	Positive Edge Triggered J/K Flip-Flop, GSR Used for Clear
FJ1S3BX	Positive Edge Triggered J/K Flip-Flop with Positive Level Asynchronous Preset
FJ1S3DX	Positive Edge Triggered J/K Flip-Flop with Positive Level Asynchronous Clear
FL1P3AZ	Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, Positive Level Data Select, and Positive Level Enable, GSR used for Clear
FL1P3AY	Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, Positive Level Data Select, and Positive Level Enable, GSR used for Preset
FL1S3AX	Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, GSR used for Clear
FL1S3AY	Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, GSR used for Preset
FT1S3AX	Positive Edge Triggered Toggle Flip-Flop
FT1S3BX	Positive Edge Triggered Toggle Flip-Flop with Positive Level Asynchronous Preset
FT1S3DX	Positive Edge Triggered Toggle Flip-Flop with Positive Level Asynchronous Clear

Multiplexers/Demultiplexers

MUX21	2 to 1 Mux

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MUX21E	2 to 1 Mux with Enable
MUX41	4 to 1 Mux
MUX41E	4 to 1 Mux with Enable
MUX81	8 to 1 Mux
MUX81E	8 to 1 Mux with Enable
DMUX24	2 to 4 DeMux
DMUX24E	2 to 4 DeMux with Enable
DMUX38	3 to 8 DeMux
DMUX38E	3 to 8 DeMux with Enable
PFUMX41	3 Input Multiplexer within the PFU, CO used for Selection with Positive Select

Registers

RD4S3A	Positive Edge Triggered 4 Bit Data Register
RD4S3B	Positive Edge Triggered 4 Bit Data Register with Positive Level Asynchronous Preset
RD4S3D	Positive Edge Triggered 4 Bit Data Register with Positive Level Asynchronous Clear
RD4S3I	Positive Edge Triggered 4 Bit Data Register with Positive Level Synchronous Clear
RD4S3J	Positive Edge Triggered 4 Bit Data Register with Positive Level Synchronous Preset
RD4P3A	Positive Edge Triggered 4 Bit Data Register with Positive Level Enable

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RD4P3B	Positive Edge Triggered 4 Bit Data Register with Positive Level Enable and Positive Level Asynchronous Preset
RD4P3D	Positive Edge Triggered 4 Bit Data Register with Positive Level Enable and Positive Level Asynchronous Clear
RD4P3I	Positive Edge Triggered 4 Bit Data Register with Positive Level Enable and Positive Level Synchronous Clear
RD4P3J	Positive Edge Triggered 4 Bit Data Register with Positive Level Enable and Positive Level Synchronous Preset
RS4S3A	Positive Edge Triggered 4 Bit Shift Register
RS4S3B	Positive Edge Triggered 4 Bit Shift Register with Positive Level Asynchronous Preset
RS4S3D	Positive Edge Triggered 4 Bit Shift Register with Positive Level Asynchronous Clear
RS4S3I	Positive Edge Triggered 4 Bit Shift Register with Positive Level Synchronous Clear
RS4S3J	Positive Edge Triggered 4 Bit Shift Register with Positive Level Synchronous Preset
RS4P3A	Positive Edge Triggered 4 Bit Shift Register with Positive Level Enable
RS4P3B	Positive Edge Triggered 4 Bit Shift Register with Positive Level Enable and Positive Level Asynchronous Preset
RS4P3D	Positive Edge Triggered 4 Bit Shift Register with Positive Level Enable and Positive Level Asynchronous Clear
RS4P3I	Positive Edge Triggered 4 Bit Shift Register with Positive Level Enable and Positive Level Synchronous Clear
RS4P3J	Positive Edge Triggered 4 Bit Shift Register with Positive Level Enable and Positive Level Synchronous Preset

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RLS4P3A	Positive Edge Triggered 4 Bit Loadable Shift Register with Positive Level Enable

Memory

RPP16X2	16 Word by 2 Bit Static Memory with Positive Write Enable
RPP16X2Z	16 Word by 2 Bit Static Memory with Tristated Outputs, Positive Write Enable and Positive Tristate Control
RPP16X4	16 Word by 4 Bit Static Memory with Positive Write Enable
RPP16X4Z	16 Word by 4 Bit Static Memory with Tristated Outputs, Positive Write Enable and Positive Tristate Control
RPE16X2	16 Word by 2 Bit Static Memory with Positive Write Enable and Positive Write Port Enable
RPE16X2Z	16 Word by 2 Bit Static Memory with Positive Write Enable, Positive Write Port Enable, and Positive Tristate Control
RPE16X4	16 Word by 4 Bit Static Memory with Positive Write Enable and Positive Write Port Enable
RPE16X4Z	16 Word by 4 Bit Static Memory with Positive Write Enable, Positive Write Port Enable, and Positive Tristate Control
RCE16X4	16 Word by 4 Bit Positive Edge Triggered Write Synchronous Single Port Memory with Positive Write Enable and Positive Write Port Enable
RCE16X4Z	16 Word by 4 Bit Positive Edge Triggered Write Synchronous Single Port Memory with Positive Write Enable, Positive Write Port Enable, and Positive Tristate Control
DCE16X2	16 Word by 2 Bit Positive Edge Triggered Write Synchronous Dual Port Memory with Positive Write Enable and Positive Write Port Enable

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DCE16X2Z	16 Word by 2 Bit Positive Edge Triggered Write Synchronous Dual Port Memory with Positive Write Enable, Positive Write Port Enable, and Positive Tristate Control
RCF16X4	16 Word by 4 Bit Fast Positive Edge Triggered Write Synchronous Single Port Memory with Positive Write Enable and Positive Write Port Enable
RCF16X4Z	16 Word by 4 Bit Fast Positive Edge Triggered Write Synchronous Single Port Memory with Positive Write Enable, Positive Write Port Enable, and Positive Tristate Control
DCF16X2	16 Word by 2 Bit Fast Positive Edge Triggered Write Synchronous Dual Port Memory with Positive Write Enable and Positive Write Port Enable
DCF16X2Z	16 Word by 2 Bit Fast Positive Edge Triggered Write Synchronous Dual Port Memory with Positive Write Enable, Positive Write Port Enable, and Positive Tristate Control

Special Elements

BNDSCAN	Boundary Scan — Logic Control Circuit
OSCIL	Internal Oscillator
READBK	Readback Controller
STRTUP	Startup Controller
GSR	Global Set/Reset Interface
TSALL	Global Tristate Interface

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ALPHANUMERIC LIST OF CELLS

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ADD

1 Bit Adder

ORCA Series		
2	3	4
✓		

ADD

INPUTS: A,B,CI
OUTPUTS: CO,S
PINORDER: A B CI CO S
MINIMUM CELL AREA: 0.25

Truth Table:

INPUTS			OUTPUTS	
A	B	CI	CO	S
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

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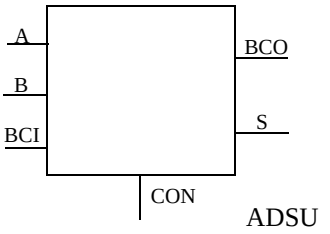
ADSU

1 Bit Adder/Subtracter (two's complement)

ORCA Series		
2	3	4
✓		



ADSU

INPUTS: A,B,BCI,CON
OUTPUTS: BCO,S
PINORDER: A B BCI CON BCO S
MINIMUM CELL AREA: 0.125

Truth Table:

INPUTS				OUTPUTS	
A	B	BCI	CON	BCO	S
0	0	0	1	0	0
1	0	0	1	0	1
0	1	0	1	0	1
1	1	0	1	1	0
0	0	1	1	0	1
1	0	1	1	1	0
0	1	1	1	1	0
1	1	1	1	1	1
0	0	0	0	0	1

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INPUTS				OUTPUTS	
A	B	BCI	CON	BCO	S
1	0	0	0	1	0
0	1	0	0	0	0
1	1	0	0	0	1
0	0	1	0	1	0
1	0	1	0	1	1
0	1	1	0	0	1
1	1	1	0	1	0

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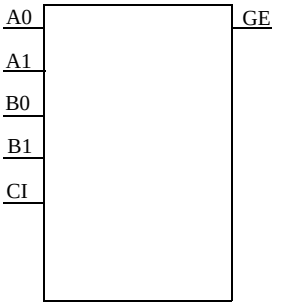
AGEB2

“A” Greater Than Or Equal To “B”

Lattice FPGA		
SC	XP	EC
✓	✓	✓



AGEB2

INPUTS: A0, A1, B0, B1, CI
OUTPUTS: GE
PINORDER: A0, A1, B0, B1, CI, GE
CELL AREA: One Slice

Description:

AGEB2 is a 2-bit comparator that can be cascaded together to build larger comparators. It has two 2-bit inputs and a carry-in input. The carry-in (CI) on the first stage should be tied HIGH. The compare-out (GE) output is HIGH if A[1:0] >= B[1:0] and LOW if A[1:0] < B[1:0]. To build larger comparators, tie the GE on the lower stage to CI on the upper stage.

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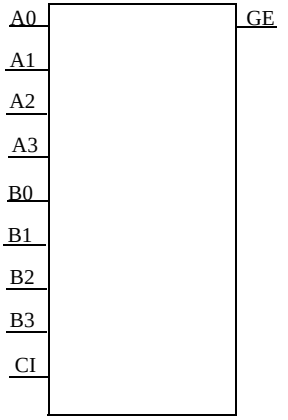
AGEB4

"A" Greater Than Or Equal To "B"

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



AGEB4

INPUTS: A0,A1,A2,A3,B0,B1,B2,B3,CI
OUTPUTS: GE
PINORDER: A0 A1 A2 A3 B0 B1 B2 B3 CI GE
MINIMUM CELL AREA (2A/2T): 0.5
MINIMUM CELL AREA (Series 3): 0.25

Description:

AGEB4 is a 4-bit comparator that can be cascaded together to build larger comparators. It has two 4-bit inputs and a carry-in input. The carry-in (CI) on the first stage should be tied HIGH. The compare-out (GE) output is HIGH if A[3:0] >= B[3:0] and LOW if A[3:0] < B[3:0]. To build larger comparators, tie the GE on the lower stage to CI on the upper stage.

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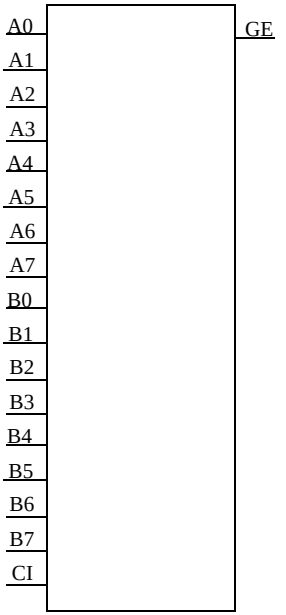
AGEB8

"A" Greater Than Or Equal To "B"

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



AGEB8

INPUTS: A0,A1,A2,A3,A4,A5,A6,A7,B0,B1,B2,B3,B4,B5,B6,B7,CI
OUTPUTS: GE
PINORDER: A0 A1 A2 A3 A4 A5 A6 A7 B0 B1 B2 B3 B4 B5 B6 B7 CI GE
MINIMUM CELL AREA: 0.5

Description:

AGEB8 is an 8-bit comparator that can be cascaded together to build larger comparators. It has two 8-bit inputs and a carry-in input. The carry-in (CI) on the first stage should be tied HIGH. The compare-out (GE) output is HIGH if A[7:0] >= B[7:0] and LOW if A[7:0] < B[7:0]. To build larger comparators, tie the GE on the lower stage to CI on the upper stage.

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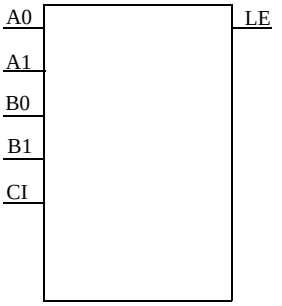
ALEB2

“A” Less Than Or Equal To “B”

Lattice FPGA		
SC	XP	EC
✓	✓	✓



ALEB2

INPUTS: A0, A1, B0, B1, CI
OUTPUTS: LE
PINORDER: A0, A1, B0, B1, CI, LE
CELL AREA: One Slice

Description:

ALEB2 is a 2-bit comparator that can be cascaded together to build larger comparators. It has two 2-bit inputs and a carry-in input. The carry-in (CI) on the first stage should be tied HIGH. The compare-out (LE) output is HIGH if A[1:0] <= B[1:0] and LOW if A[1:0] > B[1:0]. To build larger comparators, tie the LE on the lower stage to CI on the upper stage.

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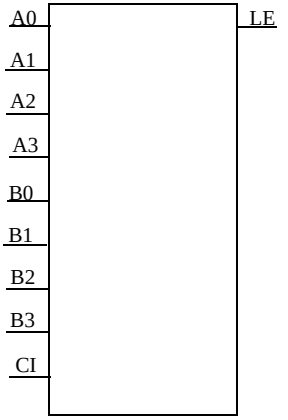
ALEB4

"A" Less Than Or Equal To "B"

ORCA Series/Lattice FPGA				
3	4	SC	XP	EC
✓	✓	✓	✓	✓



ALEB4

INPUTS: A0,A1,A2,A3,B0,B1,B2,B3,CI
OUTPUTS: LE
PINORDER: A0 A1 A2 A3 B0 B1 B2 B3 CI LE
MINIMUM CELL AREA: 0.25

Description:

ALEB4 is a 4-bit comparator that can be cascaded together to build larger comparators. It has two 4-bit inputs and a carry-in input. The carry-in (CI) on the first stage should be tied HIGH. The compare-out (LE) output is HIGH if A[3:0] <= B[3:0] and LOW if A[3:0] > B[3:0]. To build larger comparators, tie the LE on the lower stage to CI on the upper stage.

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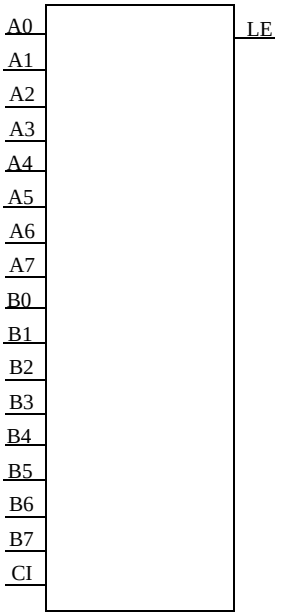
ALEB8

"A" Less Than Or Equal To "B"

ORCA Series/Lattice FPGA				
3	4	SC	XP	EC
✓	✓	✓	✓	✓



ALEB8

INPUTS: A0,A1,A2,A3,A4,A5,A6,A7,B0,B1,B2,B3,B4,B5,B6,B7,CI
OUTPUTS: LE
PINORDER: A0 A1 A2 A3 A4 A5 A6 A7 B0 B1 B2 B3 B4 B5 B6 B7 CI LE
MINIMUM CELL AREA: 0.5

Description:

ALEB8 is an 8-bit comparator that can be cascaded together to build larger comparators. It has two 8-bit inputs and a carry-in input. The carry-in (CI) on the first stage should be tied HIGH. The compare-out (LE) output is HIGH if A[7:0] <= B[7:0] and LOW if A[7:0] > B[7:0]. To build larger comparators, tie the LE on the lower stage to CI on the upper stage.

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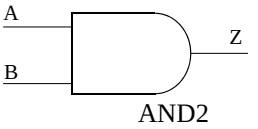
AND2

2 Input AND Gate

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



INPUTS: A,B
OUTPUTS: Z
PINORDER: A B Z
MINIMUM CELL AREA (2A/2T): 0.125
MINIMUM CELL AREA (Series 3): 0.031

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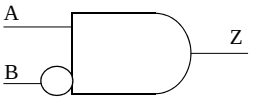
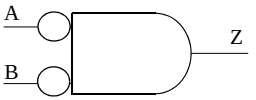
AND2B*x*

2 Input AND Gates with *x* Inputs Inverting

ORCA Series		
2	3	4
✓		



AND2B1



AND2B2

INPUTS: A,B
OUTPUTS: Z
PINORDER: A B Z
MINIMUM CELL AREA: 0.125

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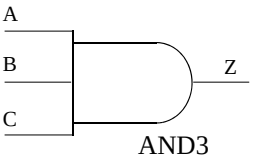
AND3

3 Input AND Gate

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



INPUTS: A,B,C
OUTPUTS: Z
PINORDER: A B C Z
MINIMUM CELL AREA (2A/2T): 0.125
MINIMUM CELL AREA (Series 3): 0.047

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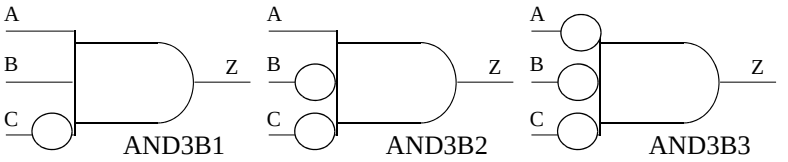
AND3B*x*

3 Input AND Gates with *x* Inputs Inverting

ORCA Series		
2	3	4
✓		



INPUTS: A,B,C
OUTPUTS: Z
PINORDER: A B C Z
MINIMUM CELL AREA: 0.125

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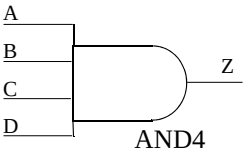
AND4

4 Input AND Gate

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



INPUTS: A,B,C,D
OUTPUTS: Z
PINORDER: A B C D Z
MINIMUM CELL AREA (2A/2T): 0.175
MINIMUM CELL AREA (Series 3): 0.0625

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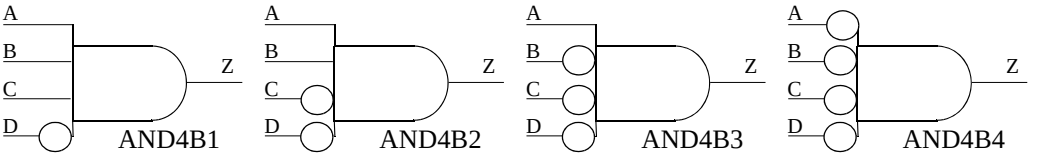
AND4B*x*

4 Input AND Gates with *x* Inputs Inverting

ORCA Series		
2	3	4
✓		



INPUTS: A,B,C,D
OUTPUTS: Z
PINORDER: A B C D Z
MINIMUM CELL AREA: 0.175

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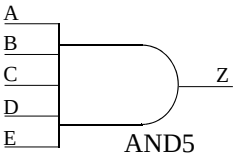
AND5

5 Input AND Gate

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



INPUTS: A,B,C,D,E
OUTPUTS: Z
PINORDER: A B C D E Z
MINIMUM CELL AREA (2A/2T): 0.25
MINIMUM CELL AREA (Series 3): 0.125

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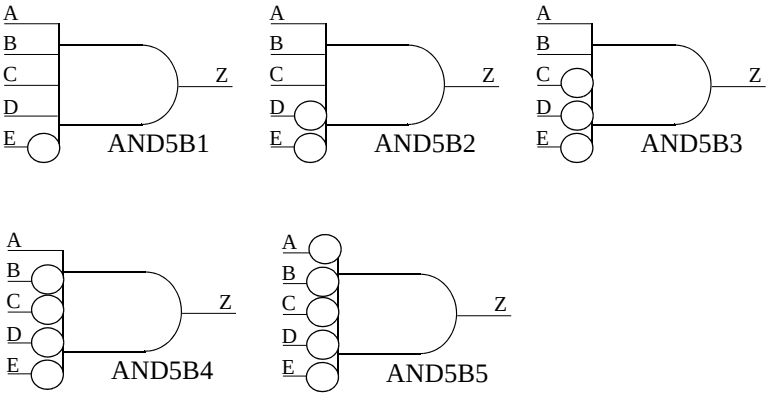
AND5B*x*

5 Input AND Gates with *x* Inputs Inverting

ORCA Series		
2	3	4
✓		



INPUTS: A,B,C,D,E
OUTPUTS: Z
PINORDER: A B C D E Z
MINIMUM CELL AREA: 0.25

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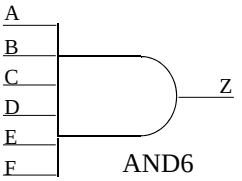
AND6

6 Input AND Gate

ORCA Series		
2	3	4
✓		



INPUTS: A,B,C,D,E,F
OUTPUTS: Z
PINORDER: A B C D E F Z
MINIMUM CELL AREA: 0.5

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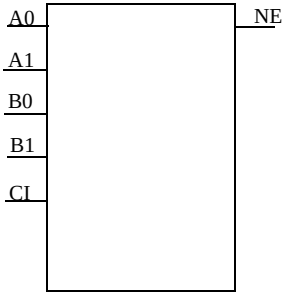
ANEB2

"A" Not Equal To "B"

Lattice FPGA		
SC	XP	EC
✓	✓	✓



ANEB2

INPUTS: A0,A1,B0,B1,CI
OUTPUTS: NE
PINORDER:A0 A1 B0 B1 CI NE
CELL AREA: One Slice

Description:

ANEB2 is a 2-bit comparator that can be cascaded together to build larger comparators. It has two 2-bit inputs and a carry-in input. The carry-in (CI) on the first stage should be tied LOW. The compare-out (NE) output is LOW if A[1:0] = B[1:0] and HIGH otherwise. To build larger comparators, tie the NE on the lower stage to CI on the upper stage.

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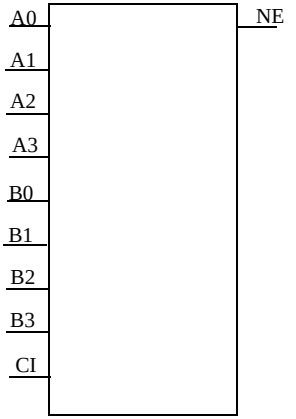
ANEB4

“A” Not Equal To “B”

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



ANEB4

INPUTS: A0,A1,A2,A3,B0,B1,B2,B3,CI
OUTPUTS: NE
PINORDER: A0 A1 A2 A3 B0 B1 B2 B3 CI NE
MINIMUM CELL AREA (2A/2T): 0.5
MINIMUM CELL AREA (Series 3): 0.25

Description:

ANEB4 is a 4-bit comparator that can be cascaded together to build larger comparators. It has two 4-bit inputs and a carry-in input. The carry-in (CI) on the first stage should be tied LOW. The compare-out (NE) output is LOW if A[3:0] = B[3:0] and HIGH otherwise. To build larger comparators, tie the NE on the lower stage to CI on the upper stage.

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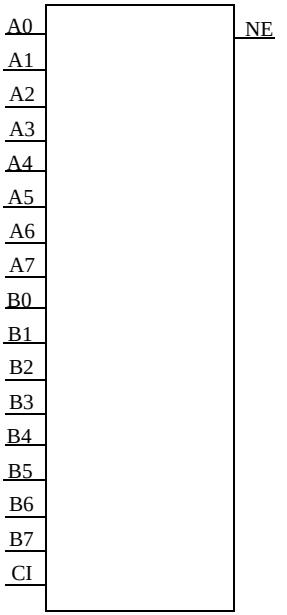
ANEB8

"A" Not Equal To "B"

ORCA Series/Lattice FPGA				
3	4	SC	XP	EC
✓	✓	✓	✓	✓



ANEB8

INPUTS: A0,A1,A2,A3,A4,A5,A6,A7,B0,B1,B2,B3,B4,B5,B6,B7,CI
OUTPUTS: NE
PINORDER: A0 A1 A2 A3 A4 A5 A6 A7 B0 B1 B2 B3 B4 B5 B6 B7 CI NE
MINIMUM CELL AREA: 0.5

Description:

ANEB8 is an 8-bit comparator that can be cascaded together to build larger comparators. It has two 8-bit inputs and a carry-in input. The carry-in (CI) on the first stage should be tied LOW. The compare-out (NE) output is LOW if A[7:0] = B[7:0] and HIGH otherwise. To build larger comparators, tie the NE on the lower stage to CI on the upper stage.

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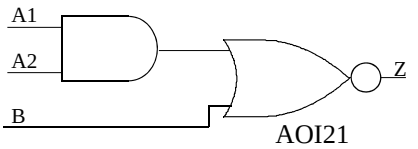
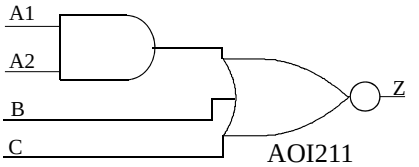
AOI

AND Array to OR Inverted

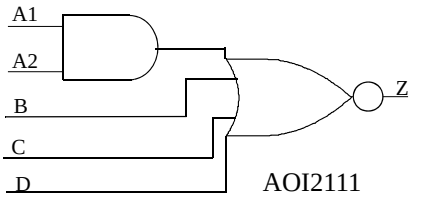
ORCA Series		
2	3	4
✓		



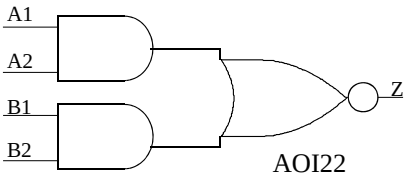
INPUTS: A1,A2,B
OUTPUTS: Z
PINORDER: A1 A2 B Z
MINIMUM CELL AREA: 0.125



INPUTS: A1,A2,B,C
OUTPUTS: Z
PINORDER: A1 A2 B C Z
MINIMUM CELL AREA: 0.175



INPUTS: A1,A2,B,C,D
OUTPUTS: Z
PINORDER:A1 A2 B C D Z
MINIMUM CELL AREA: 0.25



INPUTS: A1,A2,B1,B2
OUTPUTS: Z
PINORDER: A1 A2 B1 B2 Z
MINIMUM CELL AREA: 0.175

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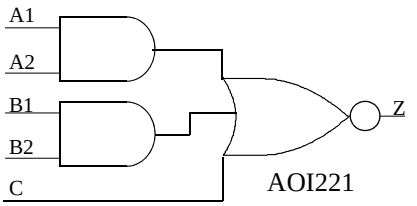
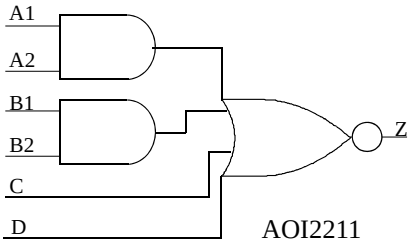
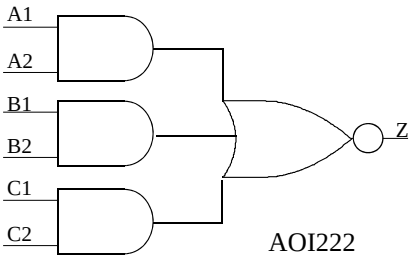


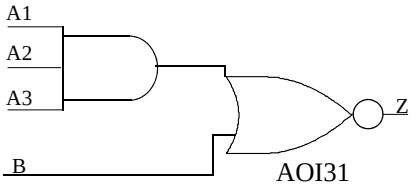
INPUTS: A1,A2,B1,B2,C
OUTPUTS: Z
PINORDER: A1 A2 B1 B2 C Z
MINIMUM CELL AREA: 0.25



INPUTS: A1,A2,B1,B2,C,D
OUTPUTS: Z
PINORDER: A1 A2 B1 B2 C D Z
MINIMUM CELL AREA: 0.5



INPUTS: A1,A2,B1,B2,C1,C2
OUTPUTS: Z
PINORDER:A1 A2 B1 B2 C1 C2 Z
MINIMUM CELL AREA: 0.5



INPUTS: A1,A2,A3,B
OUTPUTS: Z
PINORDER: A1 A2 A3 B Z
MINIMUM CELL AREA: 0.175

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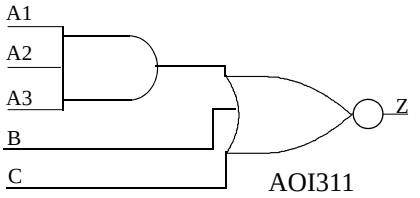
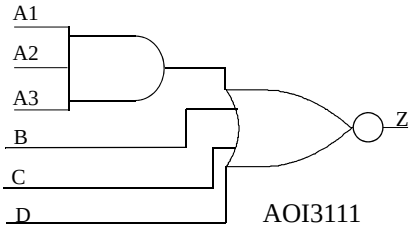
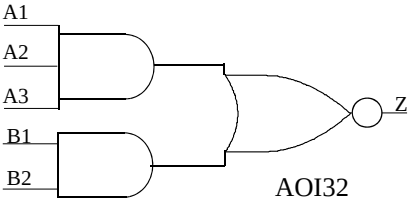


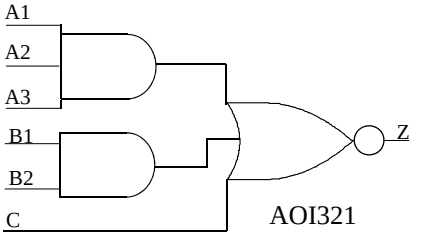
INPUTS: A1,A2,A3,B,C
OUTPUTS: Z
PINORDER: A1 A2 A3 B C Z
MINIMUM CELL AREA: 0.25



INPUTS: A1,A2,A3,B,C,D
OUTPUTS: Z
PINORDER: A1 A2 A3 B C D Z
MINIMUM CELL AREA: 0.5



INPUTS: A1,A2,A3,B1,B2
OUTPUTS: Z
PINORDER: A1 A2 A3 B1 B2 Z
MINIMUM CELL AREA: 0.25



INPUTS: A1,A2,A3,B1,B2,C
OUTPUTS: Z
PINORDER: A1 A2 A3 B1 B2 C Z
MINIMUM CELL AREA: 0.5

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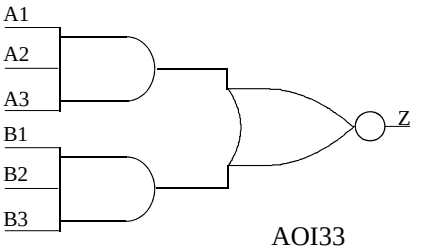
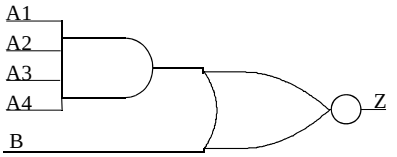


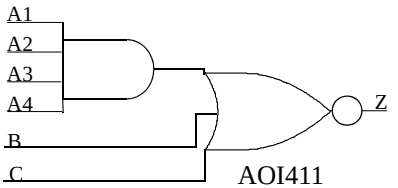
AOI33

INPUTS: A1,A2,A3,B1,B2,B3
OUTPUTS: Z
PINORDER:A1 A2 A3 B1 B2 B3 Z
MINIMUM CELL AREA: 0.5



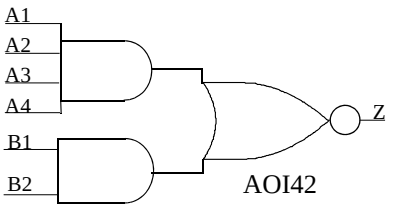
AOI41

INPUTS: A1,A2,A3,A4,B
OUTPUTS: Z
PINORDER: A1 A2 A3 A4 B Z
MINIMUM CELL AREA: 0.25



AOI411

INPUTS: A1,A2,A3,A4,B,C
OUTPUTS: Z
PINORDER: A1 A2 A3 A4 B C Z
MINIMUM CELL AREA: 0.5



AOI42

INPUTS: A1,A2,A3,A4,B1,B2
OUTPUTS: Z
PINORDER:A1 A2 A3 A4 B1 B2 Z
MINIMUM CELL AREA: 0.5

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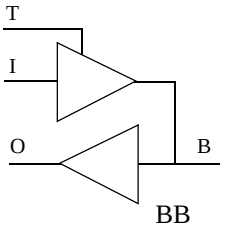
BB

CMOS Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate – BiDirectional

Lattice FPGA		
SC	XP	EC
✓	✓	✓



INPUTS: I,T; OUTPUTS: O; IOPUTS: B
PINORDER: I T O B
MINIMUM CELL AREA (All Series): 0; 3.3V PCI compliant (Series 3 only)
ATTRIBUTES (LatticeSC)
)IO_TYPE: BLVDS25, MLVDS25, HSTL15_II, HSTL18_II, SSTL25_II, SSTL33_II, LVTTL33, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVCMOS12, PCI33, PCIX33, PCIX15, AGP1X33, AGP2X33
DRIVE : NA, 2, 4, 6, 8, 12, 16, 18, 20, 24
IMPEDANCEVCCIO: OFF (default), 20, 25, 33, 50, 100
IMPEDANCEGND: OFF (default), 20, 25, 33, 50, 100
TERMINATEVCCIO: OFF (default), 33, 50, 100
TERMINATEGND: OFF (default), 33, 50, 100
PULLMODE : UP, DOWN, NONE, KEEPER, PCICLAMP

Truth Table:

INPUTS		OUTPUTS	BIDIRECTIONAL
I	T	O	B
X	1	U	Z
X	1	1	1
X	1	0	0
0	0	0	0
1	0	1	1

X = Don’t care
U = Unknown
When TSALL=0, O=U, B=Z
For PU/PD buffers, when TSALL=0, O and B will be pulled up or pulled down, respectively.

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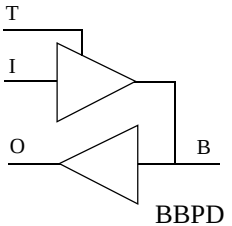
BBPD

CMOS Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate and Pull-down – BiDirectional

Lattice FPGA		
SC	XP	EC
✓	✓	✓



BBPD

INPUTS: I,T; OUTPUTS: O; IOPUTS: B
PINORDER: I T O B
MINIMUM CELL AREA (All Series): 0; 3.3V PCI compliant (Series 3 only)
ATTRIBUTES (LatticeSC)
)IO_TYPE: BLVDS25, MLVDS25, HSTL15_II, HSTL18_II, SSTL25_II, SSTL33_II, LVTTL33, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVCMOS12, PCI33, PCIX33, PCIX15, AGP1X33, AGP2X33
DRIVE : NA, 2, 4, 6, 8, 12, 16, 18, 20, 24
IMPEDANCEVCCIO: OFF (default), 20, 25, 33, 50, 100
IMPEDANCEGND: OFF (default), 20, 25, 33, 50, 100
TERMINATEVCCIO: OFF (default), 33, 50, 100
TERMINATEGND: OFF (default), 33, 50, 100
PULLMODE : UP, DOWN, NONE, KEEPER, PCICLAMP

Truth Table:

INPUTS		OUTPUTS	BIDIRECTIONAL
I	T	O	B
X	1	U	Pull0
X	1	1	1
X	1	0	0
0	0	0	0
1	0	1	1

X = Don’t care
U = Unknown
When TSALL=0, O=U, B=Z
For PU/PD buffers, when TSALL=0, O and B will be pulled up or pulled down, respectively.

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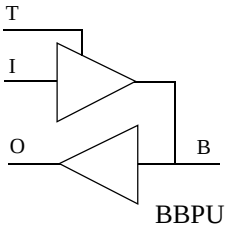
BBPU

CMOS Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate and Pull-up – BiDirectional

Lattice FPGA		
SC	XP	EC
✓	✓	✓



BBPU

INPUTS: I,T; OUTPUTS: O; IOPUTS: B
PINORDER: I T O B
MINIMUM CELL AREA (All Series): 0; 3.3V PCI compliant (Series 3 only)
ATTRIBUTES (LatticeSC)
)IO_TYPE: BLVDS25, MLVDS25, HSTL15_II, HSTL18_II, SSTL25_II, SSTL33_II, LVTTL33, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVCMOS12, PCI33, PCIX33, PCIX15, AGP1X33, AGP2X33
DRIVE : NA, 2, 4, 6, 8, 12, 16, 18, 20, 24
IMPEDANCEVCCIO: OFF (default), 20, 25, 33, 50, 100
IMPEDANCEGND: OFF (default), 20, 25, 33, 50, 100
TERMINATEVCCIO: OFF (default), 33, 50, 100
TERMINATEGND: OFF (default), 33, 50, 100
PULLMODE : UP, DOWN, NONE, KEEPER, PCICLAMP

Truth Table:

INPUTS		OUTPUTS	BIDIRECTIONAL
I	T	O	B
X	1	U	Pull1
X	1	1	1
X	1	0	0
0	0	0	0
1	0	1	1

X = Don’t care
U = Unknown
When TSALL=0, O=U, B=Z
For PU/PD buffers, when TSALL=0, O and B will be pulled up or pulled down, respectively.

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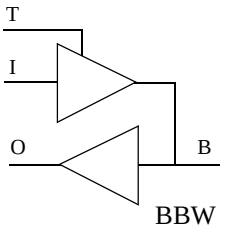
BBW

CMOS Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate – BiDirectional in keepermode

Lattice FPGA		
SC	XP	EC
✓	✓	✓



INPUTS: I,T; OUTPUTS: O; IOPUTS: B
PINORDER: I T O B
MINIMUM CELL AREA (All Series): 0; 3.3V PCI compliant (3T series only)
ATTRIBUTES (Series 5-HSI)
)IO_TYPE: BLVDS25, MLVDS25, HSTL15_II, HSTL18_II, SSTL25_II, SSTL33_II, LVTTL33, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVCMOS12, PCI33, PCIX33, PCIX15, AGP1X33, AGP2X33
DRIVE : NA, 2, 4, 6, 8, 12, 16, 18, 20, 24
IMPEDANCEVCCIO: OFF (default), 20, 25, 33, 50, 100
IMPEDANCEGND: OFF (default), 20, 25, 33, 50, 100
TERMINATEVCCIO: OFF (default), 33, 50, 100
TERMINATEGND: OFF (default), 33, 50, 100
PULLMODE : UP, DOWN, NONE, KEEPER, PCICLAMP

Truth Table:

INPUTS		OUTPUTS	BIDIRECTIONAL
I	T	O	B
0	1	0	weak 0
1	1	1	weak 1

X = Don’t care
U = Unknown

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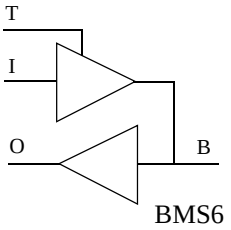
BMS6

CMOS Delayed Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate – BiDirectional

Lattice FPGA		
2	3	4
✓	✓	✓



BMS6

INPUTS: I,T
OUTPUTS: O
IOPUTS: B
PINORDER: I T O B
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVCMOS2
BUFMODE: SLEW
AMPSMODE: 6
DELAYMODE: 1
CLKMODE: SCLK (default), ECLK
INTERFACE: FASTINPUT
Note: 3.3V PCI compliant (3T series only)

Truth Table:

INPUTS		OUTPUTS	BIDIRECTIONAL
I	T	O	B
X	1	U	Z
X	1	1	1
X	1	0	0
0	0	0	0
1	0	1	1

X = Don’t care
U = Unknown
When TSALL=0, O=U, B=Z
For PU/PD buffers, when TSALL=0, O and B are pulled up or pulled down, respectively.

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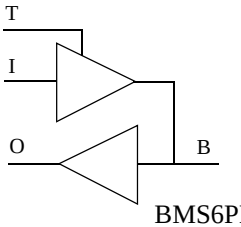
BMS6PD

CMOS Delayed Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate and Pull-down – BiDirectional

Lattice FPGA		
2	3	4
✓	✓	✓



BMS6PD

INPUTS: I,T
OUTPUTS: O
IOPUTS: B
PINORDER: I T O B
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVCMOS2
BUFMODE: SLEW
AMPSMODE: 6
DELAYMODE: 1
CLKMODE: SCLK (default), ECLK
INTERFACE: FASTINPUT
Note: 3.3V PCI compliant (3T series only)

Truth Table:

INPUTS		OUTPUTS	BIDIRECTIONAL
I	T	O	B
X	1	U	Pull0
X	1	1	1
X	1	0	0
0	0	0	0
1	0	1	1

X = Don’t care
U = Unknown
When TSALL=0, O=U, B=Z
For PU/PD buffers, when TSALL=0, O and B are pulled up or pulled down, respectively.

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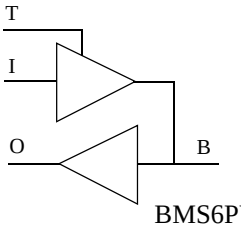
BMS6PU

CMOS Delayed Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate and Pull-up – BiDirectional

Lattice FPGA		
2	3	4
✓	✓	✓



BMS6PU

INPUTS: I,T
OUTPUTS: O
IOPUTS: B
PINORDER: I T O B
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVCMOS2
BUFMODE: SLEW
AMPSMODE: 6
DELAYMODE: 1
CLKMODE: SCLK (default), ECLK
INTERFACE: FASTINPUT
Note: 3.3V PCI compliant (3T series only)

Truth Table:

INPUTS		OUTPUTS	BIDIRECTIONAL
I	T	O	B
X	1	U	Pull1
X	1	1	1
X	1	0	0
0	0	0	0
1	0	1	1

X = Don’t care
U = Unknown
When TSALL=0, O=U, B=Z
For PU/PD buffers, when TSALL=0, O and B are pulled up or pulled down, respectively.

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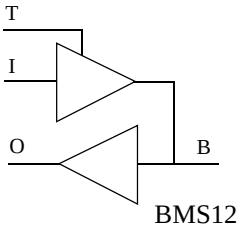
BMS12

CMOS Delayed Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate – BiDirectional

Lattice FPGA		
2	3	4
✓	✓	✓



BMS12

INPUTS: I,T
OUTPUTS: O
IOPUTS: B
PINORDER: I T O B
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVCMOS2
BUFMODE: SLEW
AMPSMODE: 12
DELAYMODE: 1
CLKMODE: SCLK (default), ECLK
INTERFACE: FASTINPUT
Note: 3.3V PCI compliant (3T series only)

Truth Table:

INPUTS		OUTPUTS	BIDIRECTIONAL
I	T	O	B
X	1	U	Z
X	1	1	1
X	1	0	0
0	0	0	0
1	0	1	1

X = Don’t care
U = Unknown
When TSALL=0, O=U, B=Z
For PU/PD buffers, when TSALL=0, O and B are pulled up or pulled down, respectively.

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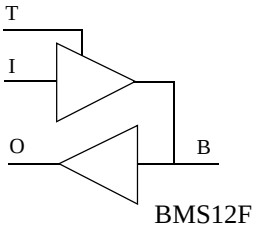
BMS12F

CMOS Delayed Input 12mA Sink 6mA Source Fast Output Buffer with Tristate – BiDirectional

Lattice FPGA		
2	3	4
✓	✓	✓



BMS12F

INPUTS: I,T
OUTPUTS: O
IOPUTS: B
PINORDER: I T O B
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVCMOS2
BUFMODE: FAST
AMPSMODE: 12
DELAYMODE: 1
CLKMODE: SCLK (default), ECLK
INTERFACE: FASTINPUT
Note: 3.3V PCI compliant (3T series only)

Truth Table:

INPUTS		OUTPUTS	BIDIRECTIONAL
I	T	O	B
X	1	U	Z
X	1	1	1
X	1	0	0
0	0	0	0
1	0	1	1

X = Don’t care
U = Unknown
When TSALL=0, O=U, B=Z
For PU/PD buffers, when TSALL=0, O and B are pulled up or pulled down, respectively.

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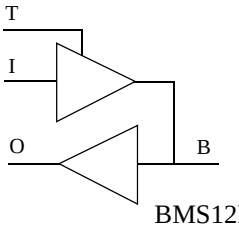
BMS12FPD

CMOS Delayed Input 12mA Sink 6mA Source Fast Output Buffer with Tristate and Pull-down – BiDirectional

Lattice FPGA		
2	3	4
✓	✓	✓



BMS12FPD

INPUTS: I,T
OUTPUTS: O
IOPUTS: B
PINORDER: I T O B
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVCMOS2
BUFMODE: FAST
AMPSMODE: 12
DELAYMODE: 1
CLKMODE: SCLK (default), ECLK
INTERFACE: FASTINPUT
Note: 3.3V PCI compliant (3T series only)

Truth Table:

INPUTS		OUTPUTS	BIDIRECTIONAL
I	T	O	B
X	1	U	Pull0
X	1	1	1
X	1	0	0
0	0	0	0
1	0	1	1

X = Don’t care
U = Unknown
When TSALL=0, O=U, B=Z
For PU/PD buffers, when TSALL=0, O and B are pulled up or pulled down, respectively.

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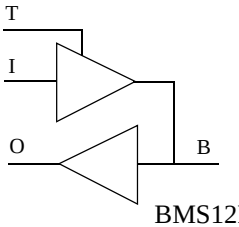
BMS12FPU

CMOS Delayed Input 12mA Sink 6mA Source Fast Output Buffer with Tristate and Pull-up – BiDirectional

Lattice FPGA		
2	3	4
✓	✓	✓



BMS12FPU

INPUTS: I,T
OUTPUTS: O
IOPUTS: B
PINORDER: I T O B
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVCMOS2
BUFMODE: FAST
AMPSMODE: 12
DELAYMODE: 1
CLKMODE: SCLK (default), ECLK
INTERFACE: FASTINPUT
Note: 3.3V PCI compliant (3T series only)

Truth Table:

INPUTS		OUTPUTS	BIDIRECTIONAL
I	T	O	B
X	1	U	Pull1
X	1	1	1
X	1	0	0
0	0	0	0
1	0	1	1

X = Don’t care
U = Unknown
When TSALL=0, O=U, B=Z
For PU/PD buffers, when TSALL=0, O and B are pulled up or pulled down, respectively.

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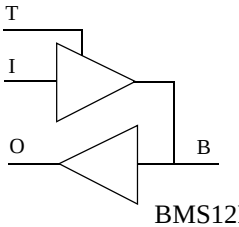
BMS12PD

CMOS Delayed Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate and Pull-down – BiDirectional

Lattice FPGA		
2	3	4
✓	✓	✓



BMS12PD

INPUTS: I,T
OUTPUTS: O
IOPUTS: B
PINORDER: I T O B
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVCMOS2
BUFMODE: SLEW
AMPSMODE: 12
DELAYMODE: 1
CLKMODE: SCLK (default), ECLK
INTERFACE: FASTINPUT
Note: 3.3V PCI compliant (3T series only)

Truth Table:

INPUTS		OUTPUTS	BIDIRECTIONAL
I	T	O	B
X	1	U	Pull0
X	1	1	1
X	1	0	0
0	0	0	0
1	0	1	1

X = Don’t care
U = Unknown
When TSALL=0, O=U, B=Z
For PU/PD buffers, when TSALL=0, O and B are pulled up or pulled down, respectively.

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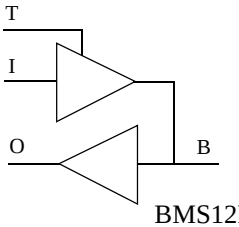
BMS12PU

CMOS Delayed Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate and Pull-up – BiDirectional

Lattice FPGA		
2	3	4
✓	✓	✓



BMS12PU

INPUTS: I,T
OUTPUTS: O
IOPUTS: B
PINORDER: I T O B
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVCMOS2
BUFMODE: SLEW
AMPSMODE: 12
DELAYMODE: 1
CLKMODE: SCLK (default), ECLK
INTERFACE: FASTINPUT
Note: 3.3V PCI compliant (3T series only)

Truth Table:

INPUTS		OUTPUTS	BIDIRECTIONAL
I	T	O	B
X	1	U	Pull1
X	1	1	1
X	1	0	0
0	0	0	0
1	0	1	1

X = Don’t care
U = Unknown
When TSALL=0, O=U, B=Z
For PU/PD buffers, when TSALL=0, O and B are pulled up or pulled down, respectively.

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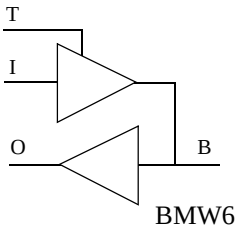
BMW6

CMOS Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate – BiDirectional

Lattice FPGA		
2	3	4
		✓



BMW6

INPUTS: I,T; OUTPUTS: O; IOPUTS: B
PINORDER: I T O B
MINIMUM CELL AREA (All Series): 0; 3.3V PCI compliant (3T series only)
ATTRIBUTES (Series 4 only)
LEVELMODE: LVTTL, LVCMOS2 (default)
BUFMODE: SLEW (default), FAST
AMPSMODE: 6 (default), 12, 24
DELAYMODE: 1, 0 (default)
CLKMODE: SCLK (default), ECLK

Note: BUFMODE and AMPSMODE are only supported when LEVELMODE = “LVTTL” or “LVCMOS2”.

Truth Table:

INPUTS		OUTPUTS	BIDIRECTIONAL
I	T	O	B
0	1	0	weak 0
1	1	1	weak 1

X = Don’t care
U = Unknown

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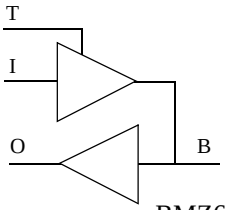
BMZ6

CMOS Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate – BiDirectional

Lattice FPGA		
2	3	4
✓	✓	✓



BMZ6

INPUTS: I,T; OUTPUTS: O; IOPUTS: B
PINORDER: I T O B
MINIMUM CELL AREA (All Series): 0; 3.3V PCI compliant (3T series only)
ATTRIBUTES (Series 4 only)
LEVELMODE: LVTTL, LVCMOS2 (default), LVCMOS18, PCI, SSTL2, SSTL3, HSTL1, HSTL3, GTL, GTLPLUS
BUFMODE: SLEW (default), FAST
AMPSMODE: 6 (default), 12, 24
DELAYMODE: 1, 0 (default)
CLKMODE: SCLK (default), ECLK
INTERFACE: FASTINPUT

Note: BUFMODE and AMPSMODE are only supported when LEVELMODE = “LVTTL” or “LVCMOS2”.

Truth Table:

INPUTS		OUTPUTS	BIDIRECTIONAL
I	T	O	B
X	1	U	Z
X	1	1	1
X	1	0	0
0	0	0	0
1	0	1	1

X = Don’t care
U = Unknown
When TSALL=0, O=U, B=Z
For PU/PD buffers, when TSALL=0, O and B will be pulled up or pulled down, respectively.

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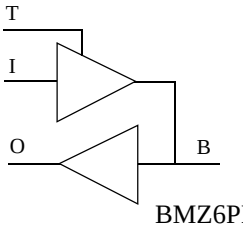
BMZ6PD

CMOS Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate and Pull-down – BiDirectional

Lattice FPGA		
2	3	4
✓	✓	✓



BMZ6PD

INPUTS: I,T; OUTPUTS: O; IOPUTS: B
PINORDER: I T O B
MINIMUM CELL AREA (All Series): 0; 3.3V PCI compliant (3T series only)
ATTRIBUTES (Series 4 only)
LEVELMODE: LVTTL, LVCMOS2 (default), LVCMOS18, PCI, SSTL2, SSTL3, HSTL1, HSTL3, GTL, GTLPLUS
BUFMODE: SLEW (default), FAST
AMPSMODE: 6 (default), 12, 24
DELAYMODE: 1, 0 (default)
CLKMODE: SCLK (default), ECLK
INTERFACE: FASTINPUT

Note: BUFMODE and AMPSMODE are only supported when LEVELMODE = “LVTTL” or “LVCMOS2”.

Truth Table:

INPUTS		OUTPUTS	BIDIRECTIONAL
I	T	O	B
X	1	U	Pull0
X	1	1	1
X	1	0	0
0	0	0	0
1	0	1	1

X = Don’t care
U = Unknown
When TSALL=0, O=U, B=Z
For PU/PD buffers, when TSALL=0, O and B will be pulled up or pulled down, respectively.

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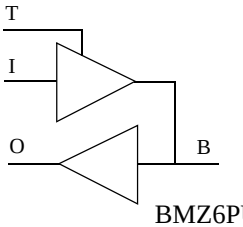
BMZ6PU

CMOS Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate and Pull-up – BiDirectional

Lattice FPGA		
2	3	4
✓	✓	✓



BMZ6PU

INPUTS: I,T; OUTPUTS: O; IOPUTS: B
PINORDER: I T O B
MINIMUM CELL AREA (All Series): 0; 3.3V PCI compliant (3T series only)
ATTRIBUTES (Series 4 only)
LEVELMODE: LVTTL, LVCMOS2 (default), LVCMOS18, PCI, SSTL2, SSTL3, HSTL1, HSTL3, GTL, GTLPLUS
BUFMODE: SLEW (default), FAST
AMPSMODE: 6 (default), 12, 24
DELAYMODE: 1, 0 (default)
CLKMODE: SCLK (default), ECLK
INTERFACE: FASTINPUT

Note: BUFMODE and AMPSMODE are only supported when LEVELMODE = “LVTTL” or “LVCMOS2”.

Truth Table:

INPUTS		OUTPUTS	BIDIRECTIONAL
I	T	O	B
X	1	U	Pull1
X	1	1	1
X	1	0	0
0	0	0	0
1	0	1	1

X = Don’t care
U = Unknown
When TSALL=0, O=U, B=Z
For PU/PD buffers, when TSALL=0, O and B will be pulled up or pulled down, respectively.

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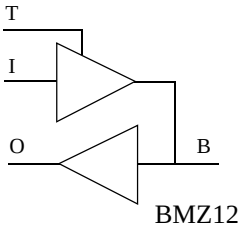
BMZ12

CMOS Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate – BiDirectional

Lattice FPGA		
2	3	4
✓	✓	✓



BMZ12

INPUTS: I,T
OUTPUTS: O
IOPUTS: B
PINORDER: I T O B
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVCMOS2
BUFMODE: SLEW
AMPSMODE: 12
DELAYMODE: 0
CLKMODE: SCLK (default), ECLK
INTERFACE: FASTINPUT
3.3V PCI compliant (3T series only)

Truth Table:

INPUTS		OUTPUTS	BIDIRECTIONAL
I	T	O	B
X	1	U	Z
X	1	1	1
X	1	0	0
0	0	0	0
1	0	1	1

X = Don’t care
U = Unknown
When TSALL=0, O=U, B=Z
For PU/PD buffers, when TSALL=0, O and B will be pulled up or pulled down, respectively.

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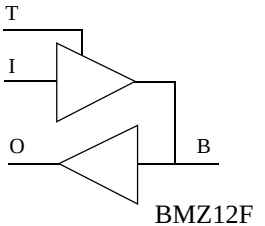
BMZ12F

CMOS Input 12mA Sink 6mA Source Fast Output Buffer with Tristate – BiDirectional

Lattice FPGA		
2	3	4
✓	✓	✓



BMZ12F

INPUTS: I,T
OUTPUTS: O
IOPUTS: B
PINORDER: I T O B
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVCMOS2
BUFMODE: FAST
AMPSMODE: 12
DELAYMODE: 0
CLKMODE: SCLK (default), ECLK
INTERFACE: FASTINPUT
3.3V PCI compliant (3T series only)

Truth Table:

INPUTS		OUTPUTS	BIDIRECTIONAL
I	T	O	B
X	1	U	Z
X	1	1	1
X	1	0	0
0	0	0	0
1	0	1	1

X = Don’t care
U = Unknown
When TSALL=0, O=U, B=Z
For PU/PD buffers, when TSALL=0, O and B will be pulled up or pulled down, respectively.

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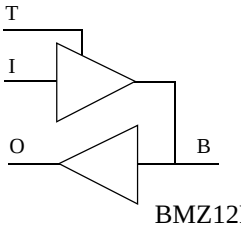
BMZ12FPD

CMOS Input 12mA Sink 6mA Source Fast Output Buffer with Tristate and Pull-down – BiDirectional

Lattice FPGA		
2	3	4
✓	✓	✓



BMZ12FPD

INPUTS: I,T
OUTPUTS: O
IOPUTS: B
PINORDER: I T O B
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVCMOS2
BUFMODE: FAST
AMPSMODE: 12
DELAYMODE: 0
CLKMODE: SCLK (default), ECLK
INTERFACE: FASTINPUT
3.3V PCI compliant (3T series only)

Truth Table:

INPUTS		OUTPUTS	BIDIRECTIONAL
I	T	O	B
X	1	U	Pull0
X	1	1	1
X	1	0	0
0	0	0	0
1	0	1	1

X = Don’t care
U = Unknown
When TSALL=0, O=U, B=Z
For PU/PD buffers, when TSALL=0, O and B will be pulled up or pulled down, respectively.

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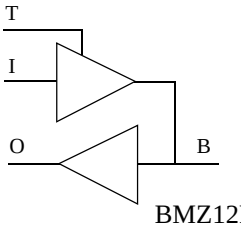
BMZ12FPU

CMOS Input 12mA Sink 6mA Source Fast Output Buffer with Tristate and Pull-up – BiDirectional

Lattice FPGA		
2	3	4
✓	✓	✓



BMZ12FPU

INPUTS: I,T
OUTPUTS: O
IOPUTS: B
PINORDER: I T O B
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVCMOS2
BUFMODE: FAST
AMPSMODE: 12
DELAYMODE: 0
CLKMODE: SCLK (default), ECLK
INTERFACE: FASTINPUT
3.3V PCI compliant (3T series only)

Truth Table:

INPUTS		OUTPUTS	BIDIRECTIONAL
I	T	O	B
X	1	U	Pull1
X	1	1	1
X	1	0	0
0	0	0	0
1	0	1	1

X = Don’t care
U = Unknown
When TSALL=0, O=U, B=Z
For PU/PD buffers, when TSALL=0, O and B will be pulled up or pulled down, respectively.

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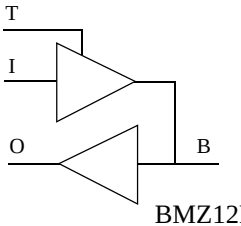
BMZ12PD

CMOS Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate and Pull-down – BiDirectional

Lattice FPGA		
2	3	4
✓	✓	✓



BMZ12PD

INPUTS: I,T
OUTPUTS: O
IOPUTS: B
PINORDER: I T O B
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVCMOS2
BUFMODE: SLEW
AMPSMODE: 12
DELAYMODE: 0
CLKMODE: SCLK (default), ECLK
INTERFACE: FASTINPUT
3.3V PCI compliant (3T series only)

Truth Table:

INPUTS		OUTPUTS	BIDIRECTIONAL
I	T	O	B
X	1	U	Pull0
X	1	1	1
X	1	0	0
0	0	0	0
1	0	1	1

X = Don’t care
U = Unknown
When TSALL=0, O=U, B=Z
For PU/PD buffers, when TSALL=0, O and B will be pulled up or pulled down, respectively.

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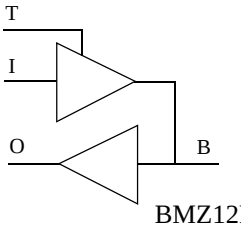
BMZ12PU

CMOS Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate and Pull-up –BiDirectional

Lattice FPGA		
2	3	4
✓	✓	✓



BMZ12PU

INPUTS: I,T
OUTPUTS: O
IOPUTS: B
PINORDER: I T O B
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVCMOS2
BUFMODE: SLEW
AMPSMODE: 12
DELAYMODE: 0
CLKMODE: SCLK (default), ECLK
INTERFACE: FASTINPUT
3.3V PCI compliant (3T series only)

Truth Table:

INPUTS		OUTPUTS	BIDIRECTIONAL
I	T	O	B
X	1	U	Pull1
X	1	1	1
X	1	0	0
0	0	0	0
1	0	1	1

X = Don’t care
U = Unknown
When TSALL=0, O=U, B=Z
For PU/PD buffers, when TSALL=0, O and B will be pulled up or pulled down, respectively.

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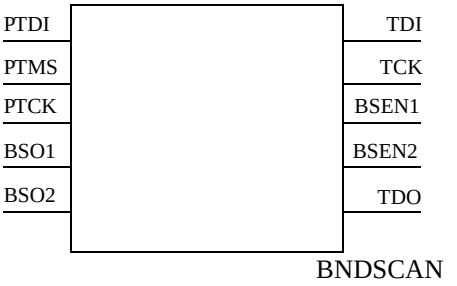
BNDSCAN

Boundary Scan — Logic Control Circuit

Lattice FPGA		
2	3	4
✓	✓	✓



INPUTS: PTDI,PTMS,PTCK,BSO1,BSO2
OUTPUTS: TDI,TCK,BSEN1,BSEN2,TDO
PINORDER: PTDI PTMS PTCK BSO1 BSO2 TDI TCK BSEN1 BSEN2 TDO
MINIMUM CELL AREA (All Series): 0

Description:

The BNDSCAN macro provides the control and interconnect circuit used by the boundary scan function. This function allows the testing of increasingly complex ICs and IC packages. The ORCA series FPGA provides four interface pins: test data in (PTDI), test mode select (PTMS), test clock (PTCK), and test data out (TDO). For more information on the boundary-scan function refer to an available data book or contact technical support.

PTDI: This is connected to a pad for a particular part and package which is the serial input to the boundary scan macro for incoming data. When used for boundary scan this pad is dedicated as an input for data. At all other times, the pad reverts to an I/O.

PTMS: During boundary-scan, this is connected to a dedicated pad for a given ORCA FPGA part and package, during boundary-scan. At all other times, the pad reverts to an I/O.

PTCK: During boundary-scan, this is the pad input for the test clock to the boundary-scan macro. At all other times, the pad resorts to an I/O.

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BSO1: Boundary Scan-ring Output 1. This is the input to scan ring 1 of the boundary scan block. This is the output of the last register of the internal scan ring 1 to the boundary scan block.

BSO2: Boundary Scan-ring Output 2. This is the input to scan ring 2 of the boundary scan block. This is the output of the last register of the internal scan ring 2 to the boundary scan block.

TDI: Test Data In. The output of the boundary scan macro from where the test data is output to the scan ring.

TCK: The boundary scan clock which is output from the boundary scan macro to the scan ring. This clock is a gated clock that is only active when BSEN1 or BSEN2 is active.

BSEN1: This output from the Boundary Scan macro is to enable the flow of data via TDI to scan ring 1 and is used to enable the test clock to the clock of scan ring 1.

BSEN2: This output from the Boundary Scan macro is to enable the flow of data via TDI to scan ring 2 and is used to enable the test clock to the clock of scan ring 2.

TDO: Test Data Out. This output from the boundary scan macro is the serial test data output.

For more information on how to use this macro and a detailed description of the input and output pin functions, refer to the Boundary Scan application note.

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BPAD

Bi-Directional PAD

Lattice FPGA		
2	3	4
✓		

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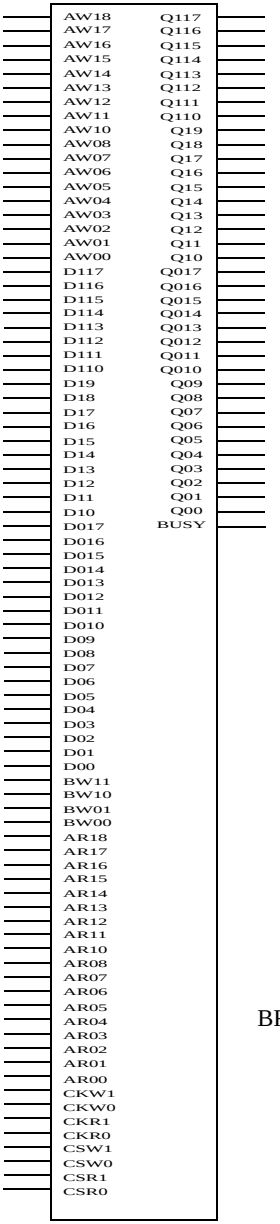
BR512X18

512 Word by 18 Bit 4 Port Block RAM

Lattice FPGA		
2	3	4
		✓



BR512X18

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INPUTS: AW18, AW17, AW16, AW15, AW14, AW13, AW12, AW11, AW10, AW08, AW07, AW06, AW05, AW04, AW03, AW02, AW01, AW00, D117, D116, D115, D114, D113, D112, D111, D110, D19, D18, D17, D16, D15, D14, D13, D12, D11, D10, D017, D016, D015, D014, D013, D012, D011, D010, D09, D08, D07, D06, D05, D04, D03, D02, D01, D00, BW11, BW10, BW01, BW00, AR18, AR17, AR16, AR15, AR14, AR13, AR12, AR11, AR10, AR08, AR07, AR06, AR05, AR04, AR03, AR02, AR01, AR00, CKW1, CKW0, CKR1, CKR0, CSW1, CSW0, CSR1, CSR0

OUTPUTS: Q117, Q116, Q115, Q114, Q113, Q112, Q111, Q110, Q19, Q18, Q17, Q16, Q15, Q14, Q13, Q12, Q11, Q10, Q017, Q016, Q015, Q014, Q013, Q012, Q011, Q010, Q09, Q08, Q07, Q06, Q05, Q04, Q03, Q02, Q01, Q00, BUSY

PINORDER: AW18 AW17 AW16 AW15 AW14 AW13 AW12 AW11 AW10 AW08 AW07 AW06 AW05 AW04 AW03 AW02 AW01 AW00 D117 D116 D115 D114 D113 D112 D111 D110 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D017 D016 D015 D014 D013 D012 D011 D010 D09 D08 D07 D06 D05 D04 D03 D02 D01 D00 BW11 BW10 BW01 BW00 AR18 AR17 AR16 AR15 AR14 AR13 AR12 AR11 AR10 AR08 AR07 AR06 AR05 AR04 AR03 AR02 AR01 AR00 CKW1 CKW0 CKR1 CKR0 CSW1 CSW0 CSR1 CSR0 Q117 Q116 Q115 Q114 Q113 Q112 Q111 Q110 Q19 Q18 Q17 Q16 Q15 Q14 Q13 Q12 Q11 Q10 Q017 Q016 Q015 Q014 Q013 Q012 Q011 Q010 Q09 Q08 Q07 Q06 Q05 Q04 Q03 Q02 Q01 Q00 BUSY

ATTRIBUTES (Series 4 only)

BRAMMODE0: NOREG, INREG, OUTREG, IOREG

BRAMMODE1: NOREG, INREG, OUTREG, IOREG

ARBITERMODE: TRUE, FALSE

Description:

There are two write ports, (AW[08:00] and AW[18:10]) and two read ports (AR[08:00] and AR[18:10]).

Example pin functions for port-1:

Function	Pins
port-1 write address	AW18, AW17,...AW10
port-1 read address	AR18, AR17,...AR10
port-1 data (18-bit)	D117, D116,...D10
port-1 byte enable	BW11, BW10

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Function	Pins
port-1 write clock	CKW1
port-1 read clock	CKR1
port-1 write enable	CSW1
port-1 read enable	CSR1

Data can be written into the memory at the rising edge of the write clock when write enable is HIGH and byte enable is HIGH.

Attribute	
BRRAMODE[*]	“INREG” - Read address is registered. “OUTREG” - Data out is registered. “IOREG” - Both read address and data out are registered. “NOREG” - (default) Nothing is registered.

When ARBITERMODE is “TRUE,” then the arbitration function is enabled. When both port-1 and port-0 write addresses are the same and both the write enables are HIGH, writing from port-0 will be blocked and the busy signal will go HIGH.

Function	Pins
port-1 output	Q117, Q116,...Q10
port-0 output	Q017, Q016,...Q00

Note: The BR512X18 element should be instantiated through SCUBA. Refer to the appropriate topic in the online help system for details.

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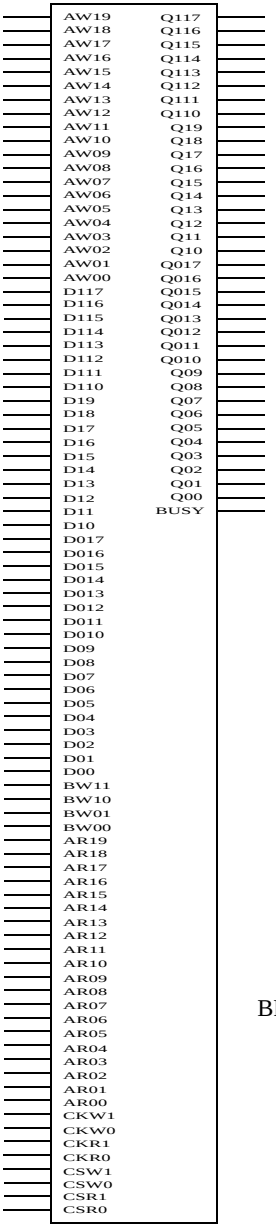
BR1024X18

1024 Word by 18 Bit 4 Port Block RAM

Lattice FPGA		
2	3	4
		✓



BR1024X18

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INPUTS: AW19, AW18, AW17, AW16, AW15, AW14, AW13, AW12, AW11, AW10, AW09, AW08, AW07, AW06, AW05, AW04, AW03, AW02, AW01, AW00, D117, D116, D115, D114, D113, D112, D111, D110, D19, D18, D17, D16, D15, D14, D13, D12, D11, D10, D017, D016, D015, D014, D013, D012, D011, D010, D09, D08, D07, D06, D05, D04, D03, D02, D01, D00, BW11, BW10, BW01, BW00, AR19, AR18, AR17, AR16, AR15, AR14, AR13, AR12, AR11, AR10, AR09, AR08, AR07, AR06, AR05, AR04, AR03, AR02, AR01, AR00, CKW1, CKW0, CKR1, CKR0, CSW1, CSW0, CSR1, CSR0

OUTPUTS: Q117, Q116, Q115, Q114, Q113, Q112, Q111, Q110, Q19, Q18, Q17, Q16, Q15, Q14, Q13, Q12, Q11, Q10, Q017, Q016, Q015, Q014, Q013, Q012, Q011, Q010, Q09, Q08, Q07, Q06, Q05, Q04, Q03, Q02, Q01, Q00, BUSY

PINORDER: AW19 AW18 AW17 AW16 AW15 AW14 AW13 AW12 AW11 AW10 AW09 AW08 AW07 AW06 AW05 AW04 AW03 AW02 AW01 AW00 D117 D116 D115 D114 D113 D112 D111 D110 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D017 D016 D015 D014 D013 D012 D011 D010 D09 D08 D07 D06 D05 D04 D03 D02 D01 D00 BW11 BW10 BW01 BW00 AR19 AR18 AR17 AR16 AR15 AR14 AR13 AR12 AR11 AR10 AR09 AR08 AR07 AR06 AR05 AR04 AR03 AR02 AR01 AR00 CKW1 CKW0 CKR1 CKR0 CSW1 CSW0 CSR1 CSR0 Q117 Q116 Q115 Q114 Q113 Q112 Q111 Q110 Q19 Q18 Q17 Q16 Q15 Q14 Q13 Q12 Q11 Q10 Q017 Q016 Q015 Q014 Q013 Q012 Q011 Q010 Q09 Q08 Q07 Q06 Q05 Q04 Q03 Q02 Q01 Q00 BUSY

ATTRIBUTES (Series 4 only)
BRAMMODE0: NOREG, INREG, OUTREG, IOREG
BRAMMODE1: NOREG, INREG, OUTREG, IOREG
ARBITERMODE: TRUE, FALSE

Description:

There are two write ports, (AW[09:19], AW[18:10]) and two read ports (AR[09:00] and AR[19:10]).

Example pin functions for port-1:.

Function	Pins
port-1 write address	AW19, AW18,...AW10
port-1 read address	AR19, AR18,...AR10
port-1 data (18-bit)	D117, D116,...D10

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Function	Pins
port-1 byte enable	BW11, BW10
port-1 write clock	CKW1, CKW0
port-1 read clock	CKR1, CKR0
port-1 write enable	CSW1, CSW0
port-1 read enable	CSR1, CSR0

Data can be written into the memory at the rising edge of the write clock when write enable is HIGH and byte enable is HIGH.

Attribute	
BRRAMODE[*]	“INREG” - Read address is registered. “OUTREG” - Data out is registered. “IOREG” - Both read address and data out are registered. “NOREG” - (default) Nothing is registered.

When ARBITERMODE is “TRUE,” then the arbitration function is enabled. When both port-1 and port-0 write addresses are the same and both the write enables are HIGH, writing from port-0 will be blocked and the busy signal will go HIGH.

Function	Pins
port-1 output	Q117, Q116,...Q10
port-0 output	Q017, Q016,...Q00

Note: The BR1024X18 element should be instantiated through SCUBA. Refer to the appropriate topic in the online help system for details.

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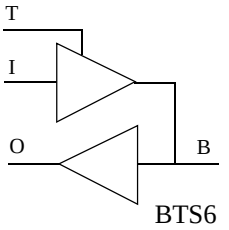
BTS6

TTL Delayed Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate – BiDirectional

Lattice FPGA		
2	3	4
✓	✓	✓



BTS6

INPUTS: I,T
OUTPUTS: O
IOPUTS: B
PINORDER: I T O B
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVTTL
BUFMODE: SLEW
AMPSMODE: 6
DELAYMODE: 1
CLKMODE: SCLK (default), ECLK

5V tolerant/5V PCI compliant (3T series only)

Truth Table:

INPUTS		OUTPUTS	BIDIRECTIONAL
I	T	O	B
X	1	U	Z
X	1	1	1
X	1	0	0
0	0	0	0
1	0	1	1

X = Don’t care
U = Unknown
When TSALL=0, O=U, B=Z
For PU/PD buffers, when TSALL=0, O and B will be pulled up or pulled down, respectively.

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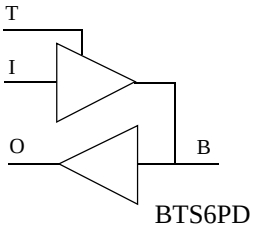
BTS6PD

TTL Delayed Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate and Pull-down – BiDirectional

Lattice FPGA		
2	3	4
✓	✓	✓



BTS6PD

INPUTS: I,T
OUTPUTS: O
IOPUTS: B
PINORDER: I T O B
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVTTL
BUFMODE: SLEW
AMPSMODE: 6
DELAYMODE: 1
CLKMODE: SCLK (default), ECLK

5V tolerant/5V PCI compliant (3T series only)

Truth Table:

INPUTS		OUTPUTS	BIDIRECTIONAL
I	T	O	B
X	1	U	Pull0
X	1	1	1
X	1	0	0
0	0	0	0
1	0	1	1

X = Don’t care
U = Unknown
When TSALL=0, O=U, B=Z
For PU/PD buffers, when TSALL=0, O and B will be pulled up or pulled down, respectively.

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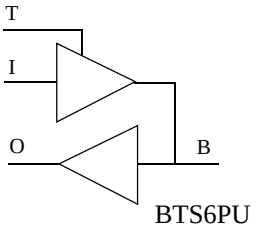
BTS6PU

TTL Delayed Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate and Pull-up – BiDirectional

Lattice FPGA		
2	3	4
✓	✓	✓



BTS6PU

INPUTS: I,T
OUTPUTS: O
IOPUTS: B
PINORDER: I T O B
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVTTL
BUFMODE: SLEW
AMPSMODE: 6
DELAYMODE: 1
CLKMODE: SCLK (default), ECLK

5V tolerant/5V PCI compliant (3T series only)

Truth Table:

INPUTS		OUTPUTS	BIDIRECTIONAL
I	T	O	B
X	1	U	Pull1
X	1	1	1
X	1	0	0
0	0	0	0
1	0	1	1

X = Don’t care
U = Unknown
When TSALL=0, O=U, B=Z
For PU/PD buffers, when TSALL=0, O and B will be pulled up or pulled down, respectively.

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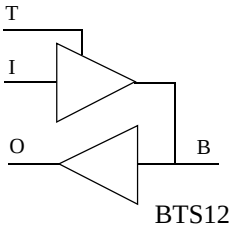
BTS12

TTL Delayed Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate – BiDirectional

Lattice FPGA		
2	3	4
✓	✓	✓



BTS12

INPUTS: I,T
OUTPUTS: O
IOPUTS: B
PINORDER: I T O B
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVTTL
BUFMODE: SLEW
AMPSMODE: 12
DELAYMODE: 1
CLKMODE: SCLK (default), ECLK

5V tolerant/5V PCI compliant (3T series only)

Truth Table:

INPUTS		OUTPUTS	BIDIRECTIONAL
I	T	O	B
X	1	U	Z
X	1	1	1
X	1	0	0
0	0	0	0
1	0	1	1

X = Don’t care
U = Unknown
When TSALL=0, O=U, B=Z
For PU/PD buffers, when TSALL=0, O and B will be pulled up or pulled down, respectively.

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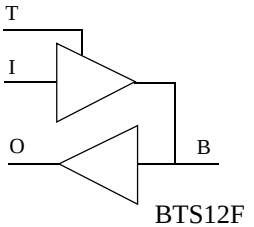
BTS12F

TTL Delayed Input 12mA Sink 6mA Source Fast Output Buffer with Tristate – BiDirectional

Lattice FPGA		
2	3	4
✓	✓	✓



BTS12F

INPUTS: I,T
OUTPUTS: O
IOPUTS: B
PINORDER: I T O B
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVTTL
BUFMODE: FAST
AMPSMODE: 12
DELAYMODE: 1
CLKMODE: SCLK (default), ECLK

5V tolerant/5V PCI compliant (3T series only)

Truth Table:

INPUTS		OUTPUTS	BIDIRECTIONAL
I	T	O	B
X	1	U	Z
X	1	1	1
X	1	0	0
0	0	0	0
1	0	1	1

X = Don’t care
U = Unknown
When TSALL=0, O=U, B=Z
For PU/PD buffers, when TSALL=0, O and B will be pulled up or pulled down, respectively.

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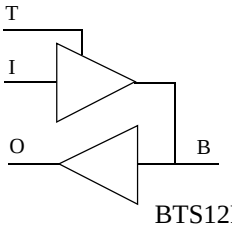
BTS12FPD

TTL Delayed Input 12mA Sink 6mA Source Fast Output Buffer with Tristate and Pull-down – BiDirectional

Lattice FPGA		
2	3	4
✓	✓	✓



BTS12FPD

INPUTS: I,T
OUTPUTS: O
IOPUTS: B
PINORDER: I T O B
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVTTL
BUFMODE: FAST
AMPSMODE: 12
DELAYMODE: 1
CLKMODE: SCLK (default), ECLK

5V tolerant/5V PCI compliant (3T series only)

Truth Table:

INPUTS		OUTPUTS	BIDIRECTIONAL
I	T	O	B
X	1	U	Pull0
X	1	1	1
X	1	0	0
0	0	0	0
1	0	1	1

X = Don’t care
U = Unknown
When TSALL=0, O=U, B=Z
For PU/PD buffers, when TSALL=0, O and B will be pulled up or pulled down, respectively.

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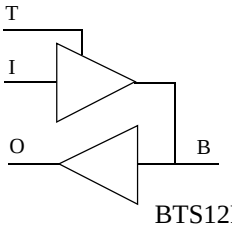
BTS12FPU

TTL Delayed Input 12mA Sink 6mA Source Fast Output Buffer with Tristate and Pull-up – BiDirectional

Lattice FPGA		
2	3	4
✓	✓	✓



BTS12FPU

INPUTS: I,T
OUTPUTS: O
IOPUTS: B
PINORDER: I T O B
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVTTL
BUFMODE: FAST
AMPSMODE: 12
DELAYMODE: 1
CLKMODE: SCLK (default), ECLK

5V tolerant/5V PCI compliant (3T series only)

Truth Table:

INPUTS		OUTPUTS	BIDIRECTIONAL
I	T	O	B
X	1	U	Pull1
X	1	1	1
X	1	0	0
0	0	0	0
1	0	1	1

X = Don’t care
U = Unknown
When TSALL=0, O=U, B=Z
For PU/PD buffers, when TSALL=0, O and B will be pulled up or pulled down, respectively.

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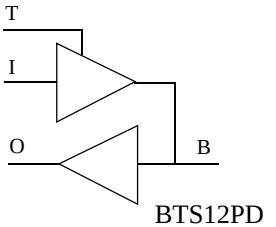
BTS12PD

TTL Delayed Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate and Pull-down – BiDirectional

Lattice FPGA		
2	3	4
✓	✓	✓



BTS12PD

INPUTS: I,T
OUTPUTS: O
IOPUTS: B
PINORDER: I T O B
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVTTL
BUFMODE: SLEW
AMPSMODE: 12
DELAYMODE: 1
CLKMODE: SCLK (default), ECLK

5V tolerant/5V PCI compliant (3T series only)

Truth Table:

INPUTS		OUTPUTS	BIDIRECTIONAL
I	T	O	B
X	1	U	Pull0
X	1	1	1
X	1	0	0
0	0	0	0
1	0	1	1

X = Don’t care
U = Unknown
When TSALL=0, O=U, B=Z
For PU/PD buffers, when TSALL=0, O and B will be pulled up or pulled down, respectively.

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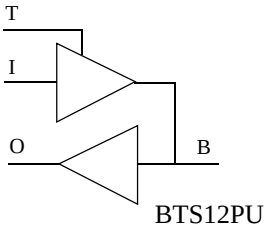
BTS12PU

TTL Delayed Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate and Pull-up – BiDirectional

Lattice FPGA		
2	3	4
✓	✓	✓



BTS12PU

INPUTS: I,T
OUTPUTS: O
IOPUTS: B
PINORDER: I T O B
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVTTL
BUFMODE: SLEW
AMPSMODE: 12
DELAYMODE: 1
CLKMODE: SCLK (default), ECLK

5V tolerant/5V PCI compliant (3T series only)

Truth Table:

INPUTS		OUTPUTS	BIDIRECTIONAL
I	T	O	B
X	1	U	Pull1
X	1	1	1
X	1	0	0
0	0	0	0
1	0	1	1

X = Don’t care
U = Unknown
When TSALL=0, O=U, B=Z
For PU/PD buffers, when TSALL=0, O and B will be pulled up or pulled down, respectively.

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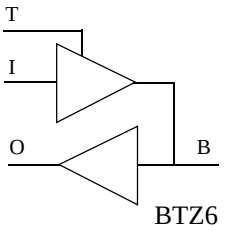
BTZ6

TTL Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate – BiDirectional

Lattice FPGA		
2	3	4
✓	✓	✓



BTZ6

INPUTS: I,T
OUTPUTS: O
IOPUTS: B
PINORDER: I T O B
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVTTL
BUFMODE: SLEW
AMPSMODE: 6
DELAYMODE: 0
CLKMODE: SCLK (default), ECLK

5V tolerant/5V PCI compliant (3T series only)

Truth Table:

INPUTS		OUTPUTS	BIDIRECTIONAL
I	T	O	B
X	1	U	Z
X	1	1	1
X	1	0	0
0	0	0	0
1	0	1	1

X = Don’t care
U = Unknown
When TSALL=0, O=U, B=Z
For PU/PD buffers, when TSALL=0, O and B will be pulled up or pulled down, respectively.

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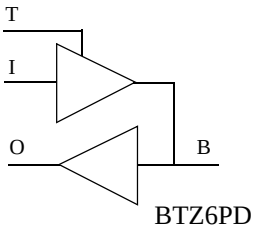
BTZ6PD

TTL Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate and Pull-down – BiDirectional

Lattice FPGA		
2	3	4
✓	✓	✓



BTZ6PD

INPUTS: I,T
OUTPUTS: O
IOPUTS: B
PINORDER: I T O B
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVTTL
BUFMODE: SLEW
AMPSMODE: 6
DELAYMODE: 0
CLKMODE: SCLK (default), ECLK

5V tolerant/5V PCI compliant (3T series only)

Truth Table:

INPUTS		OUTPUTS	BIDIRECTIONAL
I	T	O	B
X	1	U	Pull0
X	1	1	1
X	1	0	0
0	0	0	0
1	0	1	1

X = Don’t care
U = Unknown
When TSALL=0, O=U, B=Z
For PU/PD buffers, when TSALL=0, O and B will be pulled up or pulled down, respectively.

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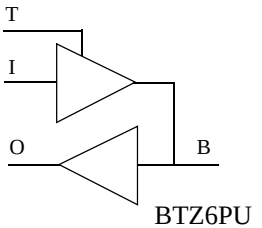
BTZ6PU

TTL Input 6mA Sink 3mA Source Sinklim Output Buffer with Tristate and Pull-up – BiDirectional

Lattice FPGA		
2	3	4
✓	✓	✓



BTZ6PU

INPUTS: I,T
OUTPUTS: O
IOPUTS: B
PINORDER: I T O B
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVTTL
BUFMODE: SLEW
AMPSMODE: 6
DELAYMODE: 0
CLKMODE: SCLK (default), ECLK

5V tolerant/5V PCI compliant (3T series only)

Truth Table:

INPUTS		OUTPUTS	BIDIRECTIONAL
I	T	O	B
X	1	U	Pull1
X	1	1	1
X	1	0	0
0	0	0	0
1	0	1	1

X = Don’t care
U = Unknown
When TSALL=0, O=U, B=Z
For PU/PD buffers, when TSALL=0, O and B will be pulled up or pulled down, respectively.

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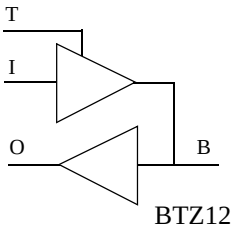
BTZ12

TTL Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate – BiDirectional

Lattice FPGA		
2	3	4
✓	✓	✓



BTZ12

INPUTS: I,T
OUTPUTS: O
IOPUTS: B
PINORDER: I T O B
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVTTL
BUFMODE: SLEW
AMPSMODE: 12
DELAYMODE: 0
CLKMODE: SCLK (default), ECLK

5V tolerant/5V PCI compliant (3T series only)

Truth Table:

INPUTS		OUTPUTS	BIDIRECTIONAL
I	T	O	B
X	1	U	Z
X	1	1	1
X	1	0	0
0	0	0	0
1	0	1	1

X = Don’t care
U = Unknown
When TSALL=0, O=U, B=Z
For PU/PD buffers, when TSALL=0, O and B will be pulled up or pulled down, respectively.

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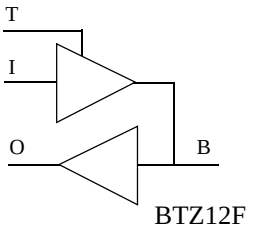
BTZ12F

TTL Input 12mA Sink 6mA Source Fast Output Buffer with Tristate – BiDirectional

Lattice FPGA		
2	3	4
✓	✓	✓



BTZ12F

INPUTS: I,T
OUTPUTS: O
IOPUTS: B
PINORDER: I T O B
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVTTL
BUFMODE: FAST
AMPSMODE: 12
DELAYMODE: 0
CLKMODE: SCLK (default), ECLK

5V tolerant/5V PCI compliant (3T series only)

Truth Table:

INPUTS		OUTPUTS	BIDIRECTIONAL
I	T	O	B
X	1	U	Z
X	1	1	1
X	1	0	0
0	0	0	0
1	0	1	1

X = Don’t care
U = Unknown
When TSALL=0, O=U, B=Z
For PU/PD buffers, when TSALL=0, O and B will be pulled up or pulled down, respectively.

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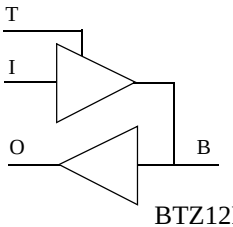
BTZ12FPD

TTL Input 12mA Sink 6mA Source Fast Output Buffer with Tristate and Pull-down – BiDirectional

Lattice FPGA		
2	3	4
✓	✓	✓



BTZ12FPD

INPUTS: I,T
OUTPUTS: O
IOPUTS: B
PINORDER: I T O B
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVTTL
BUFMODE: FAST
AMPSMODE: 12
DELAYMODE: 0
CLKMODE: SCLK (default), ECLK

5V tolerant/5V PCI compliant (3T series only)

Truth Table:

INPUTS		OUTPUTS	BIDIRECTIONAL
I	T	O	B
X	1	U	Pull0
X	1	1	1
X	1	0	0
0	0	0	0
1	0	1	1

X = Don’t care
U = Unknown
When TSALL=0, O=U, B=Z
For PU/PD buffers, when TSALL=0, O and B will be pulled up or pulled down, respectively.

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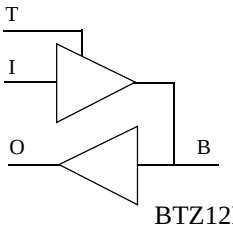
BTZ12FPU

TTL Input 12mA Sink 6mA Source Fast Output Buffer with Tristate and Pull-up – BiDirectional

Lattice FPGA		
2	3	4
✓	✓	✓



BTZ12FPU

INPUTS: I,T
OUTPUTS: O
IOPUTS: B
PINORDER: I T O B
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVTTL
BUFMODE: FAST
AMPSMODE: 12
DELAYMODE: 0
CLKMODE: SCLK (default), ECLK

5V tolerant/5V PCI compliant (3T series only)

Truth Table:

INPUTS		OUTPUTS	BIDIRECTIONAL
I	T	O	B
X	1	U	Pull1
X	1	1	1
X	1	0	0
0	0	0	0
1	0	1	1

X = Don’t care
U = Unknown
When TSALL=0, O=U, B=Z
For PU/PD buffers, when TSALL=0, O and B will be pulled up or pulled down, respectively.

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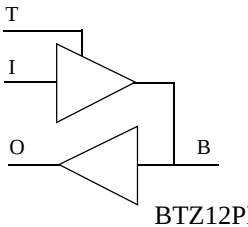
BTZ12PD

TTL Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate and Pull-down – BiDirectional

Lattice FPGA		
2	3	4
✓	✓	✓



BTZ12PD

INPUTS: I,T
OUTPUTS: O
IOPUTS: B
PINORDER: I T O B
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVTTL
BUFMODE: SLEW
AMPSMODE: 12
DELAYMODE: 0
CLKMODE: SCLK (default), ECLK

5V tolerant/5V PCI compliant (3T series only)

Truth Table:

INPUTS		OUTPUTS	BIDIRECTIONAL
I	T	O	B
X	1	U	Pull0
X	1	1	1
X	1	0	0
0	0	0	0
1	0	1	1

X = Don’t care
U = Unknown
When TSALL=0, O=U, B=Z
For PU/PD buffers, when TSALL=0, O and B will be pulled up or pulled down, respectively.

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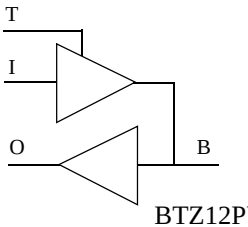
BTZ12PU

TTL Input 12mA Sink 6mA Source Slewlim Output Buffer with Tristate and Pull-up– BiDirectional

Lattice FPGA		
2	3	4
✓	✓	✓



BTZ12PU

INPUTS: I,T
OUTPUTS: O
IOPUTS: B
PINORDER: I T O B
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVTTL
BUFMODE: SLEW
AMPSMODE: 12
DELAYMODE: 0
CLKMODE: SCLK (default), ECLK

5V tolerant/5V PCI compliant (3T series only)

Truth Table:

INPUTS		OUTPUTS	BIDIRECTIONAL
I	T	O	B
X	1	U	Pull1
X	1	1	1
X	1	0	0
0	0	0	0
1	0	1	1

X = Don’t care
U = Unknown
When TSALL=0, O=U, B=Z
For PU/PD buffers, when TSALL=0, O and B will be pulled up or pulled down, respectively.

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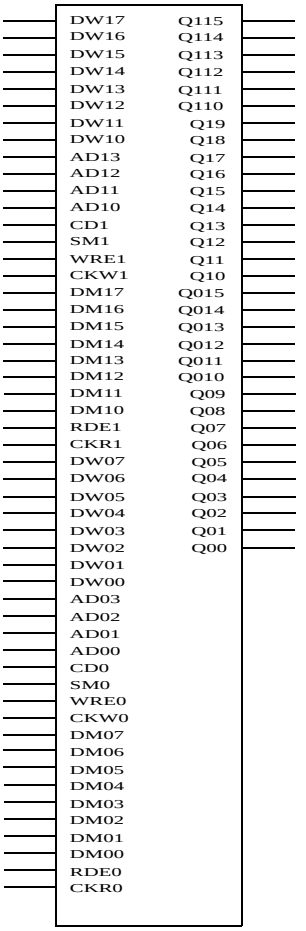
CAM2X256X16

2-256X16 Content Addressable Memory

Lattice FPGA		
2	3	4
		✓



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INPUTS: DW17, DW16, DW15, DW14, DW13, DW12, DW11, DW10, AD13, AD12, AD11, AD10, CD1, SM1, WRE1, CKW1, DM17, DM16, DM15, DM14, DM13, DM12, DM11, DM10, RDE1, CKR1, DW07, DW06, DW05, DW04, DW03, DW02, DW01, DW00, AD03, AD02, AD01, AD00, CD0, SM0, WRE0, CKW0, DM07, DM06, DM05, DM04, DM03, DM02, DM01, DM00, RDE0, CKR0
OUTPUTS: Q115, Q114, Q113, Q112, Q111, Q110, Q19, Q18, Q17, Q16, Q15, Q14, Q13, Q12, Q11, Q10, Q015, Q014, Q013, Q012, Q011, Q010, Q09, Q08, Q07, Q06, Q05, Q04, Q03, Q02, Q01, Q00
PINORDER: DW17 DW16 DW15 DW14 DW13 DW12 DW11 DW10 AD13 AD12 AD11 AD10 CD1 SM1 WRE1 CKW1 DM17 DM16 DM15 DM14 DM13 DM12 DM11 DM10 RDE1 CKR1 DW07 DW06 DW05 DW04 DW03 DW02 DW01 DW00 AD03 AD02 AD01 AD00 CD0 SM0 WRE0 CKW0 DM07 DM06 DM05 DM04 DM03 DM02 DM01 DM00 RDE0 CKR0 Q115 Q114 Q113 Q112 Q111 Q110 Q19 Q18 Q17 Q16 Q15 Q14 Q13 Q12 Q11 Q10 Q015 Q014 Q013 Q012 Q011 Q010 Q09 Q08 Q07 Q06 Q05 Q04 Q03 Q02 Q01 Q00
MINIMUM CELL AREA (Series 2): 0.5
MINIMUM CELL AREA (Series 3 and Series 4): 0.25
ATTRIBUTES (Series 4 only)
CAMMODE0: NOREG, INREG, OUTREG, IOREG
CAMMODE1: NOREG, INREG, OUTREG, IOREG

Description:

The CAM block is a content addressable memory that provides for 16, 8 bit words. The CAM block consists of two ports, port-1 provides one CAM, and port-0 the other.

The CAM has three modes, *single match*, *multiple match*, and *clear*. These can be controlled through the user inputs. Single match overwrites any previous address location for this data word. If this is low, it will write a “1” into the location it belongs, but will not write the “0” bits of the decoded address. This will result in multiple “1”s on the output. This is a multiple match condition, meaning that the same data is at two or more locations. A logical 1of SM is a single match, and logical 0 is a multiple match. Clear Data (active-HIGH) is used to clear the CAM contents. Typically, all 256 locations would be cleared consecutively. .

Function	Pins
data match port-1 and 0	DM(1:0)[7:0]

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Function	Pins
data write port-1 and 0	DW(1:0)[7:0]
single match (Active-HIGH)	SM(1:0)
clear data (active-HIGH)	CD(1:0)
data write CAM address	AD1[0:3] AD0[0:3]
read chip select (active-HIGH)	RDE1, RDE0
write chip select (active-HIGH)	WRE1, WRE0

The 8-bit data is applied to the address signals and the address is applied to the data inputs. Internally, the CAM address (physical data pins) [3:0] are decoded to 1 of 16. 0000(0) results in 0000000000000001, 0010(2) results in 0000000000000100. This decoded address is stored in the RAM and is generated when a data match is placed on the DM(1:0)[7:0] inputs. The user must encode the address or combine it with other CAM blocks to generate the final output.

In a multiple match mode, there may be multiple “1”s in the output. This means that more than one memory address contains the same data. It is left to the user to decide how to encode this and determine which address to use. For example, if the results of a match are 0100000000000100, there is a match at location 0010(2) and 1110 (14).

RDE Read chip select (active-HIGH) enables for CAM data match when enabled read port registers are used. Note that port-0 is used for CAM0 and port-1 for CAM1.

> ***Note*****:** The CAM2X256X16 element should be instantiated using Module/IP Manager to create a SCUBA module. Refer to the appropriate topic in the Module/IP Manager online help system for details.

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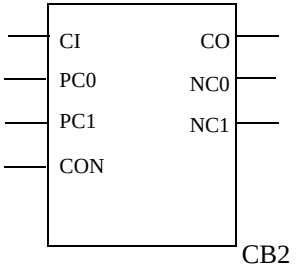
CB2

Combinational Logic for 2-Bit Bidirectional Counter using Look-Up Table

Lattice FPGA		
SC	XP	EC
	✓	✓



INPUTS: CI,PC0,PC1,CON
OUTPUTS: CO,NC0,NC1,
PINORDER: CI PC0 PC1 CON CO NC0 NC1

Description:

This macro realizes the combinational logic needed to implement a 2-bit bidirectional counter by using ripple elements. See CB4 element for functionality.

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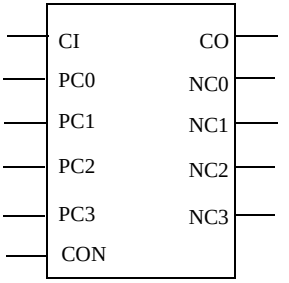
CB4

Combinational Logic for 4-Bit Bidirectional Counter using Look-Up Table

ORCA Series		
2	3	4
✓	✓	✓



CB4

INPUTS: CI,PC0,PC1,PC2,PC3,CON
OUTPUTS: CO,NC0,NC1,NC2,NC3
PINORDER: CI PC0 PC1 PC2 PC3 CON CO NC0 NC1 NC2 NC3
MINIMUM CELL AREA (Series 2): 0.5
MINIMUM CELL AREA (Series 3 and Series 4): 0.125

Description:

This macro realizes the combinational logic needed to implement a 4-bit bidirectional counter by using ripple elements.

When CON=0 and CI=0, NC[0:3]=PC[0:3]-1, and CO=0 if PC[0:3]=0000
When CON=0 and CI=1, NC[0:3]=PC[0:3] and CO=1
When CON=1 and CI=0, NC[0:3]=PC[0:3] and CO=0
When CON=1 and CI=1, NC[0:3]=PC[0:3]+1, and CO=1 if PC[0:3]=1111

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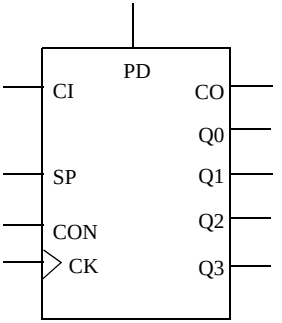
CB4P3BX

4 Bit Positive Edge Triggered Bidirectional Counter with Positive Clock Enable and Positive Asynchronous Preset

ORCA Series		
2	3	4
✓	✓	✓



CB4P3BX

INPUTS: CI,SP,CK,PD,CON
OUTPUTS: CO,Q0,Q1,Q2,Q3
PINORDER: CI SP CK PD CON CO Q0 Q1 Q2 Q3
MINIMUM CELL AREA (Series 2): 1.0
MINIMUM CELL AREA (Series 3 and Series 4): 0.25

Note: When CON = 0, CI and CO are active LOW

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Truth Table:

INPUTS					OUTPUTS	
CI	SP	CON	CK	PD	CO	Q[0:3]
0	X	1	X	1	0	1
1	X	1	X	1	1	1
0	X	1	X	0	0	Q[0:3]
1	0	1	X	0	*	Q[0:3]
1	1	1	↑	0	*	count+1
X	X	0	X	1	1	1
1	X	0	X	0	1	Q[0:3]
0	0	0	X	0	**	Q[0:3]
0	1	0	↑	0	**	count-1

X = Don’t care
* When Q[0:3] is 1111, CO will be 1; otherwise, CO will be 0
** When Q[0:3] is 0000, CO will be 0; otherwise, CO will be 1
When GSR=0, Q[0:3]=1 (SP=CK=PD=X)

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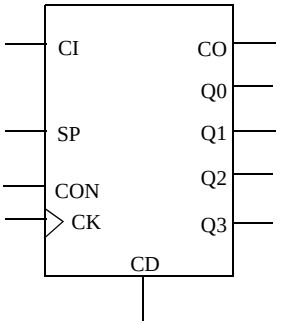
CB4P3DX

4 Bit Positive Edge Triggered Bidirectional Counter with Positive Clock Enable and Positive Asynchronous Clea

ORCA Series		
2	3	4
✓	✓	✓



CB4P3DX

INPUTS: CI,SP,CK,CD,CON
OUTPUTS: CO,Q0,Q1,Q2,Q3
PINORDER: CI SP CK CD CON CO Q0 Q1 Q2 Q3
MINIMUM CELL AREA (Series 2): 1.0
MINIMUM CELL AREA (Series 3 and Series 4): 0.25

Note: When CON = 0, CI and CO are active LOW

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Truth Table:

INPUTS					OUTPUTS	
CI	SP	CON	CK	CD	CO	Q[0:3]
X	X	1	X	1	0	0
0	X	1	X	0	0	Q[0:3]
1	0	1	X	0	*	Q[0:3]
1	1	1	↑	0	*	count+1
0	X	0	X	1	0	0
1	X	0	X	1	1	0
1	X	0	X	0	1	Q[0:3]
0	0	0	X	0	**	Q[0:3]
0	1	0	↑	0	**	count-1

X = Don’t care
* When Q[0:3] is 1111, CO will be 1; otherwise, CO will be 0
** When Q[0:3] is 0000, CO will be 0; otherwise, CO will be 1
When GSR=0, Q[0:3]=0 (SP=CK=CD=X)

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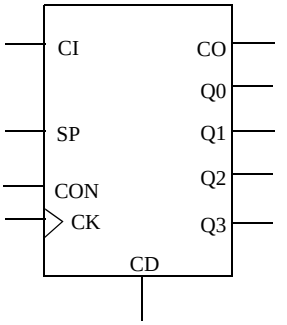
CB4P3IX

4 Bit Positive Edge Triggered Bidirectional Counter with Positive Clock Enable and Positive Synchronous Clear

ORCA Series		
2	3	4
✓	✓	✓



CB4P3IX

INPUTS: CI,SP,CK,CD,CON
OUTPUTS: CO,Q0,Q1,Q2,Q3
PINORDER: CI SP CK CD CON CO Q0 Q1 Q2 Q3
MINIMUM CELL AREA (Series 2): 1.0
MINIMUM CELL AREA (Series 3 and Series 4): 0.25

Note: When CON = 0, CI and CO are active LOW

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Truth Table:

INPUTS					OUTPUTS	
CI	SP	CON	CK	CD	CO	Q[0:3]
X	1	1	↑	1	0	0
0	0	1	X	X	0	Q[0:3]
0	X	1	X	0	0	Q[0:3]
1	0	1	X	X	*	Q[0:3]
1	1	1	↑	0	*	count+1
0	1	0	↑	1	0	0
1	1	0	↑	1	1	0
1	0	0	X	X	1	Q[0:3]
1	X	0	X	0	1	Q[0:3]
0	0	0	X	X	**	Q[0:3]
0	1	0	↑	0	**	count-1

X = Don’t care
* When Q[0:3] is 1111, CO will be 1; otherwise, CO will be 0
** When Q[0:3] is 0000, CO will be 0; otherwise, CO will be 1
When GSR=0, Q[0:3]=0 (SP=CK=CD=X)

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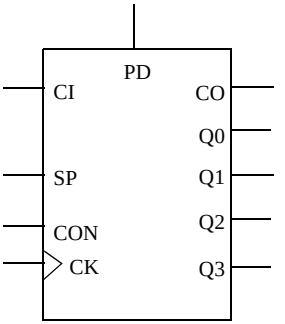
CB4P3JX

4 Bit Positive Edge Triggered Bidirectional Counter with Positive Clock Enable and Positive Synchronous Preset

ORCA Series		
2	3	4
✓	✓	✓



CB4P3JX

INPUTS: CI,SP,CK,PD,CON
OUTPUTS: CO,Q0,Q1,Q2,Q3
PINORDER: CI SP CK PD CON CO Q0 Q1 Q2 Q3
MINIMUM CELL AREA (Series 2): 1.0
MINIMUM CELL AREA (Series 3 and Series 4): 0.25

Note: When CON = 0, CI and CO are active LOW

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Truth Table:

INPUTS					OUTPUTS	
CI	SP	CON	CK	PD	CO	Q[0:3]
0	1	1	↑	1	0	1
1	1	1	↑	1	1	1
0	0	1	X	X	0	Q[0:3]
0	X	1	X	0	0	Q[0:3]
1	0	1	X	X	*	Q[0:3]
1	1	1	↑	0	*	count+1
X	1	0	↑	1	1	1
1	0	0	X	X	1	Q[0:3]
1	X	0	X	0	1	Q[0:3]
0	0	0	X	X	**	Q[0:3]
0	1	0	↑	0	**	count-1

X = Don’t care
* When Q[0:3] is 1111, CO will be 1; otherwise, CO will be 0
** When Q[0:3] is 0000, CO will be 0; otherwise, CO will be 1
When GSR=0, Q[0:3]=1 (SP=CK=PD=X)

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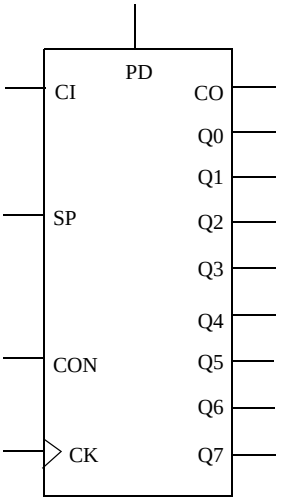
CB8P3BX

8 Bit Positive Edge Triggered Bidirectional Counter with Positive Clock Enable and Positive Asynchronous Preset

ORCA Series		
2	3	4
	✓	✓



CB8P3BX

INPUTS: CI,SP,CK,PD,CON
OUTPUTS: CO,Q0,Q1,Q2,Q3,Q4,Q5,Q6,Q7
PINORDER: CI SP CK PD CON CO Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
MINIMUM CELL AREA: 0.5

Note: When CON = 0, CI and CO are active LOW

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Truth Table:

INPUTS					OUTPUTS	
CI	SP	CON	CK	PD	CO	Q[0:7]
0	X	1	X	1	0	1
1	X	1	X	1	1	1
0	X	1	X	0	0	Q[0:7]
1	0	1	X	0	*	Q[0:7]
1	1	1	↑	0	*	count+1
X	X	0	X	1	1	1
1	X	0	X	0	1	Q[0:7]
0	0	0	X	0	**	Q[0:7]
0	1	0	↑	0	**	count-1

X = Don’t care
* When Q[0:7] is 11111111, CO will be 1; otherwise, CO will be 0
** When Q[0:7] is 00000000, CO will be 0; otherwise, CO will be 1
When GSR=0, Q[0:7]=1 (SP=CK=PD=X)

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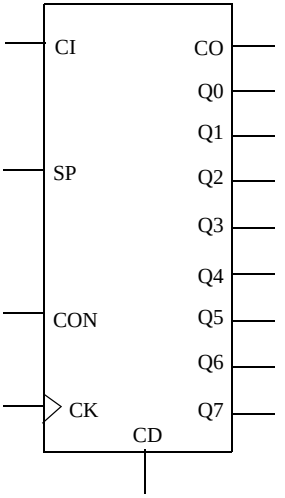
CB8P3DX

8 Bit Positive Edge Triggered Bidirectional Counter with Positive Clock Enable and Positive Asynchronous Clear

ORCA Series		
2	3	4
	✓	✓



CB8P3DX

INPUTS: CI,SP,CK,CD,CON
OUTPUTS: CO,Q0,Q1,Q2,Q3,Q4,Q5,Q6,Q7
PINORDER: CI SP CK CD CON CO Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
MINIMUM CELL AREA: 0.5

Note: When CON = 0, CI and CO are active LOW

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Truth Table:

INPUTS					OUTPUTS	
CI	SP	CON	CK	CD	CO	Q[0:7]
X	X	1	X	1	0	0
0	X	1	X	0	0	Q[0:7]
1	0	1	X	0	*	Q[0:7]
1	1	1	↑	0	*	count+1
0	X	0	X	1	0	0
1	X	0	X	1	1	0
1	X	0	X	0	1	Q[0:7]
0	0	0	X	0	**	Q[0:7]
0	1	0	↑	0	**	count-1

X = Don’t care
* When Q[0:7] is 11111111, CO will be 1; otherwise, CO will be 0
** When Q[0:7] is 00000000, CO will be 0; otherwise, CO will be 1
When GSR=0, Q[0:7]=0 (SP=CK=CD=X)

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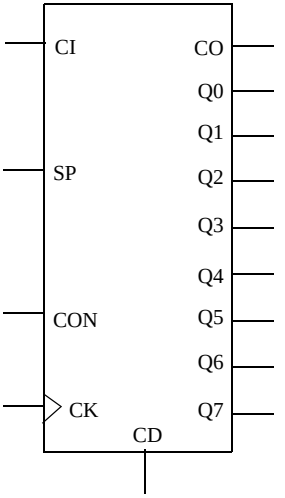
CB8P3IX

8 Bit Positive Edge Triggered Bidirectional Counter with Positive Clock Enable and Positive Synchronous Clear

ORCA Series		
2	3	4
	✓	✓



CB8P3IX

INPUTS: CI,SP,CK,CD,CON
OUTPUTS: CO,Q0,Q1,Q2,Q3,Q4,Q5,Q6,Q7
PINORDER: CI SP CK CD CON CO Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
MINIMUM CELL AREA: 0.5

Note: When CON = 0, CI and CO are active LOW

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Truth Table:

INPUTS					OUTPUTS	
CI	SP	CON	CK	CD	CO	Q[0:7]
X	1	1	↑	1	0	0
0	0	1	X	X	0	Q[0:7]
0	X	1	X	0	0	Q[0:7]
1	0	1	X	X	*	Q[0:7]
1	1	1	↑	0	*	count+1
0	1	0	↑	1	0	0
1	1	0	↑	1	1	0
1	0	0	X	X	1	Q[0:7]
1	X	0	X	0	1	Q[0:7]
0	0	0	X	X	**	Q[0:7]
0	1	0	↑	0	**	count-1

X = Don’t care
* When Q[0:7] is 11111111, CO will be 1; otherwise, CO will be 0
** When Q[0:7] is 00000000, CO will be 0; otherwise, CO will be 1
When GSR=0, Q[0:7]=0 (SP=CK=CD=X)

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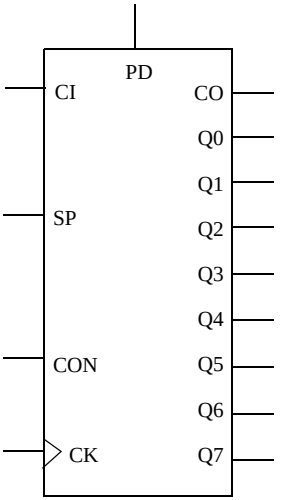
CB8P3JX

8 Bit Positive Edge Triggered Bidirectional Counter with Positive Clock Enable and Positive Synchronous Preset

ORCA Series		
2	3	4
	✓	✓



CB8P3JX

INPUTS: CI,SP,CK,PD,CON
OUTPUTS: CO,Q0,Q1,Q2,Q3,Q4,Q5,Q6,Q7
PINORDER: CI SP CK PD CON CO Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
MINIMUM CELL AREA: 0.5

Note: When CON = 0, CI and CO are active LOW

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Truth Table:

INPUTS					OUTPUTS	
CI	SP	CON	CK	PD	CO	Q[0:7]
0	1	1	↑	1	0	1
1	1	1	↑	1	1	1
0	0	1	X	X	0	Q[0:7]
0	X	1	X	0	0	Q[0:7]
1	0	1	X	X	*	Q[0:7]
1	1	1	↑	0	*	count+1
X	1	0	↑	1	1	1
1	0	0	X	X	1	Q[0:7]
1	X	0	X	0	1	Q[0:7]
0	0	0	X	X	**	Q[0:7]
0	1	0	↑	0	**	count-1

X = Don’t care
* When Q[0:7] is 11111111, CO will be 1; otherwise, CO will be 0
** When Q[0:7] is 00000000, CO will be 0; otherwise, CO will be 1
When GSR=0, Q[0:7]=1 (SP=CK=PD=X)

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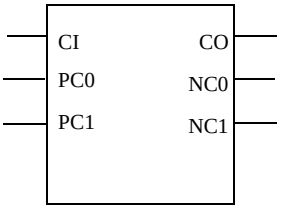
CD2

Combinational Logic for 2-Bit Down-Counter using Look-Up Table

Lattice FPGA		
SC	XP	EC
✓	✓	✓



CD2

INPUTS: CI, PC0, PC1
OUTPUTS: CO, NC0, NC1
PINORDER: CI, PC0, PC1, CO, NC0, NC1
CELL AREA: One Slice

Description:

This macro realizes the combinational logic needed to implement a 2-bit down-counter by using the look-up tables (LUTs).

When CI=0, NC[0:1]=PC[0:1]-1, and CO=0 if PC[0:1]=00
When CI=1, NC[0:1]=PC[0:1] and CO=1

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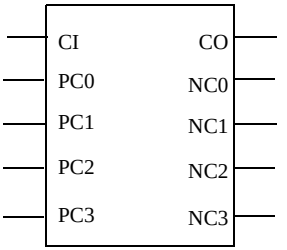
CD4

Combinational Logic for 4-Bit Down-Counter using Look-Up Table

ORCA Series/Lattice FPGA				
2	3	4	XP	EC
✓	✓	✓	✓	✓



CD4

INPUTS: CI,PC0,PC1,PC2,PC3
OUTPUTS: CO,NC0,NC1,NC2,NC3
PINORDER: CI PC0 PC1 PC2 PC3 CO NC0 NC1 NC2 NC3
MINIMUM CELL AREA (Series 2): 0.5
MINIMUM CELL AREA (Series 3 and Series 4): 0.125

Description:

This macro realizes the combinational logic needed to implement a 4-bit down-counter by using ripple elements.

When CI=0, NC[0:3]=PC[0:3]-1, and CO=0 if PC[0:3]=0000
When CI=1, NC[0:3]=PC[0:3] and CO=1

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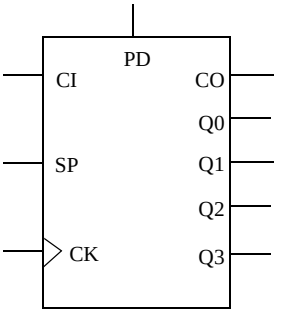
CD4P3BX

4 Bit Positive Edge Triggered Fast Down-Counter with Positive Clock Enable and Positive Asynchronous Preset

ORCA Series/Lattice FPGA				
2	3	4	XP	EC
✓	✓	✓	✓	✓



CD4P3BX

INPUTS: CI,SP,CK,PD
OUTPUTS: CO,Q0,Q1,Q2,Q3
PINORDER: CI SP CK PD CO Q0 Q1 Q2 Q3
MINIMUM CELL AREA (Series 2): 1.0
MINIMUM CELL AREA (Series 3 and Series 4): 0.25
Note: CI and CO are active LOW

Truth Table:

INPUTS				OUTPUTS	
CI	SP	CK	PD	CO	Q[0:3]
X	X	X	1	1	1
1	X	X	0	1	Q[0:3]
0	0	X	0	*	Q[0:3]
0	1	↑	0	*	count-1

X = Don't care
* When Q[0:3] is 0000, CO will be 0; otherwise, CO will be 1
When GSR=0, Q[0:3]=1 (SP=CK=PD=X)

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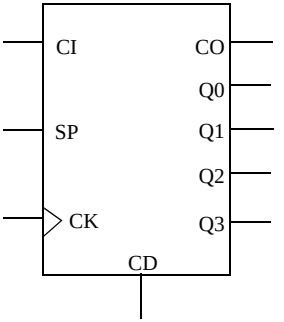
CD4P3DX

4 Bit Positive Edge Triggered Fast Down-Counter with Positive Clock Enable and Positive Asynchronous Clear

ORCA Series/Lattice FPGA				
2	3	4	XP	EC
✓	✓	✓	✓	✓



CD4P3DX

INPUTS: CI,SP,CK,CD
OUTPUTS: CO,Q0,Q1,Q2,Q3
PINORDER: CI SP CK CD CO Q0 Q1 Q2 Q3
MINIMUM CELL AREA (Series 2): 1.0
MINIMUM CELL AREA (Series 3 and Series 4): 0.25

Note: CI and CO are active LOW

Truth Table:

INPUTS				OUTPUTS	
CI	SP	CK	CD	CO	Q[0:3]
0	X	X	1	0	0
1	X	X	1	1	0
1	X	X	0	1	Q[0:3]
0	0	X	0	*	Q[0:3]
0	1	↑	0	*	count-1

X = Don't care
* When Q[0:3] is 0000, CO will be 0; otherwise, CO will be 1
When GSR=0, Q[0:3]=0 (SP=CK=CD=X)

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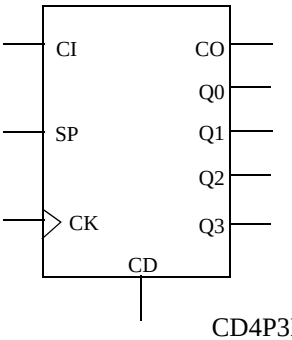
CD4P3IX

4 Bit Positive Edge Triggered Fast Down-Counter with Positive Clock Enable and Positive Synchronous Clear

ORCA Series/Lattice FPGA				
2	3	4	XP	EC
✓	✓	✓	✓	✓



CD4P3IX

INPUTS: CI,SP,CK,CD
OUTPUTS: CO,Q0,Q1,Q2,Q3
PINORDER: CI SP CK CD CO Q0 Q1 Q2 Q3
MINIMUM CELL AREA (Series 2): 1.0
MINIMUM CELL AREA (Series 3 and Series 4): 0.25
Note: CI and CO are active LOW

Truth Table:

INPUTS				OUTPUTS	
CI	SP	CK	CD	CO	Q[0:3]
0	1	↑	1	0	0
1	1	↑	1	1	0
1	0	X	X	1	Q[0:3]
1	X	X	0	1	Q[0:3]
0	0	X	X	*	Q[0:3]
0	1	↑	0	*	count-1

X = Don't care
* When Q[0:3] is 0000, CO will be 0; otherwise, CO will be 1
When GSR=0, Q[0:3]=0 (SP=CK=CD=X)

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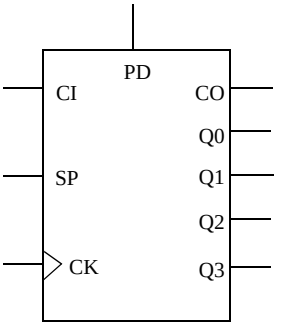
CD4P3JX

4 Bit Positive Edge Triggered Fast Down-Counter with Positive Clock Enable and Positive Synchronous Preset

ORCA Series/Lattice FPGA				
2	3	4	XP	EC
✓	✓	✓	✓	✓



CD4P3JX

INPUTS: CI,SP,CK,PD
OUTPUTS: CO,Q0,Q1,Q2,Q3
PINORDER: CI SP CK PD CO Q0 Q1 Q2 Q3
MINIMUM CELL AREA (Series 2): 1.0
MINIMUM CELL AREA (Series 3 and Series 4): 0.25
Note: CI and CO are active LOW

Truth Table:

INPUTS				OUTPUTS	
CI	SP	CK	PD	CO	Q[0:3]
X	1	↑	1	1	1
1	0	X	X	1	Q[0:3]
1	X	X	0	1	Q[0:3]
0	0	X	X	*	Q[0:3]
0	1	↑	0	*	count-1

X = Don’t care
* When Q[0:3] is 0000, CO will be 0; otherwise, CO will be 1
When GSR=0, Q[0:3]=1 (SP=CK=PD=X)

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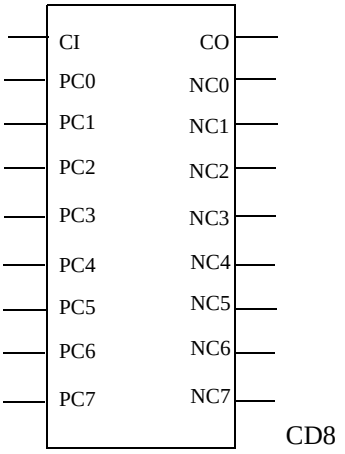
CD8

Combinational Logic for 4-Bit Down-Counter using Look-Up Table

Lattice FPGA		
SC	XP	EC
	✓	✓



INPUTS: CI,PC0,PC1,PC2,PC3, PC4, PC5, PC6, PC7
OUTPUTS: CO,NC0,NC1,NC2,NC3, NC4, NC5, NC6, NC7
PINORDER: CI,PC0,PC1,PC2,PC3, PC4, PC5, PC6, PC7, CO,NC0,NC1,NC2,NC3, NC4, NC5, NC6, NC7

Description:

This macro realizes the combinational logic needed to implement a 8-bit down-counter by using ripple elements. See CD4 for functionality.

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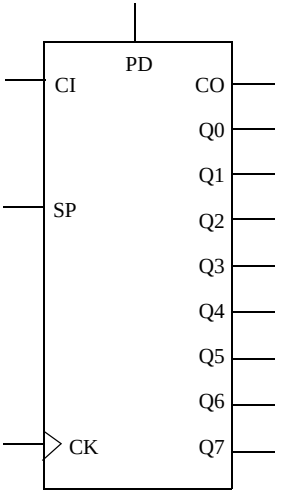
CD8P3BX

8 Bit Positive Edge Triggered Fast Down-Counter with Positive Clock Enable and Positive Asynchronous Preset

ORCA Series/Lattice			
3	4	XP	EC
✓	✓	✓	✓



CD8P3BX

INPUTS: CI,SP,CK,PD
OUTPUTS: CO,Q0,Q1,Q2,Q3,Q4,Q5,Q6,Q7
PINORDER: CI SP CK PD CO Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
MINIMUM CELL AREA: 0.5

Note: CI and CO are active LOW

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Truth Table:

INPUTS				OUTPUTS	
CI	SP	CK	PD	CO	Q[0:7]
X	X	X	1	1	1
1	X	X	0	1	Q[0:7]
0	0	X	0	*	Q[0:7]
0	1	↑	0	*	count-1

X = Don’t care

* When Q[0:7] is 00000000, CO will be 0; otherwise, CO will be 1
When GSR=0, Q[0:7]=1 (SP=CK=PD=X)

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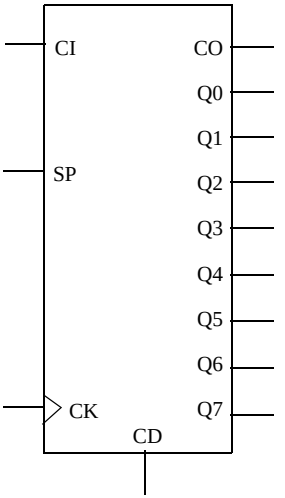
CD8P3DX

8 Bit Positive Edge Triggered Fast Down-Counter with Positive Clock Enable and Positive Asynchronous Clear

ORCA Series/Lattice			
3	4	XP	EC
✓	✓	✓	✓



CD8P3DX

INPUTS: CI,SP,CK,CD
OUTPUTS: CO,Q0,Q1,Q2,Q3,Q4,Q5,Q6,Q7
PINORDER: CI SP CK CD CO Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
MINIMUM CELL AREA: 0.5

Note: CI and CO are active LOW

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Truth Table:

INPUTS				OUTPUTS	
CI	SP	CK	CD	CO	Q[0:7]
0	X	X	1	0	0
1	X	X	1	1	0
1	X	X	0	1	Q[0:7]
0	0	X	0	*	Q[0:7]
0	1	↑	0	*	count-1

X = Don’t care

* When Q[0:7] is 00000000, CO will be 0; otherwise, CO will be 1
When GSR=0, Q[0:7]=0 (SP=CK=CD=X)

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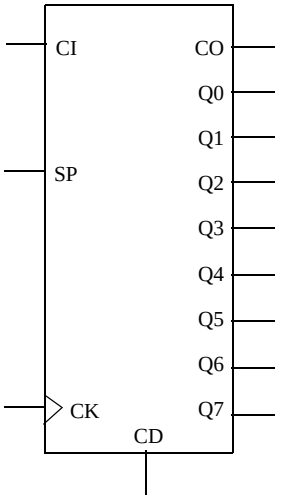
CD8P3IX

8 Bit Positive Edge Triggered Fast Down-Counter with Positive Clock Enable and Positive Synchronous Clear

ORCA Series/Lattice			
3	4	XP	EC
✓	✓	✓	✓



CD8P3IX

INPUTS: CI,SP,CK,CD
OUTPUTS: CO,Q0,Q1,Q2,Q3,Q4,Q5,Q6,Q7
PINORDER: CI SP CK CD CO Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
MINIMUM CELL AREA: 0.5

Note: CI and CO are active LOW

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Truth Table:

INPUTS				OUTPUTS	
CI	SP	CK	CD	CO	Q[0:7]
0	1	↑	1	0	0
1	1	↑	1	1	0
1	0	X	X	1	Q[0:7]
1	X	X	0	1	Q[0:7]
0	0	X	X	*	Q[0:7]
0	1	↑	0	*	count-1

X = Don’t care

* When Q[0:7] is 00000000, CO will be 0; otherwise, CO will be 1
When GSR=0, Q[0:7]=0 (SP=CK=CD=X)

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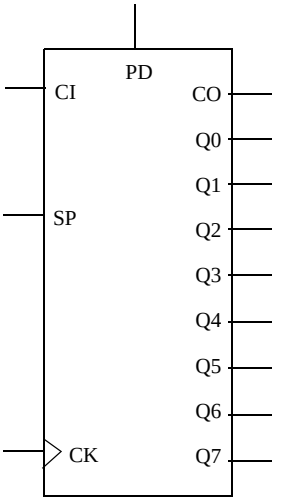
CD8P3JX

8 Bit Positive Edge Triggered Fast Down-Counter with Positive Clock Enable and Positive Synchronous Preset

ORCA Series/Lattice			
3	4	XP	EC
✓	✓	✓	✓



CD8P3JX

INPUTS: CI,SP,CK,PD
OUTPUTS: CO,Q0,Q1,Q2,Q3,Q4,Q5,Q6,Q7
PINORDER: CI SP CK PD CO Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
MINIMUM CELL AREA: 0.5

Note: CI and CO are active LOW

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Truth Table:

INPUTS				OUTPUTS	
CI	SP	CK	PD	CO	Q[0:7]
X	1	↑	1	1	1
1	0	X	X	1	Q[0:7]
1	X	X	0	1	Q[0:7]
0	0	X	X	*	Q[0:7]
0	1	↑	0	*	count-1

X = Don’t care

* When Q[0:7] is 00000000, CO will be 0; otherwise, CO will be 1
When GSR=0, Q[0:7]=1 (SP=CK=PD=X)

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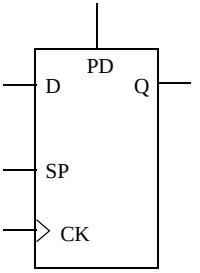
CFD1P3BX

Positive Edge Triggered D Flip-Flop with Positive Level Enable and Positive Level Asynchronous Preset (used as 9th flip-flop in the PLC only)

ORCA Series			
2	3	4	5
	✓	✓	



CFD1P3BX

INPUTS: D,SP,CK,PD
OUTPUTS: Q
PINORDER: D SP CK PD Q
MINIMUM CELL AREA: 0.0625

Truth Table:

INPUTS				OUTPUTS
D	SP	CK	PD	Q
X	0	X	0	Q
X	X	X	1	1
0	1	↑	0	0
1	1	↑	0	1

X = Don’t care
When GSR=0, Q=1 (D=SP=CK=PD=X)

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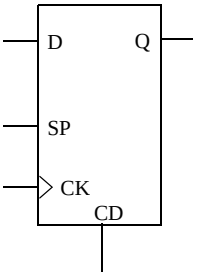
CFD1P3DX

Positive Edge Triggered D Flip-Flop with Positive Level Enable and Positive Level Asynchronous Clear (used as 9th flip-flop in the PLC only)

ORCA Series		
2	3	4
	✓	✓



CFD1P3DX

INPUTS: D,SP,CK,CD
OUTPUTS: Q
PINORDER: D SP CK CD Q
MINIMUM CELL AREA: 0.0625

Truth Table:

INPUTS				OUTPUTS
D	SP	CK	CD	Q
X	0	X	0	Q
X	X	X	1	0
0	1	↑	0	0
1	1	↑	0	1

X = Don’t care
When GSR=0, Q=0 (D=SP=CK=CD=X)

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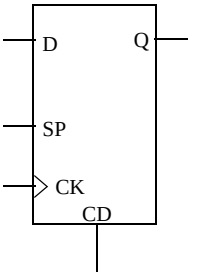
CFD1P3IX

Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Clear and Positive Level Enable (Clear overrides Enable) (used as 9th flip-flop in the PLC only)

ORCA Series		
2	3	4
	✓	✓



CFD1P3IX

INPUTS: D,SP,CK,CD
OUTPUTS: Q
PINORDER: D SP CK CD Q
MINIMUM CELL AREA: 0.0625

Truth Table:

INPUTS				OUTPUTS
D	SP	CK	CD	Q
X	0	X	0	Q
X	X	↑	1	0
0	1	↑	0	0
1	1	↑	0	1

X = Don’t care
When GSR=0, Q=0 (D=SP=CK=CD=X)

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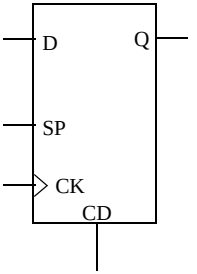
CFD1P3IZ

Positive Edge Triggered D Flip-Flop with Positive Level Enable and Positive Level Synchronous Clear (used as 9th flip-flop in the PLC only)

ORCA Series		
2	3	4
	✓	✓



CFD1P3IZ

INPUTS: D,SP,CK,CD
OUTPUTS: Q
PINORDER: D SP CK CD Q
MINIMUM CELL AREA: 0.0625

Truth Table:

INPUTS				OUTPUTS
D	SP	CK	CD	Q
X	0	X	X	Q
X	1	↑	1	0
0	1	↑	0	0
1	1	↑	0	1

X = Don’t care
When GSR=0, Q=0 (D=SP=CK=CD=X)

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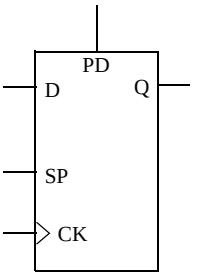
CFD1P3JX

Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Preset and Positive Level Enable (Preset overrides Enable) (used as 9th flip-flop in the PLC only)

ORCA Series		
2	3	4
	✓	✓



CFD1P3JX

INPUTS: D,SP,CK,PD
OUTPUTS: Q
PINORDER: D SP CK PD Q
MINIMUM CELL AREA: 0.0625

Truth Table:

INPUTS				OUTPUTS
D	SP	CK	PD	Q
X	0	X	0	Q
X	X	↑	1	1
0	1	↑	0	0
1	1	↑	0	1

X = Don’t care
When GSR=0, Q=1 (D=SP=CK=PD=X)

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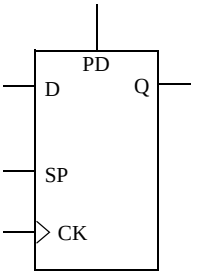
CFD1P3JZ

Positive Edge Triggered D Flip-Flop with Positive Level Enable and Positive Level Synchronous Preset (used as 9th flip-flop in the PLC only)

ORCA Series		
2	3	4
	✓	✓



CFD1P3JZ

INPUTS: D,SP,CK,PD
OUTPUTS: Q
PINORDER: D SP CK PD Q
MINIMUM CELL AREA: 0.0625

Truth Table:

INPUTS				OUTPUTS
D	SP	CK	PD	Q
X	0	X	X	Q
X	1	↑	1	1
0	1	↑	0	0
1	1	↑	0	1

X = Don’t care
When GSR=0, Q=1 (D=SP=CK=PD=X)

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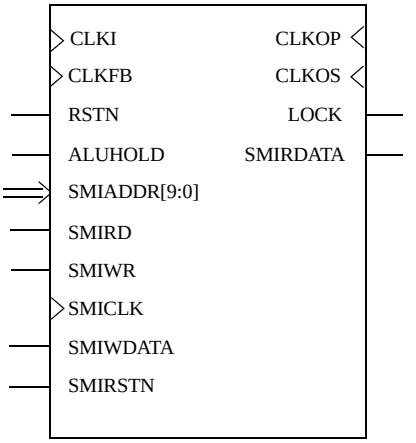
CIDDLLA

Clock Injection Delay Removal

Lattice FPGA		
SC	XP	EC
✓		



CIDDLLA

NOTE: The graphic is shown in bus notation for convenience. This element must be instantiated in expanded bus notation format with each individual bit as given below

INPUTS: CLKI, CLKFB, RSTN, ALUHOLD, SMIADDR9, SMIADDR8, SMIADDR7, SMIADDR6, SMIADDR5, SMIADDR4, SMIADDR3, SMIADDR2, SMIADDR1, SMIADDR0, SMIRD, SMIWR, SMICLK, SMIWDATA, SMIRSTN
OUTPUTS: CLKOP, CLKOS, LOCK, SMIRDATA
PINORDER: CLKI, CLKFB, RSTN, ALUHOLD, SMIADDR9, SMIADDR8, SMIADDR7, SMIADDR6, SMIADDR5, SMIADDR4, SMIADDR3, SMIADDR2, SMIADDR1, SMIADDR0, SMIRD, SMIWR, SMICLK, SMIWDATA, SMIRSTN, CLKOP, CLKOS, LOCK, SMIRDATA
CELL AREA: One Slice
ATTRIBUTES:
CLKI_PDEL: "DEL0", "DEL1", "DEL2", "DEL3"
CLKFB_PDEL: "DEL0", "DEL1", "DEL2", "DEL3"
CLKOS_FPHASE: "0", "11.25", "22.5", "45"
CLKOS_DIV: 1, 2, 4,
DISABLED_GSR: 0, 1
PHASELOCK: DISABLED, ENABLED
ALU_LOCK_CNT: 3, 4, ... 15
ALU_UNLOCK_CNT: 3, 4, ... 15
GLITCH_TOLERANCE: 0, 1, ... 7
ALU_INIT_CNTVAL: 0, 4, 8, 12, 16, 32, 48, 64, 72
SMI_ID: 000000, 000001, ... 111111
ADDR_DIS: 0000000000, 0000000001, ... 1111111111

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Description:

CIDLLA removes the clock tree delay, aligning the external feedback clock to the reference clock. It has a single output coming from the fourth delay block. It features include clock tree insertion removal, N*Tcyc=4*Tdel + Tinj, lock achieved starting from minimum delay, and when it goes through all delay stages, the minimum frequency is 1/(4*Tdel). Its requirements include external feedback only, that you must use all delay cells, a maximum frequency of 700MHz, and a minimum frequency of 100MHz.

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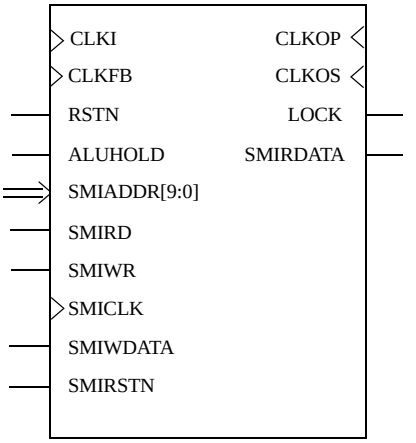
CIMDLLA

Clock Injection Match

Lattice FPGA		
SC	XP	EC
✓		



CIMDLLA

NOTE: The graphic is shown in bus notation for convenience. This element must be instantiated in expanded bus notation format with each individual bit as given below

INPUTS: CLKI, CLKFB, RSTN, ALUHOLD, UDDCNTL, SMIADDR9, SMIADDR8, SMIADDR7, SMIADDR6, SMIADDR5, SMIADDR4, SMIADDR3, SMIADDR2, SMIADDR1, SMIADDR0, SMIRD, SMIWR, SMICLK, SMIWDATA, SMIRSTN
OUTPUTS: CLKOP, CLKOS, LOCK, DCNTL0, DCNTL1, DCNTL2, DCNTL3, DCNTL4, DCNTL5, DCNTL6, DCNTL7, DCNTL8, SMIRDATA
PINORDER: CLKI, CLKFB, RSTN, ALUHOLD, UDDCNTL, SMIADDR9, SMIADDR8, SMIADDR7, SMIADDR6, SMIADDR5, SMIADDR4, SMIADDR3, SMIADDR2, SMIADDR1, SMIADDR0, SMIRD, SMIWR, SMICLK, SMIWDATA, SMIRSTN, CLKOP, CLKOS, LOCK, DCNTL0, DCNTL1, DCNTL2, DCNTL3, DCNTL4, DCNTL5, DCNTL6, DCNTL7, DCNTL8, SMIRDATA
CELL AREA: One Slice
ATTRIBUTES:
CLKI_PDEL: "DEL0", "DEL1", "DEL2", "DEL3"
CLKFB_PDEL: "DEL0", "DEL1", "DEL2", "DEL3"
CLKOS_FPHASE: "0", "11.25", "22.5", "45"
CLKOS_DIV: 1, 2, 4,
DISABLED_GSR: 0, 1
PHASELOCK: DISABLED, ENABLED
ALU_LOCK_CNT: 3, 4, ... 15
ALU_UNLOCK_CNT: 3, 4, ... 15
GLITCH_TOLERANCE : 0, 1, ... 7
DCNTL_ADJ: -127, -126, ..., -1, 0, 1, ..., 126, 127
SMI_ID: 000000, 000001, ... 111111
ADDR_DIS: 0000000000, 0000000001, ... 1111111111

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Description:

CIMDLLA matches the clock injection to one delay cell. This allows other inputs to take the registered ALU outputs and negate the clock injection delay. Its features include single clock output, lock achieved starting from minimum delay, output control bits, and allowance for +/- delay on these output control bits. Its requirements inlcude external feedback (CLKOP) only, a maximum frequency of 700MHz, a minimum frequency of100MHz, and a maximum delay compensation of 3.9ns.

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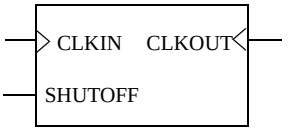
CLKCNTHB
CLKCNTHL
CLKCNTHR
CLKCNTHT

Clock Controller at Mid Site Used to Provide Ability to Shut Off the Clock in a high state.

ORCA Series		
2	3	4
	✓	



CLKCNTHB

INPUTS: CLKIN,SHUTOFF
OUTPUTS: CLKOUT
PINORDER: CLKIN SHUTOFF CLKOUT
MINIMUM CELL AREA: 0

Description:

Four clock controller cells are available at mid sites: Bottom (CLKCNTHB), Left (CLKCNTHL), Right (CLKCNTHR), and Top (CLKCNTHT). They are driven by dedicated PAD or the Programable Clock Manager (PCM). These cells drive the express clock (ECLK) along the PIO's and the center clock spine.

These cells must be instantiated when CLKIN is driven directly from an input buffer, or when a shutoff capability is desired. In all other cases the software will automatically include these cells.

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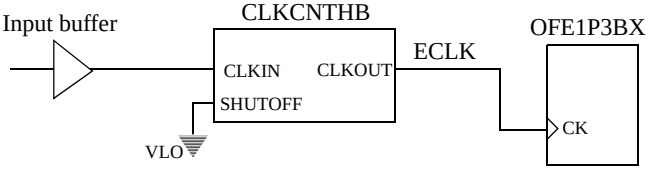
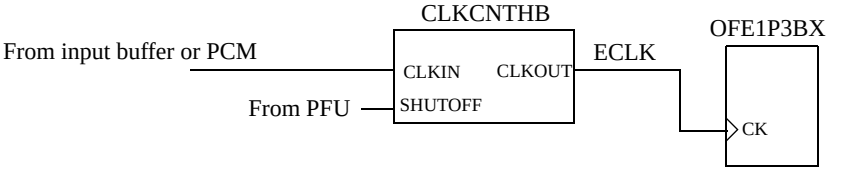
Use of CLKCNTH[B | L | R | T]

CLKCNTH circuits must be used in these situations:

(1) PIO elements using externally driven ECLK/SCLK



(2) SHUTOFF function is desired



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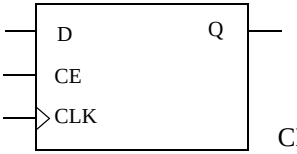
CLKCNTL

Clock Controller

Lattice FPGA		
SC	XP	EC
✓		



CLKCNTL

INPUTS: D, CE, CLK
OUTPUTS: Q
PINORDER: D, CE, CLK, Q
MINIMUM CELL AREA: 0

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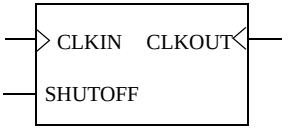
CLKCNTLB
CLKCNTLL
CLKCNTLR
CLKCNTLT

Clock Controller at Mid Site Used to Provide Ability to Shut Off the Clock

ORCA Series		
2	3	4
	✓	



CLKCNTLB

INPUTS: CLKIN,SHUTOFF
OUTPUTS: CLKOUT
PINORDER: CLKIN SHUTOFF CLKOUT
MINIMUM CELL AREA: 0

Description:

Four clock controller cells are available at mid sites: Bottom (CLKCNTLB), Left (CLKCNTLL), Right (CLKCNTLR), and Top (CLKCNTLT). They are driven by dedicated PAD or the Programable Clock Manager (PCM). These cells drive the express clock (ECLK) along the PIO's and the center clock spine.

These cells must be instantiated when CLKIN is driven directly from an input buffer, or when a shutoff capability is required. In all other cases the software will automatically include these cells.

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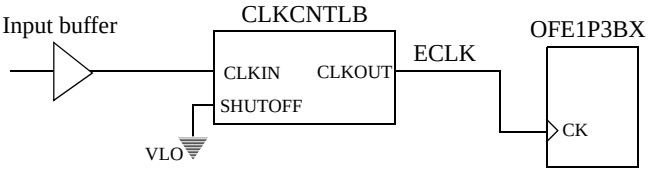
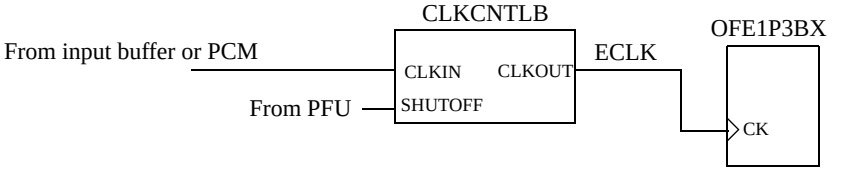
Use of CLKCNTL[B | L | R | T]

CLKCNTL circuits must be used in these situations:

(1) PIO elements using externally driven ECLK/SCLK



(2) SHUTOFF function is required



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CLKDET

Clock Detect

Lattice FPGA		
SC	XP	EC
✓		

CLKDET

INPUTS: CK, RST
OUTPUTS: Q
PINORDER: CK RST Q
MINIMUM CELL AREA: 0
ATTRIBUTES: CLKMODE: SCLK, ECLK

Truth Table:

INPUTS		OUTPUTS
CK	RST	Q
X	1	0
↑	0	1

X = Don’t care

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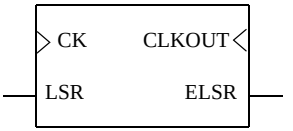
CLKDIV

Clock Divider

Lattice FPGA		
SC	XP	EC
✓		



CLKDIV

INPUTS: CK, LSR
OUTPUTS: CLKOUT, ELSR
PINORDER: CK, LS, CLKOUT, ELSR
MINIMUM CELL AREA: 0
ATTRIBUTES:
DIV: 1, 2, 4
DISABLED_GSR: 0, 1

Description:

Clock divider.

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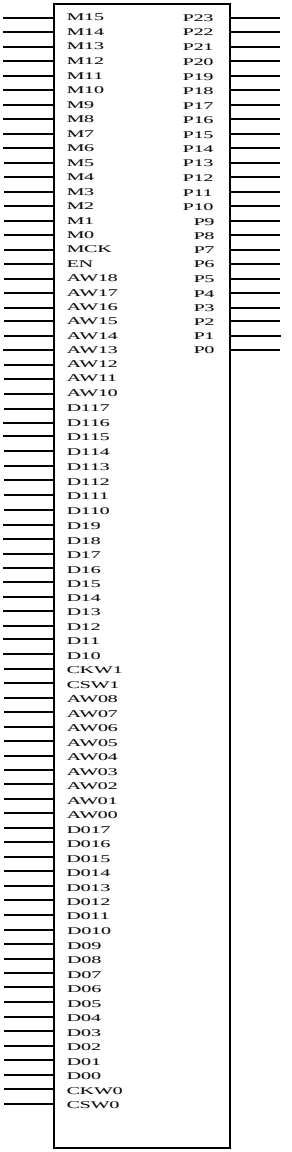
CMULT16

8 Bit or 16 Bit Constant Multiplier

ORCA Series		
2	3	4
		✓



CMULT16

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INPUTS: M15, M14, M13, M12, M11, M10, M9, M8, M7, M6, M5, M4, M3, M2, M1, M0, MCK, EN, AW18, AW17, AW16, AW15, AW14, AW13, AW12, AW11, AW10, D117, D116, D115, D114, D113, D112, D111, D110, D19, D18, D17, D16, D15, D14, D13, D12, D11, D10, CKW1, CSW1, AW08, AW07, AW06, AW05, AW04, AW03, AW02, AW01, AW00, D017, D016, D015, D014, D013, D012, D011, D010, D09, D08, D07, D06, D05, D04, D03, D02, D01, D00, CKW0, CSW0
OUTPUTS: P23, P22, P21, P20, P19, P18, P17, P16, P15, P14, P13, P12, P11, P10, P9, P8, P7, P6, P5, P4, P3, P2, P1, P0
PINORDER: M15 M14 M13 M12 M11 M10 M9 M8 M7 M6 M5 M4 M3 M2 M1 M0 MCK EN AW18 AW17 AW16 AW15 AW14 AW13 AW12 AW11 AW10 D117 D116 D115 D114 D113 D112 D111 D110 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 CKW1 CSW1 AW08 AW07 AW06 AW05 AW04 AW03 AW02 AW01 AW00 D017 D016 D015 D014 D013 D012 D011 D010 D09 D08 D07 D06 D05 D04 D03 D02 D01 D00 CKW0 CSW0 P23 P22 P21 P20 P19 P18 P17 P16 P15 P14 P13 P12 P11 P10 P9 P8 P7 P6 P5 P4 P3 P2 P1 P0
MINIMUM CELL AREA (Series 2): 0.5
MINIMUM CELL AREA (Series 3 and Series 4): 0.25
ATTRIBUTES (Series 4 only)
CMULTMODE: NOREG, INREG, OUTREG, IOREG

Description:

The constant multiplier provides a fixed 8-bit constant multiply of a 16-bit number or a fixed 16-bit constant multiply of an 8-bit number. The output will be 24 bit. Since the input and output can be registered, there are four configurations of the constant multiply mode.

Data can be written into the memory through initialization or through write address and data. When there is an 8-bit data input, the data will go into both buses (M[15:8] and M[7:0]). Both write ports are available during the multiplication mode so that the coefficients can be modified by user logic.

Function	Pins
data inputs	M[15:0]
address bits on write ports	AW(1:0)[8:0]
data inputs	D(1:0)[17:0]

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Function	Pins
write port clock (active HIGH)	CKW1, CKW0
read port clock (active HIGH)	CKR1, CKR0
write chip select (active HIGH)	CSW1, CSW0
read chip select (active HIGH)	CSR1, CSR0
output data	Q1[7:0], Q[15:0]

Note that initialization for CMULT16 is done through INITVALs. For CMULT16, there are 32 INITVAL properties, each will take 64 hex-characters, since it uses one 512X16 RAM.

For example :

INITVAL_00 = “0x012456789abcdef.....” //(64 hex-characters)
INITVAL_01 = “0x012456789abcdef.....” //(64 hex-characters)
.
.
.
INITVAL_1F = “0x012456789abcdef.....” //(64 hex-characters)

***Note*: ** The CMULT16 element should be instantiated using Module/IP Manager to create a SCUBA module. Refer to the appropriate topic in the Module/IP Manager online help system for details.

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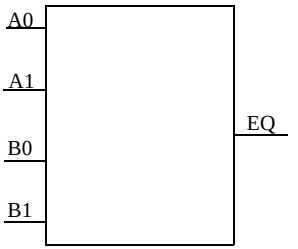
COMP

2 Bit Equality Comparator

ORCA Series		
2	3	4
✓		



COMP

INPUTS: A0,A1,B0,B1
OUTPUTS: EQ
PINORDER: A0 A1 B0 B1 EQ
MINIMUM CELL AREA: 0.125

Truth Table:

INPUTS				OUTPUTS
A0	A1	B0	B1	EQ
0	X	1	X	0
1	X	0	X	0
X	0	X	1	0
X	1	X	0	0
0	0	0	0	1
1	0	1	0	1
0	1	0	1	1
1	1	1	1	1

X = Don’t care

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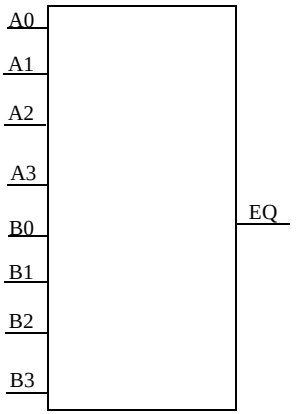
COMP4

4 Bit Equality Comparator

ORCA Series		
2	3	4
✓	✓	✓



COMP4

INPUTS: A0,A1,A2,A3,B0,B1,B2,B3
OUTPUTS: EQ
PINORDER: A0 A1 A2 A3 B0 B1 B2 B3 EQ
MINIMUM CELL AREA: 0.8

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Truth Table:

INPUTS								OUTPUTS
A0	A1	A2	A3	B0	B1	B2	B3	EQ
0	X	X	X	1	X	X	X	0
1	X	X	X	0	X	X	X	0
X	0	X	X	X	1	X	X	0
X	1	X	X	X	0	X	X	0
X	X	0	X	X	X	1	X	0
X	X	1	X	X	X	0	X	0
X	X	X	0	X	X	X	1	0
X	X	X	1	X	X	X	0	0
0	0	0	0	0	0	0	0	1
1	0	0	0	1	0	0	0	1
0	1	0	0	0	1	0	0	1
1	1	0	0	1	1	0	0	1
0	0	1	0	0	0	1	0	1
1	0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	0	1
1	1	1	0	1	1	1	0	1
0	0	0	1	0	0	0	1	1
1	0	0	1	1	0	0	1	1
0	1	0	1	0	1	0	1	1
1	1	0	1	1	1	0	1	1
0	0	1	1	0	0	1	1	1
1	0	1	1	1	0	1	1	1
0	1	1	1	0	1	1	1	1
1	1	1	1	1	1	1	1	1

X = Don’t care

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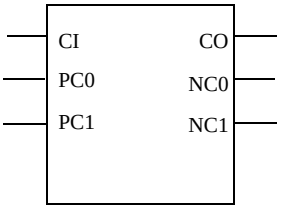
CU2

Combinational Logic for 2-Bit Up-Counter using Look-Up Table

Lattice FPGA		
SC	XP	EC
✓	✓	✓



CU2

INPUTS: CI, PC0, PC1
OUTPUTS: CO, NC0, NC1
PINORDER: CI, PC0, PC1, CO, NC0, NC1
CELL AREA: One Slice
One Slice

Description:

This macro realizes the combinational logic needed to implement a 2-bit up-counter by using the look-up tables (LUTs).

When CI=0, NC[0:1]=PC[0:1] and CO=0
When CI=1, NC[0:1]=PC[0:1]+1, and CO=1 if PC[0:1]=11

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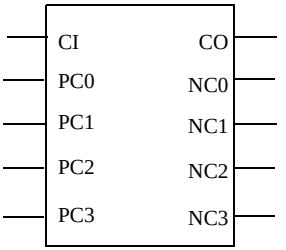
CU4

Combinational Logic for 4-Bit Up-Counter using Look-Up Table

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



CU4

INPUTS: CI,PC0,PC1,PC2,PC3
OUTPUTS: CO,NC0,NC1,NC2,NC3
PINORDER: CI PC0 PC1 PC2 PC3 CO NC0 NC1 NC2 NC3
MINIMUM CELL AREA (Series 2): 0.5
MINIMUM CELL AREA (Series 3 and Series 4): 0.125

Description:

This macro realizes the combinational logic needed to implement a 4-bit up-counter by using ripple elements.

When CI=0, NC[0:3]=PC[0:3] and CO=0
When CI=1, NC[0:3]=PC[0:3]+1, and CO=1 if PC[0:3]=1111

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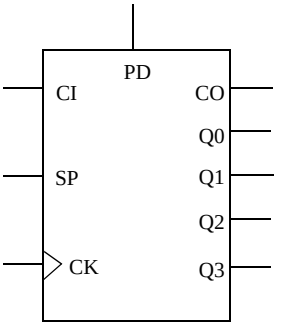
CU4P3BX

4 Bit Positive Edge Triggered Fast Up-Counter with Positive Clock Enable and Positive Asynchronous Preset

ORCA Series/Lattice FPGA				
2	3	4	XP	EC
✓	✓	✓	✓	✓



CU4P3BX

INPUTS: CI,SP,CK,PD
OUTPUTS: CO,Q0,Q1,Q2,Q3
PINORDER: CI SP CK PD CO Q0 Q1 Q2 Q3
MINIMUM CELL AREA (Series 2): 1.0
MINIMUM CELL AREA (Series 3 and Series 4): 0.25

Truth Table:

INPUTS				OUTPUTS	
CI	SP	CK	PD	CO	Q[0:3]
0	X	X	1	0	1
1	X	X	1	1	1
0	X	X	0	0	Q[0:3]
1	0	X	0	*	Q[0:3]
1	1	↑	0	*	count+1

X = Don't care
* When Q[0:3] is 1111, CO will be 1; otherwise, CO will be 0
When GSR=0, Q[0:3]=1 (SP=CK=X)

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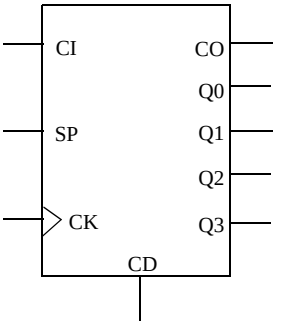
CU4P3DX

4 Bit Positive Edge Triggered Fast Up-Counter with Positive Clock Enable and Positive Asynchronous Clear

ORCA Series/Lattice FPGA				
2	3	4	XP	EC
✓	✓	✓	✓	✓



CU4P3DX

INPUTS: CI,SP,CK,CD
OUTPUTS: CO,Q0,Q1,Q2,Q3
PINORDER: CI SP CK CD CO Q0 Q1 Q2 Q3
MINIMUM CELL AREA (Series 2): 1.0
MINIMUM CELL AREA (Series 3 and Series 4): 0.25

Truth Table:

INPUTS				OUTPUTS	
CI	SP	CK	CD	CO	Q[0:3]
X	X	X	1	0	0
0	X	X	0	0	Q[0:3]
1	0	X	0	*	Q[0:3]
1	1	↑	0	*	count+1

X = Don’t care
* When Q[0:3] is 1111, CO will be 1; otherwise, CO will be 0
When GSR=0, Q[0:3]=0 (SP=CK=X)

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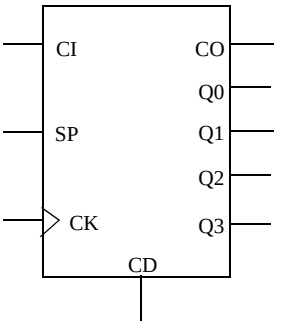
CU4P3IX

4 Bit Positive Edge Triggered Fast Up-Counter with Positive Clock Enable and Positive Synchronous Clear

ORCA Series/Lattice FPGA				
2	3	4	XP	EC
✓	✓	✓	✓	✓



CU4P3IX

INPUTS: CI,SP,CK,CD
OUTPUTS: CO,Q0,Q1,Q2,Q3
PINORDER: CI SP CK CD CO Q0 Q1 Q2 Q3
MINIMUM CELL AREA (Series 2): 1.0
MINIMUM CELL AREA (Series 3 and Series 4): 0.25

Truth Table:

INPUTS				OUTPUTS	
CI	SP	CK	CD	CO	Q[0:3]
X	1	↑	1	0	0
0	0	X	X	0	Q[0:3]
0	X	X	0	0	Q[0:3]
1	0	X	X	*	Q[0:3]
1	1	↑	0	*	count+1

X = Don't care
* When Q[0:3] is 1111, CO will be 1; otherwise, CO will be 0
When GSR=0, Q[0:3]=0 (SP=CK=X)

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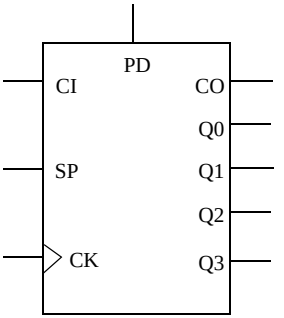
CU4P3JX

4 Bit Positive Edge Triggered Fast Up-Counter with Positive Clock Enable and Positive Synchronous Preset

ORCA Series/Lattice FPGA				
2	3	4	XP	EC
✓	✓	✓	✓	✓



CU4P3JX

INPUTS: CI,SP,CK,PD
OUTPUTS: CO,Q0,Q1,Q2,Q3
PINORDER: CI SP CK PD CO Q0 Q1 Q2 Q3
MINIMUM CELL AREA (Series 2): 1.0
MINIMUM CELL AREA (Series 3 and Series 4): 0.25

Truth Table:

INPUTS				OUTPUTS	
CI	SP	CK	PD	CO	Q[0:3]
0	1	↑	1	0	1
1	1	↑	1	1	1
0	0	X	X	0	Q[0:3]
0	X	X	0	0	Q[0:3]
1	0	X	X	*	Q[0:3]
1	1	↑	0	*	count+1

X = Don’t care
* When Q[0:3] is 1111, CO will be 1; otherwise, CO will be 0
When GSR=0, Q[0:3]=1 (SP=CK=X)

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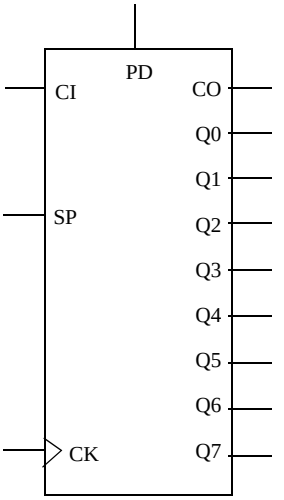
CU8P3BX

8 Bit Positive Edge Triggered Fast Up-Counter with Positive Clock Enable and Positive Asynchronous Preset

ORCA Series/Lattice			
3	4	XP	EC
✓	✓	✓	✓



CU8P3BX

INPUTS: CI,SP,CK,PD
OUTPUTS: CO,Q0,Q1,Q2,Q3,Q4,Q5,Q6,Q7
PINORDER: CI SP CK PD CO Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
MINIMUM CELL AREA: 0.5

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Truth Table:

INPUTS				OUTPUTS	
CI	SP	CK	PD	CO	Q[0:7]
0	X	X	1	0	1
1	X	X	1	1	1
0	X	X	0	0	Q[0:7]
1	0	X	0	*	Q[0:7]
1	1	↑	0	*	count+1

X = Don’t care

* When Q[0:7] is 11111111, CO will be 1; otherwise, CO will be 0
When GSR=0, Q[0:7]=1 (SP=CK=PD=X)

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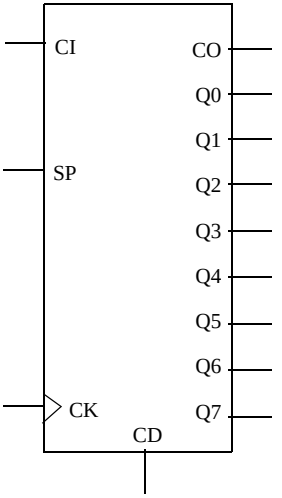
CU8P3DX

8 Bit Positive Edge Triggered Fast Up-Counter with Positive Clock Enable and Positive Asynchronous Clear

ORCA Series/Lattice			
3	4	XP	EC
✓	✓	✓	✓



CU8P3DX

INPUTS: CI,SP,CK,CD
OUTPUTS: CO,Q0,Q1,Q2,Q3,Q4,Q5,Q6,Q7
PINORDER: CI SP CK CD CO Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
MINIMUM CELL AREA: 0.5

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Truth Table:

INPUTS				OUTPUTS	
CI	SP	CK	CD	CO	Q[0:7]
X	X	X	1	0	0
0	X	X	0	0	Q[0:7]
1	0	X	0	*	Q[0:7]
1	1	↑	0	*	count+1

X = Don’t care

* When Q[0:7] is 11111111, CO will be 1; otherwise, CO will be 0
When GSR=0, Q[0:7]=0 (SP=CK=CD=X)

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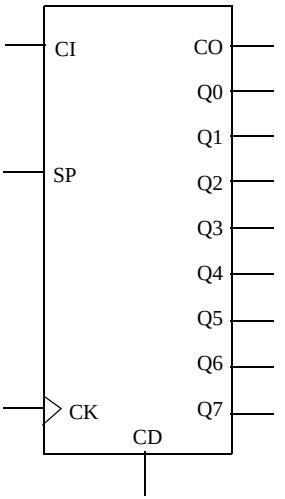
CU8P3IX

8 Bit Positive Edge Triggered Fast Up-Counter with Positive Clock Enable and Positive Synchronous Clear

ORCA Series/Lattice			
3	4	XP	EC
✓	✓	✓	✓



CU8P3IX

INPUTS: CI,SP,CK,CD
OUTPUTS: CO,Q0,Q1,Q2,Q3,Q4,Q5,Q6,Q7
PINORDER: CI SP CK CD CO Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
MINIMUM CELL AREA: 0.5

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Truth Table:

INPUTS				OUTPUTS	
CI	SP	CK	CD	CO	Q[0:7]
X	1	↑	1	0	0
0	0	X	X	0	Q[0:7]
0	X	X	0	0	Q[0:7]
1	0	X	X	*	Q[0:7]
1	1	↑	0	*	count+1

X = Don't care

* When Q[0:7] is 11111111, CO will be 1; otherwise, CO will be 0
When GSR=0, Q[0:7]=0 (SP=CK=CD=X)

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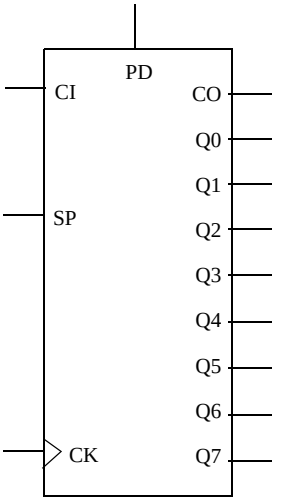
CU8P3JX

8 Bit Positive Edge Triggered Fast Up-Counter with Positive Clock Enable and Positive Synchronous Preset

ORCA Series/Lattice			
3	4	XP	EC
✓	✓	✓	✓



CU8P3JX

INPUTS: CI,SP,CK,PD
OUTPUTS: CO,Q0,Q1,Q2,Q3,Q4,Q5,Q6,Q7
PINORDER: CI SP CK PD CO Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
MINIMUM CELL AREA: 0.5

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Truth Table:

INPUTS				OUTPUTS	
CI	SP	CK	PD	CO	Q[0:7]
0	1	↑	1	0	1
1	1	↑	1	1	1
0	0	X	X	0	Q[0:7]
0	X	X	0	0	Q[0:7]
1	0	X	X	*	Q[0:7]
1	1	↑	0	*	count+1

X = Don’t care

* When Q[0:7] is 11111111, CO will be 1; otherwise, CO will be 0
When GSR=0, Q[0:7]=1 (SP=CK=PD=X)

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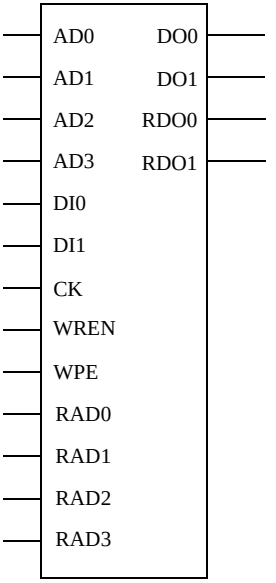
DCE16X2

16 Word by 2 Bit Positive Edge Triggered Write Synchronous Dual Port Memory with Positive Write Enable and Positive Write Port Enable

ORCA Series		
2	3	4
✓		



DCE16X2

INPUTS: AD0,AD1,AD2,AD3,DI0,DI1,CK,WREN,WPE,RAD0,RAD1,RAD2, RAD3
OUTPUTS: DO0,DO1,RDO0,RDO1
PINORDER: AD0 AD1 AD2 AD3 DI0 DI1 CK WREN WPE RAD0 RAD1 RAD2 RAD3 RDO0 RDO1 DO0 DO1
MINIMUM CELL AREA: 1.0

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Description:

The DCE16x2 symbol represents a 16 word by 2 bit synchronous dual port RAM. It has two data inputs DI[1:0], a positive Write Enable (WREN), and a positive Write Port Enable (WPE). There are two separate sets of address inputs and two separate sets of data outputs (read/write and read-only).

Writing to the RAM does not occur until *both* the WREN and WPE signals are enabled. If both the WREN and WPE signals are HIGH, the data is written into the locations specified by the read/write address lines AD[3:0] on the next positive clock (CK) edge. If *either one* or *both* of the WREN or WPE signals are LOW, an asynchronous data read operation is performed, with the memory contents specified by the read/write address inputs AD[3:0] output on the read/write data output signals DO[1:0]. The memory contents specified by the read-only addresses RAD[3:0] can also be output (asynchronously) on the read-only data outputs RDO[1:0] at any time regardless of the state of the WREN or WPE signals.

In other words, the read operation is asynchronous and is always active. The write operation is synchronous and only occurs when there is a rising edge of the clock and the write enables are high prior to that rising edge.

If desired, the contents of the DCE16x2 can be assigned an initial value, which is loaded into the RAM during configuration. The INITVAL=<*value*> parameter is used to assign the initial value. The <*value*> should consist of sixteen 2 bit binary or hexadecimal data written into the RAM from the highest address to the lowest address. For example, if the following attribute is specified:

`INITVAL=0001101100011011000110110011011` (in binary)
or
`INITVAL=0x0123012301230123` (in hex)

it implies that the above data is loaded sequentially from location FH to 0H (where FH would contain the 0 and 0H the 3). If no INITVAL= parameter is specified, the RAM is initialized with zeros on configuration.

If the INITVAL is specified as a hex string of 16 values, the values should not be greater than 3, since 3 is setting both memory locations to 1. If a value greater than 3 is used for synthesis/mapping, only the last two (least significant) bits are used for initialization by the mapper. For example,

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```
INITVAL=0x00000000ffffffff
```
is equivalent to
```
INITVAL=0x0000000033333333
```

for mapping purposes, since the first two bits of the “f” are ingnored.

If a value other than 0,1,2 or 3 is used for simulation, the simulator will return undefined (‘U’) results for the data. Therefore, simulation results and actual mapped results could vary. For this reason, it is highly recommended to restrict initial hex strings to values of 0,1,2 or 3 for 2 bit wide memories.

Truth Table:

INPUTS						OUTPUTS		OPERATION
DI[1:0]	WREN	WPE	CK	AD[3:0]	RAD[3:0]	DO[1:0]	RDO[1:0]	
DI[1:0]	1	1	↑	AD[3:0]	RAD[3:0]	MEM[AD[3:0]]	MEM[RAD[3:0]]	Write DI[1:0] into last latched AD[3:0] when CK was low
X	X	X	X	AD[3:0]	RAD[3:0]	MEM[AD[3:0]]	MEM[RAD[3:0]]	Read MEM[AD[3:0]] and MEM[RAD[3:0]]

X = Don’t care

Note: The memory is always being read. New data is read out after a write.

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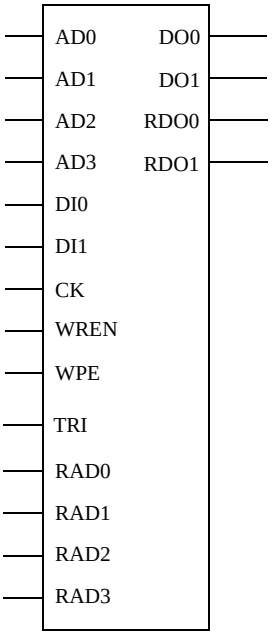
DCE16X2Z

16 Word by 2 Bit Positive Edge Triggered Write Synchronous Dual Port Memory with Positive Write Enable, Positive Write Port Enable, and Positive Tristate Control

ORCA Series		
2	3	4
✓		



DCE16X2Z

INPUTS: AD0,AD1,AD2,AD3,DI0,DI1,CK,WREN,WPE,TRI,RAD0,RAD1, RAD2, RAD3
OUTPUTS: DO0,DO1,RDO0,RDO1
PINORDER: AD0 AD1 AD2 AD3 DI0 DI1 CK WREN WPE TRI RAD0 RAD1 RAD2 RAD3
RDO0 RDO1 DO0 DO1
MINIMUM CELL AREA: 1.0

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Description:

The DCE16x2Z symbol represents a 16 word by 2 bit synchronous dual port RAM. It has two data inputs DI[1:0], a positive Write Enable (WREN), and a positive Write Port Enable (WPE). There are two separate sets of address inputs and two separate sets of data outputs (read/write and read-only).

Writing to the RAM does not occur until *both* the WREN and WPE signals are enabled. If both the WREN and WPE signals are HIGH, the data is written into the locations specified by the read/write address lines AD[3:0] on the next positive clock (CK) edge. If *either one* or *both* of the WREN or WPE signals are LOW, an asynchronous data read operation is performed, with the memory contents specified by the read/write address inputs AD[3:0] output on the read/write data output signals DO[1:0]. The memory contents specified by the read-only addresses RAD[3:0] can also be output (asynchronously) on the read-only data outputs RDO[1:0] at any time regardless of the state of the WREN or WPE signals.

In other words, the read operation is asynchronous and is always active. The write operation is synchronous and only occurs when there is a rising edge of the clock and the write enables are high prior to that rising edge.

The read-only outputs can be tristated by enabling the TRI control signal HIGH. This is to enable the use of the outputs in a bus format and to drive the outputs into a high impedance state.

Note

The read/write outputs are not controlled by the TRI signal.

If desired, the contents of the DCE16x2Z can be assigned an initial value, which is loaded into the RAM during configuration. The INITVAL=<*value*> parameter is used to assign the initial value. The <*value*> should consist of sixteen 2 bit binary or hexadecimal data written into the RAM from the highest address to the lowest address.

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For example, if the following attribute is specified:

`INITVAL=0001101100011011000110110001101 1` (in binary)
or
`INITVAL=0x0123012301230123` (in hex)

it implies that the above data is loaded sequentially from location FH to 0H (where FH would contain the 0 and 0H the 3). If no INITVAL= parameter is specified, the RAM is initialized with zeros on configuration.

If the INITVAL is specified as a hex string of 16 values, the values should not be greater than 3, since 3 is setting both memory locations to 1. If a value greater than 3 is used for synthesis/mapping, only the last two (least significant) bits are used for initialization by the mapper. For example,

`INITVAL=0x00000000ffffffff`
is equivalent to
`INITVAL=0x0000000033333333`

for mapping purposes, since the first two bits of the “f” are ingnored.

If a value other than 0,1,2 or 3 is used for simulation, the simulator will return undefined (‘U’) results for the data. Therefore, simulation results and actual mapped results could vary. For this reason, it is highly recommended to restrict initial hex strings to values of 0,1,2 or 3 for 2 bit wide memories.

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Truth Table:

INPUTS							OUTPUTS		OPERATION
DI[1:0]	WREN	WPE	TRI	CK	AD[3:0]	RAD[3:0]	DO[1:0]	RDO[1:0]	
DI[1:0]	1	1	1	↑	AD[3:0]	RAD[3:0]	MEM[AD[3:0]]	Z	Tristate the read output only, but write DI[1:0] into AD[3:0]
DI[1:0]	1	1	0	↑	AD[3:0]	RAD[3:0]	MEM[AD[3:0]]	MEM[RAD[3:0]]	Write DI[1:0] into last latched AD[3:0] when CK was low
DI[1:0]	X	X	1	X	AD[3:0]	RAD[3:0]	MEM[AD[3:0]]	Z	Tristate the read output only
X	X	X	0	X	AD[3:0]	RAD[3:0]	MEM[AD[3:0]]	MEM[RAD[3:0]]	Read MEM[AD[3:0]] and MEM[RAD[3:0]]

X = Don’t care

Note: The memory is always being read. New data is read out after a write.

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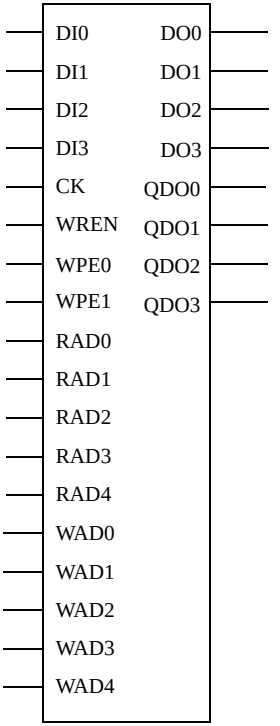
DCE32X4

32 Word by 4 Bit Negative Edge Triggered Write Synchronous Dual Port Memory with a Positive Write Enable and Two Positive Write Port Enables

ORCA Series		
2	3	4
	✓	✓



DCE32X4

INPUTS: DI0,DI1,DI2,DI3,CK,WREN,WPE0,WPE1,RAD0,RAD1,RAD2,RAD3,
RAD4,WAD0,WAD1,WAD2,WAD3,WAD4
OUTPUTS: DO0,DO1,DO2,DO3,QDO0,QDO1,QDO2,QDO3
PINORDER: DI0 DI1 DI2 DI3 CK WREN WPE0 WPE1 RAD0 RAD1 RAD2 RAD3 RAD4
WAD0 WAD1 WAD2 WAD3 WAD4 DO0 DO1 DO2 DO3 QDO0 QDO1 QDO2
QDO3
MINIMUM CELL AREA: 1.0

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Description:

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The DCE32x4 symbol represents a 32 word by 4 bit synchronous dual port RAM. It has four data inputs DI[3:0], a positive Write Enable (WREN), two positive Write Port Enables (WPE1, WPE0), and two separate sets of address inputs (read and write).

The WREN and WPE must be HIGH for the rising clock edge if the write to the RAM is occurring on the falling edge. The data is written into the locations specified by the write address lines WAD[4:0] on the next negative clock (CK) edge. If *any* of the WREN or WPE signals are LOW, an asynchronous data read operation is performed, with the memory contents specified by the read address inputs RAD[4:0] output on the data output signals DO[3:0].

In other words, the read operation is asynchronous and is always active. The write operation is synchronous and only occurs when there is a falling edge of the clock and the write enables are high prior to that falling edge. Newly written data shows up at the output only when the read and write addresses are the same.

This RAM also has registered data outputs (QDO[3:0]), which are registered on the rising edge of the clock.

If desired, the contents of the DCE32x4 can be assigned an initial value, which is loaded into the RAM during configuration. The INITVAL=<*value*> parameter is used to assign the initial value. The <*value*> should consist of 32 4-bit binary or hexadecimal data written into the RAM from the highest address to the lowest address. For example, if the following attribute is specified:

```
INITVAL=00000001001000110100010101100111100010011010101111001101111011111000000010010001101000101011001111000100110101011
1100110111101111 (in binary)
```
or
```
INITVAL=0x0123456789ABCDEF0123456789ABCDEF (in hex)
```

it implies that the above data is loaded sequentially from location 1FH to 0H (where 1FH would contain the 0 and 0H the F). If no INITVAL= parameter is specified, the RAM is initialized with zeros on configuration.

For simulation with a 3C RAM or ROM cell, you must instantiate a GSR in your netlist, and pulse the GSR high to low at the beginning of the simulation.

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Truth Table:

INPUTS							OUTPUTS		OPERATION
DI[3:0]	WREN	WPE0	WPE1	CK	WAD[4:0]	RAD[4:0]	DO[3:0]	QDO[3:0]	
DI[3:0]	1	1	1	↓	WAD[4:0]	RAD[4:0]	MEM[RAD[4:0]]	QDO[3:0]	Write DI[3:0] into WAD[4:0]
X	X	X	X	X	WAD[4:0]	RAD[4:0]	MEM[RAD[4:0]]	QDO[3:0]	Read MEM[RAD[4:0]]
X	X	X	X	↑	WAD[4:0]	RAD[4:0]	MEM[RAD[4:0]]	MEM[RAD[4:0]]	Read MEM[RAD[4:0]] Register data output
X	X	X	X	X	WAD[4:0]	WAD[4:0]	MEM[WAD[4:0]]	QDO[3:0]	Read MEM[WAD[4:0]]
X	X	X	X	↑	WAD[4:0]	WAD[4:0]	MEM[WAD[4:0]]	MEM[WAD[4:0]]	Read MEM[WAD[4:0]] Register data output

X = Don’t care
When GSR=0, WREN=WPE0=WPE1=RAD[4:0]=WAD[4:0]=DO[3:0]=QDO[3:0]=0

Note: The memory is always being read. New data is read out after a write.

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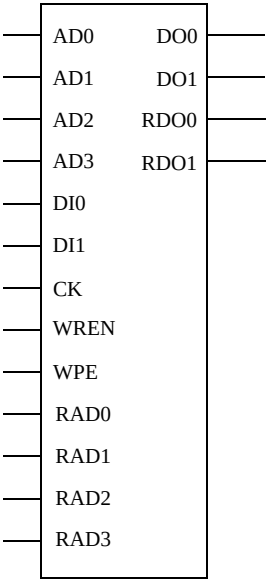
DCF16X2

16 Word by 2 Bit Fast Positive Edge Triggered Write Synchronous Dual Port Memory with Positive Write Enable and Positive Write Port Enable

ORCA Series		
2	3	4
✓		



DCF16X2

INPUTS: AD0,AD1,AD2,AD3,DI0,DI1,CK,WREN,WPE,RAD0,RAD1,RAD2, RAD3
OUTPUTS: DO0,DO1,RDO0,RDO1
PINORDER: AD0 AD1 AD2 AD3 DI0 DI1 CK WREN WPE RAD0 RAD1 RAD2 RAD3 RDO0 RDO1 DO0 DO1
MINIMUM CELL AREA: 1.0

Note

This RAM cell is used in the fast mode. It allows for greater performance (clock speeds) when compared to DCE16X2. Please refer to your datasheet for the appropriate timing information. This RAM cell is not supported when using the Readback capability.

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Description:

The DCF16x2 symbol represents a 16 word by 2 bit synchronous dual port fast RAM. It has two data inputs DI[1:0], a positive Write Enable (WREN), and a positive Write Port Enable (WPE). There are two separate sets of address inputs and two separate sets of data outputs (read/write and read-only).

Writing to the RAM does not occur until *both* the WREN and WPE signals are enabled. If both the WREN and WPE signals are HIGH, the data is written into the locations specified by the read/write address lines AD[3:0] on the next positive clock (CK) edge. If *either one* or *both* of the WREN or WPE signals are LOW, an asynchronous data read operation is performed, with the memory contents specified by the read/write address inputs AD[3:0] output on the read/write data output signals DO[1:0]. The memory contents specified by the read-only addresses RAD[3:0] can also be output (asynchronously) on the read-only data outputs RDO[1:0] at any time regardless of the state of the WREN or WPE signals.

In other words, the read operation is asynchronous and is always active. The write operation is synchronous and only occurs when there is a rising edge of the clock and the write enables are high prior to that rising edge.

If desired, the contents of the DCF16x2 can be assigned an initial value, which is loaded into the RAM during configuration. The INITVAL=<*value*> parameter is used to assign the initial value. The <*value*> should consist of sixteen 2 bit binary or hexadecimal data written into the RAM from the highest address to the lowest address. For example, if the following attribute is specified:

`INITVAL=0001101100011011000110110011011` (in binary)
is equivalent to
`INITVAL=0x0123012301230123` (in hex)

it implies that the above data is loaded sequentially from location FH to 0H (where FH would contain the 0 and 0H the 3). If no INITVAL= parameter is specified, the RAM is initialized with zeros on configuration.

If the INITVAL is specified as a hex string of 16 values, the values should not be greater than 3, since 3 is setting both memory locations to 1. If a value greater than 3 is used for synthesis/mapping, only the last two (least significant) bits are used for initialization by the mapper. For example,

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```
INITVAL=0x00000000ffffffff
```
is equivalent to
```
INITVAL=0x0000000033333333
```

for mapping purposes, since the first two bits of the “f” are ingnored.

If a value other than 0,1,2 or 3 is used for simulation, the simulator will return undefined (‘U’) results for the data. Therefore, simulation results and actual mapped results could vary. For this reason, it is highly recommended to restrict initial hex strings to values of 0,1,2 or 3 for 2 bit wide memories.

Truth Table:

INPUTS						OUTPUTS		OPERATION
DI[1:0]	WREN	WPE	CK	AD[3:0]	RAD[3:0]	DO[1:0]	RDO[1:0]	
DI[1:0]	1	1	↑	AD[3:0]	RAD[3:0]	MEM[AD[3:0]]	MEM[RAD[3:0]]	Write DI[3:0] into last latched AD[3:0] when CK was low
X	X	X	X	AD[3:0]	RAD[3:0]	MEM[AD[3:0]]	MEM[RAD[3:0]]	Read MEM[AD[3:0]] and MEM[RAD[3:0]]

X = Don’t care

Note: The memory is always being read. New data is read out after a write.

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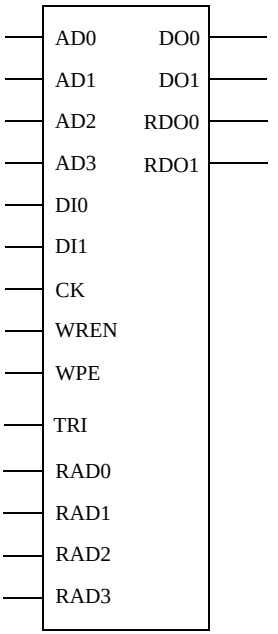
DCF16X2Z

16 Word by 2 Bit Fast Positive Edge Triggered Write Synchronous Dual Port Memory with Positive Write Enable, Positive Write Port Enable, and Positive Tristate Control

ORCA Series		
2	3	4
✓		



DCF16X2Z

INPUTS: AD0,AD1,AD2,AD3,DI0,DI1,CK,WREN,WPE,TRI,RAD0,RAD1, RAD2, RAD3
OUTPUTS: DO0,DO1,RDO0,RDO1
PINORDER: AD0 AD1 AD2 AD3 DI0 DI1 CK WREN WPE TRI RAD0 RAD1 RAD2 RAD3
RDO0 RDO1 DO0 DO1
MINIMUM CELL AREA: 1.0

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Note

This RAM cell is used in the fast mode. It allows for greater performance (clock speeds) when compared to DCE16X2Z. Please refer to your datasheet for the appropriate timing information. This RAM cell is not supported when using the Readback capability.

Description:

The DCE16x2Z symbol represents a 16 word by 2 bit synchronous dual port fast RAM. It has two data inputs DI[1:0], a positive Write Enable (WREN), and a positive Write Port Enable (WPE). There are two separate sets of address inputs and two separate sets of data outputs (read/write and read-only).

Writing to the RAM does not occur until *both* the WREN and WPE signals are enabled. If both the WREN and WPE signals are HIGH, the data is written into the locations specified by the read/write address lines AD[3:0] on the next positive clock (CK) edge. If *either one* or *both* of the WREN or WPE signals are LOW, an asynchronous data read operation is performed, with the memory contents specified by the read/write address inputs AD[3:0] output on the read/write data output signals DO[1:0]. The memory contents specified by the read-only addresses RAD[3:0] can also be output (asynchronously) on the read-only data outputs RDO[1:0] at any time regardless of the state of the WREN or WPE signals.

In other words, the read operation is asynchronous and is always active. The write operation is synchronous and only occurs when there is a rising edge of the clock and the write enables are high prior to that rising edge.

The read-only outputs can be tristated by enabling the TRI control signal HIGH. This is to enable the use of the outputs in a bus format and to drive the outputs into a high impedance state.

Note

The read/write outputs are not controlled by the TRI signal.

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If desired, the contents of the DCF16x2Z can be assigned an initial value, which is loaded into the RAM during configuration. The INITVAL=<*value*> parameter is used to assign the initial value. The <*value*> should consist of sixteen 2 bit binary or hexadecimal data written into the RAM from the highest address to the lowest address. For example, if the following attribute is specified:

`INITVAL=0001101100011011000110110011011` (in binary)
or
`INITVAL=0x0123012301230123` (in hex)

it implies that the above data is loaded sequentially from location FH to 0H (where FH would contain the 0 and 0H the 3). If no INITVAL= parameter is specified, the RAM is initialized with zeros on configuration.

If desired, the contents of the DCF16x2 can be assigned an initial value, which is loaded into the RAM during configuration. The INITVAL=<*value*> parameter is used to assign the initial value. The <*value*> should consist of sixteen 2 bit binary or hexadecimal data written into the RAM from the highest address to the lowest address. For example, if the following attribute is specified:

`INITVAL=0001101100011011000110110011011` (in binary)
is equivalent to
`INITVAL=0x0123012301230123` (in hex)

it implies that the above data is loaded sequentially from location FH to 0H (where FH would contain the 0 and 0H the 3). If no INITVAL= parameter is specified, the RAM is initialized with zeros on configuration.

This RAM cell is used in the fast mode. It is not supported when using the Readback capability. Please refer to your datasheet for the appropriate timing information. [see next page for truth table]

Truth Table:

INPUTS							OUTPUTS		OPERATION
DI[1:0]	WREN	WPE	TRI	CK	AD[3:0]	RAD[3:0]	DO[1:0]	RDO[1:0]	
DI[1:0]	1	1	1	↑	AD[3:0]	RAD[3:0]	MEM[AD[3:0]]	Z	Tristate the read output only, but write DI[3:0] into AD[3:0]

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INPUTS							OUTPUTS		OPERATION
DI[1:0]	WREN	WPE	TRI	CK	AD[3:0]	RAD[3:0]	DO[1:0]	RDO[1:0]	
DI[1:0]	1	1	0	↑	AD[3:0]	RAD[3:0]	MEM[AD[3:0]]	MEM[RAD[3:0]]	Write DI[3:0] into last latched AD[3:0] when CK was low
DI[1:0]	X	X	1	X	AD[3:0]	RAD[3:0]	MEM[AD[3:0]]	Z	Tristate the read output only
X	X	X	0	X	AD[3:0]	RAD[3:0]	MEM[AD[3:0]]	MEM[RAD[3:0]]	Read MEM[AD[3:0]] and MEM[RAD[3:0]]

X = Don’t care

Note: The memory is always being read. New data is read out after a write, except when in tristate.

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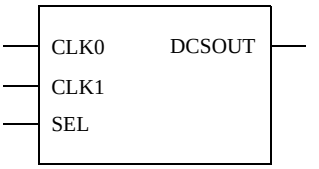
DCS

Dynamic Clock Selection Multiplexer

Lattice FPGA		
SC	XP	EC
✓	✓	✓



DCS

INPUTS: CLK0 CLK1 SEL
OUTPUTS: DCSOUT
PINORDER: CLK0 CLK1 SEL DCSOUT
ATTRIBUTES:
DCSMODE: NEG , POS , HIGH_LOW , HIGH_HIGH , LOW_LOW , LOW_HIGH , CLK0 , CLK1

Description:

DCS is a global clock buffer incorporating a smart multiplexer function that takes two independent input clock sources and avoids glitches or runt pulses on the output clock, regardless of where the enable signal is toggled. Located in pairs at the center of each edge, there are eight DCS elements per device.

Function	Pins
Input Clock Select	SEL
Primary Clock Input 0	CLK0
Primary Clock Input 1	CLK1
To Primary Clock Mid-Mux	DCSOUT

For each DCS:

- Inputs are from primary clocks at PLC routing block (one branch per DCS)
- Selects are from a routing block's LUT port (A0, B0, etc.)
- Outputs are connected to the DCS output sources of the feedline muxes

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The outputs of the DCS then reach primary clock distribution via the feedlines. The connections from CIB to DCS are shown in the table below. The selected CIB interfaces to a PIC and is located at the center of each bank and next to the mid-muxes. Note that the CIB to DCS connections are merged with the existing PIC-CIB connections at that CIB. It is up to the hardware designer to select the most convenient CIB.

CIB to DCS Connections

CIB	DCS
C7	SEL
CLK0(jclk0)	CLK0
CLK1(jclk2)	CLK1

DCS Attributes:

Attribute Name	Description	Output		Value	DCS Fuse Settings				
		SEL = 0	SEL = 1		0	1	2	3	4
DCS MODE	Rising edge triggered, latched state is high	CLK0	CLK1	POS	1	0	0	0	0
	Falling edge triggered, latched state is low	CLK0	CLK1	NEG	0	0	0	0	0
	Sel is active high, Disabled output is low	0	CLK1	HIGH_LOW	0	1	0	0	0
	Sel is active high, Disabled output is high	1	CLK1	HIGH_HIGH	1	1	0	0	0
	Sel is active low, Disabled output is low	CLK0	0	LOW_LOW	0	0	1	0	0
	Sel is active low, Disabled output is high	CLK0	1	LOW_HIGH	1	0	1	0	0
	Buffer for CLK0	CLK0	CLK0	CLK0	0	0	1	0	1
	Buffer for CLK1	CLK1	CLK1	CLK1	0	1	0	1	0

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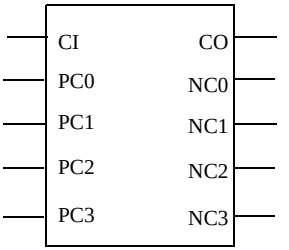
DEC4

Combinational Logic for 4 Bit Down Counter using Look-Up Table

ORCA Series		
2	3	4
	✓	✓



DEC4

INPUTS: CI,PC0,PC1,PC2,PC3
OUTPUTS: CO,NC0,NC1,NC2,NC3
PINORDER: CI PC0 PC1 PC2 PC3 CO NC0 NC1 NC2 NC3
MINIMUM CELL AREA: 0.125

Description:

This macro realizes the combinational logic needed to implement a 4 bit down counter by using ripple elements.

When CI=0, NC[0:3]=PC[0:3]-1, and CO=0 if PC[0:3]=0000
When CI=1, NC[0:3]=PC[0:3] and CO=1

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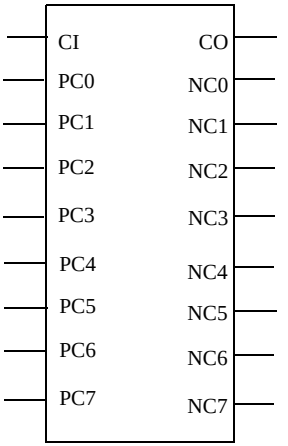
DEC8

Combinational Logic for 8 Bit Down Counter using Look-Up Table

ORCA Series		
2	3	4
	✓	✓



DEC8

INPUTS: CI,PC0,PC1,PC2,PC3,PC4,PC5,PC6,PC7
OUTPUTS: CO,NC0,NC1,NC2,NC3,NC4,NC5,NC6,NC7
PINORDER: CI PC0 PC1 PC2 PC3 PC4 PC5 PC6 PC7 CO NC0 NC1 NC2 NC3 NC4 NC5 NC6 NC7
MINIMUM CELL AREA: 0.25

Description:

This macro realizes the combinational logic needed to implement an 8 bit down counter by using ripple elements.

When CI=0, NC[0:7]=PC[0:7]-1, and CO=0 if PC[0:7]=00000000
When CI=1, NC[0:7]=PC[0:7] and CO=1

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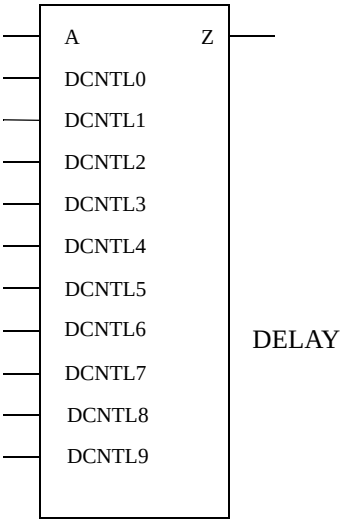
DELAY



Lattice FPGA		
SC	XP	EC
✓		

INPUTS: A, DCNTL0, DCNTL1, DCNTL2, DCNTL3, DCNTL4, DCNTL5, DCNTL6, DCNTL7, DCNTL8
OUTPUTS: Z
PINORDER: A, DCNTL0, DCNTL1, DCNTL2, DCNTL3, DCNTL4, DCNTL5, DCNTL6, DCNTL7, DCNTL8, Z
MINIMUM CELL AREA: 0
ATTRIBUTES:
DELAYTYPE: MANUAL, DLL, PCLK, ECLK
COARSE: CDEL0, CDEL1, CDEL2, CDEL3
FINE: FDEL0, FDEL1, FDEL2, ... FDEL47

Description:

Sets the input delay for an input. You can choose either dynamic delay or the static delay.

Truth Table:

INPUTS	OUTPUTS
A	Z
0	0

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INPUTS	OUTPUTS
A	Z
1	1

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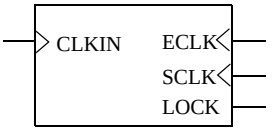
DLL1XB

Programmable Clock Manager (Delay Locked Loop) — Bottom

ORCA Series		
2	3	4
	✓	✓



DLL1XB

INPUTS: CLKIN
OUTPUTS: ECLK,SCLK,LOCK
PINORDER: CLKIN ECLK SCLK LOCK
MINIMUM CELL AREA: 0

ATTRIBUTES: DUTY,DIV0

Description:

The delay locked loop is one of the functions performed by the PCM which is user selectable through configuration logic.

DLL1XB generates output signals ECLK and SCLK, which are at the same frequency as the input clock signals if DIV0 = 1 after adjusting the DUTY cycle.

The LOCK output is asserted high when the ECLK and SCLK outputs are valid.

Feclk = Fsclk = Fin/DIV0
DUTY = Property to control the duty cycle (default 50)
DIV0 = Property to divide the input clock frequency (default 1)
DISABLED_GSR= Property to disable global set/reset
CLKIN = Clock in
ECLK = Express clock out
SCLK = System clock out
LOCK = Lock output

Duty cycle can be adjusted in 1/32 (3.125%) increments of the clock period after the input clock frequency is being divided by DIV0 value.

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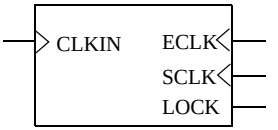
DLL1XT

Programmable Clock Manager (Delay Locked Loop) — Top

ORCA Series		
2	3	4
	✓	✓



DLL1XT

INPUTS: CLKIN
OUTPUTS: ECLK,SCLK,LOCK
PINORDER: CLKIN ECLK SCLK LOCK
MINIMUM CELL AREA: 0

ATTRIBUTES: DUTY,DIV0

Description:

The delay locked loop is one of the functions performed by the PCM which is user selectable through configuration logic.

DLL1XT generates output signals ECLK and SCLK, which are at the same frequency as the input clock signals if DIV0 = 1 after adjusting the DUTY cycle.

The LOCK output is asserted high when the ECLK and SCLK outputs are valid.

Feclk = Fsclk = Fin/DIV0
DUTY = Property to control the duty cycle (default 50)
DIV0 = Property to divide the input clock frequency (default 1)
DISABLED_GSR= Property to disable global set/reset
CLKIN = Clock in
ECLK = Express clock out
SCLK = System clock out
LOCK = Lock output

Duty cycle can be adjusted in 1/32 (3.125%) increments of the clock period after the input clock frequency is being divided by DIV0 value.

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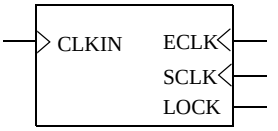
DLLPDB

Programmable Clock Manager (Programmable Delay, Delay Locked Loop) — Bottom

ORCA Series		
2	3	4
	✓	✓



DLLPDB

INPUTS: CLKIN
OUTPUTS: ECLK,SCLK,LOCK
PINORDER: CLKIN ECLK SCLK LOCK
MINIMUM CELL AREA: 0
ATTRIBUTES: DIV2,PDELAY,DIV0

Description:

The delay locked loop is one of the functions performed by the PCM which is user selectable through configuration logic.

DLLPDB generates output signals ECLK and SCLK, which are the input clock signals delayed by 1/32 ... 31/32 T, where T is the period of the input clock.

The LOCK output is asserted high when the ECLK and SCLK outputs are valid.

Feclk = Fin/(DIV2*DIV0)
Fsclk = Fin/DIV0
PDELAY = Attribute to denote the delay tap numbers (range 1–32; default 1)
DIV2 = The denominator in the fraction (range 1–8; default 1)
DISABLED_GSR= Property to disable global set/reset
CLKIN = Clock in
ECLK = Express clock out
SCLK = System clock out

LOCK = Lock output
DIV0 = Property to divide the input clock frequency (default 1)

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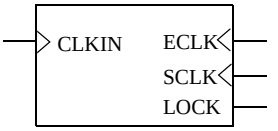
DLLPDT

Programmable Clock Manager (Programmable Delay, Delay Locked Loop) — Top

ORCA Series		
2	3	4
	✓	✓



DLLPDT

INPUTS: CLKIN
OUTPUTS: ECLK,SCLK,LOCK
PINORDER: CLKIN ECLK SCLK LOCK
MINIMUM CELL AREA: 0
ATTRIBUTES: DIV2,PDELAY,DIV0

Description:

The delay locked loop is one of the functions performed by the PCM which is user selectable through configuration logic.

DLLPDBT generates output signals ECLK and SCLK, which are the input clock signals delayed by 1/32 ... 31/32 T, where T is the period of the input clock.

The LOCK output is asserted high when the ECLK and SCLK outputs are valid.

Feclk = Fin/(DIV2*DIV0)
Fsclk = Fin/DIV0
PDELAY = Attribute to denote the delay tap numbers (range 1–32; default 1)
DIV2 = The denominator in the fraction (range 1–8; default 1)
DISABLED_GSR= Property to disable global set/reset
CLKIN = Clock in
ECLK = Express clock out
SCLK = System clock out

LOCK = Lock output
DIV0 = Property to divide the input clock frequency (default 1)

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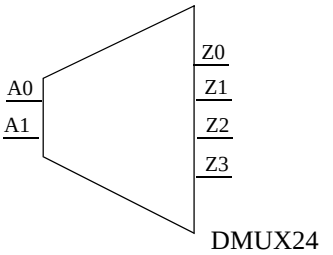
DMUX24

2 to 4 DeMux

ORCA Series		
2	3	4
✓		



DMUX24

INPUTS: A0,A1
OUTPUTS: Z0,Z1,Z2,Z3
PINORDER: A0 A1 Z0 Z1 Z2 Z3
MINIMUM CELL AREA: 0.5

Truth Table:

INPUTS		OUTPUTS			
A0	A1	Z0	Z1	Z2	Z3
0	0	1	0	0	0
1	0	0	1	0	0
0	1	0	0	1	0
1	1	0	0	0	1

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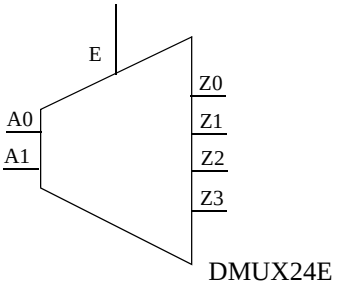
DMUX24E

2 to 4 DeMux with Enable

ORCA Series		
2	3	4
✓		



DMUX24E

INPUTS: A0,A1,E
OUTPUTS: Z0,Z1,Z2,Z3
PINORDER: A0 A1 E Z0 Z1 Z2 Z3
MINIMUM CELL AREA: 0.5

Truth Table:

INPUTS			OUTPUTS			
A0	A1	E	Z0	Z1	Z2	Z3
X	X	0	0	0	0	0
0	0	1	1	0	0	0
1	0	1	0	1	0	0
0	1	1	0	0	1	0
1	1	1	0	0	0	1

X = Don’t care

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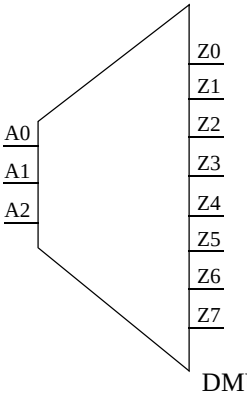
DMUX38

3 to 8 DeMux

ORCA Series		
2	3	4
✓		



DMUX38

INPUTS: A0,A1,A2
OUTPUTS: Z0,Z1,Z2,Z3,Z4,Z5,Z6,Z7
PINORDER: A0 A1 A2 Z0 Z1 Z2 Z3 Z4 Z5 Z6 Z7
MINIMUM CELL AREA: 1.0

Truth Table:

Inputs			Outputs							
A0	A1	A2	Z0	Z1	Z2	Z3	Z4	Z5	Z6	Z7
0	0	0	1	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
1	1	0	0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

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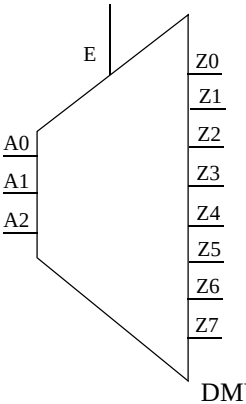
DMUX38E

3 to 8 DeMux with Enable

ORCA Series		
2	3	4
✓		



DMUX38E

INPUTS: A0,A1,A2,E
OUTPUTS: Z0,Z1,Z2,Z3,Z4,Z5,Z6,Z7
PINORDER: A0 A1 A2 E Z0 Z1 Z2 Z3 Z4 Z5 Z6 Z7
MINIMUM CELL AREA: 1.0

continued

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Truth Table:

Inputs				Outputs							
A0	A1	A2	E	Z0	Z1	Z2	Z3	Z4	Z5	Z6	Z7
X	X	X	0	0	0	0	0	0	0	0	0
0	0	0	1	1	0	0	0	0	0	0	0
1	0	0	1	0	1	0	0	0	0	0	0
0	1	0	1	0	0	1	0	0	0	0	0
1	1	0	1	0	0	0	1	0	0	0	0
0	0	1	1	0	0	0	0	1	0	0	0
1	0	1	1	0	0	0	0	0	1	0	0
0	1	1	1	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	1

X = Don’t care

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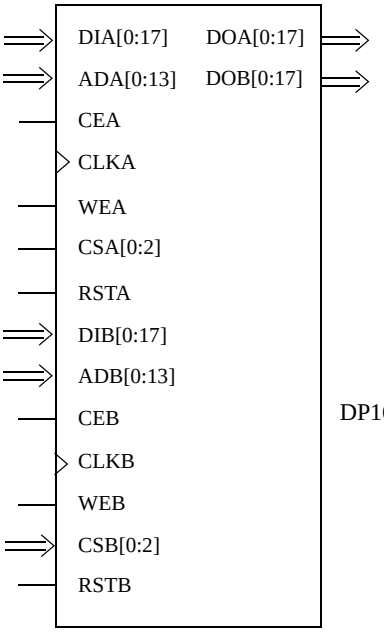
DP16KA

16K Dual Port Block RAM

Lattice FPGA		
SC	XP	EC
✓		



NOTE: The graphic is shown in bus notation for convenience. This element must be instantiated in expanded bus notation format with each individual bit as given below.

INPUT : DIA0, DIA1, DIA2, DIA3, DIA4, DIA5, DIA6, DIA7, DIA8, DIA9, DIA10, DIA11, DIA12, DIA13, DIA14, DIA15, DIA16, DIA17, ADA0, ADA1, ADA2, ADA3, ADA4, ADA5, ADA6, ADA7, ADA8, ADA9, ADA10, ADA11, ADA12, ADA13, CEA, CLKA, WEA, CSA0, CSA1, CSA2, RSTA, DIB0, DIB1, DIB2, DIB3, DIB4, DIB5, DIB6, DIB7, DIB8, DIB9, DIB10, DIB11, DIB12, DIB13, DIB14, DIB15, DIB16, DIB17, ADB0, ADB1, ADB2, ADB3, ADB4, ADB5, ADB6, ADB7, ADB8, ADB9, ADB10, ADB11, ADB12, ADB13, CEB, CLKB, WEB, CSB0, CSB1, CSB2, RSTB

OUTPUT : DOA0, DOA1, DOA2, DOA3, DOA4, DOA5, DOA6, DOA7, DOA8, DOA9, DOA10, DOA11, DOA12, DOA13, DOA14, DOA15, DOA16, DOA17, DOB0, DOB1, DOB2, DOB3, DOB4, DOB5, DOB6, DOB7, DOB8, DOB9, DOB10, DOB11, DOB12, DOB13, DOB14, DOB15, DOB16, DOB17

PINORDER: DIA0, DIA1, DIA2, DIA3, DIA4, DIA5, DIA6, DIA7, DIA8, DIA9, DIA10, DIA11, DIA12, DIA13, DIA14, DIA15, DIA16, DIA17, ADA0, ADA1, ADA2, ADA3, ADA4, ADA5, ADA6, ADA7, ADA8, ADA9, ADA10, ADA11, ADA12, ADA13, CEA, CLKA, WEA, CSA0, CSA1, CSA2, RSTA, DIB0, DIB1, DIB2, DIB3, DIB4, DIB5, DIB6, DIB7, DIB8, DIB9, DIB10, DIB11, DIB12, DIB13, DIB14, DIB15, DIB16, DIB17, ADB0, ADB1, ADB2, ADB3, ADB4, ADB5, ADB6, ADB7, ADB8,

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ADB9, ADB10, ADB11, ADB12, ADB13, CEB, CLKB, WEB, CSB0, CSB1, CSB2, RSTB, DOA0, DOA1, DOA2, DOA3, DOA4, DOA5, DOA6, DOA7, DOA8, DOA9, DOA10, DOA11, DOA12, DOA13, DOA14, DOA15, DOA16, DOA17, DOB0, DOB1, DOB2, DOB3, DOB4, DOB5, DOB6, DOB7, DOB8, DOB9, DOB10, DOB11, DOB12, DOB13, DOB14, DOB15, DOB16, DOB17

ATTRIBUTES (LatticeSC)

DATA_WIDTH_A : 1, 2, 4, 9, 18
DATA_WIDTH_B : 1, 2, 4, 9, 18
REGMODE_A : NOREG, OUTREG
REGMODE_B : NOREG, OUTREG
RESETMODE : ASYNC, SYNC
CSDECODE_A : 000, 001, 010, 011, 100, 101, 110, 111
CSDECODE_B : 000, 001, 010, 011, 100, 101, 110, 111
WRITEMODE_A : NORMAL, WRITETHROUGH, READBEFOREWRITE
WRITEMODE_B : NORMAL, WRITETHROUGH, READBEFOREWRITE
DISABLED_GSR : 0, 1
INIT : DISABLED, ENABLED
INIT_RECFG : DISABLED, ENABLED
INIT_ID : "0000000000"

Description:

Dual Port RAM. See “Dual Port RAM Port Definitions” on page 2.

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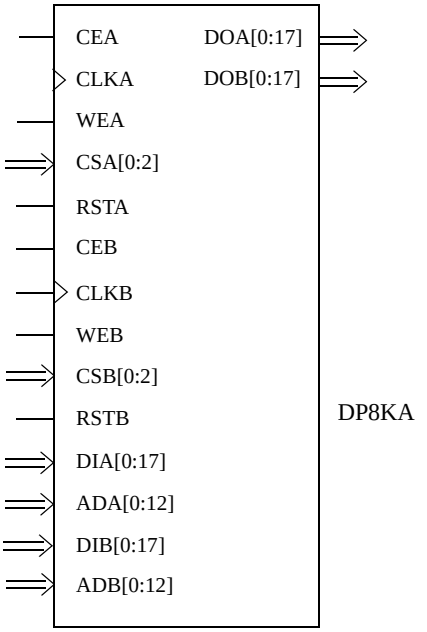
DP8KA

8K Dual Port Block RAM

Lattice FPGA		
SC	XP	EC
	✓	✓



NOTE: The graphic is shown in bus notation for convenience. This element must be instantiated in expanded bus notation format with each individual bit as given below.

INPUT : CEA, CLKA, WEA, CSA0, CSA1, CSA2, RSTA, CEB, CLKB, WEB, CSB0, CSB1, CSB2, RSTB, DIA0, DIA1, DIA2, DIA3, DIA4, DIA5, DIA6, DIA7, DIA8, DIA9, DIA10, DIA11, DIA12, DIA13, DIA14, DIA15, DIA16, DIA17, ADA0, ADA1, ADA2, ADA3, ADA4, ADA5, ADA6, ADA7, ADA8, ADA9, ADA10, ADA11, ADA12, DIB0, DIB1, DIB2, DIB3, DIB4, DIB5, DIB6, DIB7, DIB8, DIB9, DIB10, DIB11, DIB12, DIB13, DIB14, DIB15, DIB16, DIB17, ADB0, ADB1, ADB2, ADB3, ADB4, ADB5, ADB6, ADB7, ADB8, ADB9, ADB10, ADB11, ADB12

OUTPUT : DOA0, DOA1, DOA2, DOA3, DOA4, DOA5, DOA6, DOA7, DOA8, DOA9, DOA10, DOA11, DOA12, DOA13, DOA14, DOA15, DOA16, DOA17, DOB0, DOB1, DOB2, DOB3, DOB4, DOB5, DOB6, DOB7, DOB8, DOB9, DOB10, DOB11, DOB12, DOB13, DOB14, DOB15, DOB16, DOB17

PINORDER:CEA, CLKA, WEA, CSA0, CSA1, CSA2, RSTA, CEB, CLKB, WEB, CSB0, CSB1, CSB2, RSTB, DIA0, DIA1, DIA2, DIA3, DIA4, DIA5, DIA6, DIA7, DIA8, DIA9, DIA10, DIA11, DIA12, DIA13, DIA14, DIA15, DIA16, DIA17, ADA0, ADA1, ADA2, ADA3, ADA4, ADA5, ADA6, ADA7, ADA8, ADA9, ADA10, ADA11, ADA12, DIB0, DIB1, DIB2, DIB3, DIB4, DIB5, DIB6, DIB7, DIB8, DIB9, DIB10, DIB11, DIB12, DIB13, DIB14, DIB15, DIB16, DIB17, ADB0, ADB1, ADB2, ADB3, ADB4, ADB5, ADB6, ADB7, ADB8, ADB9, ADB10, ADB11, ADB12, DOA0,

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DOA1, DOA2, DOA3, DOA4, DOA5, DOA6, DOA7, DOA8, DOA9, DOA10, DOA11, DOA12, DOA13, DOA14, DOA15, DOA16, DOA17, DOB0, DOB1, DOB2, DOB3, DOB4, DOB5, DOB6, DOB7, DOB8, DOB9, DOB10, DOB11, DOB12, DOB13, DOB14, DOB15, DOB16, DOB17

ATTRIBUTES (LatticeXP/EC)

DATA_WIDTH_A : 1, 2, 4, 9, 18
DATA_WIDTH_B : 1, 2, 4, 9, 18
REGMODE_A : NOREG, OUTREG
REGMODE_B : NOREG, OUTREG
RESETMODE : ASYNC, SYNC
CSDECODE_A : 000, 001, 010, 011, 100, 101, 110, 111
CSDECODE_B : 000, 001, 010, 011, 100, 101, 110, 111
WRITEMODE_A : NORMAL, WRITETHROUGH, READBEFOREWRITE
WRITEMODE_B : NORMAL, WRITETHROUGH, READBEFOREWRITE
INITVAL_00 to _3F : 0xXX….X (80 hex characters)

Description:

Dual Port RAM. See “Dual Port RAM Port Definitions” on page 2.

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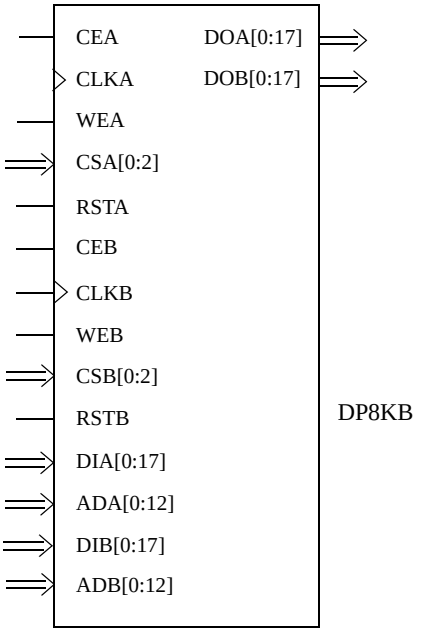
DP8KB

8K Dual Port Block RAM



Lattice FPGA			
SC	XP	EC	MX
			✓

NOTE: The graphic is shown in bus notation for convenience. This element must be instantiated in expanded bus notation format with each individual bit as given below.

INPUT : CEA, CLKA, WEA, CSA0, CSA1, CSA2, RSTA, CEB, CLKB, WEB, CSB0, CSB1, CSB2, RSTB, DIA0, DIA1, DIA2, DIA3, DIA4, DIA5, DIA6, DIA7, DIA8, DIA9, DIA10, DIA11, DIA12, DIA13, DIA14, DIA15, DIA16, DIA17, ADA0, ADA1, ADA2, ADA3, ADA4, ADA5, ADA6, ADA7, ADA8, ADA9, ADA10, ADA11, ADA12, DIB0, DIB1, DIB2, DIB3, DIB4, DIB5, DIB6, DIB7, DIB8, DIB9, DIB10, DIB11, DIB12, DIB13, DIB14, DIB15, DIB16, DIB17, ADB0, ADB1, ADB2, ADB3, ADB4, ADB5, ADB6, ADB7, ADB8, ADB9, ADB10, ADB11, ADB12

OUTPUT : DOA0, DOA1, DOA2, DOA3, DOA4, DOA5, DOA6, DOA7, DOA8, DOA9, DOA10, DOA11, DOA12, DOA13, DOA14, DOA15, DOA16, DOA17, DOB0, DOB1, DOB2, DOB3, DOB4, DOB5, DOB6, DOB7, DOB8, DOB9, DOB10, DOB11, DOB12, DOB13, DOB14, DOB15, DOB16, DOB17

PINORDER:CEA, CLKA, WEA, CSA0, CSA1, CSA2, RSTA, CEB, CLKB, WEB, CSB0, CSB1, CSB2, RSTB, DIA0, DIA1, DIA2, DIA3, DIA4, DIA5, DIA6, DIA7, DIA8, DIA9, DIA10, DIA11, DIA12, DIA13, DIA14, DIA15, DIA16, DIA17, ADA0, ADA1, ADA2, ADA3, ADA4, ADA5, ADA6, ADA7, ADA8, ADA9, ADA10, ADA11, ADA12, DIB0, DIB1, DIB2, DIB3, DIB4, DIB5, DIB6, DIB7, DIB8, DIB9, DIB10, DIB11, DIB12, DIB13, DIB14, DIB15, DIB16, DIB17, ADB0, ADB1, ADB2, ADB3, ADB4, ADB5, ADB6, ADB7, ADB8, ADB9, ADB10, ADB11, ADB12, DOA0,

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DOA1, DOA2, DOA3, DOA4, DOA5, DOA6, DOA7, DOA8, DOA9, DOA10, DOA11, DOA12, DOA13, DOA14, DOA15, DOA16, DOA17, DOB0, DOB1, DOB2, DOB3, DOB4, DOB5, DOB6, DOB7, DOB8, DOB9, DOB10, DOB11, DOB12, DOB13, DOB14, DOB15, DOB16, DOB17

ATTRIBUTES (LatticeXP/EC)

DATA_WIDTH_A : 1, 2, 4, 9, 18
DATA_WIDTH_B : 1, 2, 4, 9, 18
REGMODE_A : NOREG, OUTREG
REGMODE_B : NOREG, OUTREG
RESETMODE : ASYNC, SYNC
CSDECODE_A : 000, 001, 010, 011, 100, 101, 110, 111
CSDECODE_B : 000, 001, 010, 011, 100, 101, 110, 111
WRITEMODE_A : NORMAL, WRITETHROUGH, READBEFOREWRITE
WRITEMODE_B : NORMAL, WRITETHROUGH, READBEFOREWRITE
ARRAY_SIZE : 9216 (number), NOT USED
GSR : ENABLED, DISABLED
INITVAL_00 to _3F : 0xXX….X (80 hex characters)

Description:

Dual Port RAM. See “Dual Port RAM Port Definitions” on page 2. The DP8KB was introduced for MachXO.

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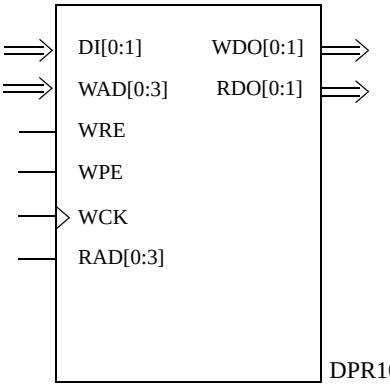
DPR16X2

16K Dual Port Block RAM



Lattice FPGA		
SC	XP	EC
✓		

NOTE: The graphic is shown in bus notation for convenience. This element must be instantiated in expanded bus notation format with each individual bit as given below.

INPUT : DI0, DI1, WAD0, WAD1, WAD2, WAD3, WRE, WPE, WCK, RAD0, RAD1, RAD2, RAD3
OUTPUT : WDO0, WDO1, RDO0, RDO1
PINORDER: DI0, DI1, WAD0, WAD1, WAD2, WAD3, WRE, WPE, WCK, RAD0, RAD1, RAD2, RAD3, WDO0, WDO1, RDO0, RDO1
ATTRIBUTES (LatticeSC)
INITVAL: [63:0] 64'h00000000
DISABLED_GSR: 0, 1

Description:

Dual Port Block RAM. See “Dual Port RAM Port Definitions” on page 2.

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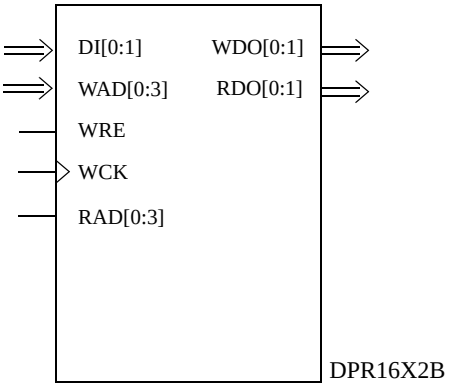
DPR16X2B

16K Dual Port Block RAM



Lattice FPGA		
SC	XP	EC
	✓	✓

NOTE: The graphic is shown in bus notation for convenience. This element must be instantiated in expanded bus notation format with each individual bit as given below.

INPUT : DI0, DI1, WAD0, WAD1, WAD2, WAD3, WRE, WCK, RAD0, RAD1, RAD2, RAD3
OUTPUT : WDO0, WDO1, RDO0, RDO1
PINORDER: DI0, DI1, WAD0, WAD1, WAD2, WAD3, WRE, WCK, RAD0, RAD1, RAD2, RAD3, WDO0, WDO1, RDO0, RDO1
ATTRIBUTES (LatticeSC)
INITVAL: [63:0] 64'h00000000

Description:

Dual Port Block RAM. See “Dual Port RAM Port Definitions” on page 2.

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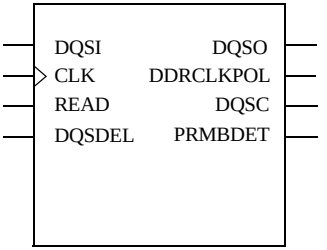
DQSBUFB

DDR DQS Buffer used as DDR memory DQS generator I

Lattice FPGA		
SC	XP	EC
	✓	✓



DQSBUFB

INPUTS: DQSI CLK READ DQSDEL
OUTPUTS: DQSO DDRCLKPOL DQSC PRMBDET
PINORDER: DQSI CLK READ DQSDEL DQSO DDRCLKPOL DQSC PRMBDET
ATTRIBUTES

Description:

This cell is used to indicate how many DDR I/Os need to be tied together, aligning the placement of the DDR cell. The input goes to the clock and the output goes to the clock on the DDR cell.

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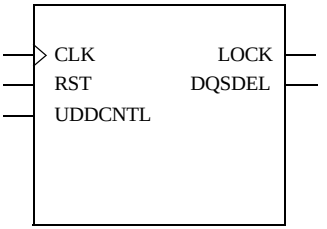
DQSDLL

DLL used as DDR memory DQS DLL I

Lattice FPGA		
SC	XP	EC
	✓	✓



DQSDLL

INPUTS: CLK RST UDDCNTL
OUTPUTS: LOCK DQSDEL
PINORDER: CLK RST UDDCNTL LOCK DQSDEL
ATTRIBUTES

Description:

DLL used as DDR memory DQS DLL. UDDCNTL input is an active low port.

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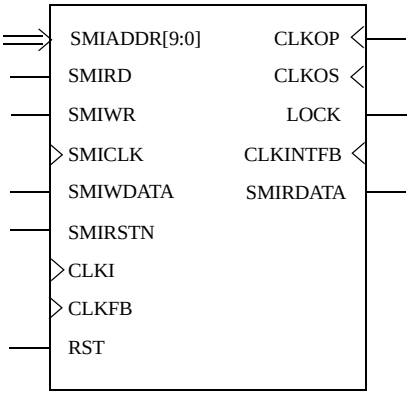
EHXPLLA

Enhanced High Performance with Dynamic Input Delay Control PLL

Lattice FPGA		
SC	XP	EC
✓		



EHXPLLA

NOTE: The graphic is shown in bus notation for convenience. This element must be instantiated in expanded bus notation format with each individual bit as given below

INPUTS: SMIADDR9, SMIADDR8, SMIADDR7, SMIADDR6, SMIADDR5, SMIADDR4, SMIADDR3, SMIADDR2, SMIADDR1, SMIADDR0, SMIRD, SMIWR, SMICLK, SMIWDATA, SMIRSTN, CLKI, CLKFB, RST
OUTPUTS: CLKOP, CLKOS, LOCK, CLKINTFB, SMIRDATA
PINORDER: SMIADDR9, SMIADDR8, SMIADDR7, SMIADDR6, SMIADDR5, SMIADDR4, SMIADDR3, SMIADDR2, SMIADDR1, SMIADDR0, SMIRD, SMIWR, SMICLK, SMIWDATA, SMIRSTN, CLKI, CLKFB, RST, CLKOP, CLKOS, LOCK, CLKINTFB, SMIRDATA
ATTRIBUTES
CLKI_DIV: "1", "2", "3", ... "63", "64"
CLKFB_DIV: "1", "2", "3", ... "63", "64"
CLKOP_DIV: "1", "2", "3", ... "63", "64"
CLKOS_DIV: "1", "2", "3", ... "63", "64"
CLKI_FDEL: 0, 100, 200, ... 700
CLKI_PDEL: "DEL0", "DEL1", "DEL2", "DEL3"
CLKFB_FDEL: 0, 100, 200, ... 700
CLKFB_PDEL: "DEL0", "DEL1", "DEL2", "DEL3"
CLKOP_MODE: BYPASS, FDEL0, VCO, DIV
CLKOS_MODE: BYPASS, FDEL, VCO, DIV
CLKOS_FDEL: 0, 100, 200, ... 700
CLKOS_DIV_ADJ: DISABLED, ENABLED
CLKOS_DIV_ADJVAL: <string>
PHASEADJ: 0, 45, 90, 135, 190, 225, 270, 315
DISABLED_GSR: 0, 1

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VCO_LOWERFREQ: DISABLED, ENABLED
GMCFREQSEL: HIGH, LOW
FREQLOCK: ENABLED, DISABLED
PHASELOCK: ENABLED, DISABLED
LF_IX5UA: 0, 1, ...31
LF_RESISTOR: 0b000000, ...
SPREAD: DISABLED, ENABLED
SPREAD_DIV1: 2, 3, 4, ... 8
SPREAD_DIV2: 2, 4, 8, 16, 32, 128, ... 4096, 8192
SPREAD_DRIFT: 1, 2, 3
SPREAD_FILTER: DISABLED, ENABLED
SMI_ID: 000000, 000001, ... 111111
ADDR_DIS: 0000000000, 0000000001, ... 1111111111

Description:

The Enhanced Extended Performance PLL (EHXPLLA) includes all features available in the PLL. This element includes SMI access so that you may configure the PLL as you require. The EHXPLLA element can be created through Module/IP Manager.

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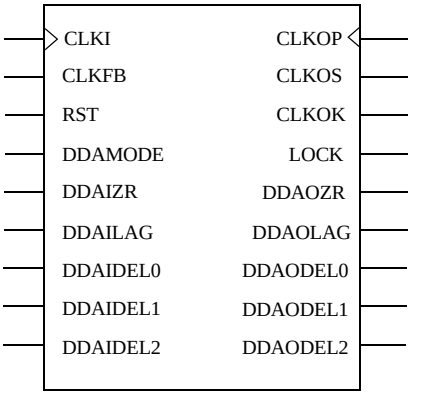
EHXPLLB

Enhanced High Performance with Dynamic Input Delay Control PLL

Lattice FPGA		
SC	XP	EC
	✓	✓



EHXPLLB

INPUTS: CLKI CLKFB RST DDAMODE DDAIZR DDAILAG DDAIDEL0 DDAIDEL1 DDAIDEL2
OUTPUTS: CLKOP CLKOS CLKOK LOCK DDAOZR DDAOLAG DDAODEL0 DDAODEL1 DDAODEL2
PINORDER: CLKI CLKFB RST DDAMODE DDAIZR DDAILAG DDAIDEL0 DDAIDEL1 DDAIDEL2 CLKOP CLKOS CLKOK LOCK DDAOZR DDAOLAG DDAODEL0 DDAODEL1 DDAODEL2
ATTRIBUTES
FIN: 20.0000 to 420.0000 (MHz)
CLKI_DIV: 1 to 256 (defaut is 1)
CLKFB_DIV: 1 to 256 (defaut is 1)
CLKOP_DIV: 2,4,6,..,126,128
CLKOK_DIV: 2,4,6,..,126,128 (default is 2)
FDEL: -8 to 80 (default is 0)
PHASEADJ: 0, 45, 90...315 (default is 0)
DUTY: 1 to 7 (default is 4)
WAKE_ON_LOCK: ON, OFF (default)
DELAY_CNTL: DYNAMIC, STATIC (default)

Description:

The following are descriptions of EHXPLLB pin functions.

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Input pins:

Pin	Function
CLKI	Global clock input; freq. 20 – 420 MHz
CLKFB	External feedback, Internal feedback from CLKOP Divider; freq. 20 – 420 MHz
RST	“1” to Reset M-divider
DDAMODE	DDA Mode. “1” Pin control (dynamic), “0” : Fuse Control (static)
DDAIZR	DDA Delay Zero. “1” : delay = 0, “0” : delay = on
DDAILAG	DDA Lag/Lead. “1” : Lag, “0” : Lead
DDAIDEL[0:2]	DDA Delay

Output pins:

Pin	Function
CLKOP	PLL output clock to clock tree (No phase shift); freq. 20 – 420 MHz
CLKOS	PLL output clock to clock tree (phase shifted/duty cycle changed); freq. 20 – 420 MHz
CLKOK	PLL output to clock tree (K divider, low speed, output); freq. 0.156 – 210 MHz.
LOCK	“1” indicates PLL LOCK to CLK_IN
DDAOZR	DDA Delay Zero Output
DDAOLAG	DDA Lag/Lead Output
DDAODEL[0:2]	DDA Delay Output

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Dynamic Delay Adjustment

The Dynamic Delay Adjustment is controlled by DDAMODE input. This feature is available in EHXPLLB primitive only. When the DDAMODE input is set to “1”, the delay control is done through the inputs, DDAIZR, DDAILAG and DDAIDEL(2:0). For this mode, the attribute “DELAY_CNTL” must be set to “DYNAMIC”.

Equations for Generating Input and Output Frequency Ranges

These values of f_{IN}, f_{OUT}, f_{VCO} are the absolute frequency ranges for the PLL. The values of f_{INMIN}, f_{INMAX}, f_{OUTMIN}, and f_{OUTMAX}, are the calculated frequency ranges based on the divider settings. These calculated frequency ranges become the limits for the specific divider settings used in the design.

$f_{OUT} = f_{IN} * (N/M)$
$f_{VCO} = f_{OUT} * V = f_{IN} * (N/M) * V$
$f_{IN} = (f_{VCO} /(V*N))*M$

Where M = CLKI DIV

N = CLKFB DIV
V = CLKOP DIV
K = CLKOK DIV

$f_{INMIN} = ((f_{VCOMIN} /(V*N))*M$, if below 33 * M round up to 33 * M
$f_{INMAX} = (f_{VCOMAX}/(V*N))*M$, if above 420 round down to 420
$f_{OUTMIN} = f_{INMIN}*(N/M)$, if below 33 * N round up to 33 * N
$f_{OUTMAX} = f_{INMAX}*(N/M)$, if above 420 round down to 420

$f_{OUTKMIN} = f_{OUTMIN} /K$
$f_{OUTKMAX} = f_{OUTMAX} /K$

For more description on LatticeXP and LatticeEC PLL cells and their usage, see related application notes for usage models or contact technical support.

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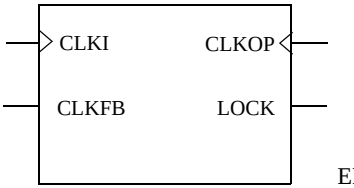
EPLLB

Enchanced PLL

Lattice FPGA		
SC	XP	EC
	✓	✓



EPLLB

INPUTS: CLKI CLKFB
OUTPUTS: CLKOP LOCK
PINORDER: CLKI CLKFB CLKOP LOCK
ATTRIBUTES
FIN: 20.0000 to 420.0000 (MHz)
CLKI_DIV: 1 to 256 (defaut is 1)
CLKFB_DIV: 1 to 256 (defaut is 1)
CLKOP_DIV: 2,4,6,..,126,128
FDEL: -8 to 80 (default is 0)
WAKE_ON_LOCK: ON, OFF (default)

Description:

The following are descriptions of EHXPLLB pin functions.

Input pins:

Pin	Function
CLKI	Global clock input; freq. 20 – 420 MHz
CLKFB	External feedback, Internal feedback from CLKOP Divider; freq. 20 – 420 MHz

Output pins:

Pin	Function
CLKOP	PLL output clock to clock tree (No phase shift); freq. 20 – 420 MHz

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LOCK	“1” indicates PLL LOCK to CLK_IN

For more description on LatticeXP and LatticeEC PLL cells and their usage, see related application notes for usage models or contact technical support.

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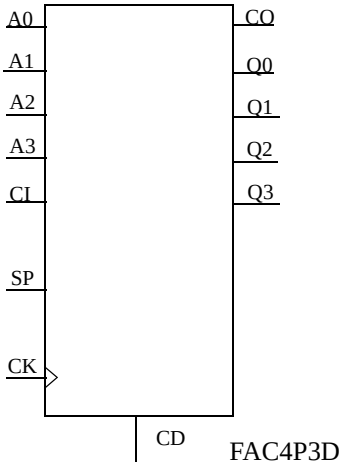
FAC4P3D

4 Bit Fast Accumulator with Positive Level Enable and Positive Level Asynchronous Clear

ORCA Series		
2	3	4
✓		



FAC4P3D

INPUTS: A0,A1,A2,A3,CI,SP,CK,CD
OUTPUTS: CO,Q0,Q1,Q2,Q3
PINORDER: A0 A1 A2 A3 CI SP CK CD CO Q0 Q1 Q2 Q3
MINIMUM CELL AREA: 1.0

Truth Table:

INPUTS					OUTPUTS	
CI	A[0:3]	SP	CD	CK	CO	Q[0:3]
X	X	X	1	X	CI + A + Q	
X	X	0	0	0	CI + A + Q	
CI	A[0:3]	1	0	↑	CI + A + Q	

X = Don’t care

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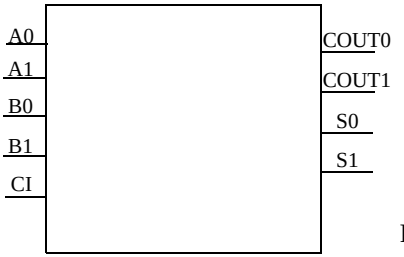
FADD2

Fast 2 Bit Adder

Lattice FPGA		
SC	XP	EC
✓	✓	✓



FADD2

INPUTS: A1, A0, B1, B0, CI
OUTPUTS: COUT1, COUT0, S1, S0
PINORDER: A1, A0, B1, B0, CI, COUT1, COUT0, S1, S0

Description:

FADD2 is a 2-bit adder. It has a carry-in input (CI) and two 2-bit input (A0, A1 and B0, B1). The FADD2 produces a 2-bit sum output (S0, S1) along with a 2-bit carry-out output (COUT1, COUT).

Example pin functions:

Function	Pins
input	A1, A0, B1, B0
output	S1, S0
carry-in input	CI
carry-out output (Bit-0)	COUT0
carry-out output (Bit-1)	COUT1

continued

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Truth Table:

INPUTS					OUTPUTS			
A0	A1	B0	B1	CI	S0	COUT0	S0	COUT1
0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	1	0	1
0	0	1	1	0	0	1	0	1
1	1	1	1	0	1	0	1	0
0	0	0	0	1	0	1	0	1
1	1	0	0	1	1	0	1	0
0	0	1	1	1	1	0	1	0
1	1	1	1	1	1	1	1	1

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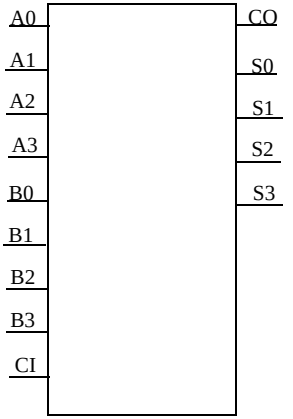
FADD4

4 Bit Fast Adder

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



FADD4

INPUTS: A0,A1,A2,A3,B0,B1,B2,B3,CI
OUTPUTS: CO,S0,S1,S2,S3
PINORDER: A0 A1 A2 A3 B0 B1 B2 B3 CI CO S0 S1 S2 S3
MINIMUM CELL AREA (2A/2T): 0.5
MINIMUM CELL AREA (Series 3): 0.25

Description:

FADD4 is a 4 bit adder. It has a carry-in input (CI) and two 4 bit inputs (A0:A3 and B0:B3). The FADD4 produces a 4 bit sum output (S0:S3) along with a carry-out output (CO).

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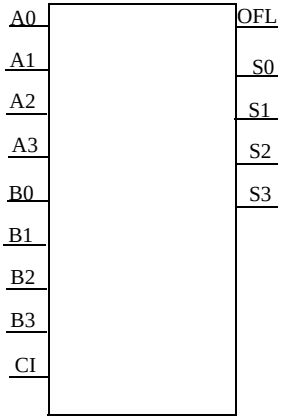
FADD4O

4 Bit Fast Adder with Overflow

ORCA Series		
2	3	4
✓	✓	✓



FADD4O

INPUTS: A0,A1,A2,A3,B0,B1,B2,B3,CI
OUTPUTS: OFL,S0,S1,S2,S3
PINORDER: A0 A1 A2 A3 B0 B1 B2 B3 CI OFL S0 S1 S2 S3
MINIMUM CELL AREA (2A/2T): 0.5
MINIMUM CELL AREA (Series 3): 0.25

Description:

FADD4O is a 4 bit adder with overflow. It has a carry-in input (CI) and two 4 bit inputs (A0:A3 and B0:B3). The FADD4O produces a 4 bit sum output (S0:S3) along with an overflow output (OFL), which is the exclusive-OR of the carry-in to S3 and the carry-out from S3.

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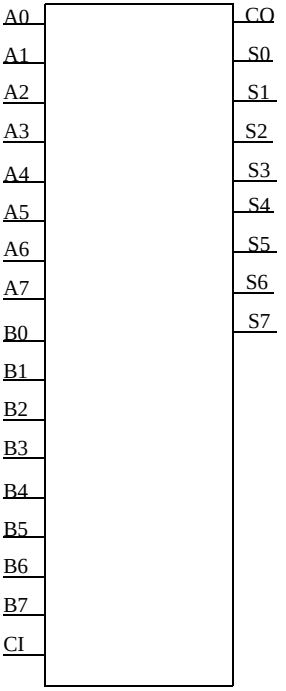
FADD8

8 Bit Fast Adder

ORCA Series/Lattice FPGA				
3	4	SC	XP	EC
✓	✓	✓	✓	✓



FADD8

INPUTS: A0,A1,A2,A3,A4,A5,A6,A7,B0,B1,B2,B3,B4,B5,B6,B7,CI
OUTPUTS: CO,S0,S1,S2,S3,S4,S5,S6,S7
PINORDER: A0 A1 A2 A3 A4 A5 A6 A7 B0 B1 B2 B3 B4 B5 B6 B7 CI CO
S0 S1 S2 S3 S4 S5 S6 S7
MINIMUM CELL AREA: 0.5

Description:

FADD8 is an 8 bit adder. It has a carry-in input (CI) and two 8 bit inputs (A7:A0 and B7:B0). The FADD8 produces an 8 bit sum output (S7:S0) along with a carry-out output (CO).

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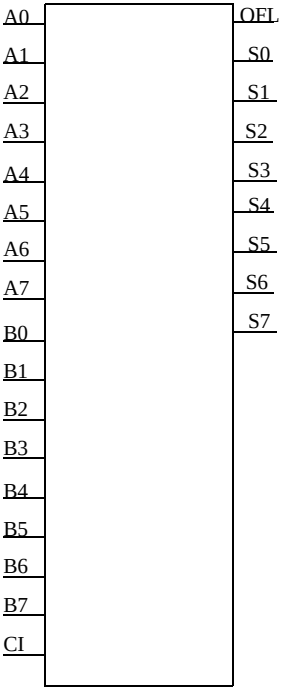
FADD8O

8 Bit Fast Adder with Overflow

ORCA Series		
2	3	4
	✓	✓



FADD80

INPUTS: A0,A1,A2,A3,A4,A5,A6,A7,B0,B1,B2,B3,B4,B5,B6,B7,CI
OUTPUTS: OFL,S0,S1,S2,S3,S4,S5,S6,S7
PINORDER: A0 A1 A2 A3 A4 A5 A6 A7 B0 B1 B2 B3 B4 B5 B6 B7 CI OFL
S0 S1 S2 S3 S4 S5 S6 S7
MINIMUM CELL AREA: 0.5

Description:

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FADD8O is an 8 bit adder with overflow. It has a carry-in input (CI) and two 8 bit inputs (A7:A0 and B7:B0). The FADD8O produces an 8 bit sum output (S7:S0) along with an overflow output (OFL), which is the exclusive-OR of the carry-in to S7 and the carry-out from S7.

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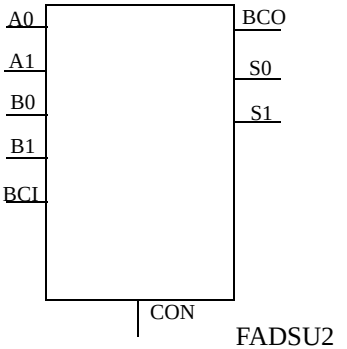
FADSU2

2 Bit Fast Adder/Subtracter (two's complement)

ORCA Series/Lattice FPGA					
2	3	4	XP	EC	MX
✓	✓	✓	✓	✓	✓



FADSU2

INPUTS: A0,A1,B0,B1,BCI,CON
OUTPUTS: BCO,S0,S1
PINORDER: A0 A1 B0 B1 BCI CON BCO S0 S1

Description:

FADSU2 is a 2 bit adder/subtracter. See FADSU4 for details on functionality.

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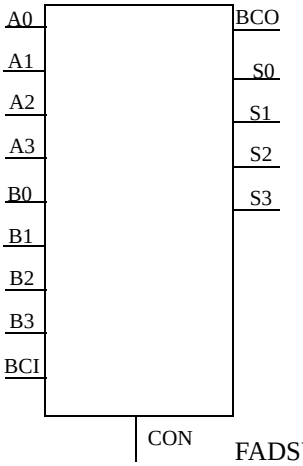
FADSU4

4 Bit Fast Adder/Subtracter (two's complement)

ORCA Series/Lattice FPGA				
2	3	4	XP	EC
✓	✓	✓	✓	✓



FADSU4

INPUTS: A0,A1,A2,A3,B0,B1,B2,B3,BCI,CON
OUTPUTS: BCO,S0,S1,S2,S3
PINORDER: A0 A1 A2 A3 B0 B1 B2 B3 BCI CON BCO S0 S1 S2 S3
MINIMUM CELL AREA (2A/2T): 0.5
MINIMUM CELL AREA (Series 3): 0.25

Description:

FADSU4 is a 4 bit adder/subtracter. When the control signal (CON) is high FADSU4 functions as a 4 bit adder with a carry-in input (BCI) and two 4 bit inputs (A0:A3 and B0:B3), producing a 4 bit SUM output (S0:S3) along with a carry-out output (BCO).

When the control signal (CON) is low FADSU4 functions as a 4 bit two's complement subtracter with a borrow-in input (BCI) and two 4 bit inputs (A0:A3 and B0:B3), producing a 4 bit two's complement output of A minus B (S0:S3) along with a borrow-out output (BCO).

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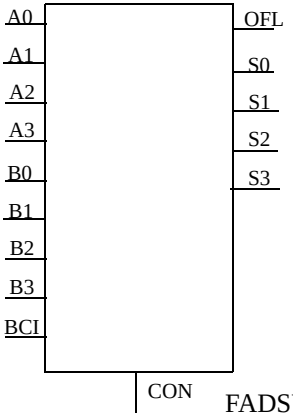
FADSU4O

4 Bit Fast Adder/Subtracter (two's complement) with Overflow

ORCA Series		
2	3	4
✓	✓	✓



FADSU4O

INPUTS: A0,A1,A2,A3,B0,B1,B2,B3,BCI,CON
OUTPUTS: OFL,S0,S1,S2,S3
PINORDER: A0 A1 A2 A3 B0 B1 B2 B3 BCI CON OFL S0 S1 S2 S3
MINIMUM CELL AREA (2A/2T): 0.5
MINIMUM CELL AREA (Series 3): 0.25

Description:

FADSU4O is a 4 bit adder/subtracter (two's complement) with overflow. When the control signal (CON) is high FADSU4O functions as a 4 bit adder with a carry-in input (BCI) and two 4 bit inputs (A0:A3 and B0:B3), producing a 4 bit sum output (S0:S3) along with an overflow output (OFL), which is the exclusive-OR of the BCI and the carry-out that is internally generated during the addition.

When the control signal (CON) is low FADSU4O functions as a 4 bit two's complement subtracter with a borrow-in input (BCI) and two 4 bit inputs (A0:A3 and B0:B3), producing a 4 bit two's complement output of A minus B (S0:S3) along with an overflow output (OFL), which is the exclusive-OR of the carry-in to S3 and the carry-out from S3.

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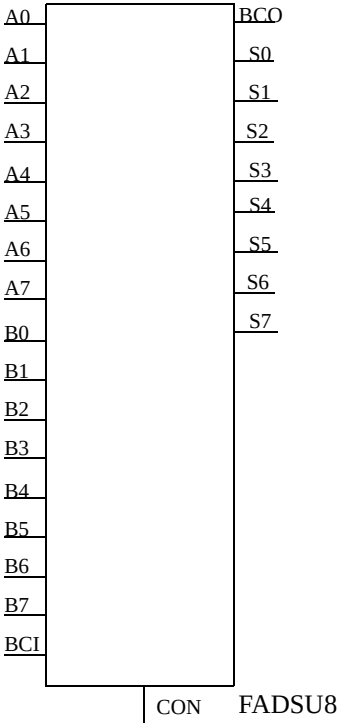
FADSU8

8 Bit Fast Adder/Subtracter (two's complement)

ORCA Series/Lattice FPGA				
3	4	SC	XP	EC
✓	✓	✓	✓	✓



INPUTS: A0,A1,A2,A3,A4,A5,A6,A7,B0,B1,B2,B3,B4,B5,B6,B7,BCI,CON
OUTPUTS: BCO,S0,S1,S2,S3,S4,S5,S6,S7
PINORDER: A0 A1 A2 A3 A4 A5 A6 A7 B0 B1 B2 B3 B4 B5 B6 B7 BCI CON BCO S0 S1 S2 S3 S4 S5 S6 S7
MINIMUM CELL AREA: 0.5

continued

Description:

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FADSU8 is an 8 bit adder/subtracter. When the control signal (CON) is high FADSU8 functions as an 8 bit adder with a carry-in input (BCI) and two 8 bit inputs (A7:A0 and B7:B0), producing an 8 bit SUM output (S7:S0) along with a carry-out output (BCO).

When the control signal (CON) is low FADSU8 functions as an 8 bit two's complement subtracter with a borrow-in input (BCI) and two 8 bit inputs (A7:A0 and B7:B0), producing an 8 bit two's complement output of A minus B (S7:S0) along with a borrow-out output (BCO).

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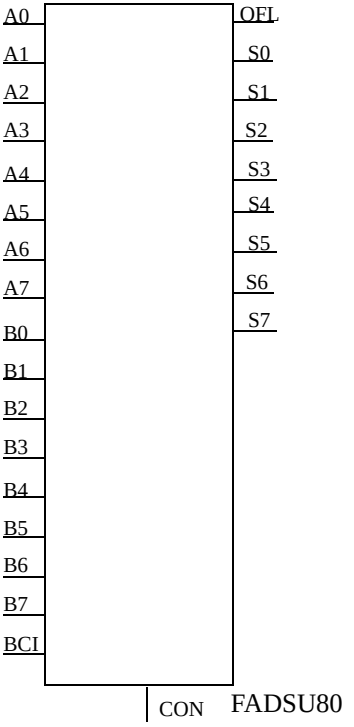
FADSU8O

8 Bit Fast Adder/Subtracter (two's complement) with Overflow

ORCA Series		
2	3	4
	✓	✓



INPUTS: A0,A1,A2,A3,A4,A5,A6,A7,B0,B1,B2,B3,B4,B5,B6,B7,BCI,CON
OUTPUTS: OFL,S0,S1,S2,S3,S4,S5,S6,S7
PINORDER: A0 A1 A2 A3 A4 A5 A6 A7 B0 B1 B2 B3 B4 B5 B6 B7 BCI CON OFL S0 S1 S2 S3 S4 S5 S6 S7
MINIMUM CELL AREA: 0.5

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Description:

FADSU8O is an 8 bit adder/subtracter (two's complement) with overflow. When the control signal (CON) is high FADSU8O functions as an 8 bit adder with a carry-in input (BCI) and two 8 bit inputs (A7:A0 and B7:B0), producing an 8 bit sum output (S7:S0) along with an overflow output (OFL), which is the exclusive-OR of the BCI and the carry-out that is internally generated during the addition.

When the control signal (CON) is low FADSU8O functions as an 8 bit two's complement subtracter with a borrow-in input (BCI) and two 8 bit inputs (A7:A0 and B7:B0), producing an 8 bit two's complement output of A minus B (S7:S0) along with an overflow output (OFL), which is the exclusive-OR of the carry-in to S7 and the carry-out from S7.

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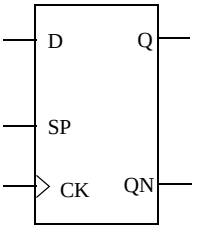
FD1P3AX

Positive Edge Triggered D Flip-Flop with Positive Level Enable, GSR used for Clear

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



FD1P3AX

NOTE: The QN output pin does not exist for FPGA architectures higher than ORCA Series 4. It is not recommended to migrate ORCA netlists to Lattice-based FPGA architectures for this reason. Synthesize your netlist using the appropriate Lattice-based libraries.

INPUTS: D,SP,CK
OUTPUTS: Q,QN
PINORDER: D SP CK Q QN
MINIMUM CELL AREA (2A/2T): 0.125
MINIMUM CELL AREA (Series 3): 0.0625

Truth Table:

INPUTS			OUTPUTS	
D	SP	CK	Q	QN
X	0	X	Q	QN
0	1	↑	0	1
1	1	↑	1	0

X = Don’t care
When GSR=0, Q=0, QN=1 (D=SP=CK=X)

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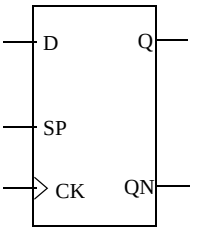
FD1P3AY

Positive Edge Triggered D Flip-Flop with Positive Level Enable, GSR used for Preset

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



FD1P3AY

NOTE: The QN output pin does not exist for FPGA architectures higher than ORCA Series 4. It is not recommended to migrate ORCA netlists to Lattice-based FPGA architectures for this reason. Synthesize your netlist using the appropriate Lattice-based libraries.

INPUTS: D,SP,CK
OUTPUTS: Q,QN
PINORDER: D SP CK Q QN
MINIMUM CELL AREA (2A/2T): 0.125
MINIMUM CELL AREA (Series 3): 0.0625

Truth Table:

INPUTS			OUTPUTS	
D	SP	CK	Q	QN
X	0	X	Q	QN
0	1	↑	0	1
1	1	↑	1	0

X = Don’t care
When GSR=0, Q=1, QN=0 (D=SP=CK=X)

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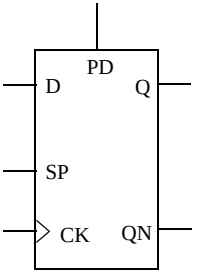
FD1P3BX

Positive Edge Triggered D Flip-Flop with Positive Level Enable and Positive Level Asynchronous Preset

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



FD1P3BX

NOTE: The QN output pin does not exist for FPGA architectures higher than ORCA Series 4. It is not recommended to migrate ORCA netlists to Lattice-based FPGA architectures for this reason. Synthesize your netlist using the appropriate Lattice-based libraries.

INPUTS: D,SP,CK,PD
OUTPUTS: Q,QN
PINORDER: D SP CK PD Q QN
MINIMUM CELL AREA (2A/2T): 0.125
MINIMUM CELL AREA (Series 3): 0.0625

Truth Table:

INPUTS				OUTPUTS	
D	SP	CK	PD	Q	QN
X	0	X	0	Q	QN
X	X	X	1	1	0
0	1	↑	0	0	1
1	1	↑	0	1	0

X = Don’t care
When GSR=0, Q=1, QN=0 (D=SP=CK=PD=X)

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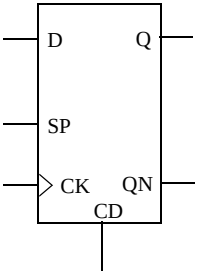
FD1P3DX

Positive Edge Triggered D Flip-Flop with Positive Level Enable and Positive Level Asynchronous Clear

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



FD1P3DX

NOTE: The QN output pin does not exist for FPGA architectures higher than ORCA Series 4. It is not recommended to migrate ORCA netlists to Lattice-based FPGA architectures for this reason. Synthesize your netlist using the appropriate Lattice-based libraries.

INPUTS: D,SP,CK,CD
OUTPUTS: Q,QN
PINORDER: D SP CK CD Q QN
MINIMUM CELL AREA (2A/2T): 0.125
MINIMUM CELL AREA (Series 3): 0.0625

Truth Table:

INPUTS				OUTPUTS	
D	SP	CK	CD	Q	QN
X	0	X	0	Q	QN
X	X	X	1	0	1
0	1	↑	0	0	1
1	1	↑	0	1	0

X = Don’t care
When GSR=0, Q=0, QN=1 (D=SP=CK=CD=X)

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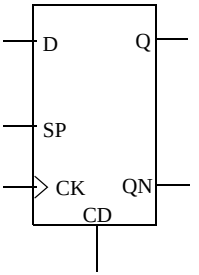
FD1P3IX

Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Clear and Positive Level Enable (Clear overrides Enable)

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



FD1P3IX

NOTE: The QN output pin does not exist for FPGA architectures higher than ORCA Series 4. It is not recommended to migrate ORCA netlists to Lattice-based FPGA architectures for this reason. Synthesize your netlist using the appropriate Lattice-based libraries.

INPUTS: D,SP,CK,CD
OUTPUTS: Q,QN
PINORDER: D SP CK CD Q QN
MINIMUM CELL AREA (2A/2T): 0.125
MINIMUM CELL AREA (Series 3): 0.0625

Truth Table:

INPUTS				OUTPUTS	
D	SP	CK	CD	Q	QN
X	0	X	0	Q	QN
X	X	↑	1	0	1
0	1	↑	0	0	1
1	1	↑	0	1	0

X = Don’t care
When GSR=0, Q=0, QN=1 (D=SP=CK=CD=X)

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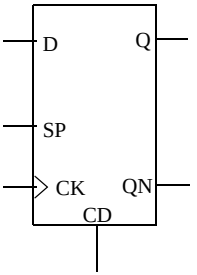
FD1P3IZ

Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Clear and Positive Level Enable (Enable overrides Clear)

ORCA Series		
2	3	4
✓	✓	✓



FD1P3IZ

NOTE: The QN output pin does not exist for FPGA architectures higher than ORCA Series 4. It is not recommended to migrate ORCA netlists to Lattice-based FPGA architectures for this reason. Synthesize your netlist using the appropriate Lattice-based libraries.

INPUTS: D,SP,CK,CD
OUTPUTS: Q,QN
PINORDER: D SP CK CD Q QN
MINIMUM CELL AREA (2A/2T): 0.125
MINIMUM CELL AREA (Series 3): 0.0625

Truth Table:

INPUTS				OUTPUTS	
D	SP	CK	CD	Q	QN
X	0	X	X	Q	QN
X	1	↑	1	0	1
0	1	↑	0	0	1
1	1	↑	0	1	0

X = Don’t care
When GSR=0, Q=0, QN=1 (D=SP=CK=CD=X)

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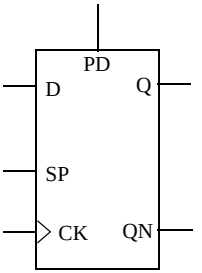
FD1P3JX

Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Preset and Positive Level Enable (Preset overrides Enable)

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



FD1P3JX

NOTE: The QN output pin does not exist for FPGA architectures higher than ORCA Series 4. It is not recommended to migrate ORCA netlists to Lattice-based FPGA architectures for this reason. Synthesize your netlist using the appropriate Lattice-based libraries.

INPUTS: D,SP,CK,PD
OUTPUTS: Q,QN
PINORDER: D SP CK PD Q QN
MINIMUM CELL AREA (2A/2T): 0.125
MINIMUM CELL AREA (Series 3): 0.0625

Truth Table:

INPUTS				OUTPUTS	
D	SP	CK	PD	Q	QN
X	0	X	0	Q	QN
X	X	↑	1	1	0
0	1	↑	0	0	1
1	1	↑	0	1	0

X = Don’t care
When GSR=0, Q=1, QN=0 (D=SP=CK=PD=X)

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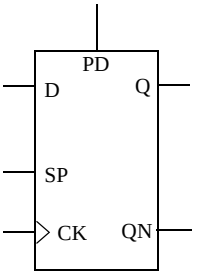
FD1P3JZ

Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Preset and Positive Level Enable (Enable overrides Preset)

ORCA Series		
2	3	4
✓	✓	✓



FD1P3JZ

NOTE: The QN output pin does not exist for FPGA architectures higher than ORCA Series 4. It is not recommended to migrate ORCA netlists to Lattice-based FPGA architectures for this reason. Synthesize your netlist using the appropriate Lattice-based libraries.

INPUTS: D,SP,CK,PD
OUTPUTS: Q,QN
PINORDER: D SP CK PD Q QN
MINIMUM CELL AREA (2A/2T): 0.125
MINIMUM CELL AREA (Series 3): 0.0625

Truth Table:

INPUTS				OUTPUTS	
D	SP	CK	PD	Q	QN
X	0	X	X	Q	QN
X	1	↑	1	1	0
0	1	↑	0	0	1
1	1	↑	0	1	0

X = Don’t care
When GSR=0, Q=1, QN=0 (D=SP=CK=PD=X)

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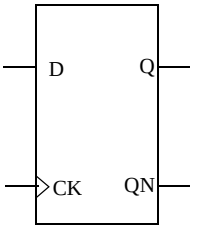
FD1S1A

Positive Level Data Latch with GSR Used for Clear

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



FD1S1A

NOTE: The QN output pin does not exist for FPGA architectures higher than ORCA Series 4. It is not recommended to migrate ORCA netlists to Lattice-based FPGA architectures for this reason. Synthesize your netlist using the appropriate Lattice-based libraries.

INPUTS: D,CK
OUTPUTS: Q,QN
PINORDER: D CK Q QN
MINIMUM CELL AREA (2A/2T): 0.125
MINIMUM CELL AREA (Series 3): 0.0625

Truth Table:

INPUTS		OUTPUTS	
D	CK	Q	QN
X	0	Q	QN
0	1	0	1
1	1	1	0

X = Don’t care
When GSR=0, Q=0, QN=1 (D=CK=X)

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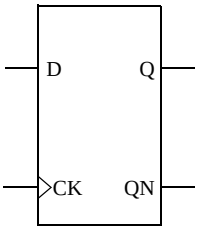
FD1S1AY

Positive Level Data Latch with GSR Used for Preset

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



FD1S1AY

NOTE: The QN output pin does not exist for FPGA architectures higher than ORCA Series 4. It is not recommended to migrate ORCA netlists to Lattice-based FPGA architectures for this reason. Synthesize your netlist using the appropriate Lattice-based libraries.

INPUTS: D,CK
OUTPUTS: Q,QN
PINORDER: D CK Q QN
MINIMUM CELL AREA (2A/2T): 0.125
MINIMUM CELL AREA (Series 3): 0.0625

Truth Table:

INPUTS		OUTPUTS	
D	CK	Q	QN
X	0	Q	QN
0	1	0	1
1	1	1	0

X = Don’t care
When GSR=0, Q=1, QN=0 (D=CK=X)

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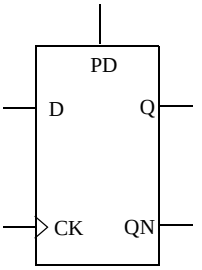
FD1S1B

Positive Level Data Latch with Positive Level Asynchronous Preset

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



FD1S1B

NOTE: The QN output pin does not exist for FPGA architectures higher than ORCA Series 4. It is not recommended to migrate ORCA netlists to Lattice-based FPGA architectures for this reason. Synthesize your netlist using the appropriate Lattice-based libraries.

INPUTS: D,CK,PD
OUTPUTS: Q,QN
PINORDER: D CK PD Q QN
MINIMUM CELL AREA (2A/2T): 0.125
MINIMUM CELL AREA (Series 3): 0.0625

Truth Table:

INPUTS			OUTPUTS	
D	CK	PD	Q	QN
X	0	0	Q	QN
X	X	1	1	0
0	1	0	0	1
1	1	0	1	0

X= Don’t care
When GSR=0, Q=1, QN=0 (D=CK=PD=X)

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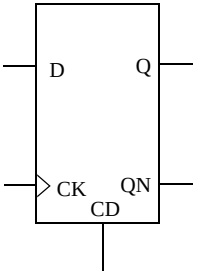
FD1S1D

Positive Level Data Latch with Positive Level Asynchronous Clear

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



FD1S1D

NOTE: The QN output pin does not exist for FPGA architectures higher than ORCA Series 4. It is not recommended to migrate ORCA netlists to Lattice-based FPGA architectures for this reason. Synthesize your netlist using the appropriate Lattice-based libraries.

INPUTS: D,CK,CD
OUTPUTS: Q,QN
PINORDER: D CK CD Q QN
MINIMUM CELL AREA (2A/2T): 0.125
MINIMUM CELL AREA (Series 3): 0.0625

Truth Table:

INPUTS			OUTPUTS	
D	CK	CD	Q	QN
X	0	0	Q	QN
X	X	1	0	1
0	1	0	0	1
1	1	0	1	0

X = Don’t care
When GSR=0, Q=0, QN=1 (D=CK=CD=X)

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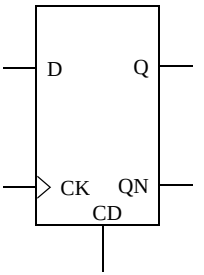
FD1S1I

Positive Level Data Latch with Positive Level Synchronous Clear

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



FD1S1I

NOTE: The QN output pin does not exist for FPGA architectures higher than ORCA Series 4. It is not recommended to migrate ORCA netlists to Lattice-based FPGA architectures for this reason. Synthesize your netlist using the appropriate Lattice-based libraries.

INPUTS: D,CK,CD
OUTPUTS: Q,QN
PINORDER: D CK CD Q QN
MINIMUM CELL AREA (2A/2T): 0.125
MINIMUM CELL AREA (Series 3): 0.0625

Truth Table:

INPUTS			OUTPUTS	
D	CK	CD	Q	QN
X	0	0	Q	QN
X	1	1	0	1
0	1	0	0	1
1	1	0	1	0

X = Don’t care
When GSR=0, Q=0, QN=1 (D=CK=CD=X)

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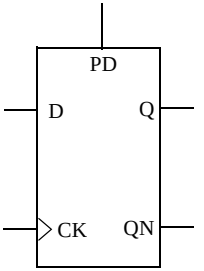
FD1S1J

Positive Level Data Latch with Positive Level Synchronous Preset

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



FD1S1J

NOTE: The QN output pin does not exist for FPGA architectures higher than ORCA Series 4. It is not recommended to migrate ORCA netlists to Lattice-based FPGA architectures for this reason. Synthesize your netlist using the appropriate Lattice-based libraries.

INPUTS: D,CK,PD
OUTPUTS: Q,QN
PINORDER: D CK PD Q QN
MINIMUM CELL AREA (2A/2T): 0.125
MINIMUM CELL AREA (Series 3): 0.0625

Truth Table:

INPUTS			OUTPUTS	
D	CK	PD	Q	QN
X	0	0	Q	QN
X	1	1	1	0
0	1	0	0	1
1	1	0	1	0

X = Don’t care
When GSR=0, Q=1, QN=0 (D=CK=PD=X)

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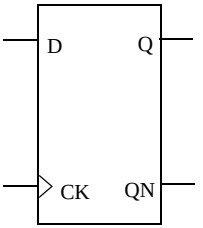
FD1S3AX

Positive Edge Triggered D Flip-Flop, GSR Used for Clear

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



FD1S3AX

NOTE: The QN output pin does not exist for FPGA architectures higher than ORCA Series 4. It is not recommended to migrate ORCA netlists to Lattice-based FPGA architectures for this reason. Synthesize your netlist using the appropriate Lattice-based libraries.

INPUTS: D,CK
OUTPUTS: Q,QN
PINORDER: D CK Q QN
MINIMUM CELL AREA (2A/2T): 0.125
MINIMUM CELL AREA (Series 3): 0.0625

Truth Table:

INPUTS		OUTPUTS	
D	CK	Q	QN
0	↑	0	1
1	↑	1	0

X = Don’t care
When GSR=0, Q=0, QN=1 (D=CK=X)

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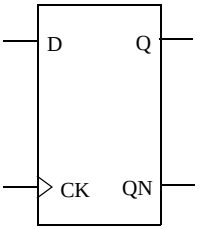
FD1S3AY

Positive Edge Triggered D Flip-Flop, GSR Used for Preset

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



FD1S3AY

NOTE: The QN output pin does not exist for FPGA architectures higher than ORCA Series 4. It is not recommended to migrate ORCA netlists to Lattice-based FPGA architectures for this reason. Synthesize your netlist using the appropriate Lattice-based libraries.

INPUTS: D,CK
OUTPUTS: Q,QN
PINORDER: D CK Q QN
MINIMUM CELL AREA (2A/2T): 0.125
MINIMUM CELL AREA (Series 3): 0.0625

Truth Table:

INPUTS		OUTPUTS	
D	CK	Q	QN
0	↑	0	1
1	↑	1	0

X = Don’t care
When GSR=0, Q=1, QN=0 (D=CK=X)

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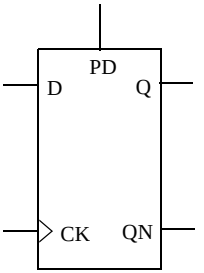
FD1S3BX

Positive Edge Triggered D Flip-Flop with Positive Level Asynchronous Preset

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



FD1S3BX

NOTE: The QN output pin does not exist for FPGA architectures higher than ORCA Series 4. It is not recommended to migrate ORCA netlists to Lattice-based FPGA architectures for this reason. Synthesize your netlist using the appropriate Lattice-based libraries.

INPUTS: D,CK,PD
OUTPUTS: Q,QN
PINORDER: D CK PD Q QN
MINIMUM CELL AREA (2A/2T): 0.125
MINIMUM CELL AREA (Series 3): 0.0625

Truth Table:

INPUTS			OUTPUTS	
D	CK	PD	Q	QN
X	X	1	1	0
0	↑	0	0	1
1	↑	X	1	0

X = Don’t care
When GSR=0, Q=1, QN=0 (D=CK=PD=X)

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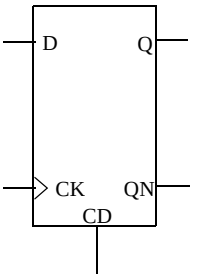
FD1S3DX

Positive Edge Triggered D Flip-Flop with Positive Level Asynchronous Clear

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



FD1S3DX

NOTE: The QN output pin does not exist for FPGA architectures higher than ORCA Series 4. It is not recommended to migrate ORCA netlists to Lattice-based FPGA architectures for this reason. Synthesize your netlist using the appropriate Lattice-based libraries.

INPUTS: D,CK,CD
OUTPUTS: Q,QN
PINORDER: D CK CD Q QN
MINIMUM CELL AREA (2A/2T): 0.125
MINIMUM CELL AREA (Series 3): 0.0625

Truth Table:

INPUTS			OUTPUTS	
D	CK	CD	Q	QN
X	X	1	0	1
0	↑	0	0	1
1	↑	0	1	0

X = Don’t care
When GSR=0, Q=0, QN=1 (D=CK=CD=X)

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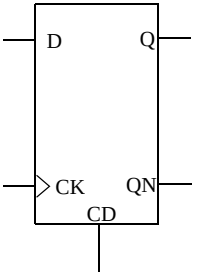
FD1S3IX

Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Clear

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



FD1S3IX

NOTE: The QN output pin does not exist for FPGA architectures higher than ORCA Series 4. It is not recommended to migrate ORCA netlists to Lattice-based FPGA architectures for this reason. Synthesize your netlist using the appropriate Lattice-based libraries.

INPUTS: D,CK,CD
OUTPUTS: Q,QN
PINORDER: D CK CD Q QN
MINIMUM CELL AREA (2A/2T): 0.125
MINIMUM CELL AREA (Series 3): 0.0625

Truth Table:

INPUTS			OUTPUTS	
D	CK	CD	Q	QN
X	↑	1	0	1
0	↑	0	0	1
1	↑	0	1	0

X = Don’t care
When GSR=0, Q=0, QN=1 (D=CK=CD=X)

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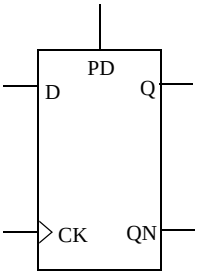
FD1S3JX

Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Preset

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



FD1S3JX

NOTE: The QN output pin does not exist for FPGA architectures higher than ORCA Series 4. It is not recommended to migrate ORCA netlists to Lattice-based FPGA architectures for this reason. Synthesize your netlist using the appropriate Lattice-based libraries.

INPUTS: D,CK,PD
OUTPUTS: Q,QN
PINORDER: D CK PD Q QN
MINIMUM CELL AREA (2A/2T): 0.125
MINIMUM CELL AREA (Series 3): 0.0625

Truth Table:

INPUTS			OUTPUTS	
D	CK	PD	Q	QN
X	↑	1	1	0
0	↑	0	0	1
1	↑	X	1	0

X = Don’t care
When GSR=0, Q=1, QN=0 (D=CK=PD=X)

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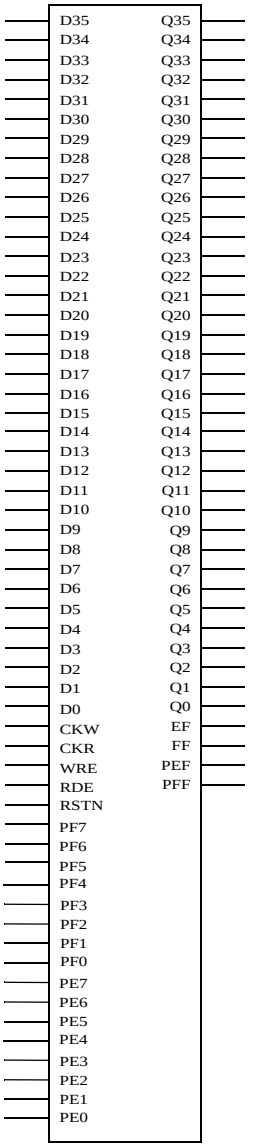
FF256X36

256x36 FIFO

ORCA Series		
2	3	4
		✓



FF256X36

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INPUTS: D35, D34, D33, D32, D31, D30, D29, D28, D27, D26, D25, D24, D23, D22, D21, D20, D19, D18, D17, D16, D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0, CKW, CKR, WRE, RDE, RSTN, PF7, PF6, PF5, PF4, PF3, PF2, PF1, PF0, PE7, PE6, PE5, PE4, PE3, PE2, PE1, PE0
OUTPUTS: Q35, Q34, Q33, Q32, Q31, Q30, Q29, Q28, Q27, Q26, Q25, Q24, Q23, Q22, Q21, Q20, Q19, Q18, Q17, Q16, Q15, Q14, Q13, Q12, Q11, Q10, Q9, Q8, Q7, Q6, Q5, Q4, Q3, Q2, Q1, Q0, EF, FF, PEF, PFF
PINORDER: D35 D34 D33 D32 D31 D30 D29 D28 D27 D26 D25 D24 D23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0 CKW CKR WRE RDE RSTN PF7 PF6 PF5 PF4 PF3 PF2 PF1 PF0 PE7 PE6 PE5 PE4 PE3 PE2 PE1 PE0 Q35 Q34 Q33 Q32 Q31 Q30 Q29 Q28 Q27 Q26 Q25 Q24 Q23 Q22 Q21 Q20 Q19 Q18 Q17 Q16 Q15 Q14 Q13 Q12 Q11 Q10 Q9 Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0 EF FF PEF PFF
MINIMUM CELL AREA (Series 2): 0.5
MINIMUM CELL AREA (Series 3 and Series 4): 0.25
ATTRIBUTES (Series 4 only)
FFMODE: NOREG, OUTREG
INHIBITMODE: TRUE, FALSE
ASYNCMODE: FALSE, TRUE

Description:

Data is written into this FIFO at the rising edge of the write port clock (CKW) when the write enable (WRE) is HIGH. Using the FFMODE attribute, input or output data can be set to be registered or not registered at all. In OUTREG, output data is registered and NOREG prevents all data from being registered.

FIFO pin functions:

Function	Pins
all data	D35, D34,...D0
write port clock	CKW
read port clock	CKR
write enable	WRE
read enable	RDE

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Function	Pins
reset (active LOW)	RSTN
address pointer for partial full flag	PF7, PF6, ...PF0
address pointer for partial empty flag	PE7, PE6, ...PE0
outputs	Q35, Q34,...Q0
empty flag	EF
full flag	FF
partial empty flag	PEF
partial full flag	PFF

Using the INHIBITMODE attribute, the FIFO can be set to accept or deny new data even when the FIFO is full.

Attribute	Value functions
FFMODE	“OUTREG” - Data out is registered. “NOREG” - Nothing is registered. The default behavior is to register nothing (NOREG).
INHIBITMODE	“TRUE” - (default) When FIFO is full, no new data is accepted. “FALSE” - Even if full, the FIFO will accept new data.
ASYNCMODE	“FALSE” - (default) When both CKW and CKR are the same clock. “TRUE” - When both CKW and CKR are different clocks.

Note that in INHIBITMODE = “TRUE” when both read and write are enabled, the FIFO may prevent data from being written when the full flag goes HIGH due to glitches. Even if the FIFO is not full, INHIBITMODE = “FALSE” disables the write/read inhibits in the FIFO.

Note**:** The FF256X36 element should be instantiated through SCUBA. Refer to the appropriate topic in the online help system for details.

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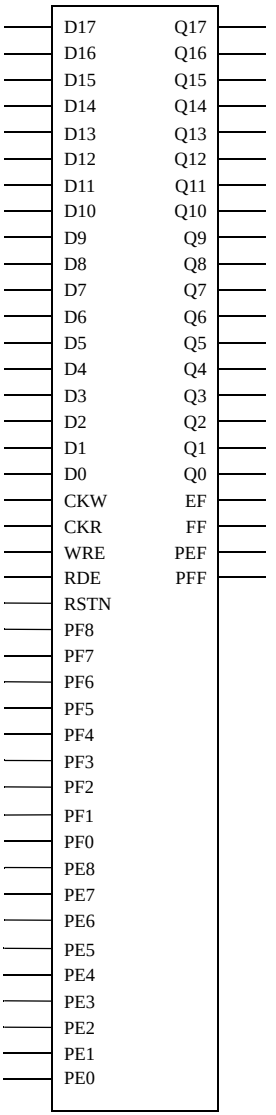
FF512X18

512 Word by 18 Bit FIFO

ORCA Series		
2	3	4
		✓



FF512X18

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INPUTS: D17, D16, D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0, CKW, CKR, WRE, RDE, RSTN, PF8, PF7, PF6, PF5, PF4, PF3, PF2, PF1, PF0, PE8, PE7, PE6, PE5, PE4, PE3, PE2, PE1, PE0
OUTPUTS: Q17, Q16, Q15, Q14, Q13, Q12, Q11, Q10, Q9, Q8, Q7, Q6, Q5, Q4, Q3, Q2, Q1, Q0, EF, FF, PEF, PFF
PINORDER: D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0 CKW CKR WRE RDE RSTN PF8 PF7 PF6 PF5 PF4 PF3 PF2 PF1 PF0 PE8 PE7 PE6 PE5 PE4 PE3 PE2 PE1 PE0 Q17 Q16 Q15 Q14 Q13 Q12 Q11 Q10 Q9 Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0 EF FF PEF PFF
ATTRIBUTES (Series 4 only)
FFMODE: NOREG, OUTREG
INHIBITMODE: TRUE, FALSE
ASYNCMODE: FALSE, TRUE

Description:

Data is written into this FIFO at the rising edge of the write port clock (CKW) when the write enable (WRE) is HIGH. Using the FFMODE attribute, input or output data can be set to be registered or not registered at all. In OUTREG, output data is registered and NOREG prevents all data from being registered.

FIFO pin functions:

Function	Pins
all data	D17, D16,...D0
write port clock	CKW
read port clock	CKR
write enable	WRE
read enable	RDE
reset (active LOW)	RSTN
address pointer for partial full flag	PF8, PF7, ...PF0
address pointer for partial empty flag	PE8, PE7, ...PE0

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Function	Pins
output data	Q17, Q16,...Q0
empty flag	EF
full flag	FF
partial empty flag	PEF
partial full flag	PFF

Using the INHIBITMODE attribute, the FIFO can be set to accept or deny new data even when the FIFO is full.

Attribute	Value functions
FFMODE	“OUTREG” - Data out is registered. “NOREG” - Nothing is registered. The default behavior is to register nothing (NOREG).
INHIBITMODE	“TRUE” - (default) When FIFO is full, no new data is accepted. “FALSE” - Even if full, the FIFO will accept new data.
ASYNCMODE	“FALSE” - (default) When both CKW and CKR are the same clock. “TRUE” - When both CKW and CKR are different clocks.

Note that in INHIBITMODE = “TRUE” when both read and write are enabled, the FIFO may prevent data from being written when the full flag goes HIGH due to glitches. Even if the FIFO is not full, INHIBITMODE = “FALSE” disables the write/read inhibits in the FIFO.

***Note*:** The FF512X18 element should be instantiated through SCUBA. Refer to the appropriate topic in the online help system for details.

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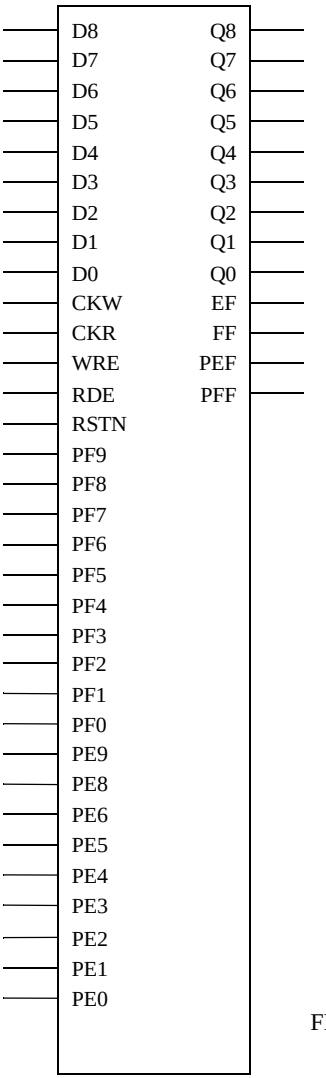
FF1024X9

1024x9 FIFO

ORCA Series		
2	3	4
		✓



FF1024X9

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INPUTS: D8, D7, D6, D5, D4, D3, D2, D1, D0, CKW, CKR, WRE, RDE, RSTN, PF9, PF8, PF7, PF6, PF5, PF4, PF3, PF2, PF1, PF0, PE9, PE8, PE7, PE6, PE5, PE4, PE3, PE2, PE1, PE0
OUTPUTS: Q8, Q7, Q6, Q5, Q4, Q3, Q2, Q1, Q0, EF, FF, PEF, PFF
PINORDER: D8 D7 D6 D5 D4 D3 D2 D1 D0 CKW CKR WRE RDE RSTN PF9 PF8 PF7 PF6 PF5 PF4 PF3 PF2 PF1 PF0 PE9 PE8 PE7 PE6 PE5 PE4 PE3 PE2 PE1 PE0 Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0 EF FF PEF PFF
ATTRIBUTES (Series 4 only)
FFMODE: NOREG, OUTREG
INHIBITMODE: TRUE, FALSE
ASYNCMODE: FALSE, TRUE

Description:

Data is written into the FIFO at the rising edge of the write port (CKW) when the write enable (WRE) is HIGH. Using the FFMODE attribute, input or output data can be set to be registered or not registered at all. In OUTREG, output data is registered and NOREG prevents all data from being registered.

FIFO pin functions:

Function	Pins
all data	D8, D7,...D0
write port clock	CKW
read port clock	CKR
write enable	WRE
read enable	RDE
reset (active LOW)	RSTN
address pointer for partial full flag	PF9, PF8, ...PF0
address pointer for partial empty flag	PE9, PE8, ...PE0
output data	Q8, Q7,...Q0

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Function	Pins
empty flag	EF
full flag	FF
partial empty flag	PEF
partial full flag	PFF

Using the INHIBITMODE attribute, the FIFO can be set to accept or deny new data even when the FIFO is full.

Attribute	Value functions
FFMODE	“OUTREG” - Data out is registered. “NOREG” - Nothing is registered. The default behavior is to register nothing (NOREG).
INHIBITMODE	“TRUE” - (default) When FIFO is full, no new data is accepted. “FALSE” - Even if full, the FIFO will accept new data.
ASYNCMODE	“FALSE” - (default) When both CKW and CKR are the same clock. “TRUE” - When both CKW and CKR are different clocks.

Note that in INHIBITMODE = “TRUE” when both read and write are enabled, the FIFO may prevent data from being written when the full flag goes HIGH due to glitches. Even if the FIFO is not full, INHIBITMODE = “FALSE” disables the write/read inhibits in the FIFO.

> ***Note*****:** The FF1024X9 element should be instantiated through SCUBA. Refer to the appropriate topic in the online help system for details.

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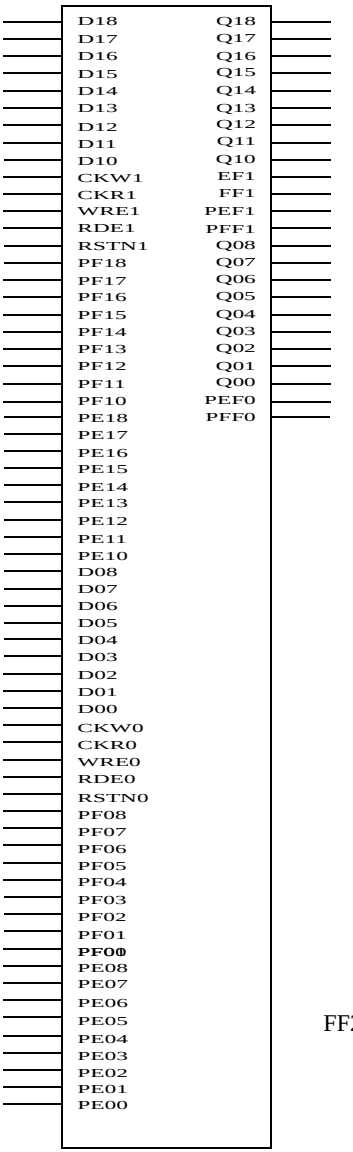
FF2X512X9

2 512 Word by 9 Bit FIFO

ORCA Series		
2	3	4
		✓



FF2X512X9

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INPUTS: D18, D17, D16, D15, D14, D13, D12, D11, D10, CKW1, CKR1, WRE1, RDE1, RSTN1, PF18, PF17, PF16, PF15, PF14, PF13, PF12, PF11, PF10, PE18, PE17, PE16, PE15, PE14, PE13, PE12, PE11, PE10, D08, D07, D06, D05, D04, D03, D02, D01, D00, CKW0, CKR0, WRE0, RDE0, RSTN0, PF08, PF07, PF06, PF05, PF04, PF03, PF02, PF01, PF00, PE08, PE07, PE06, PE05, PE04, PE03, PE02, PE01, PE00
OUTPUTS: Q18, Q17, Q16, Q15, Q14, Q13, Q12, Q11, Q10, EF1, FF1, PEF1, PFF1 Q08, Q07, Q06, Q05, Q04, Q03, Q02, Q01, Q00, EF0, FF0, PEF0, PFF0
PINORDER: D18 D17 D16 D15 D14 D13 D12 D11 D10 CKW1 CKR1 WRE1 RDE1 RSTN1 PF18 PF17 PF16 PF15 PF14 PF13 PF12 PF11 PF10 PE18 PE17 PE16 PE15 PE14 PE13 PE12 PE11 PE10 D08 D07 D06 D05 D04 D03 D02 D01 D00 CKW0 CKR0 WRE0 RDE0 RSTN0 PF08 PF07 PF06 PF05 PF04 PF03 PF02 PF01 PF00 PE08 PE07 PE06 PE05 PE04 PE03 PE02 PE01 PE00 Q18 Q17 Q16 Q15 Q14 Q13 Q12 Q11 Q10 EF1 FF1 PEF1 PFF1 Q08 Q07 Q06 Q05 Q04 Q03 Q02 Q01 Q00 EF0 FF0 PEF0 PFF0
ATTRIBUTES (Series 4 only)
FFMODE0: NOREG, OUTREG
FFMODE1: NOREG, OUTREG
INHIBITMODE0: TRUE, FALSE
INHIBITMODE1: TRUE, FALSE
ASYNCMODE0: FALSE, TRUE

Description:

The FIFO consists of two 512 x 9 FIFOs, FIFO0 and FIFO1. Data is written into the FIFO at the rising edge of the write port clock (CKW) when the write enable (WRE) is HIGH. Using the FFMODE attribute, input or output data can be set to be registered or not registered at all. In OUTREG, output data is registered and NOREG prevents all data from being registered.

FIFO pin functions (FIFO1 and FIFO0):

Function	Pins
all data	D18, D17,...D10 and D08, D07,...D00
write port clock	CKW1, CKW0
read port clock	CKR1, CKR0
write enable	WRE1, WRE0
read enable	RDE1, RDE0

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Function	Pins
reset (active LOW)	RSTN1, RSTN0
address pointer for partial full flag	PF[18:10] and PF[08:00]
address pointer for partial empty flag	PE[18:10] and PE[08:00]
output data	Q[18:10] and Q[08:00]
empty flag	EF1, EF0
full flag	FF1, FF0
partial empty flag	PEF1, PEF0
partial full flag	PFF1, PFF0

Using the INHIBITMODE attribute, the FIFO can be set to accept or deny new data even when the FIFO is full.

Attribute	Value functions
FFMODE[0,1]	“OUTREG” - Data out is registered. “NOREG” - Nothing is registered. The default behavior is to register nothing (NOREG).
INHIBITMODE[0,1]	“TRUE” - (default) When FIFO is full, no new data is accepted. “FALSE” - Even if full, the FIFO will accept new data.
ASYNCMODE0	“FALSE” - (default) When both CKW and CKR are the same clock. “TRUE” - When both CKW and CKR are different clocks.

Note that in INHIBITMODE = “TRUE” when both read and write are enabled, the FIFO may prevent data from being written when the full flag goes HIGH due to glitches. Even if the FIFO is not full, INHIBITMODE = “FALSE” disables the write/read inhibits in the FIFO.

Note**:** The FF2X512X9 element should be instantiated through SCUBA. Refer to the appropriate topic in the online help system for details.

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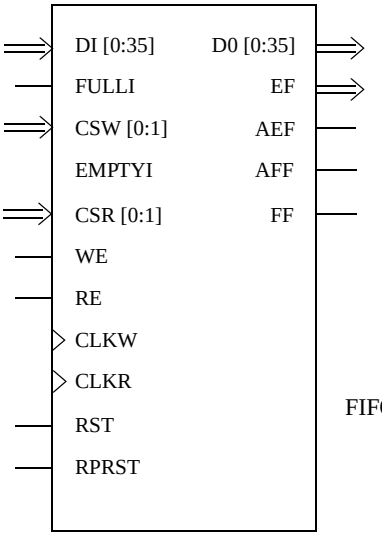
FIFO16KA

16K FIFO

Lattice FPGA		
SC	XP	EC
✓		



NOTE: The graphic is shown in bus notation for convenience. This element must be instantiated in expanded bus notation format with each individual bit as given below.

INPUT : DI0, DI1, DI2, DI3, DI4, DI5, DI6, DI7, DI8, DI9, DI10, DI11, DI12, DI13, DI14, DI15, DI16, DI17, DI18, DI19, DI20, DI21, DI22, DI23, DI24, DI25, DI26, DI27, DI28, DI29, DI30, DI31, DI32, DI33, DI34, DI35, FULLI, CSW0, CSW1, EMPTYI, CSR0, CSR1, WE, RE, CLKW, CLKR, RST, RPRST;

OUTPUT : DO0, DO1, DO2, DO3, DO4, DO5, DO6, DO7, DO8, DO9, DO10, DO11, DO12, DO13, DO14, DO15, DO16, DO17, DO18, DO19, DO20, DO21, DO22, DO23, DO24, DO25, DO26, DO27, DO28, DO29, DO30, DO31, DO32, DO33, DO34, DO35, EF, AEF, AFF, FF

PINORDER: DI0, DI1, DI2, DI3, DI4, DI5, DI6, DI7, DI8, DI9, DI10, DI11, DI12, DI13, DI14, DI15, DI16, DI17, DI18, DI19, DI20, DI21, DI22, DI23, DI24, DI25, DI26, DI27, DI28, DI29, DI30, DI31, DI32, DI33, DI34, DI35, FULLI, CSW0, CSW1, EMPTYI, CSR1, CSR2, WE, RE, CLKW, CLKR, RST, RPRST; DO0, DO1, DO2, DO3, DO4, DO5, DO6, DO7, DO8, DO9, DO10, DO11, DO12, DO13, DO14, DO15, DO16, DO17, DO18, DO19, DO20, DO21, DO22, DO23, DO24, DO25, DO26, DO27, DO28, DO29, DO30, DO31, DO32, DO33, DO34, DO35, EF, AEF, AFF, FF

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ATTRIBUTES (LatticeSC)
DATA_WIDTH_W: 1, 2, 4, 9, 18, 36
DATA_WIDTH_R: 1, 2, 4, 9, 18, 36
REGMODE: NOREG, OUTREG
RESETMODE: ASYNC, SYNC
CSDECODE_W: 00, 01, 10, 11
CSDECODE_R: 00, 01, 10, 11
DISABLED_GSR: 0, 1
AEPOINTER: 00000000000000, ..., 11111111111111
AFPOINTER: 00000000000000, ..., 11111111111111
FULLPOINTER: 00000000000000, ..., 11111111111111
AEPOINTER1: 00000000000000, ..., 11111111111111
AFPOINTER1: 00000000000000, ..., 11111111111111
FULLPOINTER1: 00000000000000, ..., 11111111111111

Description:

FIFO. See “FIFO Port Definitions” on page 3.

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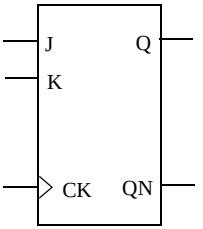
FJ1S3AX

Positive Edge Triggered J/K Flip-Flop, GSR Used for Clear

ORCA Series		
2	3	4
✓		



FJ1S3AX

NOTE: The QN output pin does not exist for FPGA architectures higher than ORCA Series 4. It is not recommended to migrate ORCA netlists to Lattice-based FPGA architectures for this reason. Synthesize your netlist using the appropriate Lattice-based libraries.

INPUTS: J,K,CK
OUTPUTS: Q,QN
PINORDER: J K CK Q QN
MINIMUM CELL AREA: 0.25

Truth Table:

INPUTS			OUTPUTS	
J	K	CK	Q	QN
0	0	↑	Q	QN
0	1	↑	0	1
1	0	↑	1	0
1	1	↑	QN	Q

X = Don’t care
When GSR=0, Q=0, QN=1 (J=K=CK=X)

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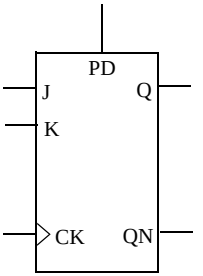
FJ1S3BX

Positive Edge Triggered J/K Flip-Flop with Positive Level Asynchronous Preset

ORCA Series		
2	3	4
✓		



FJ1S3BX

NOTE: The QN output pin does not exist for FPGA architectures higher than ORCA Series 4. It is not recommended to migrate ORCA netlists to Lattice-based FPGA architectures for this reason. Synthesize your netlist using the appropriate Lattice-based libraries.

INPUTS: J,K,CK,PD
OUTPUTS: Q,QN
PINORDER: J K CK PD Q QN
MINIMUM CELL AREA: 0.25

Truth Table:

INPUTS				OUTPUTS	
J	K	CK	PD	Q	QN
0	0	↑	0	Q	QN
X	X	X	1	1	0
0	1	↑	0	0	1
1	0	↑	0	1	0
1	1	↑	0	QN	Q

X = Don’t care
When GSR=0, Q=1, QN=0 (J=K=CK=PD=X)

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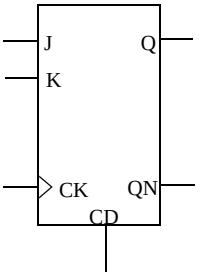
FJ1S3DX

Positive Edge Triggered J/K Flip-Flop with Positive Level Asynchronous Clear

ORCA Series		
2	3	4
✓		



FJ1S3DX

NOTE: The QN output pin does not exist for FPGA architectures higher than ORCA Series 4. It is not recommended to migrate ORCA netlists to Lattice-based FPGA architectures for this reason. Synthesize your netlist using the appropriate Lattice-based libraries.

INPUTS: J,K,CK,CD
OUTPUTS: Q,QN
PINORDER: J K CK CD Q QN
MINIMUM CELL AREA: 0.25

Truth Table:

INPUTS				OUTPUTS	
J	K	CK	CD	Q	QN
0	0	↑	0	Q	QN
X	X	X	1	0	1
0	1	↑	0	0	1
1	0	↑	0	1	0
1	1	↑	0	QN	Q

X = Don’t care
When GSR=0, Q=0, QN=1 (J=K=CK=CD=X)

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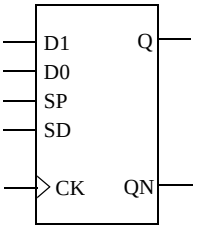
FL1P3AY

Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, Positive Level Data Select, and Positive Level Enable, GSR used for Preset

ORCA Series			
2	3	4	SC
✓	✓	✓	✓



FL1P3AY

NOTE: The QN output pin does not exist for FPGA architectures higher than ORCA Series 4. It is not recommended to migrate ORCA netlists to Lattice-based FPGA architectures for this reason. Synthesize your netlist using the appropriate Lattice-based libraries.

INPUTS: D0,D1,SP,CK,SD
OUTPUTS: Q,QN
PINORDER: D0 D1 SP CK SD Q QN
D1 is a direct input D0 input comes from logic (LUT)

MINIMUM CELL AREA (2A/2T): 0.125
MINIMUM CELL AREA (Series 3): 0.0625

Truth Table:

INPUTS					OUTPUTS	
D0	D1	SP	SD	CK	Q	QN
X	X	0	X	X	Q	QN
0	X	1	0	↑	0	1
1	X	1	0	↑	1	0
X	0	1	1	↑	0	1
X	1	1	1	↑	1	0

X = Don’t care
When GSR=0, Q=1, QN=0 (D0=D1=SP=SD=CK=X)

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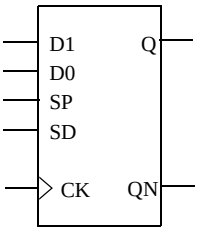
FL1P3AZ

Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, Positive Level Data Select, and Positive Level Enable, GSR used for Clear

ORCA Series			
2	3	4	SC
✓	✓	✓	✓



FL1P3AZ

NOTE: The QN output pin does not exist for FPGA architectures higher than ORCA Series 4. It is not recommended to migrate ORCA netlists to Lattice-based FPGA architectures for this reason. Synthesize your netlist using the appropriate Lattice-based libraries.

INPUTS: D0,D1,SP,CK,SD
OUTPUTS: Q,QN
PINORDER: D0 D1 SP CK SD Q QN
D1 is a direct input D0 input comes from logic (LUT)

MINIMUM CELL AREA (2A/2T): 0.125
MINIMUM CELL AREA (Series 3): 0.0625

Truth Table:

INPUTS					OUTPUTS	
D0	D1	SP	SD	CK	Q	QN
X	X	0	X	X	Q	QN
0	X	1	0	↑	0	1
1	X	1	0	↑	1	0
X	0	1	1	↑	0	1
X	1	1	1	↑	1	0

X = Don’t care
When GSR=0, Q=0, QN=1 (D0=D1=SP=SD=CK=X)

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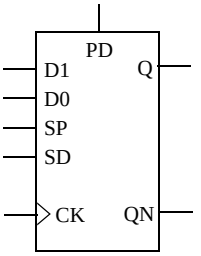
FL1P3BX

Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, Positive Level Data Select, Positive Level Asynchronous Preset, and Positive Level Enable

ORCA Series			
2	3	4	SC
	✓	✓	✓



FL1P3BX

NOTE: The QN output pin does not exist for FPGA architectures higher than ORCA Series 4. It is not recommended to migrate ORCA netlists to Lattice-based FPGA architectures for this reason. Synthesize your netlist using the appropriate Lattice-based libraries.

INPUTS: D0,D1,SP,CK,SD,PD
OUTPUTS: Q,QN
PINORDER: D0 D1 SP CK SD PD Q QN
D1 is a direct input D0 input comes from logic (LUT)
MINIMUM CELL AREA: 0.0625

Truth Table:

INPUTS						OUTPUTS	
D0	D1	SP	SD	CK	PD	Q	QN
X	X	0	X	X	0	Q	QN
X	X	X	X	X	1	1	0
0	X	1	0	↑	0	0	1
1	X	1	0	↑	X	1	0
X	0	1	1	↑	0	0	1
X	1	1	1	↑	X	1	0

X = Don’t care
When GSR=0, Q=1, QN=0 (D0=D1=SP=SD=CK=PD=X)

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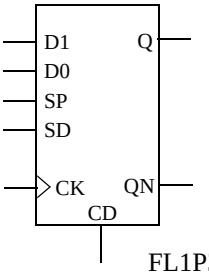
FL1P3DX

Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, Positive Level Data Select, Positive Level Asynchronous Clear, and Positive Level Enable

ORCA Series			
2	3	4	SC
	✓	✓	✓



FL1P3DX

NOTE: The QN output pin does not exist for FPGA architectures higher than ORCA Series 4. It is not recommended to migrate ORCA netlists to Lattice-based FPGA architectures for this reason. Synthesize your netlist using the appropriate Lattice-based libraries.

INPUTS: D0,D1,SP,CK,SD,CD
OUTPUTS: Q,QN
PINORDER: D0 D1 SP CK SD CD Q QN
D1 is a direct input D0 input comes from logic (LUT)
MINIMUM CELL AREA: 0.0625

Truth Table:

INPUTS						OUTPUTS	
D0	D1	SP	SD	CK	CD	Q	QN
X	X	0	X	X	0	Q	QN
X	X	X	X	X	1	0	1
0	X	1	0	↑	0	0	1
1	X	1	0	↑	X	1	0
X	0	1	1	↑	0	0	1
X	1	1	1	↑	X	1	0

X = Don’t care
When GSR=0, Q=0, QN=1 (D0=D1=SP=SD=CK=CD=X)

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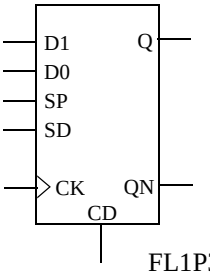
FL1P3IY

Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, Positive Level Data Select, Positive Level Synchronous Clear, and Positive Level Enable (Clear overrides Enable)

ORCA Series			
2	3	4	SC
	✓	✓	✓



FL1P3IY

NOTE: The QN output pin does not exist for FPGA architectures higher than ORCA Series 4. It is not recommended to migrate ORCA netlists to Lattice-based FPGA architectures for this reason. Synthesize your netlist using the appropriate Lattice-based libraries.

INPUTS: D0,D1,SP,CK,SD,CD
OUTPUTS: Q,QN
PINORDER: D0 D1 SP CK SD CD Q QN
D1 is a direct input D0 input comes from logic (LUT)
MINIMUM CELL AREA: 0.0625

Truth Table:

INPUTS						OUTPUTS	
D0	D1	SP	SD	CK	CD	Q	QN
X	X	0	X	X	0	Q	QN
X	X	X	X	↑	1	0	1
0	X	1	0	↑	X	0	1
1	X	1	0	↑	0	1	0
X	0	1	1	↑	X	0	1
X	1	1	1	↑	0	1	0

X = Don’t care
When GSR=0, Q=1, QN=0 (D0=D1=SP=SD=CK=CD=X)

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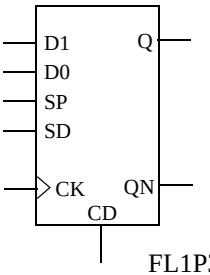
FL1P3IZ

Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, Positive Level Data Select, Positive Level Synchronous Clear, and Positive Level Enable (Enable overrides Clear)

ORCA Series		
2	3	4
	✓	✓



FL1P3IZ

NOTE: The QN output pin does not exist for FPGA architectures higher than ORCA Series 4. It is not recommended to migrate ORCA netlists to Lattice-based FPGA architectures for this reason. Synthesize your netlist using the appropriate Lattice-based libraries.

INPUTS: D0,D1,SP,CK,SD,CD
OUTPUTS: Q,QN
PINORDER: D0 D1 SP CK SD CD Q QN
D1 is a direct input D0 input comes from logic (LUT)
MINIMUM CELL AREA: 0.0625

Truth Table:

INPUTS						OUTPUTS	
D0	D1	SP	SD	CK	CD	Q	QN
X	X	0	X	X	X	Q	QN
X	X	1	X	↑	1	0	1
0	X	1	0	↑	X	0	1
1	X	1	0	↑	0	1	0
X	0	1	1	↑	X	0	1
X	1	1	1	↑	0	1	0

X = Don’t care
When GSR=0, Q=1, QN=0 (D0=D1=SP=SD=CK=CD=X)

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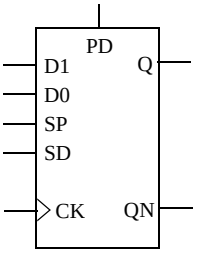
FL1P3JY

Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, Positive Level Data Select, Positive Level Synchronous Preset, and Positive Level Enable (Preset overrides Enable)

ORCA Series			
2	3	4	SC
	✓	✓	✓



FL1P3JY

NOTE: The QN output pin does not exist for FPGA architectures higher than ORCA Series 4. It is not recommended to migrate ORCA netlists to Lattice-based FPGA architectures for this reason. Synthesize your netlist using the appropriate Lattice-based libraries.

INPUTS: D0,D1,SP,CK,SD,PD
OUTPUTS: Q,QN
PINORDER: D0 D1 SP CK SD PD Q QN
D1 is a direct input D0 input comes from logic (LUT)
MINIMUM CELL AREA: 0.0625

Truth Table:

INPUTS						OUTPUTS	
D0	D1	SP	SD	CK	PD	Q	QN
X	X	0	X	X	0	Q	QN
X	X	X	X	↑	1	1	0
0	X	1	0	↑	0	0	1
1	X	1	0	↑	X	1	0
X	0	1	1	↑	0	0	1
X	1	1	1	↑	X	1	0

X = Don’t care
When GSR=0, Q=1, QN=0 (D0=D1=SP=SD=CK=PD=X)

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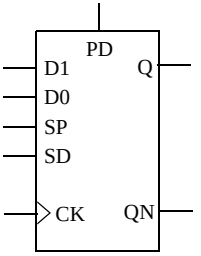
FL1P3JZ

Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, Positive Level Data Select, Positive Level Synchronous Preset, and Positive Level Enable (Enable overrides Preset)

ORCA Series		
2	3	4
	✓	✓



FL1P3JZ

NOTE: The QN output pin does not exist for FPGA architectures higher than ORCA Series 4. It is not recommended to migrate ORCA netlists to Lattice-based FPGA architectures for this reason. Synthesize your netlist using the appropriate Lattice-based libraries.

INPUTS: D0,D1,SP,CK,SD,PD
OUTPUTS: Q,QN
PINORDER: D0 D1 SP CK SD PD Q QN
D1 is a direct input D0 input comes from logic (LUT)
MINIMUM CELL AREA: 0.0625

Truth Table:

INPUTS						OUTPUTS	
D0	D1	SP	SD	CK	PD	Q	QN
X	X	0	X	X	X	Q	QN
X	X	1	X	↑	1	1	0
0	X	1	0	↑	0	0	1
1	X	1	0	↑	X	1	0
X	0	1	1	↑	0	0	1
X	1	1	1	↑	X	1	0

X = Don’t care
When GSR=0, Q=1, QN=0 (D0=D1=SP=SD=CK=PD=X)

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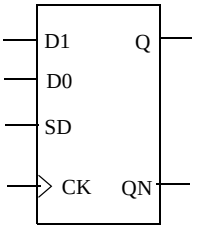
FL1S1A

Positive Level Loadable Latch with Positive Select, GSR Used for Clear

ORCA Series			
2	3	4	SC
✓	✓	✓	✓



FL1S1A

NOTE: The QN output pin does not exist for FPGA architectures higher than ORCA Series 4. It is not recommended to migrate ORCA netlists to Lattice-based FPGA architectures for this reason. Synthesize your netlist using the appropriate Lattice-based libraries.

INPUTS: D0,D1,CK,SD
OUTPUTS: Q,QN
PINORDER: D0 D1 CK SD Q QN
D1 is a direct input D0 input comes from logic (LUT)

MINIMUM CELL AREA (2A/2T): 0.125
MINIMUM CELL AREA (Series 3): 0.0625

Truth Table:

INPUTS				OUTPUTS	
D0	D1	SD	CK	Q	QN
0	X	0	1	0	1
1	X	0	1	1	0
X	0	1	1	0	1
X	1	1	1	1	0

X = Don’t care
When GSR=0, Q=0, QN=1 (D0=D1=SD=CK=X)

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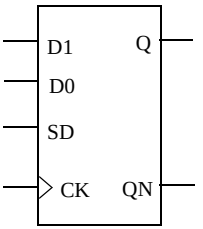
FL1S1AY

Positive Level Loadable Latch with Positive Select, GSR Used for Preset

ORCA Series			
2	3	4	SC
✓	✓	✓	✓



FL1S1AY

NOTE: The QN output pin does not exist for FPGA architectures higher than ORCA Series 4. It is not recommended to migrate ORCA netlists to Lattice-based FPGA architectures for this reason. Synthesize your netlist using the appropriate Lattice-based libraries.

INPUTS: D0,D1,CK,SD
OUTPUTS: Q,QN
PINORDER: D0 D1 CK SD Q QN
D1 is a direct input D0 input comes from logic (LUT)

MINIMUM CELL AREA (2A/2T): 0.125
MINIMUM CELL AREA (Series 3): 0.0625

Truth Table:

INPUTS				OUTPUTS	
D0	D1	SD	CK	Q	QN
0	X	0	1	0	1
1	X	0	1	1	0
X	0	1	1	0	1
X	1	1	1	1	0

X = Don’t care
When GSR=0, Q=1, QN=0 (D0=D1=SD=CK=X)

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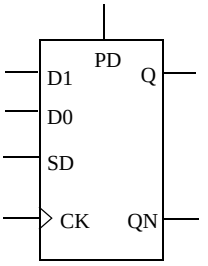
FL1S1B

Positive Level Loadable Latch with Positive Level Data Select and Positive Level Asynchronous Preset

ORCA Series			
2	3	4	SC
	✓	✓	✓



FL1S1B

NOTE: The QN output pin does not exist for FPGA architectures higher than ORCA Series 4. It is not recommended to migrate ORCA netlists to Lattice-based FPGA architectures for this reason. Synthesize your netlist using the appropriate Lattice-based libraries.

INPUTS: D0,D1,CK,SD,PD
OUTPUTS: Q,QN
PINORDER: D0 D1 CK SD PD Q QN
MINIMUM CELL AREA: 0.0625

Truth Table:

INPUTS					OUTPUTS	
D0	D1	SD	CK	PD	Q	QN
X	X	X	0	0	Q	QN
X	X	X	X	1	1	0
0	X	0	1	0	0	1
1	X	0	1	X	1	0
X	0	1	1	0	0	1
X	1	1	1	X	1	0

X= Don’t care
When GSR=0, Q=1, QN=0 (D0=D1=SD=CK=PD=X)

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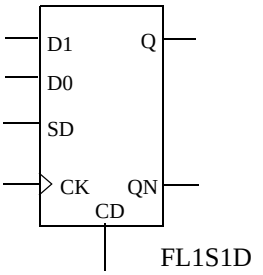
FL1S1D

Positive Level Loadable Latch with Positive Level Data Select and Positive Level Asynchronous Clear

ORCA Series			
2	3	4	SC
	✓	✓	✓



FL1S1D

NOTE: The QN output pin does not exist for FPGA architectures higher than ORCA Series 4. It is not recommended to migrate ORCA netlists to Lattice-based FPGA architectures for this reason. Synthesize your netlist using the appropriate Lattice-based libraries.

INPUTS: D0,D1,CK,SD,CD
OUTPUTS: Q,QN
PINORDER: D0 D1 CK SD CD Q QN
MINIMUM CELL AREA: 0.0625

Truth Table:

INPUTS					OUTPUTS	
D0	D1	SD	CK	CD	Q	QN
X	X	X	0	0	Q	QN
X	X	X	X	1	0	1
0	X	0	1	X	0	1
1	X	0	1	0	1	0
X	0	1	1	X	0	1
X	1	1	1	0	1	0

X = Don’t care
When GSR=0, Q=0, QN=1 (D0=D1=SD=CK=CD=X)

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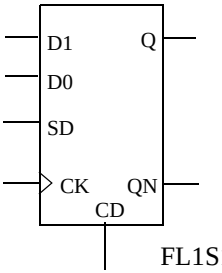
FL1S1I

Positive Level Loadable Latch with Positive Level Data Select and Positive Level Synchronous Clear

ORCA Series			
2	3	4	SC
	✓	✓	✓



FL1S1I

NOTE: The QN output pin does not exist for FPGA architectures higher than ORCA Series 4. It is not recommended to migrate ORCA netlists to Lattice-based FPGA architectures for this reason. Synthesize your netlist using the appropriate Lattice-based libraries.

INPUTS: D0,D1,CK,SD,CD
OUTPUTS: Q,QN
PINORDER: D0 D1 CK SD CD Q QN
MINIMUM CELL AREA: 0.0625

Truth Table:

INPUTS					OUTPUTS	
D0	D1	SD	CK	CD	Q	QN
X	X	X	0	0	Q	QN
X	X	X	1	1	0	1
0	X	0	1	X	0	1
1	X	0	1	0	1	0
X	0	1	1	X	0	1
X	1	1	1	0	1	0

X = Don’t care
When GSR=0, Q=0, QN=1 (D0=D1=SD=CK=CD=X)

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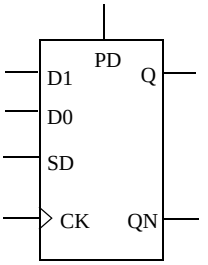
FL1S1J

Positive Level Loadable Latch with Positive Level Data Select and Positive Level Synchronous Preset

ORCA Series			
2	3	4	SC
	✓	✓	✓



FL1S1J

NOTE: The QN output pin does not exist for FPGA architectures higher than ORCA Series 4. It is not recommended to migrate ORCA netlists to Lattice-based FPGA architectures for this reason. Synthesize your netlist using the appropriate Lattice-based libraries.

INPUTS: D0,D1,CK,SD,PD
OUTPUTS: Q,QN
PINORDER: D0 D1 CK SD PD Q QN
MINIMUM CELL AREA: 0.0625

Truth Table:

INPUTS					OUTPUTS	
D0	D1	SD	CK	PD	Q	QN
X	X	X	0	0	Q	QN
X	X	X	1	1	1	0
0	X	0	1	0	0	1
1	X	0	1	X	1	0
X	0	1	1	0	0	1
X	1	1	1	X	1	0

X = Don’t care
When GSR=0, Q=1, QN=0 (D0=D1=SD=CK=PD=X)

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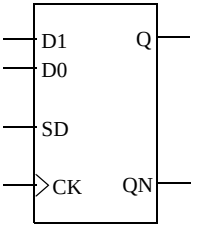
FL1S3AX

Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, GSR used for Clear

ORCA Series			
2	3	4	SC
✓	✓	✓	✓



FL1S3AX

NOTE: The QN output pin does not exist for FPGA architectures higher than ORCA Series 4. It is not recommended to migrate ORCA netlists to Lattice-based FPGA architectures for this reason. Synthesize your netlist using the appropriate Lattice-based libraries.

INPUTS: D0,D1,CK,SD
OUTPUTS: Q,QN
PINORDER: D0 D1 CK SD Q QN
D1 is a direct input D0 input comes from logic (LUT)

MINIMUM CELL AREA (2A/2T): 0.125
MINIMUM CELL AREA (Series 3): 0.0625

Truth Table:

INPUTS				OUTPUTS	
D0	D1	SD	CK	Q	QN
0	X	0	↑	0	1
1	X	0	↑	1	0
X	0	1	↑	0	1
X	1	1	↑	1	0

X = Don’t care
When GSR=0, Q=0, QN=1 (D0=D1=SD=CK=X)

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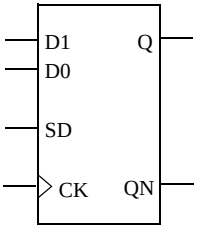
FL1S3AY

Positive Edge Triggered D Flip-Flop with 2 Input Data Mux, GSR used for Preset

ORCA Series			
2	3	4	SC
✓	✓	✓	✓



FL1S3AY

NOTE: The QN output pin does not exist for FPGA architectures higher than ORCA Series 4. It is not recommended to migrate ORCA netlists to Lattice-based FPGA architectures for this reason. Synthesize your netlist using the appropriate Lattice-based libraries.

INPUTS: D0,D1,CK,SD
OUTPUTS: Q,QN
PINORDER: D0 D1 CK SD Q QN
D1 is a direct input D0 input comes from logic (LUT)

MINIMUM CELL AREA (2A/2T): 0.125
MINIMUM CELL AREA (Series 3): 0.0625

Truth Table:

INPUTS				OUTPUTS	
D0	D1	SD	CK	Q	QN
0	X	0	↑	0	1
1	X	0	↑	1	0
X	0	1	↑	0	1
X	1	1	↑	1	0

X = Don’t care
When GSR=0, Q=1, QN=0 (D0=D1=SD=CK=X)

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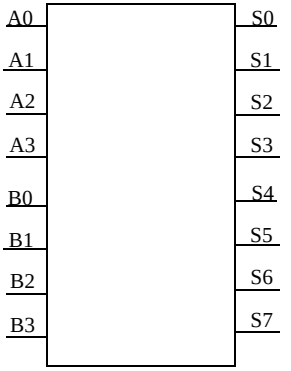
FMULT4

4 X 4 Multiplier

ORCA Series		
2	3	4
✓		



FMULT4

INPUTS: A0,A1,A2,A3,B0,B1,B2,B3
OUTPUTS: S0,S1,S2,S3,S4,S5,S6,S7
PINORDER: A0 A1 A2 A3 B0 B1 B2 B3 S0 S1 S2 S3 S4 S5 S6 S7
MINIMUM CELL AREA: 7.0

Truth Table:

INPUTS		OUTPUTS
A[0:3]	B[0:3]	S[0:7]
A[0:3]	B[0:3]	A[0:3] x B[0:3]

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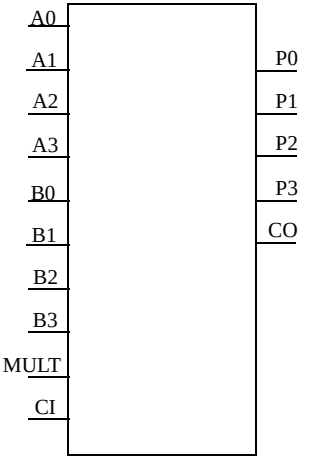
FMULT41

4 X 1 Fast Multiplier

ORCA Series		
2	3	4
✓	✓	✓



FMULT41

INPUTS: A0,A1,A2,A3,B0,B1,B2,B3,MULT,CI
OUTPUTS: CO,P0,P1,P2,P3
PINORDER: A0 A1 A2 A3 B0 B1 B2 B3 MULT CI CO P0 P1 P2 P3
MINIMUM CELL AREA (2A/2T): 0.5
MINIMUM CELL AREA (Series 3): 0.25

Description:

FMULT41 is a fast 4x1 multiplier macro.

More than one FMULT41 cell can be combined to form larger multipliers like 4x2, 4x3, 4x4, 4x5, etc. The B[3:0] inputs are the 4 bits of the multiplicand, MULT is the 1 bit multiplier input, A[3:0] are the partial sum inputs (from a previous multiplier stage), and CI is the carry-in input. The carry-out output is CO, and P[3:0] are the partial sum (or final stage) result outputs.

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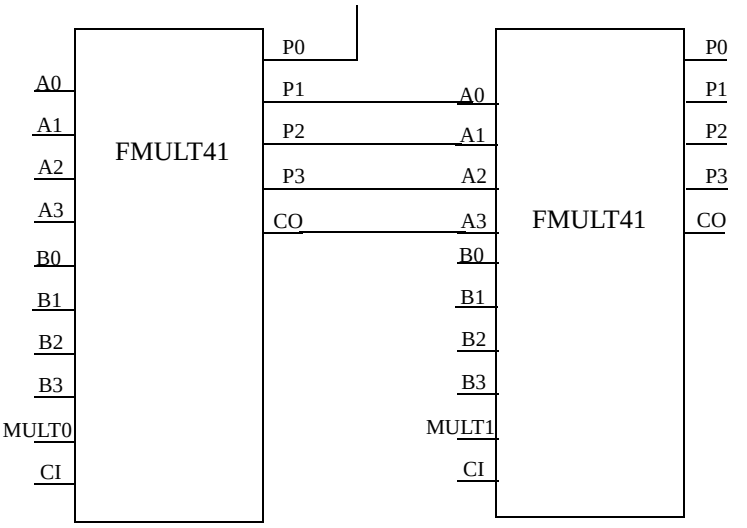
Example:

To create a 4x2 multiplier:

We need two FMULT41 cells. A[0:3} of the first stage are to be driven low. B[0:3] are the multiplicand inputs The LSB of the multiplier will drive the MULT pin of the first stage. CI of all the stages are to be driven low.

P0 of the first stage is the LSB of the final output. P1, P2, P3, CO will be driving A0, A1, A2, A3, respectively, of the second stage FMULT41.

B[0:3] are the multiplicand inputs and the MSB of the multiplier is the MULT input of the second stage. P[0:3] and CO are the other final outputs of the second stage.



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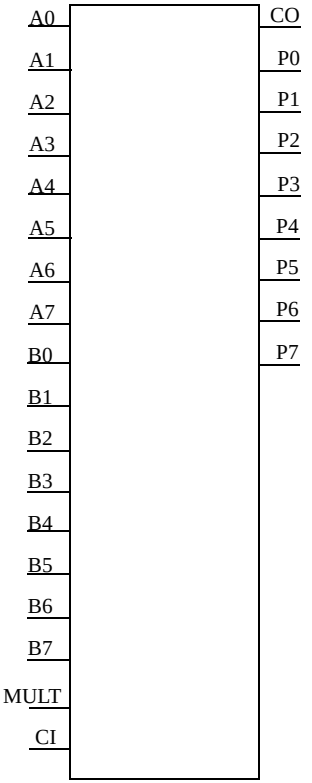
FMULT81

8 X 1 Fast Multiplier

ORCA Series		
2	3	4
	✓	✓



FMULT81

INPUTS: A0,A1,A2,A3,A4,A5,A6,A7,B0,B1,B2,B3,B4,B5,B6,B7,MULT,CI
OUTPUTS: CO,P0,P1,P2,P3,P4,P5,P6,P7
PINORDER: A0 A1 A2 A3 A4 A5 A6 A7 B0 B1 B2 B3 B4 B5 B6 B7 MULT CI CO P0 P1 P2 P3 P4 P5 P6 P7
MINIMUM CELL AREA: 0.5

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Description:

FMULT81 is a fast 8x1 multiplier macro. More than one FMULT81 cell can be combined to form larger multipliers. (See FMULT41 on the previous page for an example.) The B[7:0] inputs are the 8 bits of the multiplicand, MULT is the 1 bit multiplier input, A[7:0] are the partial sum inputs (from a previous multiplier stage), and CI is the carry-in input. The carry-out output is CO, and P[7:0] are the partial sum (or final stage) result outputs.

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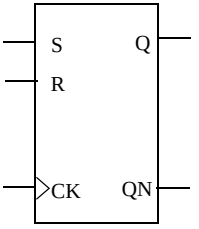
FS1S1A

Positive Level R/S Latch, GSR Used for Clear

ORCA Series		
2	3	4
✓		



FS1S1A

NOTE: The QN output pin does not exist for FPGA architectures higher than ORCA Series 4. It is not recommended to migrate ORCA netlists to Lattice-based FPGA architectures for this reason. Synthesize your netlist using the appropriate Lattice-based libraries.

INPUTS: S,R,CK
OUTPUTS: Q,QN
PINORDER: S R CK Q QN
MINIMUM CELL AREA: 0.125

Truth Table:

INPUTS			OUTPUTS	
S	R	CK	Q	QN
X	X	0	Q	QN
0	0	1	Q	QN
1	0	1	1	0
0	1	1	0	1
1	1	1	0	1

X = Don’t care
When GSR=0, Q=0, QN=1 (S=R=CK=X)

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FSUB2

2 Bit Fast Subtracter (two's complement)

Lattice FPGA		
SC	XP	EC
✓	✓	✓

FSUB2

INPUTS: A1, A0, B1, B0, BI
OUTPUTS: BOUT1, BOUT0, S1, S0
PINORDER: A1, A0, B1, B0, BI, BOUT1, BOUT0, S1, S0
CELL AREA: One Slice

Description:

FSUB2 is a 2-bit twos compliment subtractor. It has a borrow-in input (BI) and two 2-bit input (A0, A1 and B0, B1). The FSUB2 produces a 2-bit difference output (S0, S1) along with a 2-bit borrow-out output (BOUT1, BOUT).

Example pin functions:

Function	Pins
input	A1, A0, B1, B0
output	S1, S0
borrow-in input	BI
borrow-out output (Bit-0)	BOUT0
borrow-out output (Bit-1)	BOUT1

continued

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Truth Table:

INPUTS	INPUTS				OUTPUTS			
A0	A1	B0	B1	CI	SO	BOUT0	S1	BOUT1
0	0	0	0	0	0	0	1	0
1	1	0	0	0	1	1	0	1
0	0	1	1	0	0	0	0	0
1	1	1	1	0	0	0	1	0
0	0	0	0	1	1	1	0	1
1	1	0	0	1	1	1	1	1
0	0	1	1	1	0	0	1	0
1	1	1	1	1	1	1	0	1

Note: BI and BO are inverse from standard two's complement behavior.

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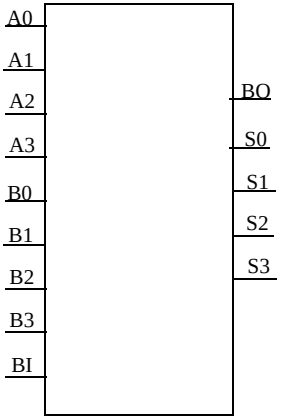
FSUB4

4 Bit Fast Subtracter (two's complement)

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



FSUB4

INPUTS: A0,A1,A2,A3,B0,B1,B2,B3,BI
OUTPUTS: BO,S0,S1,S2,S3
PINORDER: A0 A1 A2 A3 B0 B1 B2 B3 BI BO S0 S1 S2 S3
MINIMUM CELL AREA (2A/2T): 0.5
MINIMUM CELL AREA (Series 3): 0.25

Description:

FSUB4 is a 4 bit two's complement subtracter. It has a borrow-in input (BI) and two 4 bit inputs (A[3:0] and B[3:0]). The FSUB4 produces a 4 bit two's complement output of A minus B (S[3:0]) along with a borrow-out output (BO).

Note: BI and BO are inverse from standard two's complement notation.

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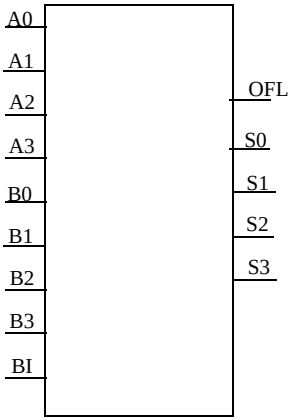
FSUB4O

4 Bit Fast Subtracter (two's complement) with Overflow

ORCA Series		
2	3	4
✓	✓	✓



FSUB4O

INPUTS: A0,A1,A2,A3,B0,B1,B2,B3,BI
OUTPUTS: OFL,S0,S1,S2,S3
PINORDER: A0 A1 A2 A3 B0 B1 B2 B3 BI OFL S0 S1 S2 S3
MINIMUM CELL AREA (2A/2T): 0.5
MINIMUM CELL AREA (Series 3): 0.25

Description:

FSUB4O is a 4 bit two's complement subtracter with overflow. It has a borrow-in input (BI) and two 4 bit inputs (A[3:0] and B[3:0]). The FSUB4O produces a 4 bit two's complement output of A minus B (S[3:0]) along with an overflow output (OFL), which is the exclusive-OR of the borrow-in to S3 and the borrow-out from S3.

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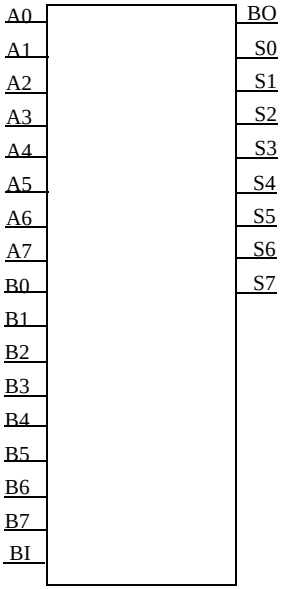
FSUB8

8 Bit Fast Subtracter (two's complement)

ORCA Series/Lattice			
3	4	XP	EC
✓	✓	✓	✓



FSUB8

INPUTS: A0,A1,A2,A3,A4,A5,A6,A7,B0,B1,B2,B3,B4,B5,B6,B7,BI
OUTPUTS: BO,S0,S1,S2,S3,S4,S5,S6,S7
PINORDER: A0 A1 A2 A3 A4 A5 A6 A7 B0 B1 B2 B3 B4 B5 B6 B7 BI BO S0 S1 S2 S3 S4 S5 S6 S7
MINIMUM CELL AREA: 0.5

Description:

FSUB8 is an 8 bit two's complement subtracter. It has a borrow-in input (BI) and two 8 bit inputs (A[7:0] and B[7:0]). The FSUB8 produces an 8 bit two's complement output of A minus B (S[7:0]) along with a borrow-out output (BO).

Note: BI and BO are inverse from standard two's complement notation.

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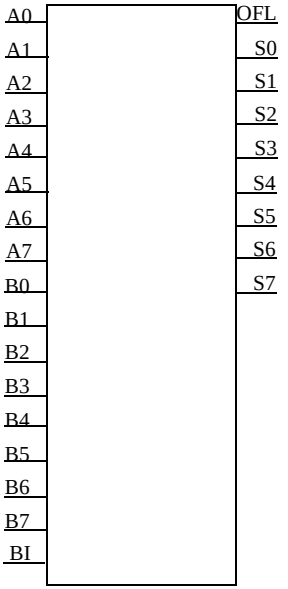
FSUB8O

8 Bit Fast Subtracter (two's complement) with Overflow

ORCA Series		
2	3	4
	✓	✓



FSUB8O

INPUTS: A0,A1,A2,A3,A4,A5,A6,A7,B0,B1,B2,B3,B4,B5,B6,B7,BI
OUTPUTS: OFL,S0,S1,S2,S3,S4,S5,S6,S7
PINORDER: A0 A1 A2 A3 A4 A5 A6 A7 B0 B1 B2 B3 B4 B5 B6 B7 BI OFL S0 S1 S2 S3 S4 S5 S6 S7
MINIMUM CELL AREA: 0.5

Description:

FSUB8O is an 8 bit two's complement subtracter with overflow. It has a borrow-in input (BI) and two 8 bit inputs (A[7:0] and B[7:0]). The FSUB8O produces an 8 bit two's complement output of A minus B (S[7:0]) along with an overflow output (OFL), which is the exclusive-OR of the borrow-in to S7 and the borrow-out from S7.

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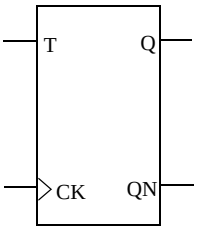
FT1S3AX

Positive Edge Triggered Toggle Flip-Flop

ORCA Series		
2	3	4
✓		



FT1S3AX

INPUTS: T,CK
OUTPUTS: Q,QN
PINORDER: T CK Q QN
MINIMUM CELL AREA: 0.25

Truth Table:

INPUTS		OUTPUTS	
T	CK	Q	QN
0	↑	Q	QN
1	↑	QN	Q

X = Don’t care
When GSR=0, Q=0, QN=1 (T=CK=X)

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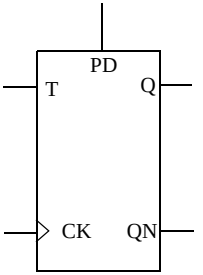
FT1S3BX

Positive Edge Triggered Toggle Flip-Flop with Positive Level Asynchronous Preset

ORCA Series		
2	3	4
✓		



FT1S3BX

INPUTS: T,CK,PD
OUTPUTS: Q,QN
PINORDER: T CK PD Q QN
MINIMUM CELL AREA: 0.25

Truth Table:

INPUTS			OUTPUTS	
T	CK	PD	Q	QN
X	X	1	1	0
0	↑	0	Q	QN
1	↑	0	QN	Q

X = Don’t care
When GSR=0, Q=1, QN=0 (T=CK=PD=X

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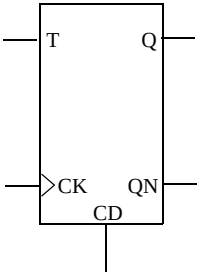
FT1S3DX

Positive Edge Triggered Toggle Flip-Flop with Positive Level Asynchronous Clear

ORCA Series		
2	3	4
✓		



FT1S3DX

INPUTS: T,CK,CD
OUTPUTS: Q,QN
PINORDER: T CK CD Q QN
MINIMUM CELL AREA: 0.25

Truth Table:

INPUTS			OUTPUTS	
T	CK	CD	Q	QN
X	X	1	0	1
0	↑	0	Q	QN
1	↑	0	QN	Q

X = Don’t care
When GSR=0, Q=0, QN=1 (T=CK=CD=X)

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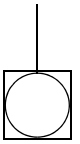
GOE

Global Output Enable

Lattice FPGA			
SC	XP	EC	MX
			✓



GOE

INPUTS: GOE
PINORDER: GOE
MINIMUM CELL AREA (All Series): 0

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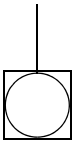
GSR

Global Set/Reset Interface

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



GSR

INPUTS: GSR
PINORDER: GSR
MINIMUM CELL AREA (All Series): 0

Description:

GSR is used to reset or set all register elements in your design. The GSR component can be connected to a net from an input buffer or an internally generated net. It is active LOW and when pulsed will set or reset all flip-flops, latches, registers, and counters to the same state as the local set or reset functionality.

It is not necessary to connect signals for GSR to any register elements explictly. The function will be implicitly connected globally. The functionality of the GSR for sequential cells without a local set or reset are described in the appropriate library manual page.

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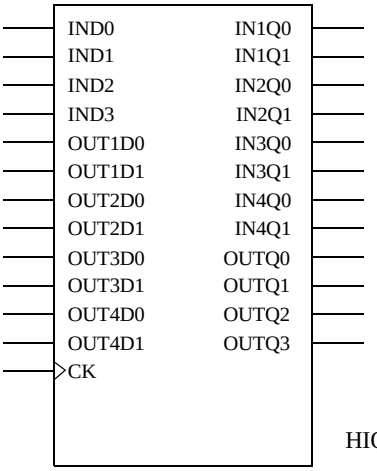
HIODDR

High-speed Input/Output DDR

ORCA Series		
2	3	4
		✓



HIODDR

INPUTS: IND0, IND1, IND2, IND3, OUT1D0, OUT1D1, OUT2D0, OUT2D1, OUT3D0, OUT3D1, OUT4D0, OUT4D1, CK
OUTPUTS: IN1Q0, IN1Q1, IN2Q0, IN2Q1, IN3Q0 IN3Q1, IN4Q0, IN4Q1, OUTQ0, OUTQ1, OUTQ2, OUTQ3
PINORDER: IND0 IND1 IND2 IND3 OUT1D0 OUT1D1 OUT2D0 OUT2D1 OUT3D0 OUT3D1 OUT4D0 OUT4D1 CK IN1Q0 IN1Q1 IN2Q0 IN2Q1 IN3Q0 IN3Q1 IN4Q0 IN4Q1 OUTQ0 OUTQ1 OUTQ2 OUTQ3
MINIMUM CELL AREA (All Series): 0
INPUT DDR MODE: IN (D0, D1, D2, D3) CK
IN1, IN2, IN3, IN4 (Q0, Q1)
OUTPUT DDR MODE: OUT1, OUT2, OUT3, OUT4 (D0, D1), CK
OUT (Q0, Q1, Q2, Q3)

Description:

Note that each HIODDR is only available to four PIOs. IND0 to IND3 come from the PADs and OUTQ0 to OUTQ3 go to the PADs, so at any given time the input and output with the same index cannot be connected to the same PAD. For example, IND0 and OUTQ0 cannot be used at the same time. Any combination of corresponding input and output mode pins in this element is allowable with respect to the PAD limitation. See diagrams and table on following pages.

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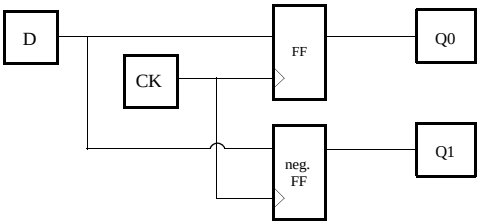
The HIODDR element uses an edge clock. You must pass the property INTERFACE:FASTINPUT to the input pads driving this element and also address the special requirement of the clock source with this property on pad C.

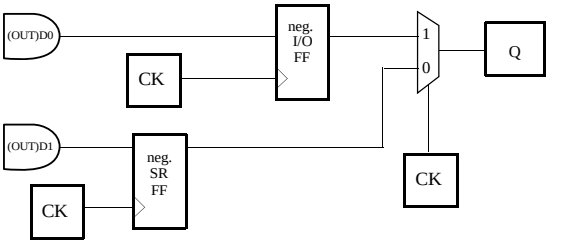
The diagram below illustrates the connectivity and functionality of the HIODDR in DDR input mode:

INDDR



The diagram below illustrates the connectivity and functionality of the HIODDR in DDR output mode:

OUTDDR



To further illustrate the pin functionality and connectivity of the HIODDR, the table below shows the functionality of pin combinations when the inputs are connected to their possible outputs to the right.

Input Pin(s)	Functionality	Output Pin(s)
INPUT DDR MODE		

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IND0	Flip-flop output (positive edge-triggered)	IN1Q0
	Flip-flop output (negative edge-triggered)	IN1Q1
Input Pin(s)	**Functionality**	**Output Pin(s)**
IND1	Flip-flop output (positive edge-triggered)	IN2Q0
	Flip-flop output (negative edge-triggered)	IN2Q1
IND2	Flip-flop output (positive edge-triggered)	IN3Q0
	Flip-flop output (negative edge-triggered)	IN3Q1
IND3	Flip-flop output (positive edge-triggered)	IN4Q0
	Flip-flop output (negative edge-triggered)	IN4Q1
OUTPUT DDR MODE		
OUT1D0	I/O Flip-flop input (negative edge-triggered)	OUTQ0
OUT1D1	SR Flip-flop input (negative edge-triggered)	
OUT2D0	I/O Flip-flop input (negative edge-triggered)	OUTQ1
OUT2D1	SR Flip-flop input (negative edge-triggered)	
OUT3D0	I/O Flip-flop input (negative edge-triggered)	OUTQ2
OUT3D1	SR Flip-flop input (negative edge-triggered)	
OUT4D0	I/O Flip-flop input (negative edge-triggered)	OUTQ3
OUT4D1	SR Flip-flop input (negative edge-triggered)	

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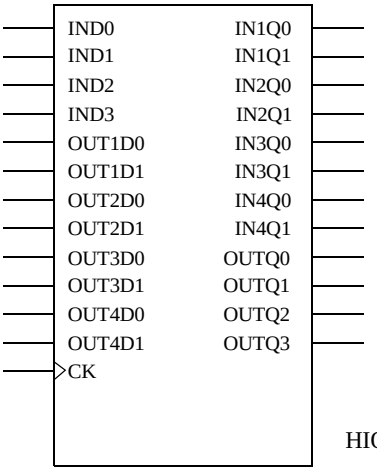
HIODDRN

High-speed Input/Output DDR

ORCA Series		
2	3	4
		✓



HIODDRN

INPUTS: IND0, IND1, IND2, IND3, OUT1D0, OUT1D1, OUT2D0, OUT2D1, OUT3D0, OUT3D1, OUT4D0, OUT4D1, CK
OUTPUTS: IN1Q0, IN1Q1, IN2Q0, IN2Q1, IN3Q0 IN3Q1, IN4Q0, IN4Q1, OUTQ0, OUTQ1, OUTQ2, OUTQ3
PINORDER: IND0 IND1 IND2 IND3 OUT1D0 OUT1D1 OUT2D0 OUT2D1 OUT3D0 OUT3D1 OUT4D0 OUT4D1 CK IN1Q0 IN1Q1 IN2Q0 IN2Q1 IN3Q0 IN3Q1 IN4Q0 IN4Q1 OUTQ0 OUTQ1 OUTQ2 OUTQ3
MINIMUM CELL AREA (All Series): 0
INPUT DDR MODE: IN (D0, D1, D2, D3) CK
IN1, IN2, IN3, IN4 (Q0, Q1)
OUTPUT DDR MODE: OUT1, OUT2, OUT3, OUT4 (D0, D1), CK
OUT (Q0, Q1, Q2, Q3)

Description:

Note that each HIODDRN is only available to four PIOs. IND0 to IND3 come from the PADs and OUTQ0 to OUTQ3 go to the PADs, so at any given time the input and output with the same index cannot be connected to the same PAD. For example, IND0 and OUTQ0 cannot be used at the same time. Any combination of corresponding input and output mode pins in this element is allowable with respect to the PAD limitation. See diagrams and table on following pages.

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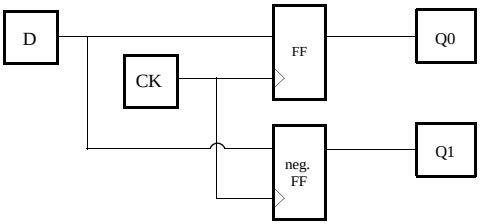
The HIODDRN element uses an edge clock. You must pass the property INTERFACE:FASTINPUT to the input pads driving this element and also address the special requirement of the clock source with this property on pad C.

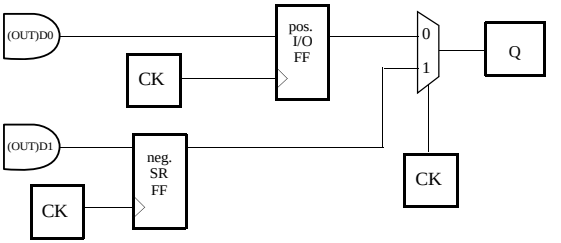
The diagram below illustrates the connectivity and functionality of the HIODDRN in DDR input mode:

INDDR



The diagram below illustrates the connectivity and functionality of the HIODDRN in DDR output mode:

OUTDDR



To further illustrate the pin functionality and connectivity of the HIODDRN, the table below shows the functionality of pin combinations when the inputs are connected to their possible outputs to the right.

Input Pin(s)	Functionality	Output Pin(s)
INPUT DDR MODE		

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IND0	Flip-flop output (positive edge-triggered)	IN1Q0
	Flip-flop output (negative edge-triggered)	IN1Q1
Input Pin(s)	**Functionality**	**Output Pin(s)**
IND1	Flip-flop output (positive edge-triggered)	IN2Q0
	Flip-flop output (negative edge-triggered)	IN2Q1
IND2	Flip-flop output (positive edge-triggered)	IN3Q0
	Flip-flop output (negative edge-triggered)	IN3Q1
IND3	Flip-flop output (positive edge-triggered)	IN4Q0
	Flip-flop output (negative edge-triggered)	IN4Q1
OUTPUT DDR MODE		
OUT1D0	I/O Flip-flop input (positive edge-triggered)	OUTQ0
OUT1D1	SR Flip-flop input (negative edge-triggered)	
OUT2D0	I/O Flip-flop input (positive edge-triggered)	OUTQ1
OUT2D1	SR Flip-flop input (negative edge-triggered)	
OUT3D0	I/O Flip-flop input (positive edge-triggered)	OUTQ2
OUT3D1	SR Flip-flop input (negative edge-triggered)	
OUT4D0	I/O Flip-flop input (positive edge-triggered)	OUTQ3
OUT4D1	SR Flip-flop input (negative edge-triggered)	

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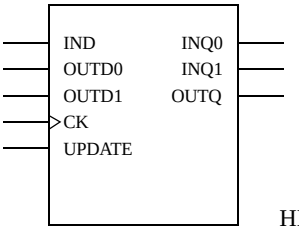
HIOSR2

High-speed Input/Output 2-Bit Shift Register

ORCA Series		
2	3	4
		✓



HIOSR2

INPUTS: IND, OUTD0, OUTD1, CK, UPDATE
OUTPUTS: INQ0, INQ1, OUTQ
PINORDER: IND, OUTD0, OUTD1, CK, UPDATE, INQ0, INQ1, OUTQ
MINIMUM CELL AREA (All Series): 0

Description:

For input shift registers, IND is the input and INQ0 and INQ1 are the two outputs. For output shift registers OUTD0, OUTD1 are the two inputs and OUTQ is the output. The HIOSR2 element uses an edge clock. You must pass the property INTERFACE:FASTINPUT to the input pads driving this element and also address the special requirement of the clock source with this property on pad C.

Refer to the HIOSR4 element for a better understanding of output and input modes for the IOSR2 element. Shift register timing is also comparable in the HIOSR4 and you should refer to the HIOSR4 *OUTPUT Shift Register Timing Diagram* and *INPUT Shift Register Timing Diagram* for more information.

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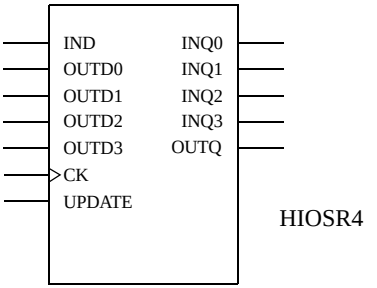
HIOSR4

High-speed Input/Output 4-Bit Shift Register

ORCA Series		
2	3	4
		✓



HIOSR4

INPUTS: IND, OUTD0, OUTD1, OUTD2, OUTD3, CK, UPDATE
OUTPUTS: INQ0, INQ1, INQ2, INQ3, OUTQ
PINORDER: IND, OUTD0, OUTD1, OUTD2, OUTD3, CK, UPDATE, INQ0, INQ1, INQ2, INQ3, OUTQ
MINIMUM CELL AREA (All Series): 0

Description:

For input shift registers, IND is the input and INQ0, INQ1, INQ2, and INQ3 are the four outputs. For output shift registers OUTD0, OUTD1, OUTD2, and OUTD3 are the four inputs and OUTQ is the output. The HIOSR4 element uses an edge clock. You must pass the property INTERFACE:FASTINPUT to the input pads driving this element and also address the special requirement of the clock source with this property on pad C.

Shift Register Timing

The waveform diagrams on the following page illustrate output and input shift register timing in the HIOSR4 element. Please refer to these waveforms for the HIOSR2 element as well.

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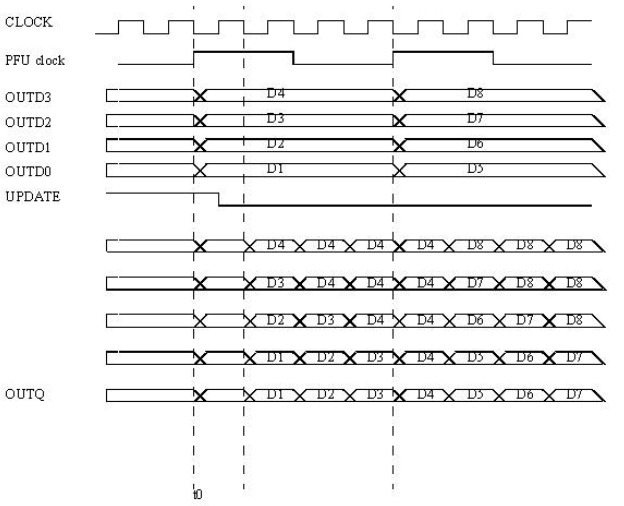
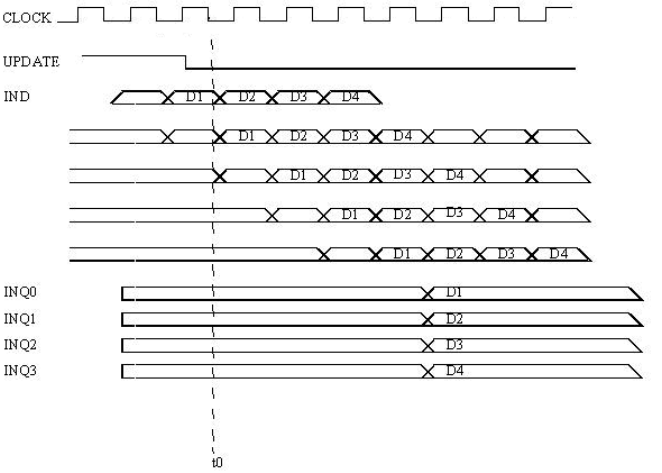
OUTPUT Shift Register Timing Diagram



INPUT Shift Register Timing Diagram



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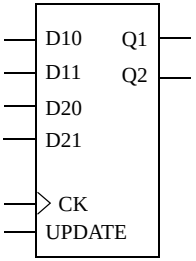
HOSR2X2

High-speed Output Dual 2-Bit Shift Register

ORCA Series		
2	3	4
		✓



HOSR2X2

INPUTS: D10,D11,D20,D21,CK,UPDATE
OUTPUTS: Q1,Q2
PINORDER: I O
MINIMUM CELL AREA (All Series): 0

Description:

D10 and D11 are the inputs and Q1 is the output of shift register 1. D20 and D21 are the inputs and Q2 is the output of shift register 2. The HOSR2X2 element uses an edge clock. You must pass the property INTERFACE:FASTINPUT to the input pads driving this element and also address the special requirement of the clock source with this property on pad C..

continued

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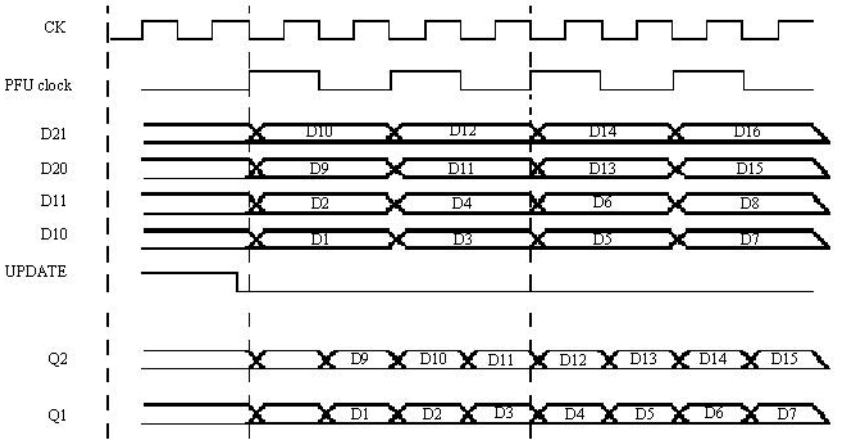
Below is a waveform showing the inputs/outputs of the HOSR2X2 element.



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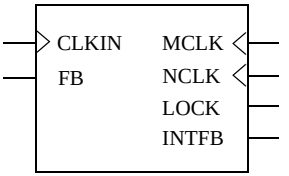
HPPLL

High Frequency Programmable Clock Manager (Programmable general purpose Phase Locked Loop)

ORCA Series		
2	3	4
		✓



HPPLL

INPUTS: CLKIN,FB
OUTPUTS: MCLK,NCLK,LOCK,INTFB
PINORDER: CLKIN FB MCLK NCLK LOCK INTFB
MINIMUM CELL AREA: 0
ATTRIBUTES (Series 4 only)
DIV0: 1, 2, 3, 4, 5, 6, 7, 8
DIV1: 1, 2, 3, 4, 5, 6, 7, 8
DIV2: 1, 2, 3, 4, 5, 6, 7, 8
DIV3: 1, 2, 3, 4, 5, 6, 7, 8
MCLKMODE: BYPASS, DUTYCYCLE, PHSHIFT, DELAY
NCLKMODE: BYPASS, DUTYCYCLE, PHSHIFT, DELAY
VCOTAP: 0, 1, 2, 3, 4, 5, 6, 7
DISABLED_GSR: 0, 1
FB_PDEL: DEL0, DEL1, DEL2, DEL3

Description:

The phase locked loop is one of the functions performed by the PCM which is user selectable through configuration logic and/or a PCM_FPGA interface.

***Notes*:** The HPPLL element should be instantiated through SCUBA. Refer to the appropriate topic in the online help system for details. In addition, the FB_PDEL property should be used only if the FB port is driven from external routing (e.g., MCLK or NCLK).

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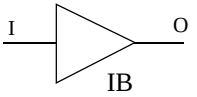
IB

Input Buffer

Lattice FPGA		
SC	XP	EC
✓	✓	✓



INPUTS: I
OUTPUTS: O
PINORDER: I O
MINIMUM CELL AREA: 0
ATTRIBUTES (LatticeSC)
IO_TYPE: LVDS, BLVDS25, MLVDS25, HYPT, LVPECL25, LVPECL33, HSTL15_I, HSTL15_II, HSTL15_III, HSTL15_IV, HSTL15D_I, HSTL15D_II, HSTL18_I, HSTL18_II, HSTL18_III, HSTL18_IV, HSTL18D_I, HSTL18D_II, SSTL18_I, SSTL18_II, SSTL18D_I, SSTL18D_II, SSTL25_I, SSTL25_II, SSTL25D_I, SSTL25D_II, SSTL33_I, SSTL_II, SSTL33D_I, SSTL33D_II, GTLPLUS15, GTL12, LVTTL33, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVCMOS12, PCI33, PCIX33, PCIX15, AGP1X33, AGP2X33,
DIFFRESISTOR: OFF(default), 100, 150, 200 (Only for differential buffers)
TERMINATEVCCIO: OFF (default), 33, 50, 100 (Termination Up)
TERMINATEGND: OFF (default), 33, 50, 100 (Termination Down)
VCMT: OFF, ON
PULLMODE: UP, DOWN, NONE, KEEPER, PCICLAMP

Truth Table:

INPUTS	OUTPUTS
I	O
1	1
0	0
Z	U

U = Unknown

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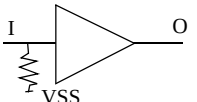
IBPD

Input Buffer with Pull-down

Lattice FPGA		
SC	XP	EC
✓	✓	✓



IBPD

INPUTS: I
OUTPUTS: O
PINORDER: I O
MINIMUM CELL AREA: 0
ATTRIBUTES (LatticeSC)
IO_TYPE: LVDS, BLVDS25, MLVDS25, HYPT, LVPECL25, LVPECL33, HSTL15_I, HSTL15_II, HSTL15_III, HSTL15_IV, HSTL15D_I, HSTL15D_II, HSTL18_I, HSTL18_II, HSTL18_III, HSTL18_IV, HSTL18D_I, HSTL18D_II, SSTL18_I, SSTL18_II, SSTL18D_I, SSTL18D_II, SSTL25_I, SSTL25_II, SSTL25D_I, SSTL25D_II, SSTL33_I, SSTL_II, SSTL33D_I, SSTL33D_II, GTLPLUS15, GTL12, LVTTL33, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVCMOS12, PCI33, PCIX33, PCIX15, AGP1X33, AGP2X33,
DIFFRESISTOR: OFF(default), 100, 150, 200 (Only for differential buffers)
TERMINATEVCCIO: OFF (default), 33, 50, 100 (Termination Up)
TERMINATEGND: OFF (default), 33, 50, 100 (Termination Down)
VCMT: OFF, ON
PULLMODE: UP, DOWN, NONE, KEEPER, PCICLAMP

Truth Table:

INPUTS	OUTPUTS
I	O
1	1
0	0
Z	0

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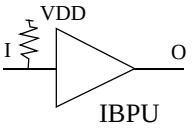
IBPU

Input Buffer with Pull-up

Lattice FPGA		
SC	XP	EC
✓	✓	✓



INPUTS: I
OUTPUTS: O
PINORDER: I O
MINIMUM CELL AREA: 0
ATTRIBUTES (LatticeSC)
IO_TYPE: LVDS, BLVDS25, MLVDS25, HYPT, LVPECL25, LVPECL33, HSTL15_I, HSTL15_II, HSTL15_III, HSTL15_IV, HSTL15D_I, HSTL15D_II, HSTL18_I, HSTL18_II, HSTL18_III, HSTL18_IV, HSTL18D_I, HSTL18D_II, SSTL18_I, SSTL18_II, SSTL18D_I, SSTL18D_II, SSTL25_I, SSTL25_II, SSTL25D_I, SSTL25D_II, SSTL33_I, SSTL_II, SSTL33D_I, SSTL33D_II, GTLPLUS15, GTL12, LVTTL33, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVCMOS12, PCI33, PCIX33, PCIX15, AGP1X33, AGP2X33,
DIFFRESISTOR: OFF(default), 100, 150, 200 (Only for differential buffers)
TERMINATEVCCIO: OFF (default), 33, 50, 100 (Termination Up)
TERMINATEGND: OFF (default), 33, 50, 100 (Termination Down)
VCMT: OFF, ON
PULLMODE: UP, DOWN, NONE, KEEPER, PCICLAMP

Truth Table:

INPUTS	OUTPUTS
I	O
1	1
0	0
Z	1

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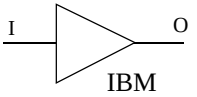
IBM

CMOS Input Buffer

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



INPUTS: I
OUTPUTS: O
PINORDER: I O
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVTTL, LVCMOS2 (default), LVDS, LVDSE, LVPECL, LVCMOS18, PCI, PECL, SSTL2, SSTL3, HSTL1, HSTL3, GTL, GTLPLUS
DELAYMODE: 1, 0 (default)
RESISTOR: OFF (default), ON (only for LVDS and LVPECL)
INTERFACE: FASTINPUT

3.3V PCI compliant (3T series only)

Note: The INTERFACE property is only supported when LEVELMODE=HSTL1.

Truth Table:

INPUTS	OUTPUTS
I	O
1	1
0	0
Z	U

U = Unknown

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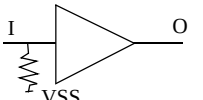
IBMPD

CMOS Input Buffer with Pull-down

ORCA Series/Lattice FPGA				
2	3	4	XP	EC
✓	✓	✓	✓	✓



IBMPD

INPUTS: I
OUTPUTS: O
PINORDER: I O
MINIMUM CELL AREA(All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVCMOS2 (default), LVTTL
DELAYMODE: 0 (default), 1

3.3V PCI compliant (3T series only)

Truth Table:

INPUTS	OUTPUTS
I	O
1	1
0	0
Z	0

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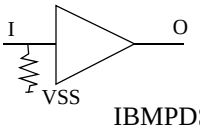
IBMPDS

CMOS Input Buffer with Pull-down and Delay

ORCA Series/Lattice FPGA				
2	3	4	XP	EC
✓	✓	✓	✓	✓



IBMPDS

INPUTS: I
OUTPUTS: O
PINORDER: I O
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVCMOS2 (default), LVTTL
DELAYMODE: 1

3.3V PCI compliant (3T series only)

Truth Table:

INPUTS	OUTPUTS
I	O
1	1
0	0
Z	0

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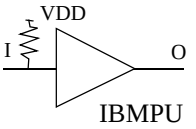
IBMPU

CMOS Input Buffer with Pull-up

ORCA Series/Lattice FPGA				
2	3	4	XP	EC
✓	✓	✓	✓	✓



INPUTS: I
OUTPUTS: O
PINORDER: I O
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVCMOS2 (default), LVTTL
DELAYMODE: 0 (default), 1

3.3V PCI compliant (3T series only)

Truth Table:

INPUTS	OUTPUTS
I	O
1	1
0	0
Z	1

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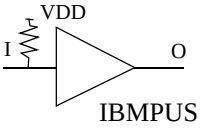
IBMPUS

CMOS Input Buffer with Pull-up and Delay

ORCA Series/Lattice FPGA				
2	3	4	XP	EC
✓	✓	✓	✓	✓



INPUTS: I
OUTPUTS: O
PINORDER: I O
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVCMOS2 (default), LVTTL
DELAYMODE: 1

3.3V PCI compliant (3T series only)

Truth Table:

INPUTS	OUTPUTS
I	O
1	1
0	0
Z	1

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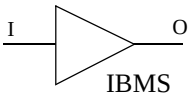
IBMS

CMOS Input Buffer with Delay

ORCA Series/Lattice FPGA				
2	3	4	XP	EC
✓	✓	✓	✓	✓



INPUTS: I
OUTPUTS: O
PINORDER: I O
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVCMOS2
DELAYMODE: 1

3.3V PCI compliant (3T series only)

Truth Table:

INPUTS	OUTPUTS
I	O
1	1
0	0
Z	U

U = Unknown

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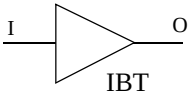
IBT

TTL Input Buffer

ORCA Series		
2	3	4
✓	✓	✓



INPUTS: I
OUTPUTS: O
PINORDER: I O
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVTTL
DELAYMODE: 0

5V tolerant/5V PCI compliant (3T series only)

Truth Table:

INPUTS	OUTPUTS
I	O
1	1
0	0
Z	U

U = Unknown

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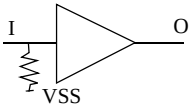
IBTPD

TTL Input Buffer with Pull-down

ORCA Series		
2	3	4
✓	✓	✓



IBTPD

INPUTS: I
OUTPUTS: O
PINORDER: I O
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVTTL
DELAYMODE: 0

5V tolerant/5V PCI compliant (3T series only)

Truth Table:

INPUTS	OUTPUTS
I	O
1	1
0	0
Z	0

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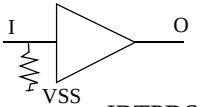
IBTPDS

TTL Input Buffer with Pull-down and Delay

ORCA Series		
2	3	4
✓	✓	✓



IBTPDS

INPUTS: I
OUTPUTS: O
PINORDER: I O
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVTTL
DELAYMODE: 1

5V tolerant/5V PCI compliant (3T series only)

Truth Table:

INPUTS	OUTPUTS
I	O
1	1
0	0
Z	0

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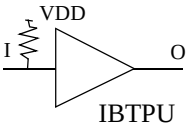
IBTPU

TTL Input Buffer with Pull-up

ORCA Series		
2	3	4
✓	✓	✓



INPUTS: I
OUTPUTS: O
PINORDER: I O
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVTTL
DELAYMODE: 0

5V tolerant/5V PCI compliant (3T series only)

Truth Table:

INPUTS	OUTPUTS
I	O
1	1
0	0
Z	1

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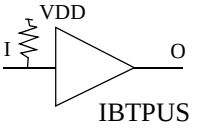
IBTPUS

TTL Input Buffer with Pull-up and Delay

ORCA Series		
2	3	4
✓	✓	✓



INPUTS: I
OUTPUTS: O
PINORDER: I O
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVTTL
DELAYMODE: 1

5V tolerant/5V PCI compliant (3T series only)

Truth Table:

INPUTS	OUTPUTS
I	O
1	1
0	0
Z	1

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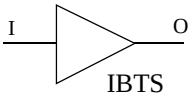
IBTS

TTL Input Buffer with Delay

ORCA Series		
2	3	4
✓	✓	✓



INPUTS: I
OUTPUTS: O
PINORDER: I O
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVTTL
DELAYMODE: 1

5V tolerant/5V PCI compliant (3T series only)

Truth Table:

INPUTS	OUTPUTS
I	O
1	1
0	0
Z	U

U = Unknown

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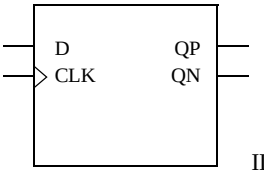
IDDR

Input DDR

ORCA Series		
2	3	4
		✓



IDDR

INPUTS: D, CLK
OUTPUTS: QP, QN
PINORDER: D, CLK, QP, QN,
MINIMUM CELL AREA: 0

Description:

Double Data Rate input logic. QP is the positive edge-triggered output and QN is the negative edge-triggered output.

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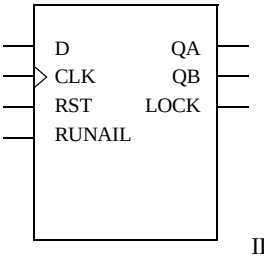
IDDRA

Input DDR

Lattice FPGA		
SC	XP	EC
✓		



IDDRA

INPUTS: D, CLK, RST, RUNAIL
OUTPUTS: QA, QB, LOCK
PINORDER: D, CLK, RST, RUNAIL, QA, QB, LOCK
ATTRIBUTES (LatticeSC)
LSRMODE: EDGE, LOCAL
CLKMODE: SCLK, ECLK
AIL: OFF, ON (Adaptive input logic mode)
STEP: ONE, TWO, THREE, FOUR (Valid only when AIL = ON)
SWAP: OFF, ON (Valid only when AIL = ON)
BESTFIT: OFF, ON
CLKEDGE: ONE, TWO (Valid only when AIL = ON)
DISABLED_GSR: 0, 1 (Valid only when AIL = ON and affects only to cntl)

Description:

Double Data Rate input logic.

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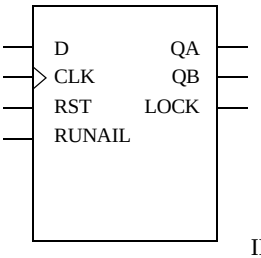
IDDRXA

Input DDR

Lattice FPGA		
SC	XP	EC
✓		



IDDRXA

INPUTS: D, CLK, RST, RUNAIL
OUTPUTS: QA, QB, LOCK
PINORDER: D, CLK, RST, RUNAIL, QA, QB, LOCK
ATTRIBUTES (LatticeSC)
LSRMODE: EDGE, LOCAL
CLKMODE: SCLK, ECLK
AIL: OFF, ON (Adaptive input logic mode)
STEP: ONE, TWO, THREE, FOUR (Valid only when AIL = ON)
SWAP: OFF, ON (Valid only when AIL = ON)
BESTFIT: OFF, ON
CLKEDGE: ONE, TWO (Valid only when AIL = ON)
DISABLED_GSR: 0, 1 (Valid only when AIL = ON and affects only to cntl)

Description:

Double Data Rate input logic with half cycle clock domain transfer for the negative edge captured data (both edges of captured data enter core with positive edge flip-flops.

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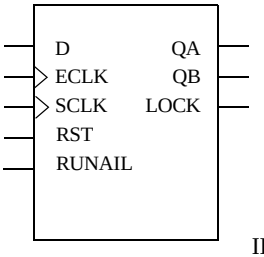
IDDRX1A

Input DDR

Lattice FPGA		
SC	XP	EC
✓		



IDDRX1A

INPUTS: D, ECLK, SCLK, RST, RUNAIL
OUTPUTS: QA, QB, LOCK
PINORDER: D, ECLK, SCLK, RST, RUN, QA, QB, LOCK
ATTRIBUTES (LatticeSC)
LSRMODE: EDGE, LOCAL
CLKMODE: SCLK, ECLK
AIL: OFF, ON (Adaptive input logic mode)
STEP: ONE, TWO, THREE, FOUR (Valid only when AIL = ON)
SWAP: OFF, ON (Valid only when AIL = ON)
BESTFIT: OFF, ON
CLKEDGE: ONE, TWO (Valid only when AIL = ON)
DISABLED_GSR: 0, 1 (Valid only when AIL = ON and affects only to cntl)

Description:

Double Data Rate input logic. The input register block captures DDR input data using edge clock to primary clock domain transfer. It can also be set to perform the same functions as in the shift mode

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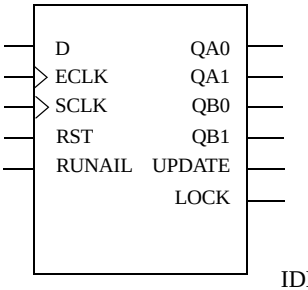
IDDRX2A

Input DDR

Lattice FPGA		
SC	XP	EC
✓		



IDDRX2A

INPUTS: D, ECLK, SCLK, RST, RUNAIL
OUTPUTS: QA0, QA1, QB0, QB1, UPDATE, LOCK
PINORDER: D, ECLK, SCLK, RST, RUNAIL, QA0, QA1, QB0, QB1, UPDATE, LOCK
MINIMUM CELL AREA: 0
ATTRIBUTES (LatticeSC)
LSRMODE: EDGE, LOCAL
AIL: OFF, ON (Adaptive input logic mode)
STEP: ONE, TWO, THREE, FOUR (Valid only when AIL = ON)
SWAP: OFF, ON (Valid only when AIL = ON)
BESTFIT: OFF, ON
CLKEDGE: ONE, TWO (Valid only when AIL = ON)
UPDT: POS, NEG
DISABLED_GSR: 0, 1 (Valid only when AIL = ON and affects only to cntl)

Description:

Double Data Rate input logic. The input register block captures DDR input data using edge clock to primary clock domain transfer. It can also be set to perform the same functions as in the shift mode.

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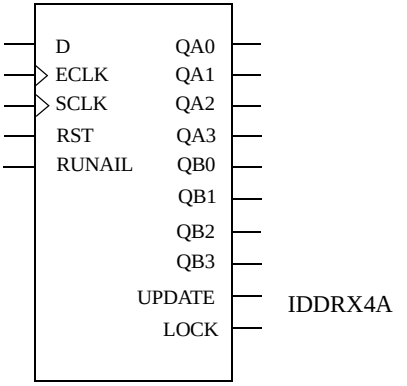
IDDRX4A

Input DDR

Lattice FPGA		
SC	XP	EC
✓		



INPUTS: D, ECLK, SCLK, RST, RUNAIL
OUTPUTS: QA0, QA1, QA2, QA3, QB0, QB1, QB2, QB3, UPDATE, LOCK
PINORDER: D, ECLK, SCLK, RST, RUNAIL, QA0, QA1, QA2, QA3, QB0, QB1, QB2, QB3, UPDATE, LOCK
MINIMUM CELL AREA: 0
ATTRIBUTES (LatticeSC)
LSRMODE: EDGE, LOCAL
AIL: OFF, ON (Adaptive input logic mode)
STEP: ONE, TWO, THREE, FOUR (Valid only when AIL = ON)
SWAP: OFF, ON (Valid only when AIL = ON)
BESTFIT: OFF, ON
CLKEDGE: ONE, TWO (Valid only when AIL = ON)
UPDT: POS, NEG
DISABLED_GSR: 0, 1 (Valid only when AIL = ON and affects only to cntl)

Description:

Double Data Rate input logic. The input register block captures DDR input data using edge clock to primary clock domain transfer. It can also be set to perform the same functions as in the shift mode.

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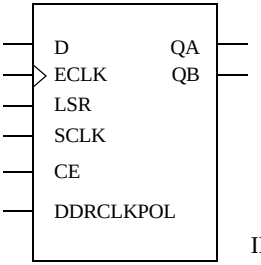
IDDRXB

Input DDR

Lattice FPGA		
SC	XP	EC
	✓	✓



IDDRXB

INPUTS: D, ECLK, LSR, SCLK, CE , DDRCLKPOL
OUTPUTS: QA, QB
PINORDER: D, ECLK, LSR, SCLK, CE , DDRCLKPOL, QA, QB
MINIMUM CELL AREA: 0
ATTRIBUTES

Description:

Double Data Rate input logic with half cycle clock domain transfer for the negative edge captured data (both edges of captured data enter core with positive edge flip-flops.

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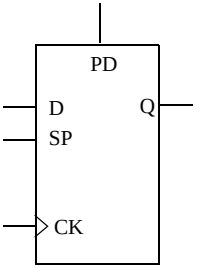
IFS1P1B

Positive Level Latch with Positive Level Enable and Positve Level Asynchronous Preset

Lattice FPGA		
SC	XP	EC
✓	✓	✓



IFS1P1B

INPUTS: D, CK, SP, PD
OUTPUTS: Q
PINORDER: D, CK, SP, PD, Q
MINIMUM CELL AREA: 0

Truth Table:

INPUTS			OUTPUTS
D	SCLK	PD	Q
X	0	0	Q
X	X	1	1
0	1	0	0
1	1	0	1

X= Don’t care
When GSR=0, Q=1 (D=SCLK=PD=X)

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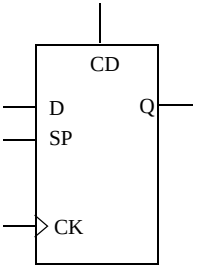
IFS1P1D

Positive Level Latch with Positive Level Enable and Positive Asynchronous Clear



IFS1P1D

Lattice FPGA		
SC	XP	EC
✓	✓	✓

INPUTS: D, CK SP, CD
OUTPUTS: Q
PINORDER: D, CK SP, CD, Q
MINIMUM CELL AREA: 0

Truth Table:

INPUTS			OUTPUTS
D	SCLK	PD	Q
X	0	0	Q
X	X	1	1
0	1	0	0
1	1	0	1

X= Don’t care
When GSR=0, Q=1 (D=SCLK=PD=X)

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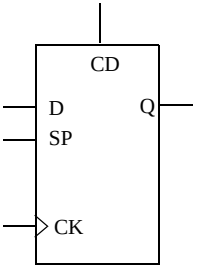
IFS1P1I

Positive Level Latch with Positive Level Enable and Positive Asynchronous Clear

Lattice FPGA		
SC	XP	EC
✓	✓	✓



IFS1P1I

INPUTS: D, CK, SP, CD
OUTPUTS: Q
PINORDER: D, CK, SP, CD, Q
MINIMUM CELL AREA: 0

Truth Table:

INPUTS			OUTPUTS
D	SCLK	PD	Q
X	0	0	Q
X	X	1	1
0	1	0	0
1	1	0	1

X= Don’t care
When GSR=0, Q=1 (D=SCLK=PD=X)

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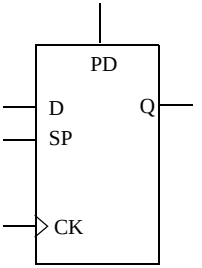
IFS1P1J

Positive Level Latch with Positive Level Enable and Positive Level Asynchronous Preset

Lattice FPGA		
SC	XP	EC
✓	✓	✓



IFS1P1J

INPUTS: D, CK, SP, PD
OUTPUTS: Q
PINORDER: D SCLK PD Q
MINIMUM CELL AREA: 0

Truth Table:

INPUTS			OUTPUTS
D	SCLK	PD	Q
X	0	0	Q
X	X	1	1
0	1	0	0
1	1	0	1

X= Don’t care
When GSR=0, Q=1 (D=SCLK=PD=X)

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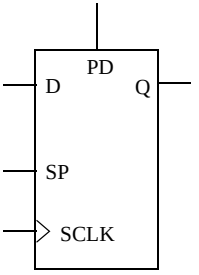
IFS1P3BX

Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Asynchronous Preset, and System Clock (used in input PIC area only)



IFS1P3BX

ORCA Series/Lattice FPGA				
3	4	SC	XP	EC
✓	✓	✓	✓	✓

Note: This element must be paired with an input or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

INPUTS: D,SP,SCLK,PD
OUTPUTS: Q
PINORDER: D SP SCLK PD Q
MINIMUM CELL AREA: 0
ATTRIBUTES (Series 4 only)
  CLKMODE: SCLK (default), ECLK

Note: ECLK can only be taken as an attribute if FASTINPUT is used on the buffer associated with the flip-flop.

Truth Table:

INPUTS				OUTPUTS
D	SP	SCLK	PD	Q
X	0	X	0	Q
X	X	X	1	1
0	1	↑	0	0
1	1	↑	0	1

X = Don’t care
When GSR=0, Q=1 (D=SP=SCLK=PD=X)

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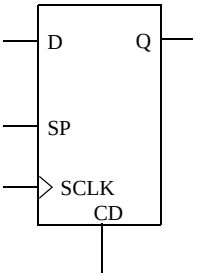
IFS1P3DX

Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Asynchronous Clear, and System Clock (used in input PIC area only)



IFS1P3DX

ORCA Series/Lattice FPGA				
3	4	SC	XP	EC
✓	✓	✓	✓	✓

Note: This element must be paired with an input or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

INPUTS: D,SP,SCLK,CD
OUTPUTS: Q
PINORDER: D SP SCLK CD Q
MINIMUM CELL AREA: 0
ATTRIBUTES (Series 4 only)
CLKMODE: SCLK (default), ECLK

Note: ECLK can only be taken as an attribute if FASTINPUT is used on the buffer associated with the flip-flop.

Truth Table:

INPUTS				OUTPUTS
D	SP	SCLK	CD	Q
X	0	X	0	Q
X	X	X	1	0
0	1	↑	0	0
1	1	↑	0	1

X = Don’t care
When GSR=0, Q=0 (D=SP=SCLK=CD=X)

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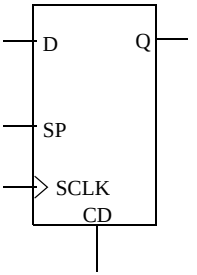
IFS1P3IX

Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Clear, Positive Level Enable, and System Clock (Clear overrides Enable) (used in input PIC area only)



IFS1P3IX

ORCA Series/Lattice FPGA				
3	4	SC	XP	EC
✓	✓	✓	✓	✓

Note: This element must be paired with an input or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

INPUTS: D,SP,SCLK,CD
OUTPUTS: Q
PINORDER: D SP SCLK CD Q
MINIMUM CELL AREA: 0
ATTRIBUTES (Series 4 only)
CLKMODE: SCLK (default), ECLK

Note: ECLK can only be taken as an attribute if FASTINPUT is used on the buffer associated with the flip-flop.

Truth Table:

INPUTS				OUTPUTS
D	SP	SCLK	CD	Q
X	0	X	0	Q
X	X	↑	1	0
0	1	↑	0	0
1	1	↑	0	1

X = Don’t care
When GSR=0, Q=0 (D=SP=SCLK=CD=X)

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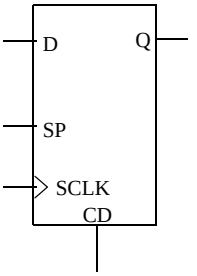
IFS1P3IZ

Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Synchronous Clear, and System Clock (used in input PIC area only)



IFS1P3IZ

ORCA Series		
2	3	4
	✓	✓

Note: This element must be paired with an input or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

INPUTS: D,SP,SCLK,CD
OUTPUTS: Q
PINORDER: D SP SCLK CD Q
MINIMUM CELL AREA: 0
ATTRIBUTES (Series 4 only)
CLKMODE: SCLK (default), ECLK

Note: ECLK can only be taken as an attribute if FASTINPUT is used on the buffer associated with the flip-flop.

Truth Table:

INPUTS				OUTPUTS
D	SP	SCLK	CD	Q
X	0	X	X	Q
X	1	↑	1	0
0	1	↑	0	0
1	1	↑	0	1

X = Don’t care
When GSR=0, Q=0 (D=SP=SCLK=CD=X)

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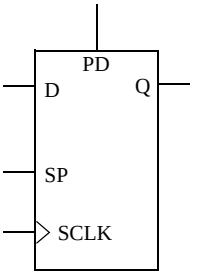
IFS1P3JX

Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Preset, Positive Level Enable, and System Clock (Preset overrides Enable) (used in input PIC area only)



IFS1P3JX

ORCA Series/Lattice FPGA				
3	4	SC	XP	EC
✓	✓	✓	✓	✓

Note: This element must be paired with an input or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

INPUTS: D,SP,SCLK,PD
OUTPUTS: Q
PINORDER: D SP SCLK PD Q
MINIMUM CELL AREA: 0
ATTRIBUTES (Series 4 only)
CLKMODE: SCLK (default), ECLK

Note: ECLK can only be taken as an attribute if FASTINPUT is used on the buffer associated with the flip-flop.

Truth Table:

INPUTS				OUTPUTS
D	SP	SCLK	PD	Q
X	0	X	0	Q
X	X	↑	1	1
0	1	↑	0	0
1	1	↑	0	1

X = Don’t care
When GSR=0, Q=1 (D=SP=SCLK=PD=X)

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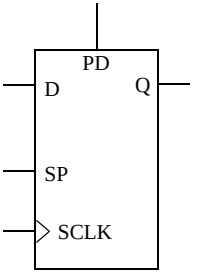
IFS1P3JZ

Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Synchronous Preset, and System Clock (used in input PIC area only)



IFS1P3JZ

ORCA Series		
2	3	4
	✓	✓

Note: This element must be paired with an input or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

INPUTS: D,SP,SCLK,PD
OUTPUTS: Q
PINORDER: D SP SCLK PD Q
MINIMUM CELL AREA: 0
ATTRIBUTES (Series 4 only)
CLKMODE: SCLK (default), ECLK

Note: ECLK can only be taken as an attribute if FASTINPUT is used on the buffer associated with the flip-flop.

Truth Table:

INPUTS				OUTPUTS
D	SP	SCLK	PD	Q
X	0	X	X	Q
X	1	↑	1	1
0	1	↑	0	0
1	1	↑	0	1

X = Don’t care
When GSR=0, Q=1 (D=SP=SCLK=PD=X)

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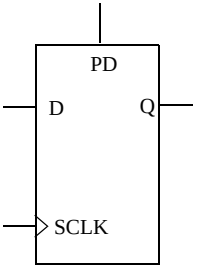
IFS1S1B

Positive Level Data Latch with Positive Level Asynchronous Preset and System Clock (used in input PIC area only)



IFS1S1B

ORCA Series/Lattice			
3	4	XP	EC
✓	✓	✓	✓

Note: This element must be paired with an input or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

INPUTS: D,SCLK,PD
OUTPUTS: Q
PINORDER: D SCLK PD Q
MINIMUM CELL AREA: 0

Truth Table:

INPUTS			OUTPUTS
D	SCLK	PD	Q
X	0	0	Q
X	X	1	1
0	1	0	0
1	1	0	1

X= Don’t care
When GSR=0, Q=1 (D=SCLK=PD=X)

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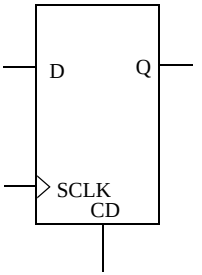
IFS1S1D

Positive Level Data Latch with Positive Level Asynchronous Clear and System Clock (used in input PIC area only)

ORCA Series/Lattice			
3	4	XP	EC
✓	✓	✓	✓



IFS1S1B

Note: This element must be paired with an input or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

INPUTS: D,SCLK,CD
OUTPUTS: Q
PINORDER: D SCLK CD Q
MINIMUM CELL AREA: 0

Truth Table:

INPUTS			OUTPUTS
D	SCLK	CD	Q
X	0	0	Q
X	X	1	0
0	1	0	0
1	1	0	1

X = Don’t care
When GSR=0, Q=0 (D=SCLK=CD=X)

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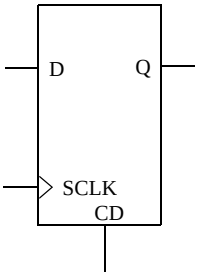
IFS1S1I

Positive Level Data Latch with Positive Level Synchronous Clear and System Clock (used in input PIC area only)

ORCA Series/Lattice			
3	4	XP	EC
✓	✓	✓	✓



IFS1S1I

Note: This element must be paired with an input or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

INPUTS: D,SCLK,CD
OUTPUTS: Q
PINORDER: D SCLK CD Q
MINIMUM CELL AREA: 0

Truth Table:

INPUTS			OUTPUTS
D	SCLK	CD	Q
X	0	0	Q
X	1	1	0
0	1	0	0
1	1	0	1

X = Don’t care
When GSR=0, Q=0 (D=SCLK=CD=X)

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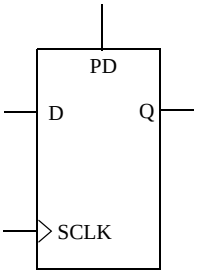
IFS1S1J

Positive Level Data Latch with Positive Level Synchronous Preset and System Clock (used in input PIC area only)

ORCA Series/Lattice			
3	4	XP	EC
✓	✓	✓	✓



IFS1S1J

Note: This element must be paired with an input or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

INPUTS: D,SCLK,PD
OUTPUTS: Q
PINORDER: D SCLK PD Q
MINIMUM CELL AREA: 0

Truth Table:

INPUTS			OUTPUTS
D	SCLK	PD	Q
X	0	0	Q
X	1	1	1
0	1	0	0
1	1	0	1

X = Don’t care
When GSR=0, Q=1 (D=SCLK=PD=X)

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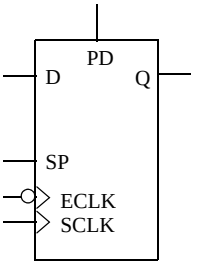
ILF2P3BX

Negative Level Express Clocked (ECLK) Latch, Feeding Positive Edge Triggered System Clocked (SCLK) Flip-Flop, and Positive Level Asynchronous Preset (used in input PIC area only)

ORCA Series		
2	3	4
	✓	✓



ILF2P3BX

INPUTS: D,SP,ECLK,SCLK,PD
OUTPUTS: Q
PINORDER: D SP ECLK SCLK PD Q
MINIMUM CELL AREA: 0

Note: This element must be paired with an input or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

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Truth Table:

INPUTS					OUTPUTS	
D	SP	ECLK	SCLK	PD	LATCH_Q	Q
X	X	X	X	1	LATCH_Q	1
X	0	1	X	0	LATCH_Q	Q
0	X	0	B	0	0	Q
1	X	0	B	0	1	Q
X	1	1	↑	0	0	0
X	1	1	↑	0	1	1
0	1	0	↑	0	0	0
1	1	0	↑	0	1	1

X = Don’t care
LATCH_Q=Output data from latch
B=Not rising edge
When GSR=0, Q=1 (D=SP=ECLK=SCLK=PD=X)

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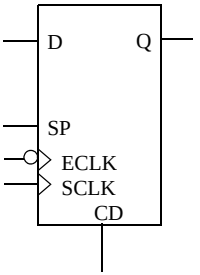
ILF2P3DX

Negative Level Express Clocked (ECLK) Latch, Feeding Positive Edge Triggered System Clocked (SCLK) Flip-Flop, and Positive Level Asynchronous Clear (used in input PIC area only)

ORCA Series		
2	3	4
	✓	✓



ILF2P3DX

INPUTS: D,SP,ECLK,SCLK,CD
OUTPUTS: Q
PINORDER: D SP ECLK SCLK CD Q
MINIMUM CELL AREA: 0

Note: This element must be paired with an input or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

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Truth Table:

INPUTS					OUTPUTS	
D	SP	ECLK	SCLK	CD	LATCH_Q	Q
X	X	X	X	1	LATCH_Q	0
X	0	1	X	0	LATCH_Q	Q
0	X	0	B	0	0	Q
1	X	0	B	0	1	Q
X	1	1	↑	0	0	0
X	1	1	↑	0	1	1
0	1	0	↑	0	0	0
1	1	0	↑	0	1	1

X = Don’t care
LATCH_Q=Output data from latch
B=Not rising edge
When GSR=0, Q=0 (D=SP=ECLK=SCLK=CD=X)

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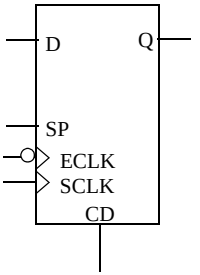
ILF2P3IX

Negative Level Express Clocked (ECLK) Latch, Feeding Positive Edge Triggered System Clocked (SCLK) Flip-Flop, with Positive Level Synchronous Clear and Positive Level Enable (Clear overrides Enable) (used in input PIC area only)

ORCA Series		
2	3	4
	✓	✓



ILF2P3IX

INPUTS: D,SP,ECLK,SCLK,CD
OUTPUTS: Q
PINORDER: D SP ECLK SCLK CD Q
MINIMUM CELL AREA: 0

Note: This element must be paired with an input or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

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Truth Table:

INPUTS					OUTPUTS	
D	SP	ECLK	SCLK	CD	LATCH_Q	Q
X	X	X	↑	1	LATCH_Q	0
X	0	1	X	0	LATCH_Q	Q
0	X	0	B	0	0	Q
1	X	0	B	0	1	Q
X	1	1	↑	0	0	0
X	1	1	↑	0	1	1
0	1	0	↑	0	0	0
1	1	0	↑	0	1	1

X = Don’t care
LATCH_Q=Output data from latch
B=Not rising edge
When GSR=0, Q=0 (D=SP=ECLK=SCLK=CD=X)

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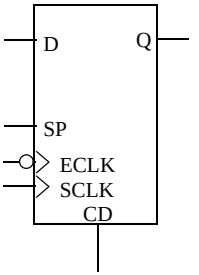
ILF2P3IZ

Negative Level Express Clocked (ECLK) Latch, Feeding Positive Edge Triggered System Clocked (SCLK) Flip-Flop, with Positive Level Synchronous Clear and Positive Level Enable (Enable overrides Clear) (used in input PIC area only)

ORCA Series		
2	3	4
	✓	✓



ILF2P3IZ

INPUTS: D,SP,ECLK,SCLK,CD
OUTPUTS: Q
PINORDER: D SP ECLK SCLK CD Q
MINIMUM CELL AREA: 0

Note: This element must be paired with an input or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

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Truth Table:

INPUTS					OUTPUTS	
D	SP	ECLK	SCLK	CD	LATCH_Q	Q
X	1	X	↑	1	LATCH_Q	0
X	0	1	X	0	LATCH_Q	Q
0	X	0	B	0	0	Q
1	X	0	B	0	1	Q
X	1	1	↑	0	0	0
X	1	1	↑	0	1	1
0	1	0	↑	0	0	0
1	1	0	↑	0	1	1

X = Don’t care
LATCH_Q=Output data from latch
B=Not rising edge
When GSR=0, Q=0 (D=SP=ECLK=SCLK=CD=X)

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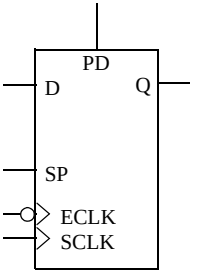
ILF2P3JX

Negative Level Express Clocked (ECLK) Latch, Feeding Positive Edge Triggered System Clocked (SCLK) Flip-Flop, and Positive Level Synchronous Preset (Preset overrides Enable) (used in input PIC area only)

ORCA Series		
2	3	4
	✓	✓



ILF2P3JX

INPUTS: D,SP,ECLK,SCLK,PD
OUTPUTS: Q
PINORDER: D SP ECLK SCLK PD Q
MINIMUM CELL AREA: 0

Note: This element must be paired with an input or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

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Truth Table:

INPUTS					OUTPUTS	
D	SP	ECLK	SCLK	PD	LATCH_Q	Q
X	X	X	↑	1	LATCH_Q	1
X	0	1	X	0	LATCH_Q	Q
0	X	0	B	0	0	Q
1	X	0	B	0	1	Q
X	1	1	↑	0	0	0
X	1	1	↑	0	1	1
0	1	0	↑	0	0	0
1	1	0	↑	0	1	1

X = Don’t care
LATCH_Q=Output data from latch
B=Not rising edge
When GSR=0, Q=1 (D=SP=ECLK=SCLK=PD=X)

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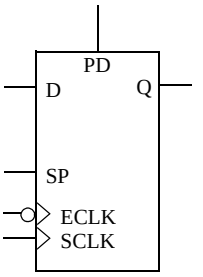
ILF2P3JZ

Negative Level Express Clocked (ECLK) Latch, Feeding Positive Edge Triggered System Clocked (SCLK) Flip-Flop, and Positive Level Synchronous Preset (used in input PIC area only)

ORCA Series		
2	3	4
	✓	✓



ILF2P3JZ

INPUTS: D,SP,ECLK,SCLK,PD
OUTPUTS: Q
PINORDER: D SP ECLK SCLK PD Q
MINIMUM CELL AREA: 0

Note: This element must be paired with an input or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

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Truth Table:

INPUTS					OUTPUTS	
D	SP	ECLK	SCLK	PD	LATCH_Q	Q
X	1	X	↑	1	LATCH_Q	1
X	0	1	X	0	LATCH_Q	Q
0	X	0	B	0	0	Q
1	X	0	B	0	1	Q
X	1	1	↑	0	0	0
X	1	1	↑	0	1	1
0	1	0	↑	0	0	0
1	1	0	↑	0	1	1

X = Don’t care
LATCH_Q=Output data from latch
B=Not rising edge
When GSR=0, Q=1 (D=SP=ECLK=SCLK=PD=X)

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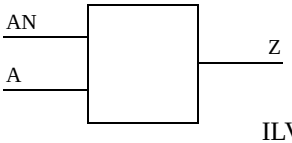
ILVDS

LVDS Input Buffer

ORCA Series			
2	3	4	SC
		✓	✓



ILVDS

INPUTS: A, AN
OUTPUTS: Z
PINORDER: A, AN, Z
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
RESISTOR: OFF (default), ON

Note: If you wish to use the LVPECL or LVDSE buffer, pass the property "LEVELMODE=LVPECL | LVDSE" in both ILVDS and OLVDS elements.

Truth Table:

INPUTS		OUTPUTS
A	AN	Z
0	1	0
1	0	1

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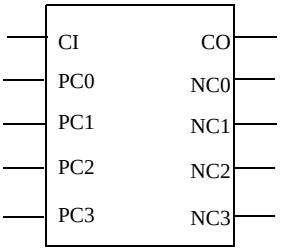
INC4

Combinational Logic for 4 Bit Up-Counter using Look-Up Table

ORCA Series		
2	3	4
	✓	✓



INC4

INPUTS: CI,PC0,PC1,PC2,PC3
OUTPUTS: CO,NC0,NC1,NC2,NC3
PINORDER: CI PC0 PC1 PC2 PC3 CO NC0 NC1 NC2 NC3
MINIMUM CELL AREA: 0.125

Description:

This macro realizes the combinational logic needed to implement a 4 bit up-counter by using ripple elements.

When CI=0, NC[0:3]=PC[0:3] and CO=0
When CI=1, NC[0:3]=PC[0:3]+1, and CO=1 if PC[0:3]=1111

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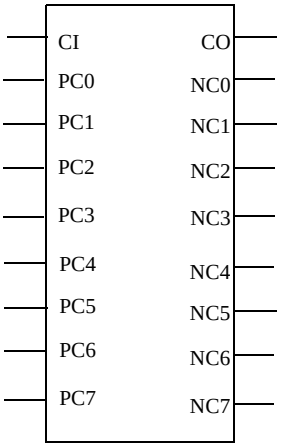
INC8

Combinational Logic for 8 Bit Up-Counter using Look-Up Table

ORCA Series		
2	3	4
	✓	✓



INC8

INPUTS: CI,PC0,PC1,PC2,PC3,PC4,PC5,PC6,PC7
OUTPUTS: CO,NC0,NC1,NC2,NC3,NC4,NC5,NC6,NC7
PINORDER: CI PC0 PC1 PC2 PC3 PC4 PC5 PC6 PC7 CO NC0 NC1 NC2 NC3 NC4 NC5 NC6 NC7
MINIMUM CELL AREA: 0.25

Description:

This macro realizes the combinational logic needed to implement an 8 bit up-counter by using ripple elements.

When CI=1, NC[0:7]=PC[0:7]+1, and CO=1 if PC[0:7]=11111111
When CI=0, NC[0:7]=PC[0:7] and CO=0

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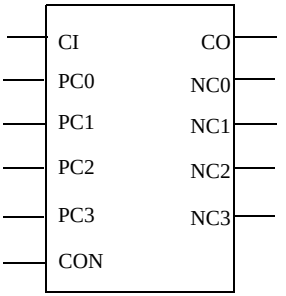
INCDEC4

Combinational Logic for 4 Bit Bidirectional Counter using Look-Up Table

ORCA Series		
2	3	4
	✓	✓



INCDEC4

INPUTS: CI,PC0,PC1,PC2,PC3,CON
OUTPUTS: CO,NC0,NC1,NC2,NC3
PINORDER: CI PC0 PC1 PC2 PC3 CON CO NC0 NC1 NC2 NC3
MINIMUM CELL AREA: 0.125

Description:

This macro realizes the combinational logic needed to implement a 4 bit bidirectional counter by using ripple elements.

When CON=0 and CI=0, NC[0:3]=PC[0:3]-1, and CO=0 if PC[0:3]=0000
When CON=0 and CI=1, NC[0:3]=PC[0:3] and CO=1
When CON=1 and CI=0, NC[0:3]=PC[0:3] and CO=0
When CON=1 and CI=1, NC[0:3]=PC[0:3]+1, and CO=1 if PC[0:3]=1111

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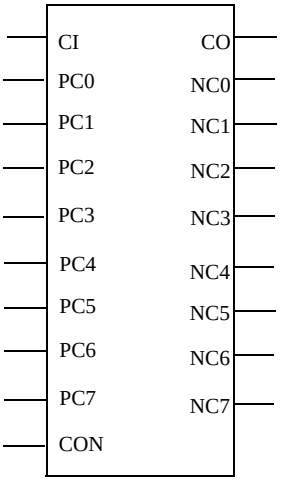
INCDEC8

Combinational Logic for 8 Bit Bidirectional Counter using Look-Up Table

ORCA Series		
2	3	4
	✓	✓



INCDEC8

INPUTS: CI,PC0,PC1,PC2,PC3,PC4,PC5,PC6,PC7,CON
OUTPUTS: CO,NC0,NC1,NC2,NC3,NC4,NC5,NC6,NC7
PINORDER: CI PC0 PC1 PC2 PC3 PC4 PC5 PC6 PC7 CON CO NC0 NC1 NC2 NC3 NC4 NC5 NC6 NC7
MINIMUM CELL AREA: 0.25

Description:

This macro realizes the combinational logic needed to implement an 8 bit bidirectional counter by using ripple elements.

When CON=0 and CI=0, NC[0:7]=PC[0:7]-1, and CO=0 if PC[0:7]=00000000
When CON=0 and CI=1, NC[0:7]=PC[0:7] and CO=1
When CON=1 and CI=0, NC[0:7]=PC[0:7] and CO=0
When CON=1 and CI=1, NC[0:7]=PC[0:7]+1, and CO=1 if PC[0:7]=11111111

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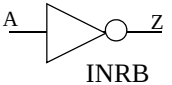
INRB

Inverter (Standard Cell equivalent)

ORCA Series		
2	3	4
✓		



INRB

INPUTS: A
OUTPUTS: Z
PINORDER: A Z
MINIMUM CELL AREA: 0.062

Note: It is possible that this element will be optimized away.

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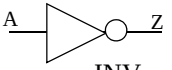
INV

Inverter

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



INV

INPUTS: A
OUTPUTS: Z
PINORDER: A Z
MINIMUM CELL AREA (2A/2T): 0.062
MINIMUM CELL AREA (Series 3): 0.001

Note: It is possible that this element will be optimized away.

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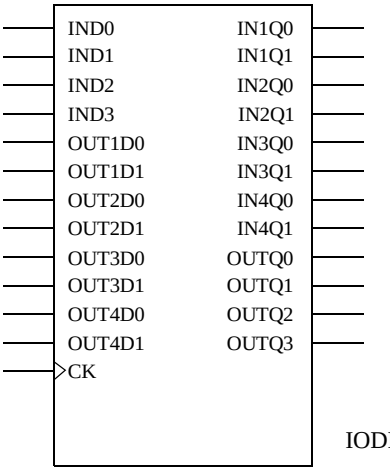
IODDR

Input/Output DDR

ORCA Series		
2	3	4
		✓



INPUTS: IND0, IND1, IND2, IND3, OUT1D0, OUT1D1, OUT2D0, OUT2D1, OUT3D0, OUT3D1, OUT4D0, OUT4D1, CK
OUTPUTS: IN1Q0, IN1Q1, IN2Q0, IN2Q1, IN3Q0 IN3Q1, IN4Q0, IN4Q1, OUTQ0, OUTQ1, OUTQ2, OUTQ3
PINORDER: IND0 IND1 IND2 IND3 OUT1D0 OUT1D1 OUT2D0 OUT2D1 OUT3D0 OUT3D1 OUT4D0 OUT4D1 CK IN1Q0 IN1Q1 IN2Q0 IN2Q1 IN3Q0 IN3Q1 IN4Q0 IN4Q1 OUTQ0 OUTQ1 OUTQ2 OUTQ3
MINIMUM CELL AREA: 0
INPUT DDR MODE: IN (D0, D1, D2, D0) CK
IN1, IN2, IN3, IN4 (Q0, Q)
OUTPUT DDR MODE: OUT1, OUT2, OUT3, OUT4 (D0, D1), CK
OUT (Q0, Q1, Q2, Q3)

Description:

Note that each IODDR is only available to four PIOs. IND0 to IND3 come from the PADs and OUTQ0 to OUTQ3 go to the PADs, so at any given time the input and output with the same index cannot be connected to the same PAD. For example, IND0 and OUTQ0 cannot be used at the same time. Any combination of corresponding input and output mode pins in this element is allowable with respect to the PAD limitation. See diagrams and table on following pages.

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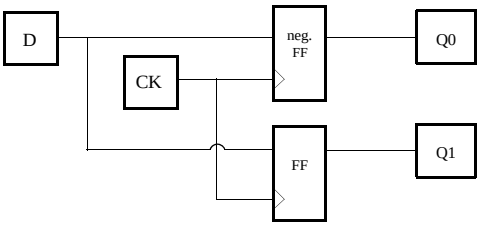
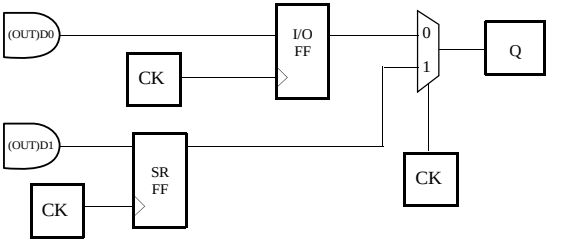
The diagram below illustrates the connectivity and functionality of the IODDR in DDR input mode:

INDDR



The diagram below illustrates the connectivity and functionality of the IODDR in DDR output mode:

OUTDDR



To further illustrate the pin functionality and connectivity of the IODDR, the table below shows the functionality of pin combinations when the inputs are connected to their possible outputs to the right.

Input Pin(s)	Functionality	Output Pin(s)
INPUT DDR MODE		
IND0	Flip-flop output (negative edge-triggered)	IN1Q0
	Flip-flop output (positive edge-triggered)	IN1Q1

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Input Pin(s)	Functionality	Output Pin(s)
IND1	Flip-flop output (negative edge-triggered)	IN2Q0
	Flip-flop output (positive edge-triggered)	IN2Q1
IND2	Flip-flop output (negative edge-triggered)	IN3Q0
	Flip-flop output (positive edge-triggered)	IN3Q1
IND3	Flip-flop output (negative edge-triggered)	IN4Q0
	Flip-flop output (positive edge-triggered)	IN4Q1
OUTPUT DDR MODE		
OUT1D0	I/O Flip-flop input (positive edge-triggered)	OUTQ0
OUT1D1	SR Flip-flop input (positive edge-triggered)	
OUT2D0	I/O Flip-flop input (positive edge-triggered)	OUTQ1
OUT2D1	SR Flip-flop input (positive edge-triggered)	
OUT3D0	I/O Flip-flop input (positive edge-triggered)	OUTQ2
OUT3D1	SR Flip-flop input (positive edge-triggered)	
OUT4D0	I/O Flip-flop input (positive edge-triggered)	OUTQ3
OUT4D1	SR Flip-flop input (positive edge-triggered)	

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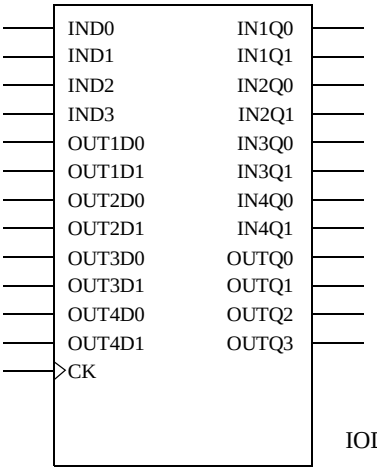
IODDRN

Input/Output DDR

ORCA Series		
2	3	4
		✓



IODDRN

INPUTS: IND0, IND1, IND2, IND3, OUT1D0, OUT1D1, OUT2D0, OUT2D1, OUT3D0, OUT3D1, OUT4D0, OUT4D1, CK
OUTPUTS: IN1Q0, IN1Q1, IN2Q0, IN2Q1, IN3Q0 IN3Q1, IN4Q0, IN4Q1, OUTQ0, OUTQ1, OUTQ2, OUTQ3
PINORDER: IND0 IND1 IND2 IND3 OUT1D0 OUT1D1 OUT2D0 OUT2D1 OUT3D0 OUT3D1 OUT4D0 OUT4D1 CK IN1Q0 IN1Q1 IN2Q0 IN2Q1 IN3Q0 IN3Q1 IN4Q0 IN4Q1 OUTQ0 OUTQ1 OUTQ2 OUTQ3
MINIMUM CELL AREA: 0
INPUT DDR MODE: IN (D0, D1, D2, D0) CK
IN1, IN2, IN3, IN4 (Q0, Q)
OUTPUT DDR MODE: OUT1, OUT2, OUT3, OUT4 (D0, D1), CK
OUT (Q0, Q1, Q2, Q3)

Description:

Note that each IODDRN is only available to four PIOs. IND0 to IND3 come from the PADs and OUTQ0 to OUTQ3 go to the PADs, so at any given time the input and output with the same index cannot be connected to the same PAD. For example, IND0 and OUTQ0 cannot be used at the same time. Any combination of corresponding input and output mode pins in this element is allowable with respect to the PAD limitation. See diagrams and table on following pages.

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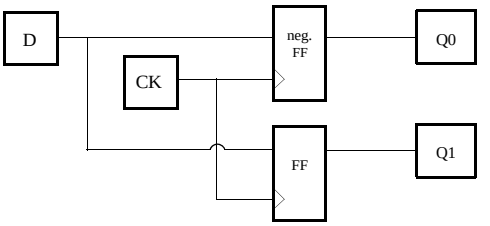
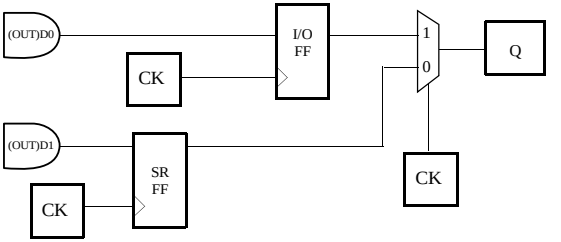
The diagram below illustrates the connectivity and functionality of the IODDRN in DDR input mode:

INDDR



The diagram below illustrates the connectivity and functionality of the IODDRN in DDR output mode:

OUTDDR



To further illustrate the pin functionality and connectivity of the IODDRN, the table below shows the functionality of pin combinations when the inputs are connected to their possible outputs to the right.

Input Pin(s)	Functionality	Output Pin(s)
INPUT DDR MODE		
IND0	Flip-flop output (negative edge-triggered)	IN1Q0
	Flip-flop output (positive edge-triggered)	IN1Q1

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Input Pin(s)	Functionality	Output Pin(s)
IND1	Flip-flop output (negative edge-triggered)	IN2Q0
	Flip-flop output (positive edge-triggered)	IN2Q1
IND2	Flip-flop output (negative edge-triggered)	IN3Q0
	Flip-flop output (positive edge-triggered)	IN3Q1
IND3	Flip-flop output (negative edge-triggered)	IN4Q0
	Flip-flop output (positive edge-triggered)	IN4Q1
OUTPUT DDR MODE		
OUT1D0	I/O Flip-flop input (negative edge-triggered)	OUTQ0
OUT1D1	SR Flip-flop input (positive edge-triggered)	
OUT2D0	I/O Flip-flop input (negative edge-triggered)	OUTQ1
OUT2D1	SR Flip-flop input (positive edge-triggered)	
OUT3D0	I/O Flip-flop input (negative edge-triggered)	OUTQ2
OUT3D1	SR Flip-flop input (positive edge-triggered)	
OUT4D0	I/O Flip-flop input (negative edge-triggered)	OUTQ3
OUT4D1	SR Flip-flop input (positive edge-triggered)	

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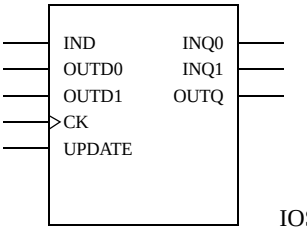
IOSR2

Input/Output 2-Bit Shift Register

ORCA Series		
2	3	4
		✓



IOSR2

INPUTS: IND, OUTD0, OUTD1, CK, UPDATE
OUTPUTS: INQ0, INQ1, OUTQ
PINORDER: IND, OUTD0, OUTD1, CK, UPDATE, INQ0, INQ1, OUTQ
MINIMUM CELL AREA: 0

Description:

For input shift registers, IND is the input and INQ0 and INQ1 are the two outputs. For output shift registers OUTD0, OUTD1 are the two inputs and OUTQ is the output.

Refer to the IOSR4 element for a better understanding of output and input modes for the IOSR2 element. Shift register timing is also comparable in the IOSR4 and you should refer to the IOSR4 *OUTPUT Shift Register Timing Diagram* and *INPUT Shift Register Timing Diagram* for more information.

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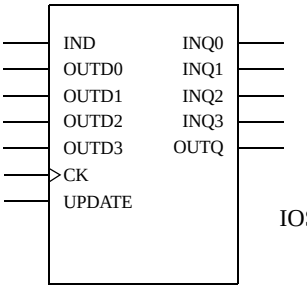
IOSR4

Input/Output 4-Bit Shift Register

ORCA Series		
2	3	4
		✓



IOSR4

INPUTS: IND, OUTD0, OUTD1, OUTD2, OUTD3, CK, UPDATE
OUTPUTS: INQ0, INQ1, INQ2, INQ3, OUTQ
PINORDER: IND, OUTD0, OUTD1, OUTD2, OUTD3, CK, UPDATE, INQ0, INQ1, INQ2, INQ3, OUTQ
MINIMUM CELL AREA: 0

Description:

For input shift registers, IND is the input and INQ0, INQ1, INQ2, and INQ3 are the four outputs. For output shift registers OUTD0, OUTD1, OUTD2, and OUTD3 are the four inputs and OUTQ is the output.

Shift Register Timing

The waveform diagrams on the following page illustrate output and input shift register timing in the IOSR4 element. Please refer to these waveforms for the IOSR2 element as well.

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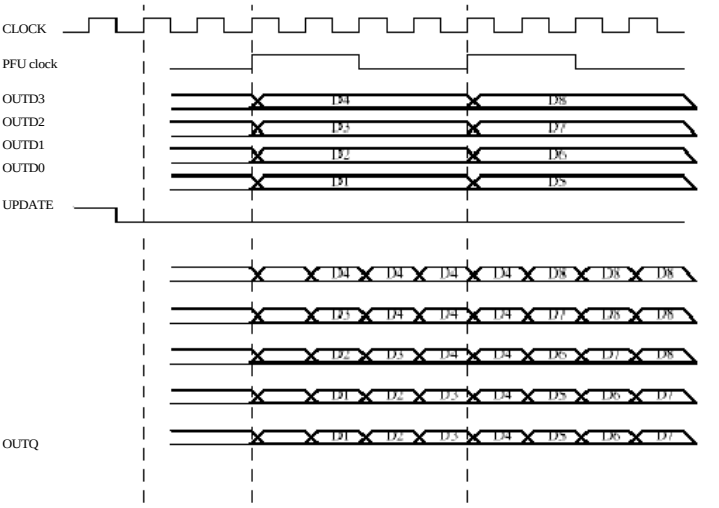
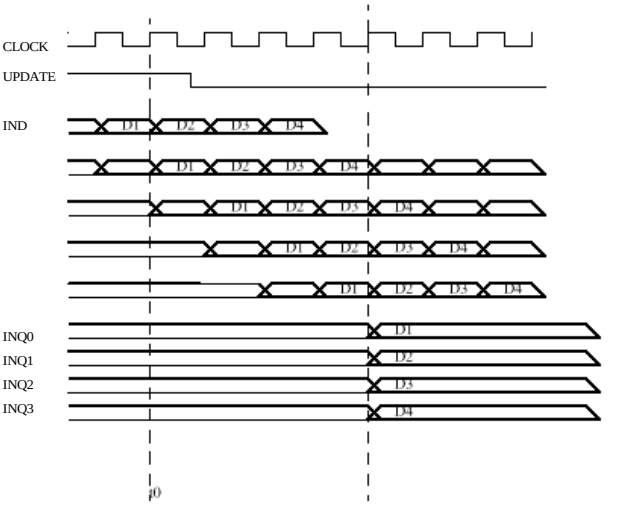
OUTPUT Shift Register Timing Diagram



INPUT Shift Register Timing Diagram



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IPAD

Input PAD

ORCA Series		
2	3	4
✓		

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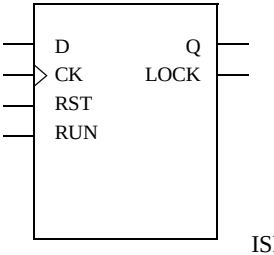
ISRX1A

Input 1-Bit Shift Register

Lattice FPGA		
SC	XP	EC
✓		



ISRX1A

INPUTS: D, CK, RST, RUN
OUTPUTS: Q, LOCK
PINORDER: D, CK, RST, RUN, Q, LOCK
MINIMUM CELL AREA: 0
ATTRIBUTES (LatticeSC)
CLKMODE: SCLK, ECLK
AIL : OFF, ON (Adaptive input logic mode)
STEP : ONE, TWO, THREE, FOUR (Valid only when AIL = ON)
SWAP : OFF, ON (Valid only when AIL = ON)
BESTFIT : OFF, ON (Valid only when AIL = ON)
CLKEDGE : ONE, TWO (Valid only when AIL = ON)
DISABLED_GSR: 0, 1 (Valid only when AIL = ON and affects only to cntl)

Description:

Shift register input logic that uses adaptive FF to capture input data.

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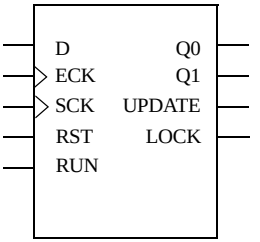
ISRX2A

Input 2-Bit Shift Register

Lattice FPGA		
SC	XP	EC
✓		



ISRX2A

INPUTS: D, ECK, SCK, RST, RUN
OUTPUTS: Q0, Q1, UPDATE, LOCK
PINORDER: D, ECK, SCK, RST, RUN, Q0, Q1, UPDATE, LOCK
MINIMUM CELL AREA: 0
ATTRIBUTES (LatticeSC)
LSRMODE: EDGE, LOCAL
UPDT: POS, NEG
AIL: OFF, ON (Adaptive input logic mode)
STEP: ONE, TWO, THREE, FOUR (Valid only when AIL = ON)
SWAP: OFF, ON (Valid only when AIL = ON)
BESTFIT: OFF, ON
CLKEDGE: ONE, TWO (Valid only when AIL = ON)
DISABLED_GSR: 0, 1 (Valid only when AIL = ON and affects only to cntl)

Description:

Shift register input logic that allows clock domain transfer from edge clock to primary clock and parallel transfer to the core of incoming serial data.

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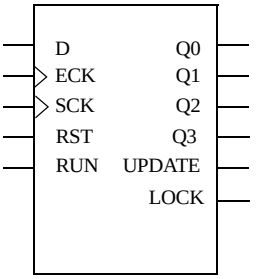
ISRX4A

Input 4-Bit Shift Register

Lattice FPGA		
SC	XP	EC
✓		



ISRX4A

INPUTS: D, ECK, SCK, RST, RUN
OUTPUTS: Q0, Q1, Q2, Q3, UPDATE, LOCK
PINORDER: D, ECK, SCK, RST, RUN, Q0, Q1, Q2, Q3, UPDATE, LOCK
MINIMUM CELL AREA: 0
ATTRIBUTES
ATTRIBUTES (LatticeSC)
LSRMODE: EDGE, LOCAL
UPDT: POS, NEG
AIL: OFF, ON (Adaptive input logic mode)
STEP: ONE, TWO, THREE, FOUR (Valid only when AIL = ON)
SWAP: OFF, ON (Valid only when AIL = ON)
BESTFIT: OFF, ON
CLKEDGE: ONE, TWO (Valid only when AIL = ON)
DISABLED_GSR: 0, 1 (Valid only when AIL = ON and affects only to cntl)

Description:

Shift register input logic that allows clock domain transfer from edge clock to primary clock and parallel transfer to the core of incoming serial data.

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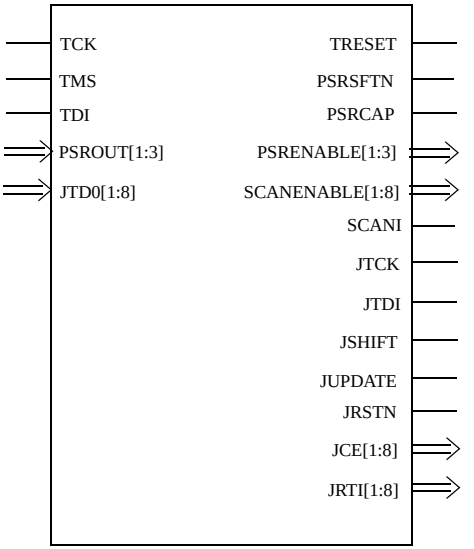
JTAGA

JTAG — Logic Control Circuit

Lattice FPGA		
SC	XP	EC
✓		



JTAGA

NOTE: The graphic is shown in bus notation for convenience. This element must be instantiated in expanded bus notation format with each individual bit as given below.

INPUTS: TCK, TMS, TDI, PSROUT1, PSROUT2, PSROUT3, JTDO1, JTDO2, JTDO3, JTDO4, JTDO5, JTDO6, JTDO7, JTDO8
OUTPUTS: TRESET, PSRSFTN, PSRCAP, PSRENABLE1, PSRENABLE2, PSRENABLE3, SCANENABLE1, SCANENABLE2, SCANENABLE3, SCANENABLE4, SCANENABLE5, SCANENABLE6, SCANENABLE7, SCANENABLE8, SCANI, JTCK, JTDI, JSHIFT, JUPDATE, JRSTN, JCE1, JCE2, JCE3, JCE4, JCE5, JCE6, JCE7, JCE8, JRTI1, JRTI2, JRTI3, JRTI4, JRTI5, JRTI6, JRTI7, JRTI8
PINORDER: TCK, TMS, TDI, PSROUT1, PSROUT2, PSROUT3, JTDO1, JTDO2, JTDO3, JTDO4, JTDO5, JTDO6, JTDO7, JTDO8, TRESET, PSRSFTN, PSRCAP, PSRENABLE1, PSRENABLE2, PSRENABLE3, SCANENABLE1, SCANENABLE2, SCANENABLE3, SCANENABLE4, SCANENABLE5, SCANENABLE6, SCANENABLE7, SCANENABLE8, SCANI, JTCK, JTDI, JSHIFT, JUPDATE, JRSTN, JCE1, JCE2, JCE3, JCE4, JCE5, JCE6, JCE7, JCE8, JRTI1, JRTI2, JRTI3, JRTI4, JRTI5, JRTI6, JRTI7, JRTI8
MINIMUM CELL AREA (All Series): 0

continued

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Description:

The JTAGA macro provides the control and interconnect circuit used by the boundary scan function. This function allows the testing of increasingly complex ICs and IC packages. The LatticeSC device has enhanced its interface capability to the PLC array with increased scan chain connectivity and tap state machine flags such as shift capture update, reset, run test idle.

Example pin functions:

Function	Pins	Description
interface pins	TCK, TMS, and TDI	Test clock (TCK), Test mode select (TMS), and Test data in (TDI) are three interface pins for this element.
user boundary scan-ring outputs	PSROUT[1:3] JTDO[1:8]	These are the outputs of the last registers of the user scan rings to the boundary scan block. Inputs to the boundary scan macro are based on the instruction loaded.
reset	TRESET	Active high output of the boundary scan macro to the routing. The output is high when the boundary scan macro is in test logic reset state.
shift_not data register	PSRSFTN	Active low output of the boundary scan macro. The output is low when the boundary scan macro is in the shift data state and the programmable scan ring instructions are loaded.
capture data register	PSRCAP	Active high output of the boundary scan macro. The output is high when the boundary scan macro is in the capture data state and the programmable scan ring instructions are loaded.
enable flag	PSRENABLE[1:3] SCANENABLE[1:8]	Active high outputs of the boundary scan macro to the routing. The output equals a high upon update of the specific instructions, PLC_SCAN_RING[1:3] and SCAN[1:8], respectively.

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scan in	SCANI	Private pin used for testing of the system bus that multiplexes the TDI and SCANOUT[11:14].
test clock	JTCK	The boundary scan clock which is output from the boundary scan macro to the scan rings.
test data in	JTDI	The output of the boundary scan macro from where the test data is output to the scan rings.
shift data register	JSHIFT	Active high output of the boundary scan macro. The output is high when the boundary scan macro is in the shift data state and the scan instructions are loaded.
update data register	JUPDATE	Active high output of the boundary scan macro. The output is high when the boundary scan macro is in the update data state and when the PLC_SCAN_RING or SCAN instructions are loaded.
reset_not	JRSTN	Active low output of the boundary scan macro to the routing. The output is low when the boundary scan macro is in test logic reset state.
clock enable	JCE[1:8]	Active high output of the boundary scan macro to the routing. The output is high when the boundary scan macro is in the SHIFT or CAPTURE state during the SCAN[1:8] instructions, respectively.
run test idle	JRTI[1:8]	Active high output of the boundary scan macro. The output is high when the boundary scan macro is in the run test idle state and during the SCAN[1:8] instructions.

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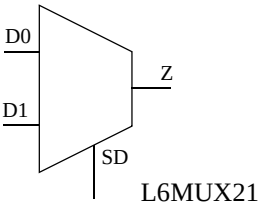
L6MUX21

2 to 1 Mux

Lattice FPGA		
SC	XP	EC
✓	✓	✓



INPUTS: D0, D1, SD
OUTPUTS: Z
PINORDER: D0, D1, SD, Z

Truth Table:

INPUTS			OUTPUTS
D0	D1	SD	Z
0	X	0	0
1	X	0	1
X	0	1	0
X	1	1	1

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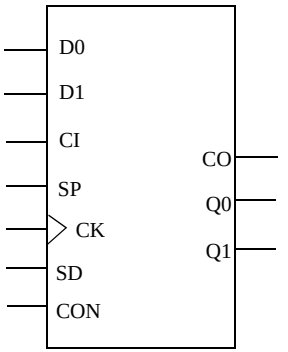
LB2P3AX

2 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable, GSR Used for Clear

Lattice FPGA		
SC	XP	EC
✓		



LB2P3AX

INPUTS: D0, D1, CI, SP, CK, SD, CON
OUTPUTS: CO, Q0, Q1
PINORDER: D0, D1, CI, SP, CK, SD, CON, CO, Q0, Q
MINIMUM CELL AREA: One Slice

Note: When CON = 0, CI and CO are active LOW

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Truth Table:

INPUTS						OUTPUTS	
D[0:1]	SD	CI	SP	CK	CON	CO	Q[0:1]
D[0:1]	1	0	1	↑	1	0	D[0:1]
D[0:1]	1	1	1	↑	1	*	D[0:1]
X	0	0	X	X	1	0	Q[0:1]
X	X	0	0	X	1	0	Q[0:1]
X	X	1	0	X	1	*	Q[0:1]
X	0	1	1	↑	1	*	count+1
D[0:1]	1	1	1	↑	0	1	D[0:1]
D[0:1]	1	0	1	↑	0	**	D[0:1]
X	0	1	X	X	0	1	Q[0:1]
X	X	1	0	X	0	1	Q[0:1]
X	X	0	0	X	0	**	Q[0:1]
X	0	0	1	↑	0	**	count-1

X = Don’t care
* When Q[0:1] is 11, CO will be 1; otherwise, CO will be 0
** When Q[0:1] is 00, CO will be 0; otherwise, CO will be 1
When GSR=0, CO=!CON•CI, Q[0:1]=0 (D[0:1]=SP=CK=SD=X)

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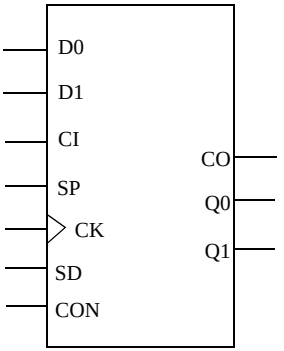
LB2P3AY

2 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable, GSR Used for Preset

Lattice FPGA		
SC	XP	EC
✓		



LB2P3AY

INPUTS: D0, D1, CI, SP, CK, SD, CON
OUTPUTS: CO, Q0, Q1
PINORDER: D0, D1, CI, SP, CK, SD, CON, CO, Q0, Q1
MINIMUM CELL AREA: One Slice

Note: When CON = 0, CI and CO are active LOW

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Truth Table:

INPUTS						OUTPUTS	
D[0:1]	SD	CI	SP	CK	CON	CO	Q[0:1]
D[0:1]	1	0	1	↑	1	0	D[0:1]
D[0:1]	1	1	1	↑	1	*	D[0:1]
X	0	0	X	X	1	0	Q[0:1]
X	X	0	0	X	1	0	Q[0:1]
X	X	1	0	X	1	*	Q[0:1]
X	0	1	1	↑	1	*	count+1
D[0:1]	1	1	1	↑	0	1	D[0:1]
D[0:1]	1	0	1	↑	0	**	D[0:1]
X	0	1	X	X	0	1	Q[0:1]
X	X	1	0	X	0	1	Q[0:1]
X	X	0	0	X	0	**	Q[0:1]
X	0	0	1	↑	0	**	count-1

X = Don’t care
* When Q[0:1] is 11, CO will be 1; otherwise, CO will be 0
** When Q[0:1] is 00, CO will be 0; otherwise, CO will be 1
When GSR=0, Q[0:1]=1, CO=!CON+CI (D[0:1]=SP=CK=SD=X)

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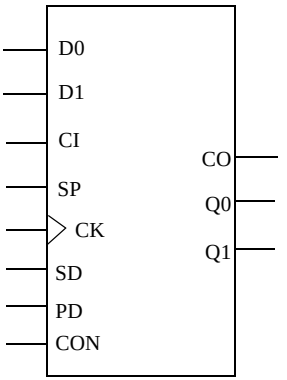
LB2P3BX

2 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable and Positive Level Asynchronous Preset

Lattice FPGA		
SC	XP	EC
✓		



LB2P3BX

INPUTS: D0, D1, CI, SP, CK, SD, PD, CON
OUTPUTS: CO, Q0, Q1
PINORDER: D0, D1, CI, SP, CK, SD, PD, CON, CO, Q0, Q1
MINIMUM CELL AREA: One Slice

Note: When CON = 0, CI and CO are active LOW

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Truth Table:

INPUTS							OUTPUTS	
D[0:1]	SD	CI	SP	CK	CON	PD	CO	Q[0:1]
X	X	0	X	X	1	1	0	1
X	X	1	X	X	1	1	1	1
D[0:1]	1	0	1	↑	1	0	0	D[0:1]
D[0:1]	1	1	1	↑	1	0	*	D[0:1]
X	0	0	X	X	1	0	0	Q[0:1]
X	X	0	0	X	1	0	0	Q[0:1]
X	X	1	0	X	1	0	*	Q[0:1]
X	0	1	1	↑	1	0	*	count+1
X	X	X	X	X	0	1	1	1
D[0:1]	1	1	1	↑	0	0	1	D[0:1]
D[0:1]	1	0	1	↑	0	0	**	D[0:1]
X	0	1	X	X	0	0	1	Q[0:1]
X	X	1	0	X	0	0	1	Q[0:1]
X	X	0	0	X	0	0	**	Q[0:1]
X	0	0	1	↑	0	0	**	count-1

X = Don’t care
* When Q[0:1] is 11, CO will be 1; otherwise, CO will be 0
** When Q[0:1] is 00, CO will be 0; otherwise, CO will be 1
When GSR=0, CO=!CON+CI, Q[0:1]=1 (D[0:1]=SP=CK=SD=PD=X)

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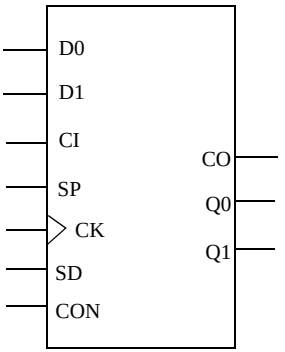
LB2P3DX

2 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable and Positive Level Asynchronous Clear

Lattice FPGA		
SC	XP	EC
✓		



LB2P3DX

INPUTS: D0, D1, CI, SP, CK, SD, CD, CON
OUTPUTS: CO, Q0, Q1
PINORDER: D0, D1, CI, SP, CK, SD, CD, CON, CO, Q0, Q1
MINIMUM CELL AREA: One Slice

Note: When CON = 0, CI and CO are active LOW

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Truth Table:

INPUTS							OUTPUTS	
D[0:1]	SD	CI	SP	CK	CON	CD	CO	Q[0:1]
X	X	X	X	X	1	1	0	0
D[0:1]	1	0	1	↑	1	0	0	D[0:1]
D[0:1]	1	1	1	↑	1	0	*	D[0:1]
X	0	0	X	X	1	0	0	Q[0:1]
X	X	0	0	X	1	0	0	Q[0:1]
X	X	1	0	X	1	0	*	Q[0:1]
X	0	1	1	↑	1	0	*	count+1
X	X	0	X	X	0	1	0	0
X	X	1	X	X	0	1	1	0
D[0:1]	1	1	1	↑	0	0	1	D[0:1]
D[0:1]	1	0	1	↑	0	0	**	D[0:1]
X	0	1	X	X	0	0	1	Q[0:1]
X	X	1	0	X	0	0	1	Q[0:1]
X	X	0	0	X	0	0	**	Q[0:1]
X	0	0	1	↑	0	0	**	count-1

X = Don’t care
* When Q[0:1] is 11, CO will be 1; otherwise, CO will be 0
** When Q[0:1] is 00, CO will be 0; otherwise, CO will be 1
When GSR=0, CO=!CON•CI, Q[0:1]=0 (D[0:1]=SP=CK=SD=CD=X)

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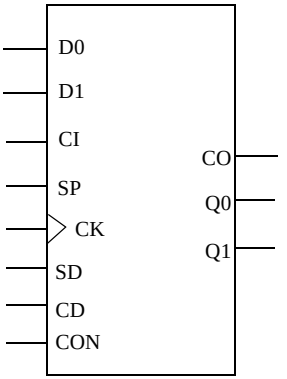
LB2P3IX

2 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable and Positive Level Synchronous Clear (Clear overrides Enable

Lattice FPGA		
SC	XP	EC
✓		



LB2P3IX

INPUTS: D0, D1, CI, SP, CK, SD, CD, CON
OUTPUTS: CO, Q0, Q1
PINORDER: D0, D1, CI, SP, CK, SD, CD, CON, CO, Q0, Q1
MINIMUM CELL AREA: One Slice

Note: When CON = 0, CI and CO are active LOW

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Truth Table:

INPUTS							OUTPUTS	
D[0:1]	SD	CI	SP	CK	CON	CD	CO	Q[0:1]
X	X	X	X	↑	1	1	0	0
D[0:1]	1	0	1	↑	1	0	0	D[0:1]
D[0:1]	1	1	1	↑	1	0	*	D[0:1]
X	0	0	X	X	1	0	0	Q[0:1]
X	X	0	0	X	1	0	0	Q[0:1]
X	X	1	0	X	1	0	*	Q[0:1]
X	0	1	1	↑	1	0	*	count+1
X	X	0	X	↑	0	1	0	0
X	X	1	X	↑	0	1	1	0
D[0:1]	1	1	1	↑	0	0	1	D[0:1]
D[0:1]	1	0	1	↑	0	0	**	D[0:1]
X	0	1	X	X	0	0	1	Q[0:1]
X	X	1	0	X	0	0	1	Q[0:1]
X	X	0	0	X	0	0	**	Q[0:1]
X	0	0	1	↑	0	0	**	count-1

X = Don’t care
* When Q[0:1] is 11, CO will be 1; otherwise, CO will be 0
** When Q[0:1] is 00, CO will be 0; otherwise, CO will be 1
When GSR=0, CO=!CON•CI, Q[0:1]=0 (D[0:1]=SP=CK=SD=CD=X)

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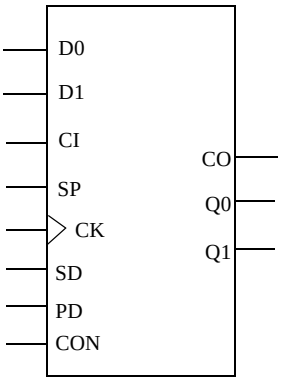
LB2P3JX

2 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable and Positive Level Synchronous Preset (Preset overrides Enable

Lattice FPGA		
SC	XP	EC
✓		



LB2P3JX

INPUTS: D0, D1, CI, SP, CK, SD, PD, CON
OUTPUTS: CO, Q0, Q1
PINORDER: D0, D1, CI, SP, CK, SD, PD, CON, CO, Q0, Q1
MINIMUM CELL AREA: One Slice

Note: When CON = 0, CI and CO are active LOW

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Truth Table:

INPUTS							OUTPUTS	
D[0:1]	SD	CI	SP	CK	CON	PD	CO	Q[0:1]
X	X	0	X	↑	1	1	0	1
X	X	1	X	↑	1	1	1	1
D[0:1]	1	0	1	↑	1	0	0	D[0:1]
D[0:1]	1	1	1	↑	1	0	*	D[0:1]
X	0	0	X	X	1	0	0	Q[0:1]
X	X	0	0	X	1	0	0	Q[0:1]
X	X	1	0	X	1	0	*	Q[0:1]
X	0	1	1	↑	1	0	*	count+1
X	X	X	X	↑	0	1	1	1
D[0:1]	1	1	1	↑	0	0	1	D[0:1]
D[0:1]	1	0	1	↑	0	0	**	D[0:1]
X	0	1	X	X	0	0	1	Q[0:1]
X	X	1	0	X	0	0	1	Q[0:1]
X	X	0	0	X	0	0	**	Q[0:1]
X	0	0	1	↑	0	0	**	count-1

X = Don’t care
* When Q[0:1] is 11, CO will be 1; otherwise, CO will be 0
** When Q[0:1] is 00, CO will be 0; otherwise, CO will be 1
When GSR=0, CO=!CON+CI, Q[0:1]=1 (D[0:1]=SP=CK=SD=PD=X)

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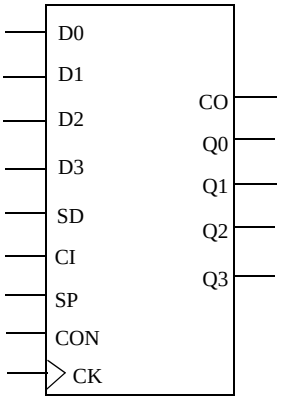
LB4P3AX

4 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable, GSR Used for Clear

ORCA Series		
2	3	4
✓	✓	✓



LB4P3AX

INPUTS: D0,D1,D2,D3,CI,SP,CK,SD,CON
OUTPUTS: CO,Q0,Q1,Q2,Q3
PINORDER: D0 D1 D2 D3 CI SP CK SD CON CO Q0 Q1 Q2 Q3
MINIMUM CELL AREA (2A/2T): 1.0
MINIMUM CELL AREA (Series 3): 0.25

Note: When CON = 0, CI and CO are active LOW

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Truth Table:

INPUTS						OUTPUTS	
D[0:3]	SD	CI	SP	CK	CON	CO	Q[0:3]
D[0:3]	1	0	1	↑	1	0	D[0:3]
D[0:3]	1	1	1	↑	1	*	D[0:3]
X	0	0	X	X	1	0	Q[0:3]
X	X	0	0	X	1	0	Q[0:3]
X	X	1	0	X	1	*	Q[0:3]
X	0	1	1	↑	1	*	count+1
D[0:3]	1	1	1	↑	0	1	D[0:3]
D[0:3]	1	0	1	↑	0	**	D[0:3]
X	0	1	X	X	0	1	Q[0:3]
X	X	1	0	X	0	1	Q[0:3]
X	X	0	0	X	0	**	Q[0:3]
X	0	0	1	↑	0	**	count-1

X = Don’t care
* When Q[0:3] is 1111, CO will be 1; otherwise, CO will be 0
** When Q[0:3] is 0000, CO will be 0; otherwise, CO will be 1
When GSR=0, CO=!CON•CI, Q[0:3]=0 (D[0:3]=SP=CK=SD=X)

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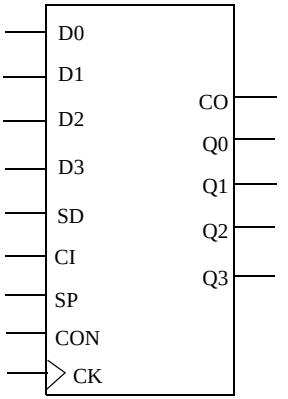
LB4P3AY

4 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable, GSR Used for Preset

ORCA Series		
2	3	4
✓	✓	✓



LB4P3AY

INPUTS: D0,D1,D2,D3,CI,SP,CK,SD,CON
OUTPUTS: CO,Q0,Q1,Q2,Q3
PINORDER: D0 D1 D2 D3 CI SP CK SD CON CO Q0 Q1 Q2 Q3
MINIMUM CELL AREA (2A/2T): 1.0
MINIMUM CELL AREA (Series 3): 0.25

Note: When CON = 0, CI and CO are active LOW

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Truth Table:

INPUTS						OUTPUTS	
D[0:3]	SD	CI	SP	CK	CON	CO	Q[0:3]
D[0:3]	1	0	1	↑	1	0	D[0:3]
D[0:3]	1	1	1	↑	1	*	D[0:3]
X	0	0	X	X	1	0	Q[0:3]
X	X	0	0	X	1	0	Q[0:3]
X	X	1	0	X	1	*	Q[0:3]
X	0	1	1	↑	1	*	count+1
D[0:3]	1	1	1	↑	0	1	D[0:3]
D[0:3]	1	0	1	↑	0	**	D[0:3]
X	0	1	X	X	0	1	Q[0:3]
X	X	1	0	X	0	1	Q[0:3]
X	X	0	0	X	0	**	Q[0:3]
X	0	0	1	↑	0	**	count-1

X = Don’t care
* When Q[0:3] is 1111, CO will be 1; otherwise, CO will be 0
** When Q[0:3] is 0000, CO will be 0; otherwise, CO will be 1
When GSR=0, Q[0:3]=1, CO=!CON+CI (D[0:3]=SP=CK=SD=X)

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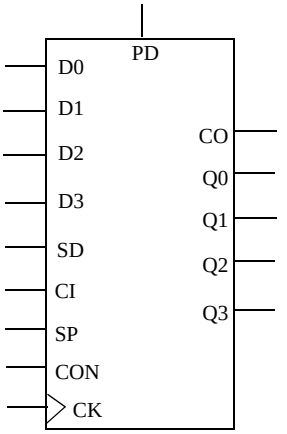
LB4P3BX

4 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable and Positive Level Asynchronous Preset

ORCA Series		
2	3	4
	✓	✓



LB4P3BX

INPUTS: D0,D1,D2,D3,CI,SP,CK,SD,PD,CON
OUTPUTS: CO,Q0,Q1,Q2,Q3
PINORDER: D0 D1 D2 D3 CI SP CK SD PD CON CO Q0 Q1 Q2 Q3
MINIMUM CELL AREA: 0.25

Note: When CON = 0, CI and CO are active LOW

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Truth Table:

INPUTS							OUTPUTS	
D[0:3]	SD	CI	SP	CK	CON	PD	CO	Q[0:3]
X	X	0	X	X	1	1	0	1
X	X	1	X	X	1	1	1	1
D[0:3]	1	0	1	↑	1	0	0	D[0:3]
D[0:3]	1	1	1	↑	1	0	*	D[0:3]
X	0	0	X	X	1	0	0	Q[0:3]
X	X	0	0	X	1	0	0	Q[0:3]
X	X	1	0	X	1	0	*	Q[0:3]
X	0	1	1	↑	1	0	*	count+1
X	X	X	X	X	0	1	1	1
D[0:3]	1	1	1	↑	0	0	1	D[0:3]
D[0:3]	1	0	1	↑	0	0	**	D[0:3]
X	0	1	X	X	0	0	1	Q[0:3]
X	X	1	0	X	0	0	1	Q[0:3]
X	X	0	0	X	0	0	**	Q[0:3]
X	0	0	1	↑	0	0	**	count-1

X = Don’t care
* When Q[0:3] is 1111, CO will be 1; otherwise, CO will be 0
** When Q[0:3] is 0000, CO will be 0; otherwise, CO will be 1
When GSR=0, CO=!CON+CI, Q[0:3]=1 (D[0:3]=SP=CK=SD=PD=X)

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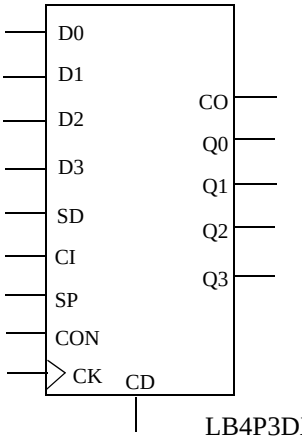
LB4P3DX

4 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable and Positive Level Asynchronous Clear

ORCA Series		
2	3	4
	✓	✓



INPUTS: D0,D1,D2,D3,CI,SP,CK,SD,CD,CON
OUTPUTS: CO,Q0,Q1,Q2,Q3
PINORDER: D0 D1 D2 D3 CI SP CK SD CD CON CO Q0 Q1 Q2 Q3
MINIMUM CELL AREA: 0.25

Note: When CON = 0, CI and CO are active LOW

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Truth Table:

INPUTS							OUTPUTS	
D[0:3]	SD	CI	SP	CK	CON	CD	CO	Q[0:3]
X	X	X	X	X	1	1	0	0
D[0:3]	1	0	1	↑	1	0	0	D[0:3]
D[0:3]	1	1	1	↑	1	0	*	D[0:3]
X	0	0	X	X	1	0	0	Q[0:3]
X	X	0	0	X	1	0	0	Q[0:3]
X	X	1	0	X	1	0	*	Q[0:3]
X	0	1	1	↑	1	0	*	count+1
X	X	0	X	X	0	1	0	0
X	X	1	X	X	0	1	1	0
D[0:3]	1	1	1	↑	0	0	1	D[0:3]
D[0:3]	1	0	1	↑	0	0	**	D[0:3]
X	0	1	X	X	0	0	1	Q[0:3]
X	X	1	0	X	0	0	1	Q[0:3]
X	X	0	0	X	0	0	**	Q[0:3]
X	0	0	1	↑	0	0	**	count-1

X = Don’t care
* When Q[0:3] is 1111, CO will be 1; otherwise, CO will be 0
** When Q[0:3] is 0000, CO will be 0; otherwise, CO will be 1
When GSR=0, CO=!CON•CI, Q[0:3]=0 (D[0:3]=SP=CK=SD=CD=X)

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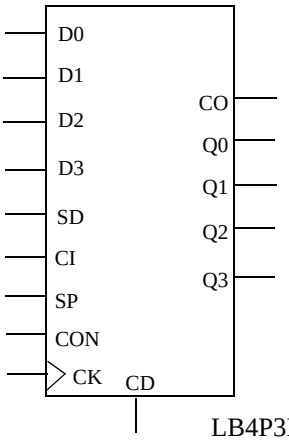
LB4P3IX

4 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable and Positive Level Synchronous Clear (Clear overrides Enable)

ORCA Series		
2	3	4
	✓	✓



INPUTS: D0,D1,D2,D3,CI,SP,CK,SD,CD,CON
OUTPUTS: CO,Q0,Q1,Q2,Q3
PINORDER: D0 D1 D2 D3 CI SP CK SD CD CON CO Q0 Q1 Q2 Q3
MINIMUM CELL AREA: 0.25

Note: When CON = 0, CI and CO are active LOW

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Truth Table:

INPUTS							OUTPUTS	
D[0:3]	SD	CI	SP	CK	CON	CD	CO	Q[0:3]
X	X	X	X	↑	1	1	0	0
D[0:3]	1	0	1	↑	1	0	0	D[0:3]
D[0:3]	1	1	1	↑	1	0	*	D[0:3]
X	0	0	X	X	1	0	0	Q[0:3]
X	X	0	0	X	1	0	0	Q[0:3]
X	X	1	0	X	1	0	*	Q[0:3]
X	0	1	1	↑	1	0	*	count+1
X	X	0	X	↑	0	1	0	0
X	X	1	X	↑	0	1	1	0
D[0:3]	1	1	1	↑	0	0	1	D[0:3]
D[0:3]	1	0	1	↑	0	0	**	D[0:3]
X	0	1	X	X	0	0	1	Q[0:3]
X	X	1	0	X	0	0	1	Q[0:3]
X	X	0	0	X	0	0	**	Q[0:3]
X	0	0	1	↑	0	0	**	count-1

X = Don’t care
* When Q[0:3] is 1111, CO will be 1; otherwise, CO will be 0
** When Q[0:3] is 0000, CO will be 0; otherwise, CO will be 1
When GSR=0, CO=!CON•CI, Q[0:3]=0 (D[0:3]=SP=CK=SD=CD=X)

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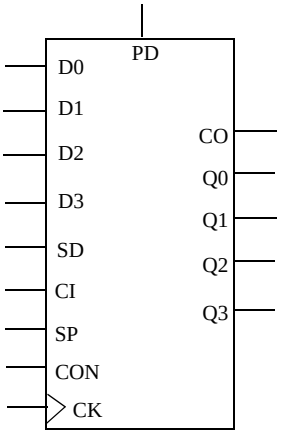
LB4P3JX

4 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable and Positive Level Synchronous Preset (Preset overrides Enable)

ORCA Series		
2	3	4
	✓	✓



LB4P3JX

INPUTS: D0,D1,D2,D3,CI,SP,CK,SD,PD,CON
OUTPUTS: CO,Q0,Q1,Q2,Q3
PINORDER: D0 D1 D2 D3 CI SP CK SD PD CON CO Q0 Q1 Q2 Q3
MINIMUM CELL AREA: 0.5

Note: When CON = 0, CI and CO are active LOW

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Truth Table:

INPUTS							OUTPUTS	
D[0:3]	SD	CI	SP	CK	CON	PD	CO	Q[0:3]
X	X	0	X	↑	1	1	0	1
X	X	1	X	↑	1	1	1	1
D[0:3]	1	0	1	↑	1	0	0	D[0:3]
D[0:3]	1	1	1	↑	1	0	*	D[0:3]
X	0	0	X	X	1	0	0	Q[0:3]
X	X	0	0	X	1	0	0	Q[0:3]
X	X	1	0	X	1	0	*	Q[0:3]
X	0	1	1	↑	1	0	*	count+1
X	X	X	X	↑	0	1	1	1
D[0:3]	1	1	1	↑	0	0	1	D[0:3]
D[0:3]	1	0	1	↑	0	0	**	D[0:3]
X	0	1	X	X	0	0	1	Q[0:3]
X	X	1	0	X	0	0	1	Q[0:3]
X	X	0	0	X	0	0	**	Q[0:3]
X	0	0	1	↑	0	0	**	count-1

X = Don’t care
* When Q[0:3] is 1111, CO will be 1; otherwise, CO will be 0
** When Q[0:3] is 0000, CO will be 0; otherwise, CO will be 1
When GSR=0, CO=!CON+CI, Q[0:3]=1 (D[0:3]=SP=CK=SD=PD=X)

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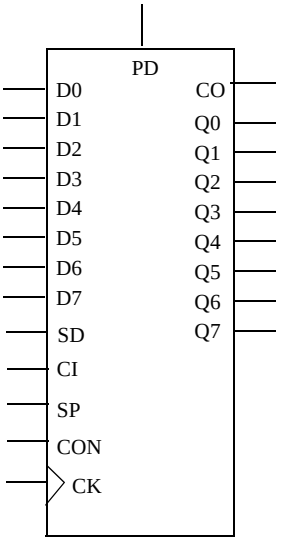
LB8P3BX

8 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable and Positive Level Asynchronous Preset

ORCA Series		
2	3	4
	✓	✓



LB8P3BX

INPUTS: D0,D1,D2,D3,D4,D5,D6,D7,CI,SP,CK,SD,PD,CON
OUTPUTS: CO,Q0,Q1,Q2,Q3,Q4,Q5,Q6,Q7
PINORDER: D0 D1 D2 D3 D4 D5 D6 D7 CI SP CK SD PD CON CO Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
MINIMUM CELL AREA: 0.5

Note: When CON = 0, CI and CO are active LOW

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Truth Table:

INPUTS							OUTPUTS	
D[0:7]	SD	CI	SP	CK	CON	PD	CO	Q[0:7]
X	X	0	X	X	1	1	0	1
X	X	1	X	X	1	1	1	1
D[0:7]	1	0	1	↑	1	0	0	D[0:7]
D[0:7]	1	1	1	↑	1	0	*	D[0:7]
X	0	0	X	X	1	0	0	Q[0:7]
X	X	0	0	X	1	0	0	Q[0:7]
X	X	1	0	X	1	0	*	Q[0:7]
X	0	1	1	↑	1	0	*	count+1
X	X	X	X	X	0	1	1	1
D[0:7]	1	1	1	↑	0	0	1	D[0:7]
D[0:7]	1	0	1	↑	0	0	**	D[0:7]
X	0	1	X	X	0	0	1	Q[0:7]
X	X	1	0	X	0	0	1	Q[0:7]
X	X	0	0	X	0	0	**	Q[0:7]
X	0	0	1	↑	0	0	**	count-1

X = Don’t care
* When Q[0:7] is 11111111, CO will be 1; otherwise, CO will be 0
** When Q[0:7] is 00000000, CO will be 0; otherwise, CO will be 1
When GSR=0, CO=!CON+CI, Q[0:7]=1 (D[0:7]=SP=CK=SD=PD=X)

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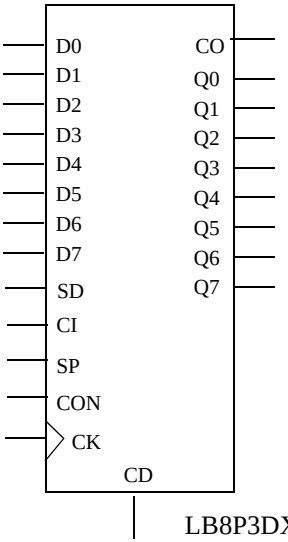
LB8P3DX

8 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable and Positive Level Asynchronous Clear

ORCA Series		
2	3	4
	✓	✓



INPUTS: D0,D1,D2,D3,D4,D5,D6,D7,CI,SP,CK,SD,CD,CON
OUTPUTS: CO,Q0,Q1,Q2,Q3,Q4,Q5,Q6,Q7
PINORDER: D0 D1 D2 D3 D4 D5 D6 D7 CI SP CK SD CD CON CO Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
MINIMUM CELL AREA: 0.5

Note: When CON = 0, CI and CO are active LOW

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Truth Table:

INPUTS							OUTPUTS	
D[0:7]	SD	CI	SP	CK	CON	CD	CO	Q[0:7]
X	X	X	X	X	1	1	0	0
D[0:7]	1	0	1	↑	1	0	0	D[0:7]
D[0:7]	1	1	1	↑	1	0	*	D[0:7]
X	0	0	X	X	1	0	0	Q[0:7]
X	X	0	0	X	1	0	0	Q[0:7]
X	X	1	0	X	1	0	*	Q[0:7]
X	0	1	1	↑	1	0	*	count+1
X	X	0	X	X	0	1	0	0
X	X	1	X	X	0	1	1	0
D[0:7]	1	1	1	↑	0	0	1	D[0:7]
D[0:7]	1	0	1	↑	0	0	**	D[0:7]
X	0	1	X	X	0	0	1	Q[0:7]
X	X	1	0	X	0	0	1	Q[0:7]
X	X	0	0	X	0	0	**	Q[0:7]
X	0	0	1	↑	0	0	**	count-1

X = Don’t care
* When Q[0:7] is 11111111, CO will be 1; otherwise, CO will be 0
** When Q[0:7] is 00000000, CO will be 0; otherwise, CO will be 1
When GSR=0, CO=!CON•CI, Q[0:7]=0 (D[0:7]=SP=CK=SD=CD=X)

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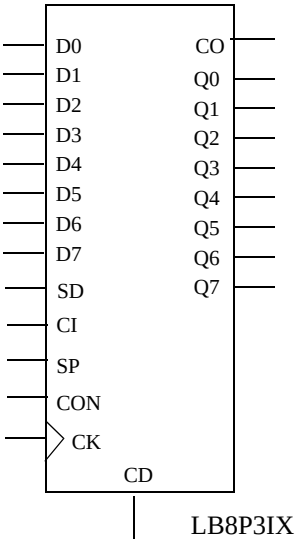
LB8P3IX

8 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable and Positive Level Synchronous Clear (Clear overrides Enable)

ORCA Series		
2	3	4
	✓	✓



INPUTS: D0,D1,D2,D3,D4,D5,D6,D7,CI,SP,CK,SD,CD,CON
OUTPUTS: CO,Q0,Q1,Q2,Q3,Q4,Q5,Q6,Q7
PINORDER: D0 D1 D2 D3 D4 D5 D6 D7 CI SP CK SD CD CON CO Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
MINIMUM CELL AREA: 0.5

Note: When CON = 0, CI and CO are active LOW

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Truth Table:

INPUTS							OUTPUTS	
D[0:7]	SD	CI	SP	CK	CON	CD	CO	Q[0:7]
X	X	X	X	↑	1	1	0	0
D[0:7]	1	0	1	↑	1	0	0	D[0:7]
D[0:7]	1	1	1	↑	1	0	*	D[0:7]
X	0	0	X	X	1	0	0	Q[0:7]
X	X	0	0	X	1	0	0	Q[0:7]
X	X	1	0	X	1	0	*	Q[0:7]
X	0	1	1	↑	1	0	*	count+1
X	X	0	X	↑	0	1	0	0
X	X	1	X	↑	0	1	1	0
D[0:7]	1	1	1	↑	0	0	1	D[0:7]
D[0:7]	1	0	1	↑	0	0	**	D[0:7]
X	0	1	X	X	0	0	1	Q[0:7]
X	X	1	0	X	0	0	1	Q[0:7]
X	X	0	0	X	0	0	**	Q[0:7]
X	0	0	1	↑	0	0	**	count-1

X = Don’t care
* When Q[0:7] is 11111111, CO will be 1; otherwise, CO will be 0
** When Q[0:7] is 00000000, CO will be 0; otherwise, CO will be 1
When GSR=0, CO=!CON•CI, Q[0:7]=0 (D[0:7]=SP=CK=SD=CD=X)

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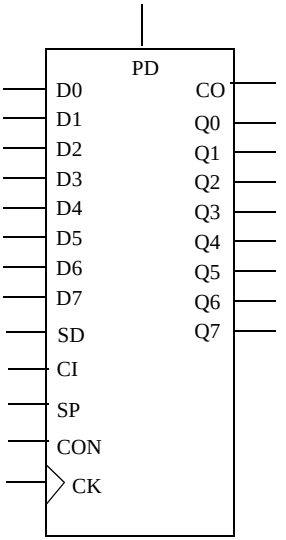
LB8P3JX

8 Bit Positive Edge Triggered Loadable Bidirectional Counter with Positive Clock Enable and Positive Level Synchronous Preset (Preset overrides Enable)

ORCA Series		
2	3	4
	✓	✓



LB8P3JX

INPUTS: D0,D1,D2,D3,D4,D5,D6,D7,CI,SP,CK,SD,PD,CON
OUTPUTS: CO,Q0,Q1,Q2,Q3,Q4,Q5,Q6,Q7
PINORDER: D0 D1 D2 D3 D4 D5 D6 D7 CI SP CK SD PD CON CO Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
MINIMUM CELL AREA: 0.5

Note: When CON = 0, CI and CO are active LOW

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Truth Table:

INPUTS							OUTPUTS	
D[0:7]	SD	CI	SP	CK	CON	PD	CO	Q[0:7]
X	X	0	X	↑	1	1	0	1
X	X	1	X	↑	1	1	1	1
D[0:7]	1	0	1	↑	1	0	0	D[0:7]
D[0:7]	1	1	1	↑	1	0	*	D[0:7]
X	0	0	X	X	1	0	0	Q[0:7]
X	X	0	0	X	1	0	0	Q[0:7]
X	X	1	0	X	1	0	*	Q[0:7]
X	0	1	1	↑	1	0	*	count+1
X	X	X	X	↑	0	1	1	1
D[0:7]	1	1	1	↑	0	0	1	D[0:7]
D[0:7]	1	0	1	↑	0	0	**	D[0:7]
X	0	1	X	X	0	0	1	Q[0:7]
X	X	1	0	X	0	0	1	Q[0:7]
X	X	0	0	X	0	0	**	Q[0:7]
X	0	0	1	↑	0	0	**	count-1

X = Don’t care
* When Q[0:7] is 11111111, CO will be 1; otherwise, CO will be 0
** When Q[0:7] is 00000000, CO will be 0; otherwise, CO will be 1
When GSR=0, CO=!CON+CI, Q[0:7]=1 (D[0:7]=SP=CK=SD=PD=X)

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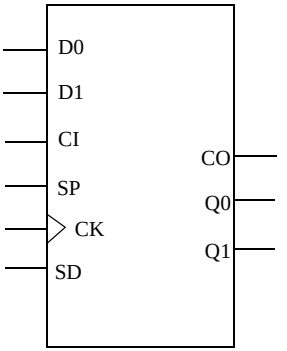
LD2P3AX

2 Bit Positive Edge Triggered Loadable Down-Counter with Positive Clock Enable, GSR Used for Clear

Lattice FPGA		
SC	XP	EC
✓		



LD2P3AX

INPUTS: D0, D1, CI, SP, CK, SD
OUTPUTS: CO, Q0, Q1
PINORDER: D0, D1, CI, SP, CK, SD, CO, Q0, Q1
MINIMUM CELL AREA: One Slice

Note: CI and CO are active LOW

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Truth Table:

INPUTS					OUTPUTS	
D[0:1]	SD	CI	SP	CK	CO	Q[0:1]
D[0:1]	1	1	1	↑	1	D[0:1]
D[0:1]	1	0	1	↑	*	D[0:1]
X	0	1	X	X	1	Q[0:1]
X	X	1	0	X	1	Q[0:1]
X	X	0	0	X	*	Q[0:1]
X	0	0	1	↑	*	count-1

X = Don’t care

* When Q[0:1] is 00, CO will be 0; otherwise, CO will be 1
When GSR=0, CO=CI, Q[0:1]=0 (D[0:1]=SP=CK=SD=X)

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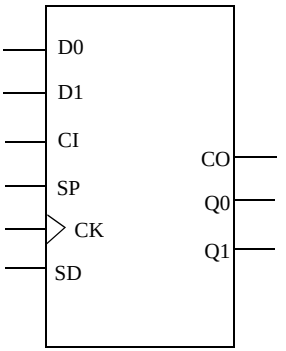
LD2P3AY

2 Bit Positive Edge Triggered Loadable Down-Counter with Positive Clock Enable, GSR Used for Preset

Lattice FPGA		
SC	XP	EC
✓		



LD2P3AY

INPUTS: D0, D1, CI, SP, CK, SD
OUTPUTS: CO, Q0, Q1
PINORDER: D0, D1, CI, SP, CK, SD, CO, Q0, Q1
MINIMUM CELL AREA: One Slice

Note: CI and CO are active LOW

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Truth Table:

INPUTS					OUTPUTS	
D[0:1]	SD	CI	SP	CK	CO	Q[0:1]
D[0:1]	1	1	1	↑	1	D[0:1]
D[0:1]	1	0	1	↑	*	D[0:1]
X	0	1	X	X	1	Q[0:1]
X	X	1	0	X	1	Q[0:1]
X	X	0	0	X	*	Q[0:1]
X	0	0	1	↑	*	count-1

X = Don’t care

* When Q[0:1] is 00, CO will be 0; otherwise, CO will be 1
When GSR=0, CO=1, Q[0:1]=1 (D[0:1]=CI=SP=CK=SD=X)

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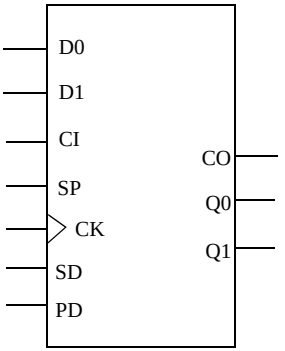
LD2P3BX

2 Bit Positive Edge Triggered Loadable Down-Counter with Positive Clock Enable and Positive Level Asynchronous Preset

Lattice FPGA		
SC	XP	EC
✓		



LD2P3BX

INPUTS: D0, D1, CI, SP, CK, SD, PD
OUTPUTS: CO, Q0, Q1
PINORDER: D0, D1, CI, SP, CK, SD, PD, CO, Q0, Q1
MINIMUM CELL AREA: One Slice

Note: CI and CO are active LOW

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Truth Table:

INPUTS						OUTPUTS	
D[0:1]	SD	CI	SP	CK	PD	CO	Q[0:1]
X	X	X	X	X	1	1	1
D[0:1]	1	1	1	↑	0	1	D[0:1]
D[0:1]	1	0	1	↑	0	*	D[0:1]
X	0	1	X	X	0	1	Q[0:1]
X	X	1	0	X	0	1	Q[0:1]
X	X	0	0	X	0	*	Q[0:1]
X	0	0	1	↑	0	*	count-1

X = Don’t care

* When Q[0:1] is 00, CO will be 0; otherwise, CO will be 1
When GSR=0, CO=1, Q[0:1]=1 (D[0:1]=SP=CK=SD=PD=X)

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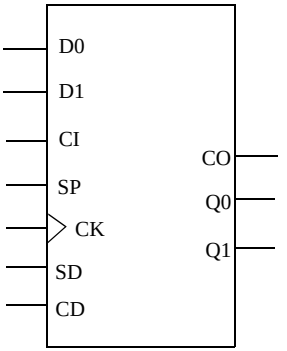
LD2P3DX

2 Bit Positive Edge Triggered Loadable Down-Counter with Positive Clock Enable and Positive Level Asynchronous Clear

Lattice FPGA		
SC	XP	EC
✓		



LD2P3DX

INPUTS: D0, D1, CI, SP, CK, SD, CD
OUTPUTS: CO, Q0, Q1
PINORDER: D0, D1, CI, SP, CK, SD, CD, CO, Q0, Q1
MINIMUM CELL AREA: One Slice

Note: CI and CO are active LOW

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Truth Table:

INPUTS						OUTPUTS	
D[0:1]	SD	CI	SP	CK	CD	CO	Q[0:1]
X	X	0	X	X	1	0	0
X	X	1	X	X	1	1	0
D[0:1]	1	1	1	↑	0	1	D[0:1]
D[0:1]	1	0	1	↑	0	*	D[0:1]
X	0	1	X	X	0	1	Q[0:1]
X	X	1	0	X	0	1	Q[0:1]
X	X	0	0	X	0	*	Q[0:1]
X	0	0	1	↑	0	*	count-1

X = Don’t care

* When Q[0:1] is 00, CO will be 0; otherwise, CO will be 1
When GSR=0, CO=CI, Q[0:1]=0 (D[0:1]=SP=CK=SD=CD=X)

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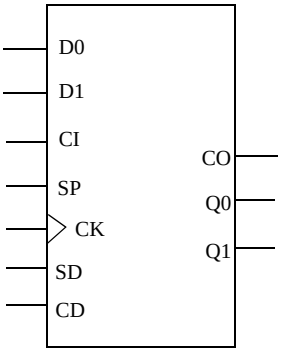
LD2P3IX

2 Bit Positive Edge Triggered Loadable Down-Counter with Positive Clock Enable and Positive Level Synchronous Clear (Clear overrides Enable)

Lattice FPGA		
SC	XP	EC
✓		



LD2P3IX

INPUTS: D0, D1, CI, SP, CK, SD, CD
OUTPUTS: CO, Q0, Q1
PINORDER: D0, D1, CI, SP, CK, SD, CD, CO, Q0, Q1
MINIMUM CELL AREA: One Slice

Note: CI and CO are active LOW

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Truth Table:

INPUTS						OUTPUTS	
D[0:1]	SD	CI	SP	CK	CD	CO	Q[0:1]
X	X	0	X	↑	1	0	0
X	X	1	X	↑	1	1	0
D[0:1]	1	1	1	↑	0	1	D[0:1]
D[0:1]	1	0	1	↑	0	*	D[0:1]
X	0	1	X	X	0	1	Q[0:1]
X	X	1	0	X	0	1	Q[0:1]
X	X	0	0	X	0	*	Q[0:1]
X	0	0	1	↑	0	*	count-1

X = Don’t care

* When Q[0:1] is 00, CO will be 0; otherwise, CO will be 1
When GSR=0, CO=CI, Q[0:1]=0 (D[0:1]=SP=CK=SD=CD=X)

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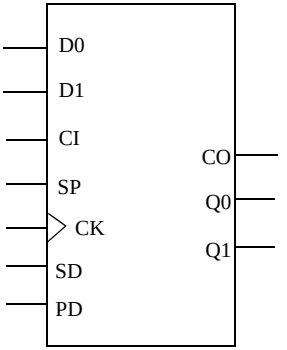
LD2P3JX

2 Bit Positive Edge Triggered Loadable Down-Counter with Positive Clock Enable and Positive Level Synchronous Preset (Preset overrides Enable)

Lattice FPGA		
SC	XP	EC
✓		



LD2P3JX

INPUTS: D0, D1, CI, SP, CK, SD, PD
OUTPUTS: CO, Q0, Q1
PINORDER: D0, D1, CI, SP, CK, SD, PD, CO, Q0, Q1
MINIMUM CELL AREA: One Slice

Note: CI and CO are active LOW

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Truth Table:

INPUTS						OUTPUTS	
D[0:1]	SD	CI	SP	CK	PD	CO	Q[0:1]
X	X	X	X	↑	1	1	1
D[0:1]	1	1	1	↑	0	1	D[0:1]
D[0:1]	1	0	1	↑	0	*	D[0:1]
X	0	1	X	X	0	1	Q[0:1]
X	X	1	0	X	0	1	Q[0:1]
X	X	0	0	X	0	*	Q[0:1]
X	0	0	1	↑	0	*	count-1

X = Don’t care

* When Q[0:1] is 00, CO will be 0; otherwise, CO will be 1
When GSR=0, CO=1, Q[0:1]=1 (D[0:1]=SP=CK=SD=PD=X)

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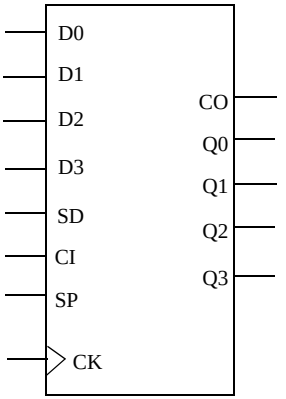
LD4P3AX

4 Bit Positive Edge Triggered Loadable Down-Counter with Positive Clock Enable, GSR Used for Clear

ORCA Series		
2	3	4
✓	✓	✓



LD4P3AX

INPUTS: D0,D1,D2,D3,CI,SP,CK,SD
OUTPUTS: CO,Q0,Q1,Q2,Q3
PINORDER: D0 D1 D2 D3 CI SP CK SD CO Q0 Q1 Q2 Q
MINIMUM CELL AREA (2A/2T): 1.0
MINIMUM CELL AREA (Series 3): 0.25

Note: CI and CO are active LOW

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Truth Table:

INPUTS					OUTPUTS	
D[0:3]	SD	CI	SP	CK	CO	Q[0:3]
D[0:3]	1	1	1	↑	1	D[0:3]
D[0:3]	1	0	1	↑	*	D[0:3]
X	0	1	X	X	1	Q[0:3]
X	X	1	0	X	1	Q[0:3]
X	X	0	0	X	*	Q[0:3]
X	0	0	1	↑	*	count-1

X = Don’t care

* When Q[0:3] is 0000, CO will be 0; otherwise, CO will be 1
When GSR=0, CO=CI, Q[0:3]=0 (D[0:3]=SP=CK=SD=X)

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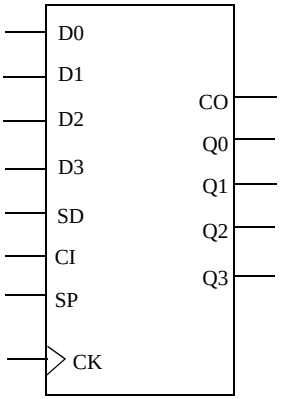
LD4P3AY

4 Bit Positive Edge Triggered Loadable Down-Counter with Positive Clock Enable, GSR Used for Preset

ORCA Series		
2	3	4
✓	✓	✓



LD4P3AY

INPUTS: D0,D1,D2,D3,CI,SP,CK,SD
OUTPUTS: CO,Q0,Q1,Q2,Q3
PINORDER: D0 D1 D2 D3 CI SP CK SD CO Q0 Q1 Q2 Q3
MINIMUM CELL AREA (2A/2T): 1.0
MINIMUM CELL AREA (Series 3): 0.25

Note: CI and CO are active LOW

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Truth Table:

INPUTS					OUTPUTS	
D[0:3]	SD	CI	SP	CK	CO	Q[0:3]
D[0:3]	1	1	1	↑	1	D[0:3]
D[0:3]	1	0	1	↑	*	D[0:3]
X	0	1	X	X	1	Q[0:3]
X	X	1	0	X	1	Q[0:3]
X	X	0	0	X	*	Q[0:3]
X	0	0	1	↑	*	count-1

X = Don’t care

* When Q[0:3] is 0000, CO will be 0; otherwise, CO will be 1
When GSR=0, CO=1, Q[0:3]=1 (D[0:3]=CI=SP=CK=SD=X)

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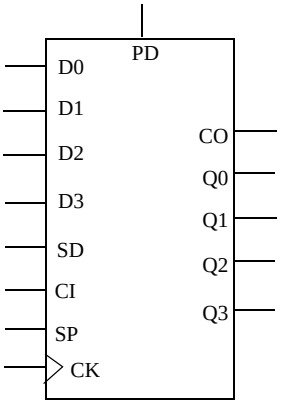
LD4P3BX

4 Bit Positive Edge Triggered Loadable Down-Counter with Positive Clock Enable and Positive Level Asynchronous Preset

ORCA Series		
2	3	4
	✓	✓



LD4P3BX

INPUTS: D0,D1,D2,D3,CI,SP,CK,SD,PD
OUTPUTS: CO,Q0,Q1,Q2,Q3
PINORDER: D0 D1 D2 D3 CI SP CK SD PD CO Q0 Q1 Q2 Q3
MINIMUM CELL AREA: 0.25

Note: CI and CO are active LOW

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Truth Table:

INPUTS						OUTPUTS	
D[0:3]	SD	CI	SP	CK	PD	CO	Q[0:3]
X	X	X	X	X	1	1	1
D[0:3]	1	1	1	↑	0	1	D[0:3]
D[0:3]	1	0	1	↑	0	*	D[0:3]
X	0	1	X	X	0	1	Q[0:3]
X	X	1	0	X	0	1	Q[0:3]
X	X	0	0	X	0	*	Q[0:3]
X	0	0	1	↑	0	*	count-1

X = Don’t care

* When Q[0:3] is 0000, CO will be 0; otherwise, CO will be 1
When GSR=0, CO=1, Q[0:3]=1 (D[0:3]=SP=CK=SD=PD=X)

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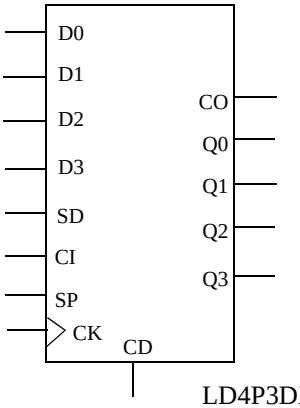
LD4P3DX

4 Bit Positive Edge Triggered Loadable Down-Counter with Positive Clock Enable and Positive Level Asynchronous Clear

ORCA Series		
2	3	4
	✓	✓



LD4P3DX

INPUTS: D0,D1,D2,D3,CI,SP,CK,SD,CD
OUTPUTS: CO,Q0,Q1,Q2,Q3
PINORDER: D0 D1 D2 D3 CI SP CK SD CD CO Q0 Q1 Q2 Q3
MINIMUM CELL AREA: 0.25

Note: CI and CO are active LOW

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Truth Table:

INPUTS						OUTPUTS	
D[0:3]	SD	CI	SP	CK	CD	CO	Q[0:3]
X	X	0	X	X	1	0	0
X	X	1	X	X	1	1	0
D[0:3]	1	1	1	↑	0	1	D[0:3]
D[0:3]	1	0	1	↑	0	*	D[0:3]
X	0	1	X	X	0	1	Q[0:3]
X	X	1	0	X	0	1	Q[0:3]
X	X	0	0	X	0	*	Q[0:3]
X	0	0	1	↑	0	*	count-1

X = Don’t care

* When Q[0:3] is 0000, CO will be 0; otherwise, CO will be 1
When GSR=0, CO=CI, Q[0:3]=0 (D[0:3]=SP=CK=SD=CD=X)

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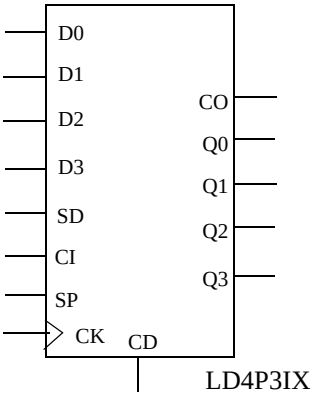
LD4P3IX

4 Bit Positive Edge Triggered Loadable Down-Counter with Positive Clock Enable and Positive Level Synchronous Clear (Clear overrides Enable)

ORCA Series		
2	3	4
	✓	✓



INPUTS: D0,D1,D2,D3,CI,SP,CK,SD,CD
OUTPUTS: CO,Q0,Q1,Q2,Q3
PINORDER: D0 D1 D2 D3 CI SP CK SD CD CO Q0 Q1 Q2 Q3
MINIMUM CELL AREA: 0.25

Note: CI and CO are active LOW

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Truth Table:

INPUTS						OUTPUTS	
D[0:3]	SD	CI	SP	CK	CD	CO	Q[0:3]
X	X	0	X	↑	1	0	0
X	X	1	X	↑	1	1	0
D[0:3]	1	1	1	↑	0	1	D[0:3]
D[0:3]	1	0	1	↑	0	*	D[0:3]
X	0	1	X	X	0	1	Q[0:3]
X	X	1	0	X	0	1	Q[0:3]
X	X	0	0	X	0	*	Q[0:3]
X	0	0	1	↑	0	*	count-1

X = Don’t care

* When Q[0:3] is 0000, CO will be 0; otherwise, CO will be 1
When GSR=0, CO=CI, Q[0:3]=0 (D[0:3]=SP=CK=SD=CD=X)

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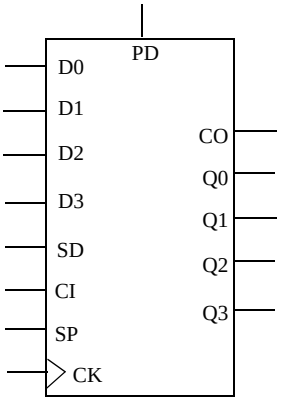
LD4P3JX

4 Bit Positive Edge Triggered Loadable Down-Counter with Positive Clock Enable and Positive Level Synchronous Preset (Preset overrides Enable)

ORCA Series		
2	3	4
	✓	✓



LD4P3JX

INPUTS: D0,D1,D2,D3,CI,SP,CK,SD,PD
OUTPUTS: CO,Q0,Q1,Q2,Q3
PINORDER: D0 D1 D2 D3 CI SP CK SD PD CO Q0 Q1 Q2 Q3
MINIMUM CELL AREA: 0.25

Note: CI and CO are active LOW

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Truth Table:

INPUTS						OUTPUTS	
D[0:3]	SD	CI	SP	CK	PD	CO	Q[0:3]
X	X	X	X	↑	1	1	1
D[0:3]	1	1	1	↑	0	1	D[0:3]
D[0:3]	1	0	1	↑	0	*	D[0:3]
X	0	1	X	X	0	1	Q[0:3]
X	X	1	0	X	0	1	Q[0:3]
X	X	0	0	X	0	*	Q[0:3]
X	0	0	1	↑	0	*	count-1

X = Don’t care

* When Q[0:3] is 0000, CO will be 0; otherwise, CO will be 1
When GSR=0, CO=1, Q[0:3]=1 (D[0:3]=SP=CK=SD=PD=X)

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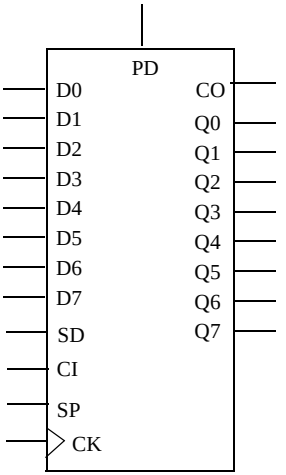
LD8P3BX

8 Bit Positive Edge Triggered Loadable Down-Counter with Positive Clock Enable and Positive Level Asynchronous Preset

ORCA Series		
2	3	4
	✓	✓



LD8P3BX

INPUTS: D0,D1,D2,D3,D4,D5,D6,D7,CI,SP,CK,SD,PD
OUTPUTS: CO,Q0,Q1,Q2,Q3,Q4,Q5,Q6,Q7
PINORDER: D0 D1 D2 D3 D4 D5 D6 D7 CI SP CK SD PD CO Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
MINIMUM CELL AREA: 0.5

Note: CI and CO are active LOW

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Truth Table:

INPUTS						OUTPUTS	
D[0:7]	SD	CI	SP	CK	PD	CO	Q[0:7]
X	X	X	X	X	1	1	1
D[0:7]	1	1	1	↑	0	1	D[0:7]
D[0:7]	1	0	1	↑	0	*	D[0:7]
X	0	1	X	X	0	1	Q[0:7]
X	X	1	0	X	0	1	Q[0:7]
X	X	0	0	X	0	*	Q[0:7]
X	0	0	1	↑	0	*	count-1

X = Don’t care

* When Q[0:7] is 00000000, CO will be 0; otherwise, CO will be 1
When GSR=0, CO=1, Q[0:7]=1 (D[0:7]=SP=CK=SD=PD=X)

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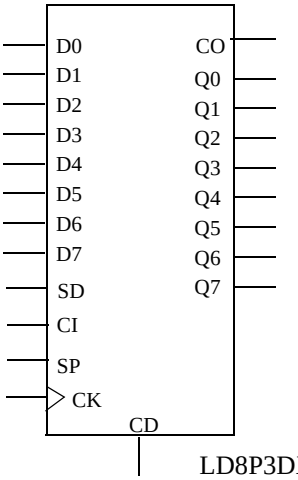
LD8P3DX

8 Bit Positive Edge Triggered Loadable Down-Counter with Positive Clock Enable and Positive Level Asynchronous Clear

ORCA Series		
2	3	4
	✓	✓



INPUTS: D0,D1,D2,D3,D4,D5,D6,D7,CI,SP,CK,SD,CD
OUTPUTS: CO,Q0,Q1,Q2,Q3,Q4,Q5,Q6,Q7
PINORDER: D0 D1 D2 D3 D4 D5 D6 D7 CI SP CK SD CD CO Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
MINIMUM CELL AREA: 0.5

Note: CI and CO are active LOW

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Truth Table:

INPUTS						OUTPUTS	
D[0:7]	SD	CI	SP	CK	CD	CO	Q[0:7]
X	X	0	X	X	1	0	0
X	X	1	X	X	1	1	0
D[0:7]	1	1	1	↑	0	1	D[0:7]
D[0:7]	1	0	1	↑	0	*	D[0:7]
X	0	1	X	X	0	1	Q[0:7]
X	X	1	0	X	0	1	Q[0:7]
X	X	0	0	X	0	*	Q[0:7]
X	0	0	1	↑	0	*	count-1

X = Don’t care

* When Q[0:7] is 00000000, CO will be 0; otherwise, CO will be 1
When GSR=0, CO=CI, Q[0:7]=0 (D[0:7]=SP=CK=SD=CD=X)

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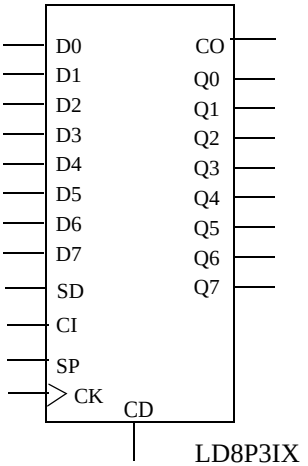
LD8P3IX

8 Bit Positive Edge Triggered Loadable Down-Counter with Positive Clock Enable and Positive Level Synchronous Clear (Clear overrides Enable)

ORCA Series		
2	3	4
	✓	✓



INPUTS: D0,D1,D2,D3,D4,D5,D6,D7,CI,SP,CK,SD,CD
OUTPUTS: CO,Q0,Q1,Q2,Q3,Q4,Q5,Q6,Q7
PINORDER: D0 D1 D2 D3 D4 D5 D6 D7 CI SP CK SD CD CO Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
MINIMUM CELL AREA: 0.5

Note: CI and CO are active LOW

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Truth Table:

INPUTS						OUTPUTS	
D[0:7]	SD	CI	SP	CK	CD	CO	Q[0:7]
X	X	0	X	↑	1	0	0
X	X	1	X	↑	1	1	0
D[0:7]	1	1	1	↑	0	1	D[0:7]
D[0:7]	1	0	1	↑	0	*	D[0:7]
X	0	1	X	X	0	1	Q[0:7]
X	X	1	0	X	0	1	Q[0:7]
X	X	0	0	X	0	*	Q[0:7]
X	0	0	1	↑	0	*	count-1

X = Don’t care

* When Q[0:7] is 00000000, CO will be 0; otherwise, CO will be 1
When GSR=0, CO=CI, Q[0:7]=0 (D[0:7]=SP=CK=SD=CD=X)

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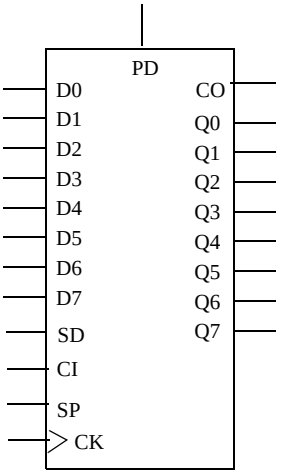
LD8P3JX

8 Bit Positive Edge Triggered Loadable Down-Counter with Positive Clock Enable and Positive Level Synchronous Preset (Preset overrides Enable)

ORCA Series		
2	3	4
	✓	✓



LD8P3JX

INPUTS: D0,D1,D2,D3,D4,D5,D6,D7,CI,SP,CK,SD,PD
OUTPUTS: CO,Q0,Q1,Q2,Q3,Q4,Q5,Q6,Q7
PINORDER: D0 D1 D2 D3 D4 D5 D6 D7 CI SP CK SD PD CO Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
MINIMUM CELL AREA: 0.5

Note: CI and CO are active LOW

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Truth Table:

INPUTS						OUTPUTS	
D[0:7]	SD	CI	SP	CK	PD	CO	Q[0:7]
X	X	X	X	↑	1	1	1
D[0:7]	1	1	1	↑	0	1	D[0:7]
D[0:7]	1	0	1	↑	0	*	D[0:7]
X	0	1	X	X	0	1	Q[0:7]
X	X	1	0	X	0	1	Q[0:7]
X	X	0	0	X	0	*	Q[0:7]
X	0	0	1	↑	0	*	count-1

X = Don’t care

* When Q[0:7] is 00000000, CO will be 0; otherwise, CO will be 1
When GSR=0, CO=1, Q[0:7]=1 (D[0:7]=SP=CK=SD=PD=X)

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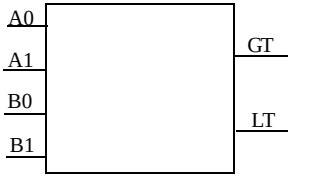
LTGT

Less Than or Greater Than

ORCA Series		
2	3	4
✓		



LTGT

INPUTS: A0,A1,B0,B1
OUTPUTS: GT,LT
PINORDER: A0 A1 B0 B1 GT LT
MINIMUM CELL AREA: 0.25

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Truth Table:

INPUTS				OUTPUTS	
A0	A1	B0	B1	GT	LT
0	0	0	0	0	0
1	0	0	0	1	0
0	1	0	0	1	0
1	1	0	0	1	0
0	0	1	0	0	1
1	0	1	0	0	0
0	1	1	0	1	0
1	1	1	0	1	0
0	0	0	1	0	1
1	0	0	1	0	1
0	1	0	1	0	0
1	1	0	1	1	0
0	0	1	1	0	1
1	0	1	1	0	1
0	1	1	1	0	1
1	1	1	1	0	0

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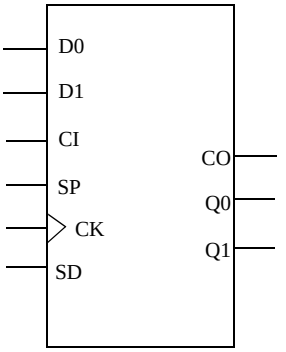
LU2P3AX

2 Bit Positive Edge Triggered Loadable Up-Counter with Positive Clock Enable, GSR Used for Clear

Lattice FPGA		
SC	XP	EC
✓		



LU2P3AX
INPUTS: D0, D1, CI, SP, CK, SD
OUTPUTS: CO, Q0, Q1
PINORDER: D0, D1, CI, SP, CK, SD, CO, Q0, Q1
MINIMUM CELL AREA: One Slice

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Truth Table:

INPUTS					OUTPUTS	
D[0:1]	SD	CI	SP	CK	CO	Q[0:1]
D[0:1]	1	0	1	↑	0	D[0:1]
D[0:1]	1	1	1	↑	*	D[0:1]
X	0	0	X	X	0	Q[0:1]
X	X	0	0	X	0	Q[0:1]
X	X	1	0	X	*	Q[0:1]
X	0	1	1	↑	*	count+1

X = Don’t care

* When Q[0:1] is 11, CO will be 1; otherwise, CO will be 0
When GSR=0, CO=0, Q[0:1]=0 (D[0:1]=SP=CK=SD=X)

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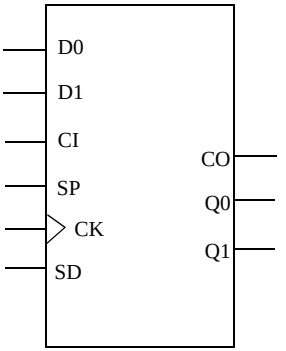
LU2P3AY

2 Bit Positive Edge Triggered Loadable Up-Counter with Positive Clock Enable, GSR Used for Preset

Lattice FPGA		
SC	XP	EC
✓		



LU2P3AY

INPUTS: D0, D1, CI, SP, CK, SD
OUTPUTS: CO, Q0, Q1
PINORDER: D0, D1, CI, SP, CK, SD, CO, Q0, Q1
MINIMUM CELL AREA: One Slice

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Truth Table:

INPUTS					OUTPUTS	
D[0:1]	SD	CI	SP	CK	CO	Q[0:1]
D[0:1]	1	0	1	↑	0	D[0:1]
D[0:1]	1	1	1	↑	*	D[0:1]
X	0	0	X	X	0	Q[0:1]
X	X	0	0	X	0	Q[0:1]
X	X	1	0	X	*	Q[0:1]
X	0	1	1	↑	*	count+1

X = Don’t care

* When Q[0:1] is 11, CO will be 1; otherwise, CO will be 0
When GSR=0, CO=CI, Q[0:1]=1 (D[0:1]=CI=SP=CK=SD=X)

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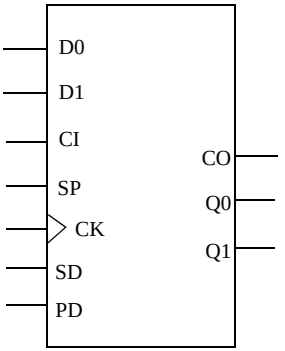
LU2P3BX

2 Bit Positive Edge Triggered Loadable Up-Counter with Positive Clock Enable and Positive Level Asynchronous Preset

Lattice FPGA		
SC	XP	EC
✓		



LU2P3BX

INPUTS: D0, D1, CI, SP, CK, SD, PD
OUTPUTS: CO, Q0, Q1
PINORDER: D0, D1, CI, SP, CK, SD, PD, CO, Q0, Q1
MINIMUM CELL AREA: One Slice

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Truth Table:

INPUTS						OUTPUTS	
D[0:1]	SD	CI	SP	CK	PD	CO	Q[0:1]
X	X	0	X	X	1	0	1
X	X	1	X	X	1	1	1
D[0:1]	1	0	1	↑	0	0	D[0:1]
D[0:1]	1	1	1	↑	0	*	D[0:1]
X	0	0	X	X	0	0	Q[0:1]
X	X	0	0	X	0	0	Q[0:1]
X	X	1	0	X	0	*	Q[0:1]
X	0	1	1	↑	0	*	count+1

X = Don’t care

* When Q[0:1] is 11, CO will be 1; otherwise, CO will be 0
When GSR=0, CO=CI, Q[0:1]=1 (D[0:1]=SP=CK=SD=PD=X)

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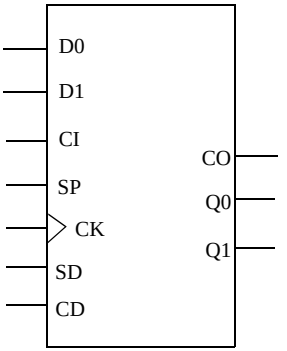
LU2P3DX

2 Bit Positive Edge Triggered Loadable Up-Counter with Positive Clock Enable and Positive Level Asynchronous Clear

Lattice FPGA		
SC	XP	EC
✓		



LU2P3DX

INPUTS: D0, D1, CI, SP, CK, SD, CD
OUTPUTS: CO, Q0, Q1
PINORDER: D0, D1, CI, SP, CK, SD, CD, CO, Q0, Q1
MINIMUM CELL AREA: One Slice

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Truth Table:

INPUTS						OUTPUTS	
D[0:1]	SD	CI	SP	CK	CD	CO	Q[0:1]
X	X	X	X	X	1	0	0
D[0:1]	1	0	1	↑	0	0	D[0:1]
D[0:1]	1	1	1	↑	0	*	D[0:1]
X	0	0	X	X	0	0	Q[0:1]
X	X	0	0	X	0	0	Q[0:1]
X	X	1	0	X	0	*	Q[0:1]
X	0	1	1	↑	0	*	count+1

X = Don’t care

* When Q[0:1] is 11, CO will be 1; otherwise, CO will be 0
When GSR=0, CO=0, Q[0:1]=0 (D[0:1]=SP=CK=SD=CD=X)

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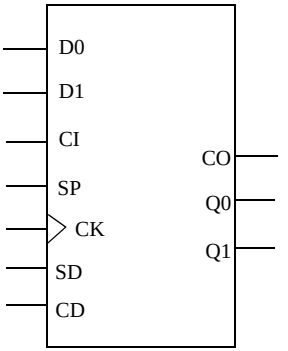
LU2P3IX

2 Bit Positive Edge Triggered Loadable Up-Counter with Positive Clock Enable and Positive Level Synchronous Clear (Clear overrides Enable

Lattice FPGA		
SC	XP	EC
✓		



LU2P3IX

INPUTS: D0, D1, CI, SP, CK, SD, CD
OUTPUTS: CO, Q0, Q1
PINORDER: D0, D1, CI, SP, CK, SD, CD, CO, Q0, Q1
MINIMUM CELL AREA: One Slice

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Truth Table:

INPUTS						OUTPUTS	
D[0:1]	SD	CI	SP	CK	CD	CO	Q[0:1]
X	X	X	X	↑	1	0	0
D[0:1]	1	0	1	↑	0	0	D[0:1]
D[0:1]	1	1	1	↑	0	*	D[0:1]
X	0	0	X	X	0	0	Q[0:1]
X	X	0	0	X	0	0	Q[0:1]
X	X	1	0	X	0	*	Q[0:1]
X	0	1	1	↑	0	*	count+1

X = Don’t care

* When Q[0:1] is 11, CO will be 1; otherwise, CO will be 0
When GSR=0, CO=0, Q[0:1]=0 (D[0:1]=SP=CK=SD=CD=X)

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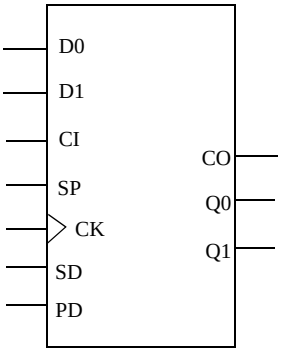
LU2P3JX

2 Bit Positive Edge Triggered Loadable Up-Counter with Positive Clock Enable and Positive Level Synchronous Preset (Preset overrides Enable

Lattice FPGA		
SC	XP	EC
✓		



LU2P3JX

INPUTS: D0, D1, CI, SP, CK, SD, PD
OUTPUTS: CO, Q0, Q1
PINORDER: D0, D1, CI, SP, CK, SD, PD, CO, Q0, Q1
MINIMUM CELL AREA: One Slice

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Truth Table:

INPUTS						OUTPUTS	
D[0:1]	SD	CI	SP	CK	PD	CO	Q[0:1]
X	X	0	X	↑	1	0	1
X	X	1	X	↑	1	1	1
D[0:1]	1	0	1	↑	0	0	D[0:1]
D[0:1]	1	1	1	↑	0	*	D[0:1]
X	0	0	X	X	0	0	Q[0:1]
X	X	0	0	X	0	0	Q[0:1]
X	X	1	0	X	0	*	Q[0:1]
X	0	1	1	↑	0	*	count+1

X = Don’t care

* When Q[0:1] is 11, CO will be 1; otherwise, CO will be 0
When GSR=0, CO=CI, Q[0:1]=1 (D[0:1]=SP=CK=SD=PD=X)

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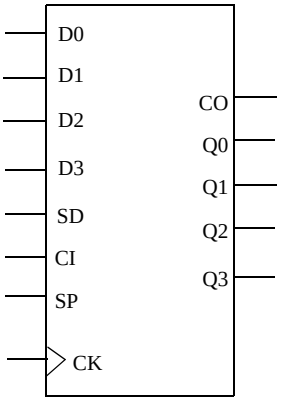
LU4P3AX

4 Bit Positive Edge Triggered Loadable Up-Counter with Positive Clock Enable, GSR Used for Clear

ORCA Series		
2	3	4
✓	✓	✓



LU4P3AX

INPUTS: D0,D1,D2,D3,CI,SP,CK,SD
OUTPUTS: CO,Q0,Q1,Q2,Q3
PINORDER: D0 D1 D2 D3 CI SP CK SD CO Q0 Q1 Q2 Q3
MINIMUM CELL AREA (2A/2T): 1.0
MINIMUM CELL AREA (Series 3): 0.25

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Truth Table:

INPUTS					OUTPUTS	
D[0:3]	SD	CI	SP	CK	CO	Q[0:3]
D[0:3]	1	0	1	↑	0	D[0:3]
D[0:3]	1	1	1	↑	*	D[0:3]
X	0	0	X	X	0	Q[0:3]
X	X	0	0	X	0	Q[0:3]
X	X	1	0	X	*	Q[0:3]
X	0	1	1	↑	*	count+1

X = Don’t care

* When Q[0:3] is 1111, CO will be 1; otherwise, CO will be 0
When GSR=0, CO=0, Q[0:3]=0 (D[0:3]=SP=CK=SD=X)

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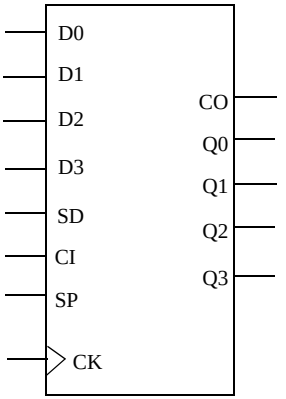
LU4P3AY

4 Bit Positive Edge Triggered Loadable Up-Counter with Positive Clock Enable, GSR Used for Preset

ORCA Series		
2	3	4
✓	✓	✓



LU4P3AY

INPUTS: D0,D1,D2,D3,CI,SP,CK,SD
OUTPUTS: CO,Q0,Q1,Q2,Q3
PINORDER: D0 D1 D2 D3 CI SP CK SD CO Q0 Q1 Q2 Q3
MINIMUM CELL AREA (2A/2T): 1.0
MINIMUM CELL AREA (Series 3): 0.25

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Truth Table:

INPUTS					OUTPUTS	
D[0:3]	SD	CI	SP	CK	CO	Q[0:3]
D[0:3]	1	0	1	↑	0	D[0:3]
D[0:3]	1	1	1	↑	*	D[0:3]
X	0	0	X	X	0	Q[0:3]
X	X	0	0	X	0	Q[0:3]
X	X	1	0	X	*	Q[0:3]
X	0	1	1	↑	*	count+1

X = Don’t care

* When Q[0:3] is 1111, CO will be 1; otherwise, CO will be 0
When GSR=0, CO=CI, Q[0:3]=1 (D[0:3]=CI=SP=CK=SD=X)

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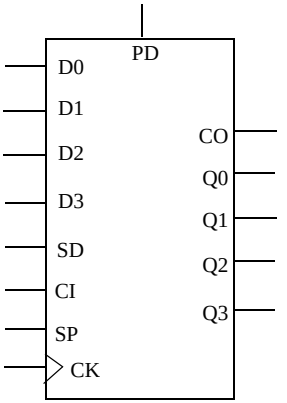
LU4P3BX

4 Bit Positive Edge Triggered Loadable Up-Counter with Positive Clock Enable and Positive Level Asynchronous Preset

ORCA Series		
2	3	4
	✓	✓



LU4P3BX

INPUTS: D0,D1,D2,D3,CI,SP,CK,SD,PD
OUTPUTS: CO,Q0,Q1,Q2,Q3
PINORDER: D0 D1 D2 D3 CI SP CK SD PD CO Q0 Q1 Q2 Q3
MINIMUM CELL AREA: 0.25

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Truth Table:

INPUTS						OUTPUTS	
D[0:3]	SD	CI	SP	CK	PD	CO	Q[0:3]
X	X	0	X	X	1	0	1
X	X	1	X	X	1	1	1
D[0:3]	1	0	1	↑	0	0	D[0:3]
D[0:3]	1	1	1	↑	0	*	D[0:3]
X	0	0	X	X	0	0	Q[0:3]
X	X	0	0	X	0	0	Q[0:3]
X	X	1	0	X	0	*	Q[0:3]
X	0	1	1	↑	0	*	count+1

X = Don’t care

* When Q[0:3] is 1111, CO will be 1; otherwise, CO will be 0
When GSR=0, CO=CI, Q[0:3]=1 (D[0:3]=SP=CK=SD=PD=X)

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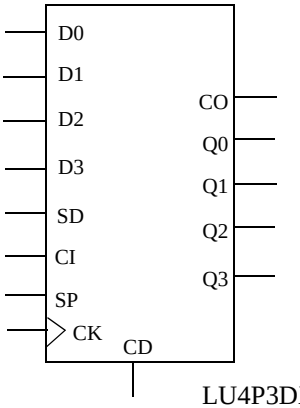
LU4P3DX

4 Bit Positive Edge Triggered Loadable Up-Counter with Positive Clock Enable and Positive Level Asynchronous Clear

ORCA Series		
2	3	4
	✓	✓



LU4P3DX

INPUTS: D0,D1,D2,D3,CI,SP,CK,SD,CD
OUTPUTS: CO,Q0,Q1,Q2,Q3
PINORDER: D0 D1 D2 D3 CI SP CK SD CD CO Q0 Q1 Q2 Q3
MINIMUM CELL AREA: 0.25

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Truth Table:

INPUTS						OUTPUTS	
D[0:3]	SD	CI	SP	CK	CD	CO	Q[0:3]
X	X	X	X	X	1	0	0
D[0:3]	1	0	1	↑	0	0	D[0:3]
D[0:3]	1	1	1	↑	0	*	D[0:3]
X	0	0	X	X	0	0	Q[0:3]
X	X	0	0	X	0	0	Q[0:3]
X	X	1	0	X	0	*	Q[0:3]
X	0	1	1	↑	0	*	count+1

X = Don’t care

* When Q[0:3] is 1111, CO will be 1; otherwise, CO will be 0
When GSR=0, CO=0, Q[0:3]=0 (D[0:3]=SP=CK=SD=CD=X)

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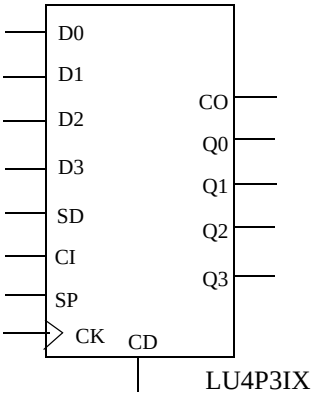
LU4P3IX

4 Bit Positive Edge Triggered Loadable Up-Counter with Positive Clock Enable and Positive Level Synchronous Clear (Clear overrides Enable)

ORCA Series		
2	3	4
	✓	✓



INPUTS: D0,D1,D2,D3,CI,SP,CK,SD,CD
OUTPUTS: CO,Q0,Q1,Q2,Q3
PINORDER: D0 D1 D2 D3 CI SP CK SD CD CO Q0 Q1 Q2 Q3
MINIMUM CELL AREA: 0.5

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Truth Table:

INPUTS						OUTPUTS	
D[0:3]	SD	CI	SP	CK	CD	CO	Q[0:3]
X	X	X	X	↑	1	0	0
D[0:3]	1	0	1	↑	0	0	D[0:3]
D[0:3]	1	1	1	↑	0	*	D[0:3]
X	0	0	X	X	0	0	Q[0:3]
X	X	0	0	X	0	0	Q[0:3]
X	X	1	0	X	0	*	Q[0:3]
X	0	1	1	↑	0	*	count+1

X = Don’t care

* When Q[0:3] is 1111, CO will be 1; otherwise, CO will be 0
When GSR=0, CO=0, Q[0:3]=0 (D[0:3]=SP=CK=SD=CD=X)

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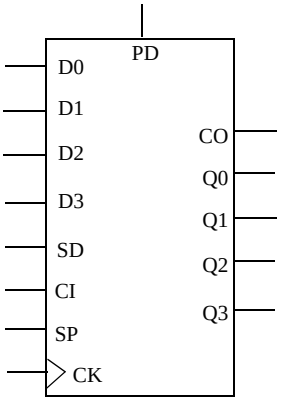
LU4P3JX

4 Bit Positive Edge Triggered Loadable Up-Counter with Positive Clock Enable and Positive Level Synchronous Preset (Preset overrides Enable)

ORCA Series		
2	3	4
	✓	✓



LU4P3JX

INPUTS: D0,D1,D2,D3,CI,SP,CK,SD,PD
OUTPUTS: CO,Q0,Q1,Q2,Q3
PINORDER: D0 D1 D2 D3 CI SP CK SD PD CO Q0 Q1 Q2 Q3
MINIMUM CELL AREA: 0.25

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Truth Table:

INPUTS						OUTPUTS	
D[0:3]	SD	CI	SP	CK	PD	CO	Q[0:3]
X	X	0	X	↑	1	0	1
X	X	1	X	↑	1	1	1
D[0:3]	1	0	1	↑	0	0	D[0:3]
D[0:3]	1	1	1	↑	0	*	D[0:3]
X	0	0	X	X	0	0	Q[0:3]
X	X	0	0	X	0	0	Q[0:3]
X	X	1	0	X	0	*	Q[0:3]
X	0	1	1	↑	0	*	count+1

X = Don’t care

* When Q[0:3] is 1111, CO will be 1; otherwise, CO will be 0
When GSR=0, CO=CI, Q[0:3]=1 (D[0:3]=SP=CK=SD=PD=X)

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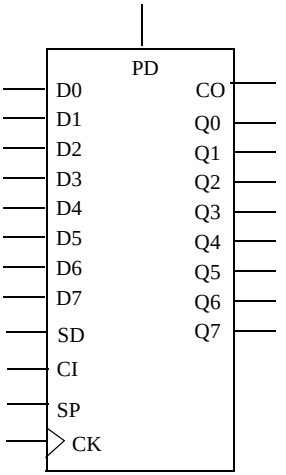
LU8P3BX

8 Bit Positive Edge Triggered Loadable Up-Counter with Positive Clock Enable and Positive Level Asynchronous Preset

ORCA Series		
2	3	4
	✓	✓



LU8P3BX

INPUTS: D0,D1,D2,D3,D4,D5,D6,D7,CI,SP,CK,SD,PD
OUTPUTS: CO,Q0,Q1,Q2,Q3,Q4,Q5,Q6,Q7
PINORDER: D0 D1 D2 D3 D4 D5 D6 D7 CI SP CK SD PD CO Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
MINIMUM CELL AREA: 0.5

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Truth Table:

INPUTS						OUTPUTS	
D[0:7]	SD	CI	SP	CK	PD	CO	Q[0:7]
X	X	0	X	X	1	0	1
X	X	1	X	X	1	1	1
D[0:7]	1	0	1	↑	0	0	D[0:7]
D[0:7]	1	1	1	↑	0	*	D[0:7]
X	0	0	X	X	0	0	Q[0:7]
X	X	0	0	X	0	0	Q[0:7]
X	X	1	0	X	0	*	Q[0:7]
X	0	1	1	↑	0	*	count+1

X = Don’t care

* When Q[0:7] is 11111111, CO will be 1; otherwise, CO will be 0
When GSR=0, CO=CI, Q[0:7]=1 (D[0:7]=SP=CK=SD=PD=X)

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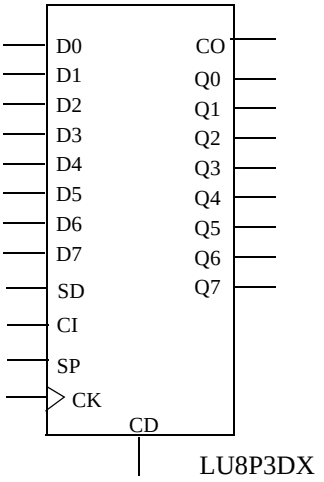
LU8P3DX

8 Bit Positive Edge Triggered Loadable Up-Counter with Positive Clock Enable and Positive Level Asynchronous Clear

ORCA Series		
2	3	4
	✓	✓



INPUTS: D0,D1,D2,D3,D4,D5,D6,D7,CI,SP,CK,SD,CD
OUTPUTS: CO,Q0,Q1,Q2,Q3,Q4,Q5,Q6,Q7
PINORDER: D0 D1 D2 D3 D4 D5 D6 D7 CI SP CK SD CD CO Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
MINIMUM CELL AREA: 0.5

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Truth Table:

INPUTS						OUTPUTS	
D[0:7]	SD	CI	SP	CK	CD	CO	Q[0:7]
X	X	X	X	X	1	0	0
D[0:7]	1	0	1	↑	0	0	D[0:7]
D[0:7]	1	1	1	↑	0	*	D[0:7]
X	0	0	X	X	0	0	Q[0:7]
X	X	0	0	X	0	0	Q[0:7]
X	X	1	0	X	0	*	Q[0:7]
X	0	1	1	↑	0	*	count+1

X = Don’t care

* When Q[0:7] is 11111111, CO will be 1; otherwise, CO will be 0
When GSR=0, CO=0, Q[0:7]=0 (D[0:7]=SP=CK=SD=CD=X)

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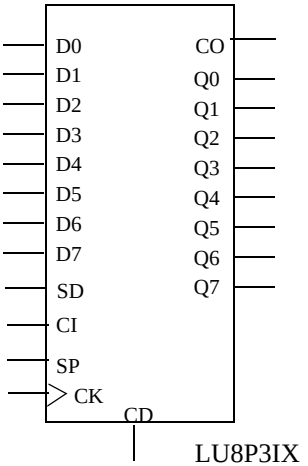
LU8P3IX

8 Bit Positive Edge Triggered Loadable Up-Counter with Positive Clock Enable and Positive Level Synchronous Clear (Clear overrides Enable)

ORCA Series		
2	3	4
	✓	✓



INPUTS: D0,D1,D2,D3,D4,D5,D6,D7,CI,SP,CK,SD,CD
OUTPUTS: CO,Q0,Q1,Q2,Q3,Q4,Q5,Q6,Q7
PINORDER: D0 D1 D2 D3 D4 D5 D6 D7 CI SP CK SD CD CO Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
MINIMUM CELL AREA: 0.5

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Truth Table:

INPUTS						OUTPUTS	
D[0:7]	SD	CI	SP	CK	CD	CO	Q[0:7]
X	X	X	X	↑	1	0	0
D[0:7]	1	0	1	↑	0	0	D[0:7]
D[0:7]	1	1	1	↑	0	*	D[0:7]
X	0	0	X	X	0	0	Q[0:7]
X	X	0	0	X	0	0	Q[0:7]
X	X	1	0	X	0	*	Q[0:7]
X	0	1	1	↑	0	*	count+1

X = Don’t care

* When Q[0:7] is 11111111, CO will be 1; otherwise, CO will be 0
When GSR=0, CO=0, Q[0:7]=0 (D[0:7]=SP=CK=SD=CD=X)

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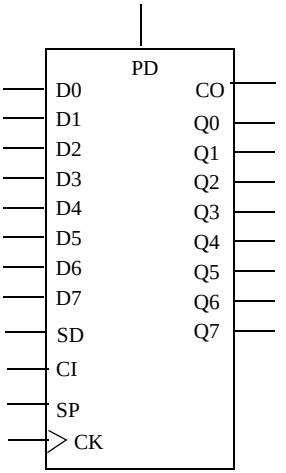
LU8P3JX

8 Bit Positive Edge Triggered Loadable Up-Counter with Positive Clock Enable and Positive Level Synchronous Preset (Preset overrides Enable)

ORCA Series		
2	3	4
	✓	✓



LU8P3JX

INPUTS: D0,D1,D2,D3,D4,D5,D6,D7,CI,SP,CK,SD,PD
OUTPUTS: CO,Q0,Q1,Q2,Q3,Q4,Q5,Q6,Q7
PINORDER: D0 D1 D2 D3 D4 D5 D6 D7 CI SP CK SD PD CO Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
MINIMUM CELL AREA: 0.25

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Truth Table:

INPUTS						OUTPUTS	
D[0:7]	SD	CI	SP	CK	PD	CO	Q[0:7]
X	X	0	X	↑	1	0	1
X	X	1	X	↑	1	1	1
D[0:7]	1	0	1	↑	0	0	D[0:7]
D[0:7]	1	1	1	↑	0	*	D[0:7]
X	0	0	X	X	0	0	Q[0:7]
X	X	0	0	X	0	0	Q[0:7]
X	X	1	0	X	0	*	Q[0:7]
X	0	1	1	↑	0	*	count+1

X = Don’t care

* When Q[0:7] is 11111111, CO will be 1; otherwise, CO will be 0
When GSR=0, CO=CI, Q[0:7]=1 (D[0:7]=SP=CK=SD=PD=X)

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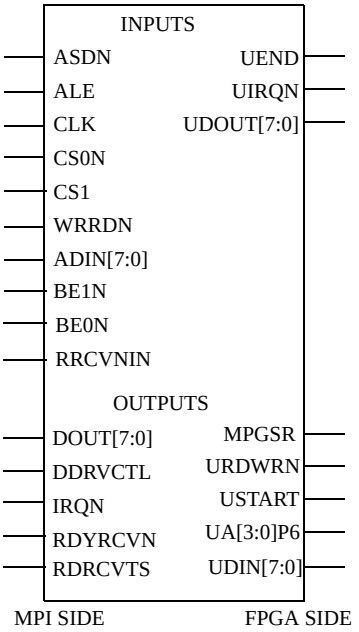
MPI960 Interface

8-Bit Interface to the Intel i960 Microprocessor

ORCA Series		
2	3	4
	✓	



i960 INTERFACE

Note: For Series 4 designs, this element is available only through the system bus (SYSBUS).

INPUTS: ADSN,ALE,CLK,CS0N,CS1,WRRDN,ADIN7,ADIN6,ADIN5,ADIN4, ADIN3,ADIN2,ADIN1,ADIN0,UEND,UIRQN,UDOUT7,UDOUT6, UDOUT5,UDOUT4,UDOUT3,UDOUT2,UDOUT1,UDOUT0
OUTPUTS: DOUT7,DOUT6,DOUT5,DOUT4,DOUT3,DOUT2,DOUT1,DOUT0, DDRVCTL,IRQN,RDYRCVN,RDRCVTS,MPGSR,URDWRN,USTART,UA3,UA2, UA1,UA0,UDIN7,UDIN6,UDIN5,UDIN4,UDIN3,UDIN2,UDIN1,UDIN0
PINORDER: ADSN ALE CLK CS0N CS1 WRRDN ADIN7 ADIN6 ADIN5 ADIN4 ADIN3 ADIN2 ADIN1 ADIN0 UEND UIRQN UDOUT7 UDOUT6 UDOUT5 UDOUT4 UDOUT3 UDOUT2 UDOUT1 UDOUT0 DOUT7 DOUT6 DOUT5 DOUT4 DOUT3 DOUT2 DOUT1 DOUT0 DDRVCTL IRQN RDYRCVN RDRCVTS MPGSR URDWRN USTART UA3 UA2 UA1 UA0 UDIN7 UDIN6 UDIN5 UDIN4 UDIN3 UDIN2 UDIN1 UDIN0
MINIMUM MINIMUM CELL AREA: 0

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Description:

The MPI960 cell is an 8-bit interface to the Intel i960 microprocessor.

For the Series 3 architecture, through the Microprocessor Interface cells, a direct connection is provided between the FPGA and the microprocessor with minimal amount of glue logic. The FPGA is treated as a peripheral device, and it presents a consistent interface to the microprocessor. The addition of a set of registers provides new features and detailed information on the configuration logic. User applications can also use the interface to communicate with the microprocessor after configuration is completed.

The Microprocessor Interface supports the following four system registers:

- Configuration Control Register I (read/write)
- Configuration Control Register II (read/write)
- Configuration Test/Scratch Register (read/write)
- Configuration Status Register (read-only)

> ***Note***: The i906 Interface element should be instantiated through SCUBA. Refer to the appropriate topic in the online help system for details.

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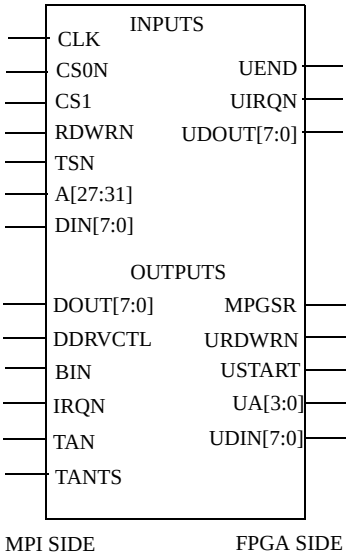
MPIPPC Interface

8-bit Interface to the PowerPC Microprocessor

ORCA Series		
2	3	4
	✓	



PowerPC INTERFACE

Note: For Series 4 designs, this element is available only through the system bus (SYSBUS).

INPUTS: CLK,CS0N,CS1,RDWRN,TSN,A27,A28,A29,A30,A31,DIN7,DIN6,DIN5, DIN4,DIN3,DIN2,DIN1,DIN0,UEND,UIRQN,UDOUT7,UDOUT6, UDOUT5,UDOUT4,UDOUT3,UDOUT2,UDOUT1,UDOUT0
OUTPUTS: DOUT7,DOUT6,DOUT5,DOUT4,DOUT3,DOUT2,DOUT1,DOUT0, DDRVCTL,BIN,IRQN,TAN,TANTS,MPGSR,URDWRN,USTART,UA3,UA2, UA1,UA0,UDIN7,UDIN6,UDIN5,UDIN4,UDIN3,UDIN2,UDIN1,UDIN0
PINORDER: CLK CS0N CS1 RDWRN TSN A27 A28 A29 A30 A31 DIN7 DIN6 DIN5 DIN4 DIN3 DIN2 DIN1 DIN0 UEND UIRQN UDOUT7 UDOUT6 UDOUT5 UDOUT4 UDOUT3 UDOUT2 UDOUT1 UDOUT0 DOUT7 DOUT6 DOUT5 DOUT4 DOUT3 DOUT2 DOUT1 DOUT0 DDRVCTL BIN IRQN TAN TANTS MPGSR URDWRN USTART UA3 UA2 UA1 UA0 UDIN7 UDIN6 UDIN5 UDIN4 UDIN3 UDIN2 UDIN1 UDIN0
MINIMUM MINIMUM CELL AREA: 0

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Description:

The MPIPPC cell is an 8-bit interface to the Motorola PowerPC microprocessor.

For the Series 3 architecture, through the Microprocessor Interface cells, a direct connection is provided between the FPGA and the microprocessor with minimal amount of glue logic. The FPGA is treated as a peripheral device, and it presents a consistent interface to the microprocessor. The addition of a set of registers provides new features and detailed information on the configuration logic. User applications can also use the interface to communicate with the microprocessor after configuration is completed.

The Microprocessor Interface supports the following four system registers:

- Configuration Control Register I (read/write)
- Configuration Control Register II (read/write)
- Configuration Test/Scratch Register (read/write)
- Configuration Status Register (read-only)

Note: The PowerPC Interface element should be instantiated through SCUBA. Refer to the appropriate topic in the online help system for details.

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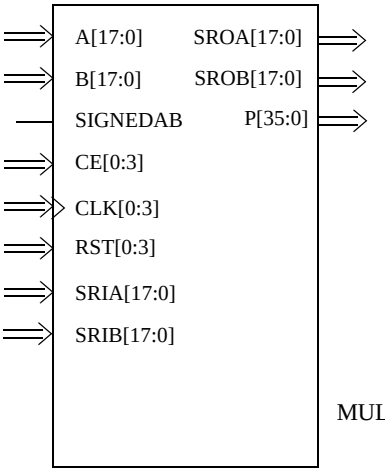
MULT18X18

ECP DSP Multiplier

Lattice FPGA		
XP	EC	ECP
		✓



MULT18X18

NOTE: The graphic is shown in bus notation for convenience. This element must be instantiated in expanded bus notation format with each individual bit as given below.

INPUTS: A17, A16, A15, A14, A13, A12, A11, A10, A9, A8, A7, A6, A5, A4, A3, A2, A1, A0, B17, B16, B15, B14, B13, B12, B11, B10, B9, B8, B7, B6, B5, B4, B3, B2, B1, B0, SIGNEDAB, CE0, CE1, CE2, CE3, CLK0, CLK1, CLK2, CLK3, RST0, RST1, RST2, RST3, SRIA17, SRIA16, SRIA15, SRIA14, SRIA13, SRIA12, SRIA11, SRIA10, SRIA9, SRIA8, SRIA7, SRIA6, SRIA5, SRIA4, SRIA3, SRIA2, SRIA1, SRIA0, SRIB17, SRIB16, SRIB15, SRIB14, SRIB13, SRIB12, SRIB11, SRIB10, SRIB9, SRIB8, SRIB7, SRIB6, SRIB5, SRIB4, SRIB3, SRIB2, SRIB1, SRIB0

OUTPUTS: SROA17, SROA16, SROA15, SROA14, SROA13, SROA12, SROA11, SROA10, SROA9, SROA8, SROA7, SROA6, SROA5, SROA4, SROA3, SROA2, SROA1, SROA0, SROB17, SROB16, SROB15, SROB14, SROB13, SROB12, SROB11, SROB10, SROB9, SROB8, SROB7, SROB6, SROB5, SROB4, SROB3, SROB2, SROB1, SROB0, P35, P34, P33, P32, P31, P30, P29, P28, P27, P26, P25, P24, P23, P22, P21, P20, P19, P18, P17, P16, P15, P14, P13, P12, P11, P10, P9, P8, P7, P6, P5, P4, P3, P2, P1, P0

PINORDER: A17, A16, A15, A14, A13, A12, A11, A10, A9, A8, A7, A6, A5, A4, A3, A2, A1, A0, B17, B16, B15, B14, B13, B12, B11, B10, B9, B8, B7, B6, B5, B4, B3, B2, B1, B0, SIGNEDAB, CE0, CE1, CE2, CE3, CLK0, CLK1, CLK2, CLK3, RST0, RST1, RST2, RST3, SRIA17, SRIA16, SRIA15, SRIA14, SRIA13, SRIA12, SRIA11, SRIA10, SRIA9, SRIA8, SRIA7, SRIA6, SRIA5, SRIA4, SRIA3, SRIA2, SRIA1, SRIA0, SRIB17, SRIB16, SRIB15, SRIB14, SRIB13, SRIB12, SRIB11, SRIB10, SRIB9, SRIB8, SRIB7, SRIB6, SRIB5, SRIB4, SRIB3, SRIB2, SRIB1, SRIB0, SROA17, SROA16, SROA15, SROA14, SROA13, SROA12, SROA11, SROA10, SROA9, SROA8, SROA7, SROA6, SROA5, SROA4, SROA3, SROA2, SROA1, SROA0, SROB17, SROB16, SROB15, SROB14, SROB13, SROB12, SROB11, SROB10,

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SROB9, SROB8, SROB7, SROB6, SROB5, SROB4, SROB3, SROB2, SROB1, SROB0, P35, P34, P33, P32, P31, P30, P29, P28, P27, P26, P25, P24, P23, P22, P21, P20, P19, P18, P17, P16, P15, P14, P13, P12, P11, P10, P9, P8, P7, P6, P5, P4, P3, P2, P1, P0

ATTRIBUTES:
REG_INPUTA_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_INPUTA_CE: "CE0", "CE1", "CE2", "CE3"
REG_INPUTA_RST: "RST0", "RST1", "RST2", "RST3"
REG_INPUTB_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_INPUTB_CE: "CE0", "CE1", "CE2", "CE3"
REG_INPUTB_RST: "RST0", "RST1", "RST2", "RST3"
REG_PIPELINE_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_PIPELINE_CE: "CE0", "CE1", "CE1", "CE3"
REG_PIPELINE_RST: "RST0", "RST1", "RST2", "RST3"
REG_OUTPUT_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_OUTPUT_CE: "CE0", "CE1", "CE2", "CE3"
REG_OUTPUT_RST: "RST0", "RST1", "RST2", "RST3"
REG_SIGNEDAB_0_CLK: "CLK0", "CLK0", "CLK0", "CLK0", "NONE"
REG_SIGNEDAB_0_CE: "CE0", "CE1", "CE2", "CE3"
REG_SIGNEDAB_0_RST: "RST0", "RST1", "RST2", "RST3"
REG_SIGNEDAB_1_CLK: "CLK0", "CLK0", "CLK0", "CLK0", "NONE"
REG_SIGNEDAB_1_CE: "CE0", "CE1", "CE2", "CE3"
REG_SIGNEDAB_1_RST: "RST0", "RST1", "RST2", "RST3"
SHIFT_IN_A: "FALSE", "TRUE"
SHIFT_IN_B: "FALSE", "TRUE"
GSR: "ENABLED", "DISABLED"

Description:

LatticeECP-DSP Block Multiplier. MULT18X18 is a combinational signed 18-bit by 18-bit multiplier used in the DSP block. The value represented in the 18-bit input A is multiplied by the value represented in the 18-bit input B. Output P is the 36-bit product of A and B. MULT18X18 may be represented as either unsigned or two’s complement signed. The element consists of three types of optional pipeline registers:

- Input registers, located before the multipliers and registering the operands
- Multiplier pipeline registers, located after the multipliers and product registration
- Output registers, located before leaving the block, and registering the mode-specific output.

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There are 12 register controls signals that enter the DSP block: CLK[0:3], CE0[0:3], and RST[0:3]. Each incoming signal also has the option of being tied high, tied low, or inverted. These 12 control signals are used to control the register banks in the DSP block. Dynamic control signals must match the register pipelining of the datapath. To facilitate this, the following bank control for each individual dynamic signal's input register and pipeline register (total 8 signals x 2 registers / signal = 16 registers) is as follows:

- Bypass or no-bypass of the registers.
- Clock is selected from CLK[0:3], one of four sources available to the DSP block.
- Clock enable is selected from CE0[0:3], one of four sources available to the DSP block.
- Reset is selected from RST[0:3], one of four sources available to the DSP block.

You can turn registers off or on via attribute settings. For example, setting REG_INPUTA_CLK= "CLK0" means the input A register is used, and the clock drive A register is coming from CLK0 of the DSP block. Setting REG_INPUTA_CE= "CE1" means input A register CE control is coming from CE1 of the DSP block. Setting REG_INPUTA_RST= "RST3" means input A register reset control is coming from RST3 of the DSP block. If REG_INPUT_A_CLK="NONE", this means the input A register is bypassed, therefore, REG_INPUT_A_RST or REG_INPUT_A_CE becomes irrelevent.

In case you want to use the register but do not care about the clock enable (CE), then this pin needs to be tied to VCC (always enabled). In this case you could set REG_INPUT_A_CE="CE3", then tie CE3 of the to VCC. If you want to use the register but do not care about the reset (RST), then this pin must to be tied to GND (always do not reset). In this case, you you could set REG_INPUT_A_RST="RST2", then tie RST2 of the to GND.

SIGNEDAB is a pin which controls whether the multiplier performs the signed or unsigned operation. It applied to both operand A and B. It can be tied to VCC (signed) or GROUND (unsigned). There are also two delay registers associated with this control pin, in order to match with incoming data. Setting REG_SIGNEDAB_0_CLK= "CLK0 | CLK1 | CLK2 | CLK3"will turn on the pipeline register for SIGNEDAB. Setting REG_SIGNEDAB_0_CLK= "NONE" will turn off the first pipeline register for SIGNEDAB. Setting REG_SIGNEDAB_1_CLK= "NONE"will turn off the second pipeline register for SIGNEDAB.

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Input registers receive operand values from a serial shift chain or routing input. There is separate control for A and B operands. When in shift chain mode, multiplier operands may be bypassed using the bank bypass feature. The shift chain supports one chain of two 18-bit operands or two chains of two 9-bit operands. GSR “DISABLED” attribute disables the asynchronous global set reset input when in user mode.

MULT18X18 pin functions:

Function	Pins
input data A and B	A[17:0], B[17:0]0
signed input	SIGNEDAB
clock enable	CE[0:3]
clock input	CLK[0:3]
reset	RST[0:3]
shifted input A and B (from previous stage)	SRIA[17:0], SRIB[17:0]
shifted output A and B (from previous stage)	SROA[17:0], SROB[17:0]
output product data	P[35:0]

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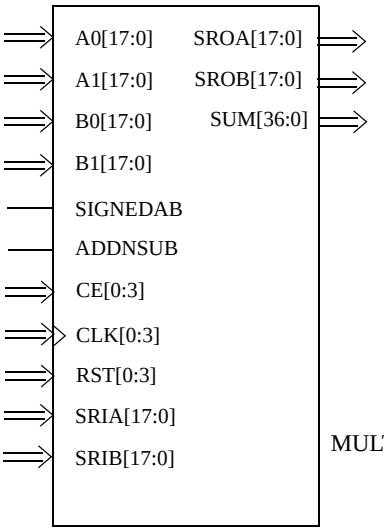
MULT18X18ADDSUB

ECP DSP Adder/Subtractor

Lattice FPGA		
XP	EC	ECP
		✓



MULT18X18ADDSUB

NOTE: The graphic is shown in bus notation for convenience. This element must be instantiated in expanded bus notation format with each individual bit as given below.

INPUTS: A017, A016, A015, A014, A013, A012, A011, A010, A09, A08, A07, A06, A05, A04, A03, A02, A01, A00, A117, A116, A115, A114, A113, A112, A111, A110, A19, A18, A17, A16, A15, A14, A13, A12, A11, A10, B017, B016, B015, B014, B013, B012, B011, B010, B09, B08, B07, B06, B05, B04, B03, B02, B01, B00, B117, B116, B115, B114, B113, B112, B111, B110, B19, B18, B17, B16, B15, B14, B13, B12, B11, B10, SIGNEDAB, ADDNSUB, CE0, CE1, CE2, CE3, CLK0, CLK1, CLK2, CLK3, RST0, RST1, RST2, RST3, SRIA17, SRIA16, SRIA15, SRIA14, SRIA13, SRIA12, SRIA11, SRIA10, SRIA9, SRIA8, SRIA7, SRIA6, SRIA5, SRIA4, SRIA3, SRIA2, SRIA1, SRIA0, SRIB17, SRIB16, SRIB15, SRIB14, SRIB13, SRIB12, SRIB11, SRIB10, SRIB9, SRIB8, SRIB7, SRIB6, SRIB5, SRIB4, SRIB3, SRIB2, SRIB1, SRIB0

OUTPUTS: SROA17, SROA16, SROA15, SROA14, SROA13, SROA12, SROA11, SROA10, SROA9, SROA8, SROA7, SROA6, SROA5, SROA4, SROA3, SROA2, SROA1, SROA0, SROB17, SROB16, SROB15, SROB14, SROB13, SROB12, SROB11, SROB10, SROB9, SROB8, SROB7, SROB6, SROB5, SROB4, SROB3, SROB2, SROB1, SROB0, SUM36, SUM35, SUM34, SUM33, SUM32, SUM31, SUM30, SUM29, SUM28, SUM27, SUM26, SUM25, SUM24, SUM23, SUM22, SUM21, SUM20, SUM19, SUM18, SUM17, SUM16, SUM15, SUM14, SUM13, SUM12, SUM11, SUM10, SUM9, SUM8, SUM7, SUM6, SUM5, SUM4, SUM3, SUM2, SUM1, SUM0

PINORDER: A017, A016, A015, A014, A013, A012, A011, A010, A09, A08, A07, A06, A05, A04, A03, A02, A01, A00, A117, A116, A115, A114, A113, A112, A111, A110, A19, A18, A17, A16, A15, A14, A13, A12, A11, A10, B017, B016, B015, B014, B013, B012,

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B011, B010, B09, B08, B07, B06, B05, B04, B03, B02, B01, B00, B117, B116, B115, B114, B113, B112, B111, B110, B19, B18, B17, B16, B15, B14, B13, B12, B11, B10, SIGNEDAB, ADDNSUB, CE0, CE1, CE2, CE3, CLK0, CLK1, CLK2, CLK3, RST0, RST1, RST2, RST3, SRIA17, SRIA16, SRIA15, SRIA14, SRIA13, SRIA12, SRIA11, SRIA10, SRIA9, SRIA8, SRIA7, SRIA6, SRIA5, SRIA4, SRIA3, SRIA2, SRIA1, SRIA0, SRIB17, SRIB16, SRIB15, SRIB14, SRIB13, SRIB12, SRIB11, SRIB10, SRIB9, SRIB8, SRIB7, SRIB6, SRIB5, SRIB4, SRIB3, SRIB2, SRIB1, SRIB0, SROA17, SROA16, SROA15, SROA14, SROA13, SROA12, SROA11, SROA10, SROA9, SROA8, SROA7, SROA6, SROA5, SROA4, SROA3, SROA2, SROA1, SROA0, SROB17, SROB16, SROB15, SROB14, SROB13, SROB12, SROB11, SROB10, SROB9, SROB8, SROB7, SROB6, SROB5, SROB4, SROB3, SROB2, SROB1, SROB0, SUM36, SUM35, SUM34, SUM33, SUM32, SUM31, SUM30, SUM29, SUM28, SUM27, SUM26, SUM25, SUM24, SUM23, SUM22, SUM21, SUM20, SUM19, SUM18, SUM17, SUM16, SUM15, SUM14, SUM13, SUM12, SUM11, SUM10, SUM9, SUM8, SUM7, SUM6, SUM5, SUM4, SUM3, SUM2, SUM1, SUM0

ATTRIBUTES:

REG_INPUTA0_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_INPUTA0_CE: "CE0", "CE1", "CE2", "CE3"
REG_INPUTA0_RST: "RST0", "RST1", "RST2", "RST3"
REG_INPUTA1_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_INPUTA1_CE: "CE0", "CE1", "CE2", "CE3"
REG_INPUTA1_RST: "RST0", "RST1", "RST2", "RST3"
REG_INPUTB01_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE”
REG_INPUTB0_CE: "CE0", "CE1", "CE2", "CE3"
REG_INPUTB0_RST: "RST0", "RST1", "RST2", "RST3"
REG_INPUTB1_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE”
REG_INPUTB1_CE: "CE0", "CE1", "CE2", "CE3"
REG_INPUTB1_RST: "RST0", "RST1", "RST2", "RST3"
REG_PIPELINE_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_PIPELINE_CE: "CE0", "CE1", "CE1", "CE3"
REG_PIPELINE_RST: "RST0", "RST1", "RST2", "RST3"
REG_OUTPUT_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_OUTPUT_CE: "CE0", "CE1", "CE2", "CE3"
REG_OUTPUT_RST: "RST0", "RST1", "RST2", "RST3"
REG_SIGNEDAB_0_CLK: "CLK0", "CLK0", "CLK0", "CLK0", "NONE"
REG_SIGNEDAB_0_CE: "CE0", "CE1", "CE2", "CE3"
REG_SIGNEDAB_0_RST: "RST0", "RST1", "RST2", "RST3"
REG_SIGNEDAB_1_CLK: "CLK0", "CLK0", "CLK0", "CLK0", "NONE"
REG_SIGNEDAB_1_CE: "CE0", "CE1", "CE2", "CE3"
REG_SIGNEDAB_1_RST: "RST0", "RST1", "RST2", "RST3"
REG_ADDNSUB_0_CLK: "CLK0", "CLK0", "CLK0", "CLK0", "NONE"
REG_ADDNSUB_0_CE: "CE0", "CE1", "CE2", "CE3"
REG_ADDNSUB_0_RST: "RST0", "RST1", "RST2", "RST3"
REG_ADDNSUB_1_CLK: "CLK0", "CLK0", "CLK0", "CLK0", "NONE"

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REG_ADDNSUB_1_CE: "CE0", "CE1", "CE2", "CE3"
REG_ADDNSUB_1_RST: "RST0", "RST1", "RST2", "RST3"
SHIFT_IN_A0: "TRUE", "FALSE"
SHIFT_IN_B0: "TRUE", "FALSE"
SHIFT_IN_A1: "TRUE", "FALSE"
SHIFT_IN_B1: "TRUE", "FALSE"
GSR: "ENABLED", "DISABLED"

Description:

LatticeECP-DSP Block Adder/Subtractor. MULT18X18ADDSUB can be configured to either add or subtract its inputs, adding or subtracting the inputs from two multiplier products. The add/subtract control is either configured as a static HIGH (Vcc), LOW (GND). In ispLEVER, the static settings are implemented by setting Vcc or GND in the CIB ISB.

The element consists of three types of optional pipeline registers:

- Input registers, located before the multipliers and registering the operands
- Multiplier pipeline registers, located after the multipliers and product registration
- Output registers, located before leaving the block, and registering the mode-specific output.

See the description of MULT18X18 for more information on control signals for DSP blocks and attributes.

MULT18X18ADDSUB pin functions:

Function	Pins
input data A and B	A0|1[17:0], B0|1[17:0]
signed input (0 = unsigned, 1 = signed)	SIGNEDAB
add/subtract (0 = add, 1 = subtract)	ADDNSUB
clock enable	CE[0:3]
clock input	CLK[0:3]

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reset	RST[0:3]
shifted input A and B (from previous stage)	SRIA[17:0], SRIB[17:0]
shifted output A and B (from previous stage)	SROA[17:0], SROB[17:0]
output product sum data	SUM[36:0]

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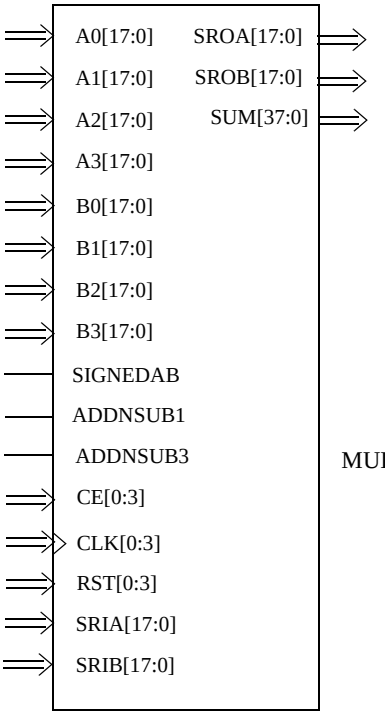
MULT18X18ADDSUBSUM

ECP DSP Adder/Subtractor/Sum

Lattice FPGA		
XP	EC	ECP
		✓



NOTE: The graphic is shown in bus notation for convenience. This element must be instantiated in expanded bus notation format with each individual bit as given below.

INPUTS: A017, A016, A015, A014, A013, A012, A011, A010, A09, A08, A07, A06, A05, A04, A03, A02, A01, A00, A117, A116, A115, A114, A113, A112, A111, A110, A19, A18, A17, A16, A15, A14, A13, A12, A11, A10, A217, A216, A215, A214, A213, A212, A211, A210, A29, A28, A27, A26, A25, A24, A23, A22, A21, A20, A317, A316, A315, A314, A313, A312, A311, A310, A39, A38, A37, A36, A35, A34, A33, A32, A31, A30, B017, B016, B015, B014, B013, B012, B011, B010, B09, B08, B07, B06, B05, B04, B03, B02, B01, B00, B117, B116, B115, B114, B113, B112, B111, B110, B19, B18, B17, B16, B15, B14, B13, B12, B11, B10, B217, B216, B215, B214, B213, B212, B211, B210, B29, B28, B27, B26, B25, B24, B23, B22, B21, B20, B317, B316, B315, B314, B313, B312, B311, B310, B39, B38, B37, B36, B35, B34, B33, B32, B31, B30, SIGNEDAB, ADDNSUB1, ADDNSUB3, CE0, CE1, CE2, CE3, CLK0, CLK1, CLK2, CLK3, RST0, RST1, RST2, RST3, SRIA17, SRIA16, SRIA15, SRIA14, SRIA13, SRIA12, SRIA11, SRIA10, SRIA9, SRIA8, SRIA7, SRIA6, SRIA5, SRIA4, SRIA3, SRIA2, SRIA1, SRIA0, SRIB17, SRIB16, SRIB15, SRIB14, SRIB13, SRIB12, SRIB11, SRIB10, SRIB9, SRIB8, SRIB7, SRIB6, SRIB5, SRIB4, SRIB3,

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SRIB2, SRIB1, SRIB0
OUTPUTS: SROA17, SROA16, SROA15, SROA14, SROA13, SROA12, SROA11, SROA10, SROA9, SROA8, SROA7, SROA6, SROA5, SROA4, SROA3, SROA2, SROA1, SROA0, SROB17, SROB16, SROB15, SROB14, SROB13, SROB12, SROB11, SROB10, SROB9, SROB8, SROB7, SROB6, SROB5, SROB4, SROB3, SROB2, SROB1, SROB0, SUM37, SUM36, SUM35, SUM34, SUM33, SUM32, SUM31, SUM30, SUM29, SUM28, SUM27, SUM26, SUM25, SUM24, SUM23, SUM22, SUM21, SUM20, SUM19, SUM18, SUM17, SUM16, SUM15, SUM14, SUM13, SUM12, SUM11, SUM10, SUM9, SUM8, SUM7, SUM6, SUM5, SUM4, SUM3, SUM2, SUM1, SUM0
PINORDER: A017, A016, A015, A014, A013, A012, A011, A010, A09, A08, A07, A06, A05, A04, A03, A02, A01, A00, A117, A116, A115, A114, A113, A112, A111, A110, A19, A18, A17, A16, A15, A14, A13, A12, A11, A10, A217, A216, A215, A214, A213, A212, A211, A210, A29, A28, A27, A26, A25, A24, A23, A22, A21, A20, A317, A316, A315, A314, A313, A312, A311, A310, A39, A38, A37, A36, A35, A34, A33, A32, A31, A30, B017, B016, B015, B014, B013, B012, B011, B010, B09, B08, B07, B06, B05, B04, B03, B02, B01, B00, B117, B116, B115, B114, B113, B112, B111, B110, B19, B18, B17, B16, B15, B14, B13, B12, B11, B10, B217, B216, B215, B214, B213, B212, B211, B210, B29, B28, B27, B26, B25, B24, B23, B22, B21, B20, B317, B316, B315, B314, B313, B312, B311, B310, B39, B38, B37, B36, B35, B34, B33, B32, B31, B30, SIGNEDAB, ADDNSUB1, ADDNSUB3, CE0, CE1, CE2, CE3, CLK0, CLK1, CLK2, CLK3, RST0, RST1, RST2, RST3, SRIA17, SRIA16, SRIA15, SRIA14, SRIA13, SRIA12, SRIA11, SRIA10, SRIA9, SRIA8, SRIA7, SRIA6, SRIA5, SRIA4, SRIA3, SRIA2, SRIA1, SRIA0, SRIB17, SRIB16, SRIB15, SRIB14, SRIB13, SRIB12, SRIB11, SRIB10, SRIB9, SRIB8, SRIB7, SRIB6, SRIB5, SRIB4, SRIB3, SRIB2, SRIB1, SRIB0, SROA17, SROA16, SROA15, SROA14, SROA13, SROA12, SROA11, SROA10, SROA9, SROA8, SROA7, SROA6, SROA5, SROA4, SROA3, SROA2, SROA1, SROA0, SROB17, SROB16, SROB15, SROB14, SROB13, SROB12, SROB11, SROB10, SROB9, SROB8, SROB7, SROB6, SROB5, SROB4, SROB3, SROB2, SROB1, SROB0, SUM37, SUM36, SUM35, SUM34, SUM33, SUM32, SUM31, SUM30, SUM29, SUM28, SUM27, SUM26, SUM25, SUM24, SUM23, SUM22, SUM21, SUM20, SUM19, SUM18, SUM17, SUM16, SUM15, SUM14, SUM13, SUM12, SUM11, SUM10, SUM9, SUM8, SUM7, SUM6, SUM5, SUM4, SUM3, SUM2, SUM1, SUM0
ATTRIBUTES:
REG_INPUTA0_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_INPUTA0_CE: "CE0", "CE1", "CE2", "CE3"
REG_INPUTA0_RST: "RST0", "RST1", "RST2", "RST3"
REG_INPUTA1_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_INPUTA1_CE: "CE0", "CE1", "CE2", "CE3"
REG_INPUTA1_RST: "RST0", "RST1", "RST2", "RST3"
REG_INPUTA2_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_INPUTA2_CE: "CE0", "CE1", "CE2", "CE3"
REG_INPUTA2_RST: "RST0", "RST1", "RST2", "RST3"
REG_INPUTA3_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"

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REG_INPUTA3_CE: "CE0", "CE1", "CE2", "CE3"
REG_INPUTA3_RST: "RST0", "RST1", "RST2", "RST3"
REG_INPUTB0_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_INPUTB0_CE: "CE0", "CE1", "CE2", "CE3"
REG_INPUTB0_RST: "RST0", "RST1", "RST2", "RST3"
REG_INPUTB1_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_INPUTB1_CE: "CE0", "CE1", "CE2", "CE3"
REG_INPUTB1_RST: "RST0", "RST1", "RST2", "RST3"
REG_INPUTB2_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_INPUTB2_CE: "CE0", "CE1", "CE2", "CE3"
REG_INPUTB2_RST: "RST0", "RST1", "RST2", "RST3"
REG_INPUTB3_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_INPUTB3_CE: "CE0", "CE1", "CE2", "CE3"
REG_INPUTB3_RST: "RST0", "RST1", "RST2", "RST3"
REG_PIPELINE0_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_PIPELINE0_CE: "CE0", "CE1", "CE1", "CE3"
REG_PIPELINE0_RST: "RST0", "RST1", "RST2", "RST3"
REG_PIPELINE1_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_PIPELINE1_CE: "CE0", "CE1", "CE1", "CE3"
REG_PIPELINE1_RST: "RST0", "RST1", "RST2", "RST3"
REG_OUTPUT_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_OUTPUT_CE: "CE0", "CE1", "CE2", "CE3"
REG_OUTPUT_RST: "RST0", "RST1", "RST2", "RST3"
REG_SIGNEDAB_0_CLK: "CLK0", "CLK0", "CLK0", "CLK0", "NONE"
REG_SIGNEDAB_0_CE: "CE0", "CE1", "CE2", "CE3"
REG_SIGNEDAB_0_RST: "RST0", "RST1", "RST2", "RST3"
REG_SIGNEDAB_1_CLK: "CLK0", "CLK0", "CLK0", "CLK0", "NONE"
REG_SIGNEDAB_1_CE: "CE0", "CE1", "CE2", "CE3"
REG_SIGNEDAB_1_RST: "RST0", "RST1", "RST2", "RST3"
REG_ADDNSUB1_0_CLK: "CLK0", "CLK0", "CLK0", "CLK0", "NONE"
REG_ADDNSUB1_0_CE: "CE0", "CE1", "CE2", "CE3"
REG_ADDNSUB1_0_RST: "RST0", "RST1", "RST2", "RST3"
REG_ADDNSUB1_1_CLK: "CLK0", "CLK0", "CLK0", "CLK0", "NONE"
REG_ADDNSUB1_1_CE: "CE0", "CE1", "CE2", "CE3"
REG_ADDNSUB1_1_RST: "RST0", "RST1", "RST2", "RST3"
REG_ADDNSUB3_0_CLK: "CLK0", "CLK0", "CLK0", "CLK0", "NONE"
REG_ADDNSUB3_0_CE: "CE0", "CE1", "CE2", "CE3"
REG_ADDNSUB3_0_RST: "RST0", "RST1", "RST2", "RST3"
REG_ADDNSUB3_1_CLK: "CLK0", "CLK0", "CLK0", "CLK0", "NONE"
REG_ADDNSUB3_1_CE: "CE0", "CE1", "CE2", "CE3"
REG_ADDNSUB3_1_RST: "RST0", "RST1", "RST2", "RST3"
SHIFT_IN_A0: "TRUE", "FALSE"
SHIFT_IN_B0: "TRUE", "FALSE"
SHIFT_IN_A1: "TRUE", "FALSE"
SHIFT_IN_B1: "TRUE", "FALSE"

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SHIFT_IN_A2: "TRUE", "FALSE"
SHIFT_IN_B2: "TRUE", "FALSE"
SHIFT_IN_A3: "TRUE", "FALSE"
SHIFT_IN_B3: "TRUE", "FALSE"
GSR: "ENABLED", "DISABLED"

Description:

LatticeECP-DSP Block Adder/Subtractor. MULT18X18ADDSUBSUM can be configured to either add or subtract its inputs, adding or subtracting the inputs from two multiplier products. The add/subtract control is either configured as a static HIGH (Vcc), LOW (GND), or as dynamic control signals ADDNSUB1 and ADDNSUB3. In ispLEVER, the static settings are implemented by setting ADDNSUB1 and ADDNSUB3 signal to Vcc or GND in the CIB ISB.

The element consists of three types of optional pipeline registers:

- Input registers, located before the multipliers and registering the operands
- Multiplier pipeline registers, located after the multipliers and product registration
- Output registers, located before leaving the block, and registering the mode-specific output.

See the description of MULT18X18 for more information on control signals for DSP blocks and attributes.

MULT18X18ADDSUBSUM pin functions:

Function	Pins
input data A and B	A0|1|2|3[17:0], B0|1|2|3[17:0]
signed input (0 = unsigned, 1 = signed)	SIGNEDAB
add/subtract (0 = add, 1 = subtract)	ADDNSUB1, ADDNSUB3
clock enable	CE[0:3]
clock input	CLK[0:3]

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reset	RST[0:3]
shifted input A and B (from previous stage)	SRIA[17:0], SRIB[17:0]
shifted output A and B (from previous stage)	SROA[17:0], SROB[17:0]
output product sum data	SUM[37:0]

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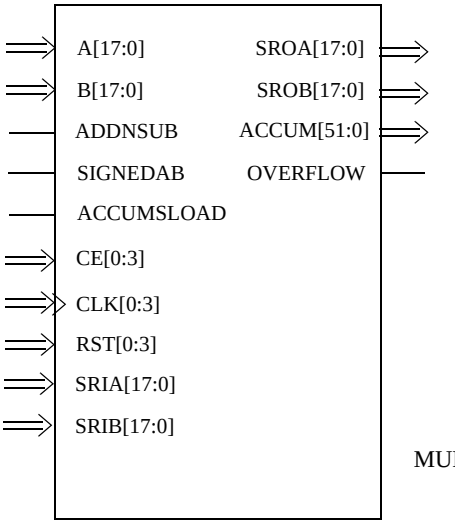
MULT18X18MAC

ECP DSP Multiplier

Lattice FPGA		
XP	EC	ECP
		✓



MULT18X18MAC

NOTE: The graphic is shown in bus notation for convenience. This element must be instantiated in expanded bus notation format with each individual bit as given below.

INPUTS: A17, A16, A15, A14, A13, A12, A11, A10, A9, A8, A7, A6, A5, A4, A3, A2, A1, A0, B17, B16, B15, B14, B13, B12, B11, B10, B9, B8, B7, B6, B5, B4, B3, B2, B1, B0, ADDNSUB, SIGNEDAB, ACCUMSLOAD, CE0, CE1, CE2, CE3, CLK0, CLK1, CLK2, CLK3, RST0, RST1, RST2, RST3, SRIA17, SRIA16, SRIA15, SRIA14, SRIA13, SRIA12, SRIA11, SRIA10, SRIA9, SRIA8, SRIA7, SRIA6, SRIA5, SRIA4, SRIA3, SRIA2, SRIA1, SRIA0, SRIB17, SRIB16, SRIB15, SRIB14, SRIB13, SRIB12, SRIB11, SRIB10, SRIB9, SRIB8, SRIB7, SRIB6, SRIB5, SRIB4, SRIB3, SRIB2, SRIB1, SRIB0

OUTPUTS: SROA17, SROA16, SROA15, SROA14, SROA13, SROA12, SROA11, SROA10, SROA9, SROA8, SROA7, SROA6, SROA5, SROA4, SROA3, SROA2, SROA1, SROA0, SROB17, SROB16, SROB15, SROB14, SROB13, SROB12, SROB11, SROB10, SROB9, SROB8, SROB7, SROB6, SROB5, SROB4, SROB3, SROB2, SROB1, SROB0, ACCUM51, ACCUM50, ACCUM49, ACCUM48, ACCUM47, ACCUM46, ACCUM45, ACCUM44, ACCUM43, ACCUM42, ACCUM41, ACCUM40, ACCUM39, ACCUM38, ACCUM37, ACCUM36, ACCUM35, ACCUM34, ACCUM33, ACCUM32, ACCUM31, ACCUM30, ACCUM29, ACCUM28, ACCUM27, ACCUM26, ACCUM25, ACCUM24, ACCUM23, ACCUM22, ACCUM21, ACCUM20, ACCUM19, ACCUM18, ACCUM17, ACCUM16, ACCUM15, ACCUM14, ACCUM13, ACCUM12, ACCUM11, ACCUM10, ACCUM9, ACCUM8, ACCUM7, ACCUM6, ACCUM5, ACCUM4, ACCUM3, ACCUM2, ACCUM1, ACCUM0, OVERFLOW

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PINORDER: A17, A16, A15, A14, A13, A12, A11, A10, A9, A8, A7, A6, A5, A4, A3, A2, A1, A0, B17, B16, B15, B14, B13, B12, B11, B10, B9, B8, B7, B6, B5, B4, B3, B2, B1, B0, ADDNSUB, SIGNEDAB, ACCUMSLOAD, CE0, CE1, CE2, CE3, CLK0, CLK1, CLK2, CLK3, RST0, RST1, RST2, RST3, SRIA17, SRIA16, SRIA15, SRIA14, SRIA13, SRIA12, SRIA11, SRIA10, SRIA9, SRIA8, SRIA7, SRIA6, SRIA5, SRIA4, SRIA3, SRIA2, SRIA1, SRIA0, SRIB17, SRIB16, SRIB15, SRIB14, SRIB13, SRIB12, SRIB11, SRIB10, SRIB9, SRIB8, SRIB7, SRIB6, SRIB5, SRIB4, SRIB3, SRIB2, SRIB1, SRIB0, SROA17, SROA16, SROA15, SROA14, SROA13, SROA12, SROA11, SROA10, SROA9, SROA8, SROA7, SROA6, SROA5, SROA4, SROA3, SROA2, SROA1, SROA0, SROB17, SROB16, SROB15, SROB14, SROB13, SROB12, SROB11, SROB10, SROB9, SROB8, SROB7, SROB6, SROB5, SROB4, SROB3, SROB2, SROB1, SROB0, ACCUM51, ACCUM50, ACCUM49, ACCUM48, ACCUM47, ACCUM46, ACCUM45, ACCUM44, ACCUM43, ACCUM42, ACCUM41, ACCUM40, ACCUM39, ACCUM38, ACCUM37, ACCUM36, ACCUM35, ACCUM34, ACCUM33, ACCUM32, ACCUM31, ACCUM30, ACCUM29, ACCUM28, ACCUM27, ACCUM26, ACCUM25, ACCUM24, ACCUM23, ACCUM22, ACCUM21, ACCUM20, ACCUM19, ACCUM18, ACCUM17, ACCUM16, ACCUM15, ACCUM14, ACCUM13, ACCUM12, ACCUM11, ACCUM10, ACCUM9, ACCUM8, ACCUM7, ACCUM6, ACCUM5, ACCUM4, ACCUM3, ACCUM2, ACCUM1, ACCUM0, OVERFLOW

ATTRIBUTES:

REG_INPUTA_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_INPUTA_CE: "CE0", "CE1", "CE2", "CE3"
REG_INPUTA_RST: "RST0", "RST1", "RST2", "RST3"
REG_INPUTB_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_INPUTB_CE: "CE0", "CE1", "CE2", "CE3"
REG_INPUTB_RST: "RST0", "RST1", "RST2", "RST3"
REG_PIPELINE_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_PIPELINE_CE: "CE0", "CE1", "CE1", "CE3"
REG_PIPELINE_RST: "RST0", "RST1", "RST2", "RST3"
REG_OUTPUT_CLK: "CLK0", "CLK1", "CLK2", "CLK3"
REG_OUTPUT_CE: "CE0", "CE1", "CE2", "CE3"
REG_OUTPUT_RST: "RST0", "RST1", "RST2", "RST3"
REG_SIGNEDAB_0_CLK: "CLK0", "CLK0", "CLK0", "CLK0", "NONE"
REG_SIGNEDAB_0_CE: "CE0", "CE1", "CE2", "CE3"
REG_SIGNEDAB_0_RST: "RST0", "RST1", "RST2", "RST3"
REG_SIGNEDAB_1_CLK: "CLK0", "CLK0", "CLK0", "CLK0", "NONE"
REG_SIGNEDAB_1_CE: "CE0", "CE1", "CE2", "CE3"
REG_SIGNEDAB_1_RST: "RST0", "RST1", "RST2", "RST3"
REG_ACCUMSLOAD_0_CLK: "CLK0", "CLK0", "CLK0", "CLK0", "NONE"
REG_ACCUMSLOAD_0_CE: "CE0", "CE1", "CE2", "CE3"
REG_ACCUMSLOAD_0_RST: "RST0", "RST1", "RST2", "RST3"
REG_ACCUMSLOAD_1_CLK: "CLK0", "CLK0", "CLK0", "CLK0", "NONE"
REG_ACCUMSLOAD_1_CE: "CE0", "CE1", "CE2", "CE3"
REG_ACCUMSLOAD_1_RST: "RST0", "RST1", "RST2", "RST3"

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SHIFT_IN_A: "TRUE", "FALSE"
SHIFT_IN_B: "TRUE", "FALSE"
GSR: "ENABLED", "DISABLED"

Description:

MULT18X18MAC supports operand bit widths for 18X18 multiplication and accumulates the output up to 52 bits. The DSP block includes optional registers for the input and intermediate pipeline stage. Pipeline stages may be set using a pipeline attribute. The output registers are required for the accumulator. Signed and unsigned arithmetic are supported. The OVERFLOW bit is also provided when the accumulated results are in the overflow condition. ACCUMSLOAD determines the mode of operation for either loading the multiplier product or to accumulate.

The element consists of three types of optional pipeline registers:

- Input registers, located before the multipliers and registering the operands
- Multiplier pipeline registers, located after the multipliers and product registration
- Output registers, located before leaving the block, and registering the mode-specific output.

See the description of MULT18X18 for more information on control signals for DSP blocks and attributes.

MULT18X18MAC pin functions:

Function	Pins
input data A and B	A[17:0], B[17:0]
signed input (0 = unsigned, 1 = signed)	SIGNEDAB
add/subtract (0 = add, 1 = subtract)	ADDNSUB
Accumulate (HIGH) /Load (LOW) Mode	ACCUMSLOAD
clock enable	CE[0:3]
clock input	CLK[0:3]

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clock reset	RST[0:3]
shifted input A and B (from previous stage)	SRIA[17:0], SRIB[17:0]
shifted output A and B (from previous stage)	SROA[17:0], SROB[17:0]
output data	ACCUM[51:0]
overflow	OVERFLOW

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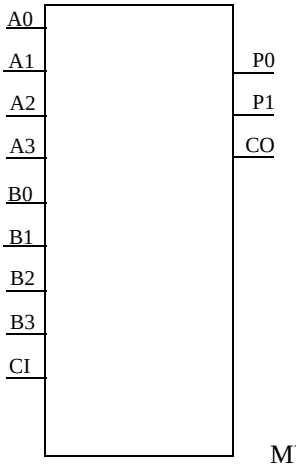
MULT2

2x2 Multiplier

Lattice FPGA			
XP	EC	ECP	MX
	✓	✓	✓



MULT2

INPUTS: A0, A1, A2, A3, B0, B1, B2, B3, CI
OUTPUTS: P0, P1, CO
PINORDER: A0, A1, A2, A3, B0, B1, B2, B3, CI, P0, P1, CO

Description:

MULT2 is a 2x2 multiplier. This element is useful when implementing an array multiplier using a dedicated carry chain. This unique configuration is made possible the two seperate "and" inputs added together to perform the add and shift operations within a single slice. MULT2 must be cascaded to form the row and columns when performing the multiply function. Here are descriptions of the MULT2 pins:

Function	Pins
multiplicand	A0, A1, A2, A3
multiplier	B0, B1, B2, B3
carry in	CI

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carry out	CO
output	P0, P1

The equations for this element are shown in the table below:

Equations

P0 = (A0 and A1) XOR (B0 AND B1) XOR CI;

P1 = (A2 and A3) XOR (B2 AND B3) XOR CO_int;

CO_int = (A0 and A1) or (B0 AND B1) or CI;

CO = (A2 and A3) or (B2 and B3) or CO_int;

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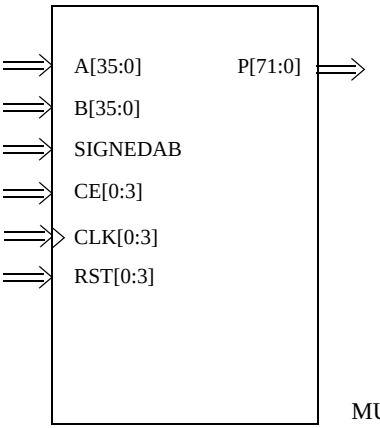
MULT36X36

ECP DSP Multiplier

Lattice FPGA		
XP	EC	ECP
		✓



MULT36X36

NOTE: The graphic is shown in bus notation for convenience. This element must be instantiated in expanded bus notation format with each individual bit as given below.

INPUTS: A35, A34, A33, A32, A31, A30, A29, A28, A27, A26, A25, A24, A23, A22, A21, A20, A19, A18, A17, A16, A15, A14, A13, A12, A11, A10, A9, A8, A7, A6, A5, A4, A3, A2, A1, A0, B35, B34, B33, B32, B31, B30, B29, B28, B27, B26, B25, B24, B23, B22, B21, B20, B19, B18, B17, B16, B15, B14, B13, B12, B11, B10, B9, B8, B7, B6, B5, B4, B3, B2, B1, B0, SIGNEDAB, CE0, CE1, CE2, CE3, CLK0, CLK1, CLK2, CLK3, RST0, RST1, RST2, RST3

OUTPUTS: P71, P70, P69, P68, P67, P66, P65, P64, P63, P62, P61, P60, P59, P58, P57, P56, P55, P54, P53, P52, P51, P50, P49, P48, P47, P46, P45, P44, P43, P42, P41, P40, P39, P38, P37, P36, P35, P34, P33, P32, P31, P30, P29, P28, P27, P26, P25, P24, P23, P22, P21, P20, P19, P18, P17, P16, P15, P14, P13, P12, P11, P10, P9, P8, P7, P6, P5, P4, P3, P2, P1, P0

PINORDER: A35, A34, A33, A32, A31, A30, A29, A28, A27, A26, A25, A24, A23, A22, A21, A20, A19, A18, A17, A16, A15, A14, A13, A12, A11, A10, A9, A8, A7, A6, A5, A4, A3, A2, A1, A0, B35, B34, B33, B32, B31, B30, B29, B28, B27, B26, B25, B24, B23, B22, B21, B20, B19, B18, B17, B16, B15, B14, B13, B12, B11, B10, B9, B8, B7, B6, B5, B4, B3, B2, B1, B0, SIGNEDAB, CE0, CE1, CE2, CE3, CLK0, CLK1, CLK2, CLK3, RST0, RST1, RST2, RST3, P71, P70, P69, P68, P67, P66, P65, P64, P63, P62, P61, P60, P59, P58, P57, P56, P55, P54, P53, P52, P51, P50, P49, P48, P47, P46, P45, P44, P43, P42, P41, P40, P39, P38, P37, P36, P35, P34, P33, P32, P31, P30, P29, P28, P27, P26, P25, P24, P23, P22, P21, P20, P19, P18, P17, P16, P15, P14, P13, P12, P11, P10, P9, P8, P7, P6, P5, P4, P3, P2, P1, P0

ATTRIBUTES:

REG_INPUTA_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"

REG_INPUTA_CE: "CE0", "CE1", "CE2", "CE3"

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REG_INPUTA_RST: "RST0", "RST1", "RST2", "RST3"
REG_INPUTB_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_INPUTB_CE: "CE0", "CE1", "CE2", "CE3"
REG_INPUTB_RST: "RST0", "RST1", "RST2", "RST3"
REG_PIPELINE_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_PIPELINE_CE: "CE0", "CE1", "CE1", "CE3"
REG_PIPELINE_RST: "RST0", "RST1", "RST2", "RST3"
REG_OUTPUT_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_OUTPUT_CE: "CE0", "CE1", "CE2", "CE3"
REG_OUTPUT_RST: "RST0", "RST1", "RST2", "RST3"
REG_SIGNEDAB_0_CLK: "CLK0", "CLK0", "CLK0", "CLK0", "NONE"
REG_SIGNEDAB_0_CE: "CE0", "CE1", "CE2", "CE3"
REG_SIGNEDAB_0_RST: "RST0", "RST1", "RST2", "RST3"
REG_SIGNEDAB_1_CLK: "CLK0", "CLK0", "CLK0", "CLK0", "NONE"
REG_SIGNEDAB_1_CE: "CE0", "CE1", "CE2", "CE3"
REG_SIGNEDAB_1_RST: "RST0", "RST1", "RST2", "RST3"
GSR: "ENABLED", "DISABLED"

Description:

LatticeECP-DSP Block Multiplier. MULT36X36 is a combinational signed 36-bit by 36-bit multiplier used in the DSP block. The value represented in the 36-bit input A is multiplied by the value represented in the 36-bit input B. Output P is the 72-bit product of A and B. MULT36X36 may be represented as either unsigned or two’s complement signed. The element consists of three types of optional pipeline registers:

- Input registers, located before the multipliers and registering the operands
- Multiplier pipeline registers, located after the multipliers and product registration
- Output registers, located before leaving the block, and registering the mode-specific output.

See the description of MULT18X18 for more information on control signals for DSP blocks and attributes.

Input registers receive operand values from a serial shift chain or routing input. There is separate control for A and B operands. When in shift chain mode, multiplier operands may be bypassed using the bank bypass feature. The shift chain supports one chain of two 18-bit operands or two chains of two 9-bit operands. GSR “DISABLED” attribute disables the asynchronous global set reset input when in user mode.

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MULT36X36 pin functions:

Function	Pins
input data A and B	A[35:0], B[35:0]
signed input (0 = unsigned, 1 = signed)	SIGNEDAB
clock enable	CE[0:3]
clock input	CLK[0:3]
clock reset	RST[0:3]
output data	P[71:0]

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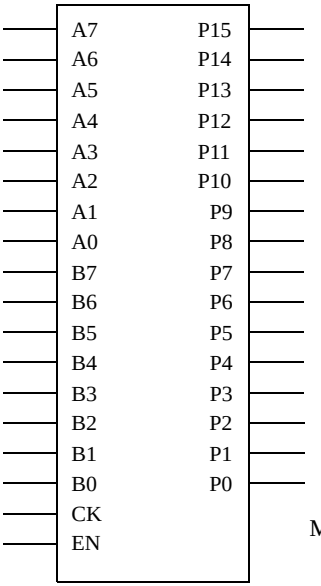
MULT8X8

8 Bit by 8 Bit Multiplier

ORCA Series		
2	3	4
		✓



INPUTS: A7, A6, A5, A4, A3, A2, A1, A0, B7, B6, B5, B4, B3, B2, B1, B0, CK, EN
OUTPUTS: P15, P14, P13, P12, P11, P10, P9, P8, P7, P6, P5, P4, P3, P2, P1, P0
PINORDER: A7 A6 A5 A4 A3 A2 A1 A0 B7 B6 B5 B4 B3 B2 B1 B0 CK EN P15 P14 P13 P12 P11 P10 P9 P8 P7 P6 P5 P4 P3 P2 P1 P0
MINIMUM CELL AREA (Series 2): 0.5
MINIMUM CELL AREA (Series 3 and Series 4): 0.25
ATTRIBUTES (Series 4 only)
MULTMODE : NOREG, INREG, OUTREG, IOREG
MINIMUM MINIMUM CELL AREA: 0

continued

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Description:

The 8x8 multiplier will multiply two 8-bit numbers. This can be either a pipelined or combinatorial multiplier. The pipelined version includes FFs at the input and/or at the output of the multipliers.

Function	Pins
multiplicand	A7, A6,...A0
multiplier	B7, B6,...B0
clock	CK
enable	EN
output	P15, P14,...P0

***Note*:** The MULT8X8 element should be instantiated using the Module/IP Manager or scuba command line. Refer to the appropriate topic in the online help system for details.

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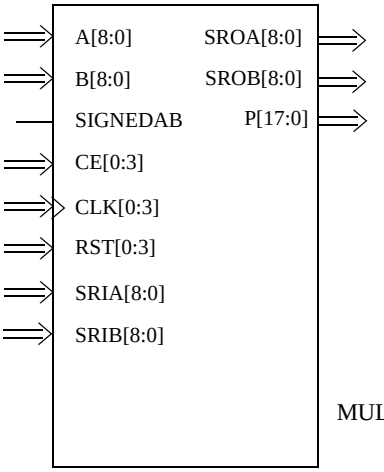
MULT9X9

ECP DSP Multiplier

Lattice FPGA		
XP	EC	ECP
		✓



NOTE: The graphic is shown in bus notation for convenience. This element must be instantiated in expanded bus notation format with each individual bit as given below.

INPUTS: A8, A7, A6, A5, A4, A3, A2, A1, A0, B8, B7, B6, B5, B4, B3, B2, B1, B0, SIGNEDAB, CE0, CE1, CE2, CE3, CLK0, CLK1, CLK2, CLK3, RST0, RST1, RST2, RST3, SRIA8, SRIA7, SRIA6, SRIA5, SRIA4, SRIA3, SRIA2, SRIA1, SRIA0, SRIB8, SRIB7, SRIB6, SRIB5, SRIB4, SRIB3, SRIB2, SRIB1, SRIB0

OUTPUTS: SROA8, SROA7, SROA6, SROA5, SROA4, SROA3, SROA2, SROA1, SROA0, SROB8, SROB7, SROB6, SROB5, SROB4, SROB3, SROB2, SROB1, SROB0, P17, P16, P15, P14, P13, P12, P11, P10, P9, P8, P7, P6, P5, P4, P3, P2, P1, P0

PINORDER: A8, A7, A6, A5, A4, A3, A2, A1, A0, B8, B7, B6, B5, B4, B3, B2, B1, B0, SIGNEDAB, CE0, CE1, CE2, CE3, CLK0, CLK1, CLK2, CLK3, RST0, RST1, RST2, RST3, SRIA8, SRIA7, SRIA6, SRIA5, SRIA4, SRIA3, SRIA2, SRIA1, SRIA0, SRIB8, SRIB7, SRIB6, SRIB5, SRIB4, SRIB3, SRIB2, SRIB1, SRIB0, SROA8, SROA7, SROA6, SROA5, SROA4, SROA3, SROA2, SROA1, SROA0, SROB8, SROB7, SROB6, SROB5, SROB4, SROB3, SROB2, SROB1, SROB0, P17, P16, P15, P14, P13, P12, P11, P10, P9, P8, P7, P6, P5, P4, P3, P2, P1, P0

ATTRIBUTES:

REG_INPUTA_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_INPUTA_CE: "CE0", "CE1", "CE2", "CE3"
REG_INPUTA_RST: "RST0", "RST1", "RST2", "RST3"
REG_INPUTB_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_INPUTB_CE: "CE0", "CE1", "CE2", "CE3"
REG_INPUTB_RST: "RST0", "RST1", "RST2", "RST3"
REG_PIPELINE_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_PIPELINE_CE: "CE0", "CE1", "CE1", "CE3"
REG_PIPELINE_RST: "RST0", "RST1", "RST2", "RST3"

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REG_OUTPUT_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_OUTPUT_CE: "CE0", "CE1", "CE2", "CE3"
REG_OUTPUT_RST: "RST0", "RST1", "RST2", "RST3"
REG_SIGNEDAB_0_CLK: "CLK0", "CLK0", "CLK0", "CLK0", "NONE"
REG_SIGNEDAB_0_CE: "CE0", "CE1", "CE2", "CE3"
REG_SIGNEDAB_0_RST: "RST0", "RST1", "RST2", "RST3"
REG_SIGNEDAB_1_CLK: "CLK0", "CLK0", "CLK0", "CLK0", "NONE"
REG_SIGNEDAB_1_CE: "CE0", "CE1", "CE2", "CE3"
REG_SIGNEDAB_1_RST: "RST0", "RST1", "RST2", "RST3"
SHIFT_IN_A: "TRUE", "FALSE"
SHIFT_IN_B: "TRUE", "FALSE"
GSR: "ENABLED", "DISABLED"

Description:

LatticeECP-DSP Block Multiplier. MULT9X9 is a combinational signed 9-bit by 9-bit multiplier used in the DSP block. The value represented in the 9-bit input A is multiplied by the value represented in the 9-bit input B. Output P is the 18-bit product of A and B. MULT9X9 may be represented as either unsigned or two’s complement signed. The element consists of three types of optional pipeline registers:

- Input registers, located before the multipliers and registering the operands
- Multiplier pipeline registers, located after the multipliers and product registration
- Output registers, located before leaving the block, and registering the mode-specific output.

See the description of MULT18X18 for more information on control signals for DSP blocks and attributes.

MULT9X9 pin functions:

Function	Pins
input data A and B	A[8:0], B[8:0]
signed input (0 = unsigned, 1 = signed)	SIGNEDAB
clock enable	CE[0:3]
clock input	CLK[0:3]

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reset	RST[0:3]
shifted input A and B (from previous stage)	SRIA[8:0], SRIB[8:0]
shifted output A and B (from previous stage)	SROA[8:0], SROB[8:0]
output product data	P[17:0]

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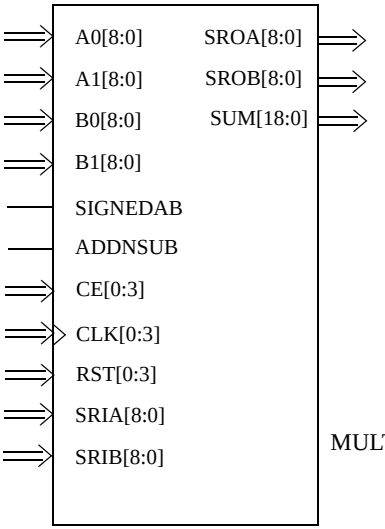
MULT9X9ADDSUB

ECP DSP Multiplier

Lattice FPGA		
XP	EC	ECP
		✓



NOTE: The graphic is shown in bus notation for convenience. This element must be instantiated in expanded bus notation format with each individual bit as given below.

INPUTS: A08, A07, A06, A05, A04, A03, A02, A01, A00, A18, A17, A16, A15, A14, A13, A12, A11, A10, B08, B07, B06, B05, B04, B03, B02, B01, B00, B18, B17, B16, B15, B14, B13, B12, B11, B10, SIGNEDAB, ADDNSUB, CE0, CE1, CE2, CE3, CLK0, CLK1, CLK2, CLK3, RST0, RST1, RST2, RST3, SRIA8, SRIA7, SRIA6, SRIA5, SRIA4, SRIA3, SRIA2, SRIA1, SRIA0, SRIB8, SRIB7, SRIB6, SRIB5, SRIB4, SRIB3, SRIB2, SRIB1, SRIB0

OUTPUTS: SROA8, SROA7, SROA6, SROA5, SROA4, SROA3, SROA2, SROA1, SROA0, SROB8, SROB7, SROB6, SROB5, SROB4, SROB3, SROB2, SROB1, SROB0, SUM18, SUM17, SUM16, SUM15, SUM14, SUM13, SUM12, SUM11, SUM10, SUM9, SUM8, SUM7, SUM6, SUM5, SUM4, SUM3, SUM2, SUM1, SUM0

PINORDER: A08, A07, A06, A05, A04, A03, A02, A01, A00, A18, A17, A16, A15, A14, A13, A12, A11, A10, B08, B07, B06, B05, B04, B03, B02, B01, B00, B18, B17, B16, B15, B14, B13, B12, B11, B10, SIGNEDAB, ADDNSUB, CE0, CE1, CE2, CE3, CLK0, CLK1, CLK2, CLK3, RST0, RST1, RST2, RST3, SRIA8, SRIA7, SRIA6, SRIA5, SRIA4, SRIA3, SRIA2, SRIA1, SRIA0, SRIB8, SRIB7, SRIB6, SRIB5, SRIB4, SRIB3, SRIB2, SRIB1, SRIB0, SROA8, SROA7, SROA6, SROA5, SROA4, SROA3, SROA2, SROA1, SROA0, SROB8, SROB7, SROB6, SROB5, SROB4, SROB3, SROB2, SROB1, SROB0, SUM18, SUM17, SUM16, SUM15, SUM14, SUM13, SUM12, SUM11, SUM10, SUM9, SUM8, SUM7, SUM6, SUM5, SUM4, SUM3, SUM2, SUM1, SUM0

ATTRIBUTES:

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REG_INPUTA0_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_INPUTA0_CE: "CE0", "CE1", "CE2", "CE3"
REG_INPUTA0_RST: "RST0", "RST1", "RST2", "RST3"
REG_INPUTA1_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_INPUTA1_CE: "CE0", "CE1", "CE2", "CE3"
REG_INPUTA1_RST: "RST0", "RST1", "RST2", "RST3"
REG_INPUTB0_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_INPUTB0_CE: "CE0", "CE1", "CE2", "CE3"
REG_INPUTB0_RST: "RST0", "RST1", "RST2", "RST3"
REG_INPUTB1_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_INPUTB1_CE: "CE0", "CE1", "CE2", "CE3"
REG_INPUTB1_RST: "RST0", "RST1", "RST2", "RST3"
REG_PIPELINE_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_PIPELINE_CE: "CE0", "CE1", "CE1", "CE3"
REG_PIPELINE_RST: "RST0", "RST1", "RST2", "RST3"
REG_OUTPUT_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_OUTPUT_CE: "CE0", "CE1", "CE2", "CE3"
REG_OUTPUT_RST: "RST0", "RST1", "RST2", "RST3"
REG_ADDNSUB_0_CLK: "CLK0", "CLK0", "CLK0", "CLK0", "NONE"
REG_ADDNSUB_0_CE: "CE0", "CE1", "CE2", "CE3"
REG_ADDNSUB_0_RST: "RST0", "RST1", "RST2", "RST3"
REG_ADDNSUB_1_CLK: "CLK0", "CLK0", "CLK0", "CLK0", "NONE"
REG_ADDNSUB_1_CE: "CE0", "CE1", "CE2", "CE3"
REG_ADDNSUB_1_RST: "RST0", "RST1", "RST2", "RST3"
REG_SIGNEDAB_0_CLK: "CLK0", "CLK0", "CLK0", "CLK0", "NONE"
REG_SIGNEDAB_0_CE: "CE0", "CE1", "CE2", "CE3"
REG_SIGNEDAB_0_RST: "RST0", "RST1", "RST2", "RST3"
REG_SIGNEDAB_1_CLK: "CLK0", "CLK0", "CLK0", "CLK0", "NONE"
REG_SIGNEDAB_1_CE: "CE0", "CE1", "CE2", "CE3"
REG_SIGNEDAB_1_RST: "RST0", "RST1", "RST2", "RST3"
SHIFT_IN_A0: "TRUE", "FALSE"
SHIFT_IN_B0: "TRUE", "FALSE"
SHIFT_IN_A1: "TRUE", "FALSE"
SHIFT_IN_B1: "TRUE", "FALSE"
GSR: "ENABLED", "DISABLED"

Description:

LatticeECP-DSP Block Adder/Subtractor. MULT18X18ADDSUB can be configured to either add or subtract its inputs, adding or subtracting the inputs from two multiplier products. The add/subtract control is either configured as a static HIGH (Vcc), LOW (GND), or as dynamic control signals ADDNSUB1 and ADDNSUB3. In ispLEVER, the static settings are implemented by setting ADDNSUB1 and ADDNSUB3 signal to Vcc or GND in the CIB ISB.

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The element consists of three types of optional pipeline registers:

- Input registers, located before the multipliers and registering the operands
- Multiplier pipeline registers, located after the multipliers and product registration
- Output registers, located before leaving the block, and registering the mode-specific output.

See the description of MULT18X18 for more information on control signals for DSP blocks and attributes.

MULT9X9ADDSUB pin functions:

Function	Pins
input data A and B	A0|1[8:0], B0|1[8:0]
signed input (0 = unsigned, 1 = signed)	SIGNEDAB
add/subtract (0 = add, 1 = subtract)	ADDNSUB
clock enable	CE[0:3]
clock input	CLK[0:3]
reset	RST[0:3]
shifted input A and B (from previous stage)	SRIA[8:0], SRIB[8:0]
shifted output A and B (from previous stage)	SROA[8:0], SROB[8:0]
output product sum data	SUM[18:0]

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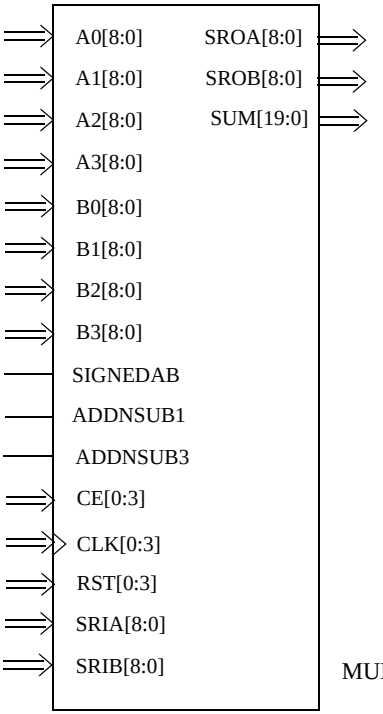
MULT9X9ADDSUBSUM

ECP DSP Adder/Subtractor/Sum

Lattice FPGA		
XP	EC	ECP
		✓



MULT9X9ADDSUBSUM

NOTE: The graphic is shown in bus notation for convenience. This element must be instantiated in expanded bus notation format with each individual bit as given below.

INPUTS: A08, A07, A06, A05, A04, A03, A02, A01, A00, A18, A17, A16, A15, A14, A13, A12, A11, A10, A28, A27, A26, A25, A24, A23, A22, A21, A20, A38, A37, A36, A35, A34, A33, A32, A31, A30, B08, B07, B06, B05, B04, B03, B02, B01, B00, B18, B17, B16, B15, B14, B13, B12, B11, B10, B28, B27, B26, B25, B24, B23, B22, B21, B20, B38, B37, B36, B35, B34, B33, B32, B31, B30, SIGNEDAB, ADDNSUB1, ADDNSUB3, CE0, CE1, CE2, CE3, CLK0, CLK1, CLK2, CLK3, RST0, RST1, RST2, RST3, SRIA8, SRIA7, SRIA6, SRIA5, SRIA4, SRIA3, SRIA2, SRIA1, SRIA0, SRIB8, SRIB7, SRIB6, SRIB5, SRIB4, SRIB3, SRIB2, SRIB1, SRIB0

OUTPUTS: SROA8, SROA7, SROA6, SROA5, SROA4, SROA3, SROA2, SROA1, SROA0, SROB8, SROB7, SROB6, SROB5, SROB4, SROB3, SROB2, SROB1, SROB0, SUM19, SUM18, SUM17, SUM16, SUM15, SUM14, SUM13, SUM12, SUM11, SUM10, SUM9, SUM8, SUM7, SUM6, SUM5, SUM4, SUM3, SUM2, SUM1, SUM0

PINORDER: A08, A07, A06, A05, A04, A03, A02, A01, A00, A18, A17, A16, A15, A14, A13, A12, A11, A10, A28, A27, A26, A25, A24, A23, A22, A21, A20, A38, A37, A36, A35, A34, A33, A32, A31, A30, B08, B07, B06, B05, B04, B03, B02, B01, B00, B18, B17,

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B16, B15, B14, B13, B12, B11, B10, B28, B27, B26, B25, B24, B23, B22, B21, B20, B38, B37, B36, B35, B34, B33, B32, B31, B30, SIGNEDAB, ADDNSUB1, ADDNSUB3, CE0, CE1, CE2, CE3, CLK0, CLK1, CLK2, CLK3, RST0, RST1, RST2, RST3, SRIA8, SRIA7, SRIA6, SRIA5, SRIA4, SRIA3, SRIA2, SRIA1, SRIA0, SRIB8, SRIB7, SRIB6, SRIB5, SRIB4, SRIB3, SRIB2, SRIB1, SRIB0, SROA8, SROA7, SROA6, SROA5, SROA4, SROA3, SROA2, SROA1, SROA0, SROB8, SROB7, SROB6, SROB5, SROB4, SROB3, SROB2, SROB1, SROB0, SUM19, SUM18, SUM17, SUM16, SUM15, SUM14, SUM13, SUM12, SUM11, SUM10, SUM9, SUM8, SUM7, SUM6, SUM5, SUM4, SUM3, SUM2, SUM1, SUM0

ATTRIBUTES:

REG_INPUTA0_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_INPUTA0_CE: "CE0", "CE1", "CE2", "CE3"
REG_INPUTA0_RST: "RST0", "RST1", "RST2", "RST3"
REG_INPUTA1_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_INPUTA1_CE: "CE0", "CE1", "CE2", "CE3"
REG_INPUTA1_RST: "RST0", "RST1", "RST2", "RST3"
REG_INPUTA2_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_INPUTA2_CE: "CE0", "CE1", "CE2", "CE3"
REG_INPUTA2_RST: "RST0", "RST1", "RST2", "RST3"
REG_INPUTA3_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_INPUTA3_CE: "CE0", "CE1", "CE2", "CE3"
REG_INPUTA3_RST: "RST0", "RST1", "RST2", "RST3"
REG_INPUTB0_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_INPUTB0_CE: "CE0", "CE1", "CE2", "CE3"
REG_INPUTB0_RST: "RST0", "RST1", "RST2", "RST3"
REG_INPUTB1_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_INPUTB1_CE: "CE0", "CE1", "CE2", "CE3"
REG_INPUTB1_RST: "RST0", "RST1", "RST2", "RST3"
REG_INPUTB2_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_INPUTB2_CE: "CE0", "CE1", "CE2", "CE3"
REG_INPUTB2_RST: "RST0", "RST1", "RST2", "RST3"
REG_INPUTB3_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_INPUTB3_CE: "CE0", "CE1", "CE2", "CE3"
REG_INPUTB3_RST: "RST0", "RST1", "RST2", "RST3"
REG_PIPELINE0_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_PIPELINE0_CE: "CE0", "CE1", "CE1", "CE3"
REG_PIPELINE0_RST: "RST0", "RST1", "RST2", "RST3"
REG_PIPELINE1_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_PIPELINE1_CE: "CE0", "CE1", "CE1", "CE3"
REG_PIPELINE1_RST: "RST0", "RST1", "RST2", "RST3"
REG_OUTPUT_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_OUTPUT_CE: "CE0", "CE1", "CE2", "CE3"
REG_OUTPUT_RST: "RST0", "RST1", "RST2", "RST3"
REG_SIGNEDAB_0_CLK: "CLK0", "CLK0", "CLK0", "CLK0", "NONE"
REG_SIGNEDAB_0_CE: "CE0", "CE1", "CE2", "CE3"

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REG_SIGNEDAB_0_RST: "RST0", "RST1", "RST2", "RST3"
REG_SIGNEDAB_1_CLK: "CLK0", "CLK0", "CLK0", "CLK0", "NONE"
REG_SIGNEDAB_1_CE: "CE0", "CE1", "CE2", "CE3"
REG_SIGNEDAB_1_RST: "RST0", "RST1", "RST2", "RST3"
REG_ADDNSUB1_0_CLK: "CLK0", "CLK0", "CLK0", "CLK0", "NONE"
REG_ADDNSUB1_0_CE: "CE0", "CE1", "CE2", "CE3"
REG_ADDNSUB1_0_RST: "RST0", "RST1", "RST2", "RST3"
REG_ADDNSUB1_1_CLK: "CLK0", "CLK0", "CLK0", "CLK0", "NONE"
REG_ADDNSUB1_1_CE: "CE0", "CE1", "CE2", "CE3"
REG_ADDNSUB1_1_RST: "RST0", "RST1", "RST2", "RST3"
REG_ADDNSUB3_0_CLK: "CLK0", "CLK0", "CLK0", "CLK0", "NONE"
REG_ADDNSUB3_0_CE: "CE0", "CE1", "CE2", "CE3"
REG_ADDNSUB3_0_RST: "RST0", "RST1", "RST2", "RST3"
REG_ADDNSUB3_1_CLK: "CLK0", "CLK0", "CLK0", "CLK0", "NONE"
REG_ADDNSUB3_1_CE: "CE0", "CE1", "CE2", "CE3"
REG_ADDNSUB3_1_RST: "RST0", "RST1", "RST2", "RST3"
SHIFT_IN_A0: "TRUE", "FALSE"
SHIFT_IN_B0: "TRUE", "FALSE"
SHIFT_IN_A1: "TRUE", "FALSE"
SHIFT_IN_B1: "TRUE", "FALSE"
SHIFT_IN_A2: "TRUE", "FALSE"
SHIFT_IN_B2: "TRUE", "FALSE"
SHIFT_IN_A3: "TRUE", "FALSE"
SHIFT_IN_B3: "TRUE", "FALSE"
GSR: "ENABLED", "DISABLED"

Description:

LatticeECP-DSP Block Adder/Subtractor. MULT9X9ADDSUBSUM can be configured to either add or subtract its inputs, adding or subtracting the inputs from two multiplier products. The add/subtract control is either configured as a static HIGH (Vcc), LOW (GND), or as dynamic control signals ADDNSUB1 and ADDNSUB3. In ispLEVER, the static settings are implemented by setting ADDNSUB1 and ADDNSUB3 signal to Vcc or GND in the CIB ISB.

The element consists of three types of optional pipeline registers:

- Input registers, located before the multipliers and registering the operands
- Multiplier pipeline registers, located after the multipliers and product registration
- Output registers, located before leaving the block, and registering the mode-specific output.

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See the description of MULT18X18 for more information on control signals for DSP blocks and attributes.

MULT9X9ADDSUBSUM pin functions:

Function	Pins
input data A and B	A0|1|2|3[8:0], B0|1|2|3[8:0]
signed input (0 = unsigned, 1 = signed)	SIGNEDAB
add/subtract (0 = add, 1 = subtract)	ADDNSUB1, ADDNSUB3
clock enable	CE[0:3]
clock input	CLK[0:3]
reset	RST[0:3]
shifted input A and B (from previous stage)	SRIA[8:0], SRIB[8:0]
shifted output A and B (from previous stage)	SROA[8:0], SROB[8:0]
output product sum data	SUM[19:0]

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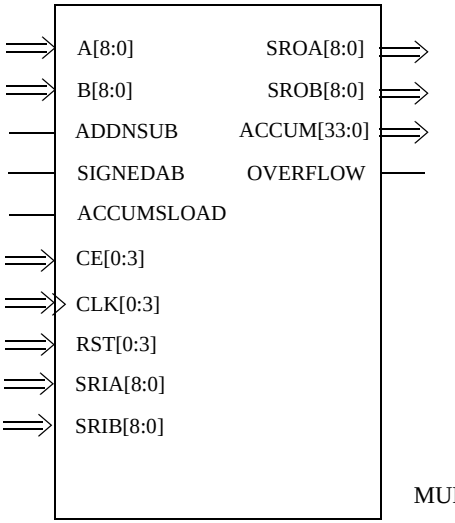
MULT9X9MAC

ECP DSP Multiplier

Lattice FPGA		
XP	EC	ECP
		✓



MULT9X9MAC

NOTE: The graphic is shown in bus notation for convenience. This element must be instantiated in expanded bus notation format with each individual bit as given below.

INPUTS: A8, A7, A6, A5, A4, A3, A2, A1, A0, B8, B7, B6, B5, B4, B3, B2, B1, B0, ADDNSUB, SIGNEDAB, ACCUMSLOAD, CE0, CE1, CE2, CE3, CLK0, CLK1, CLK2, CLK3, RST0, RST1, RST2, RST3, SRIA8, SRIA7, SRIA6, SRIA5, SRIA4, SRIA3, SRIA2, SRIA1, SRIA0, SRIB8, SRIB7, SRIB6, SRIB5, SRIB4, SRIB3, SRIB2, SRIB1, SRIB0

OUTPUTS: SROA8, SROA7, SROA6, SROA5, SROA4, SROA3, SROA2, SROA1, SROA0, SROB8, SROB7, SROB6, SROB5, SROB4, SROB3, SROB2, SROB1, SROB0, ACCUM33, ACCUM32, ACCUM31, ACCUM30, ACCUM29, ACCUM28, ACCUM27, ACCUM26, ACCUM25, ACCUM24, ACCUM23, ACCUM22, ACCUM21, ACCUM20, ACCUM19, ACCUM18, ACCUM17, ACCUM16, ACCUM15, ACCUM14, ACCUM13, ACCUM12, ACCUM11, ACCUM10, ACCUM9, ACCUM8, ACCUM7, ACCUM6, ACCUM5, ACCUM4, ACCUM3, ACCUM2, ACCUM1, ACCUM0, OVERFLOW

PINORDER: A8, A7, A6, A5, A4, A3, A2, A1, A0, B8, B7, B6, B5, B4, B3, B2, B1, B0, ADDNSUB, SIGNEDAB, ACCUMSLOAD, CE0, CE1, CE2, CE3, CLK0, CLK1, CLK2, CLK3, RST0, RST1, RST2, RST3, SRIA8, SRIA7, SRIA6, SRIA5, SRIA4, SRIA3, SRIA2, SRIA1, SRIA0, SRIB8, SRIB7, SRIB6, SRIB5, SRIB4, SRIB3, SRIB2, SRIB1, SRIB0, SROA8, SROA7, SROA6, SROA5, SROA4, SROA3, SROA2, SROA1, SROA0, SROB8, SROB7, SROB6, SROB5, SROB4, SROB3, SROB2, SROB1, SROB0, ACCUM33, ACCUM32, ACCUM31, ACCUM30, ACCUM29, ACCUM28, ACCUM27, ACCUM26, ACCUM25, ACCUM24, ACCUM23, ACCUM22, ACCUM21, ACCUM20, ACCUM19, ACCUM18, ACCUM17, ACCUM16, ACCUM15, ACCUM14, ACCUM13, ACCUM12, ACCUM11,

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ACCUM10, ACCUM9, ACCUM8, ACCUM7, ACCUM6, ACCUM5, ACCUM4, ACCUM3, ACCUM2, ACCUM1, ACCUM0, OVERFLOW

ATTRIBUTES:
REG_INPUTA_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_INPUTA_CE: "CE0", "CE1", "CE2", "CE3"
REG_INPUTA_RST: "RST0", "RST1", "RST2", "RST3"
REG_INPUTB_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_INPUTB_CE: "CE0", "CE1", "CE2", "CE3"
REG_INPUTB_RST: "RST0", "RST1", "RST2", "RST3"
REG_PIPELINE_CLK: "CLK0", "CLK1", "CLK2", "CLK3", "NONE"
REG_PIPELINE_CE: "CE0", "CE1", "CE1", "CE3"
REG_PIPELINE_RST: "RST0", "RST1", "RST2", "RST3"
REG_OUTPUT_CLK: "CLK0", "CLK1", "CLK2", "CLK3"
REG_OUTPUT_CE: "CE0", "CE1", "CE2", "CE3"
REG_OUTPUT_RST: "RST0", "RST1", "RST2", "RST3"
REG_SIGNEDAB_0_CLK: "CLK0", "CLK0", "CLK0", "CLK0", "NONE"
REG_SIGNEDAB_0_CE: "CE0", "CE1", "CE2", "CE3"
REG_SIGNEDAB_0_RST: "RST0", "RST1", "RST2", "RST3"
REG_SIGNEDAB_1_CLK: "CLK0", "CLK0", "CLK0", "CLK0", "NONE"
REG_SIGNEDAB_1_CE: "CE0", "CE1", "CE2", "CE3"
REG_SIGNEDAB_1_RST: "RST0", "RST1", "RST2", "RST3"
REG_ACCUMSLOAD_0_CLK: "CLK0", "CLK0", "CLK0", "CLK0", "NONE"
REG_ACCUMSLOAD_0_CE: "CE0", "CE1", "CE2", "CE3"
REG_ACCUMSLOAD_0_RST: "RST0", "RST1", "RST2", "RST3"
REG_ACCUMSLOAD_1_CLK: "CLK0", "CLK0", "CLK0", "CLK0", "NONE"
REG_ACCUMSLOAD_1_CE: "CE0", "CE1", "CE2", "CE3"
REG_ACCUMSLOAD_1_RST: "RST0", "RST1", "RST2", "RST3"
SHIFT_IN_A: "TRUE", "FALSE"
SHIFT_IN_B: "TRUE", "FALSE"
GSR: "ENABLED", "DISABLED"

Description:

MULT9X9MAC supports operand bit widths for 9X9 multiplication and accumulates the output up to 34 bits. The DSP block includes optional registers for the input and intermediate pipeline stage. Pipeline stages may be set using a pipeline attribute. The output registers are required for the accumulator. Signed and unsigned arithmetic are supported. The OVERFLOW bit is also provided when the accumulated results are in the overflow condition. ACCUMSLOAD determines the mode of operation for either loading the multiplier product or to accumulate.

The element consists of three types of optional pipeline registers:

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- Input registers, located before the multipliers and registering the operands
- Multiplier pipeline registers, located after the multipliers and product registration
- Output registers, located before leaving the block, and registering the mode-specific output.

See the description of MULT18X18 for more information on control signals for DSP blocks.

MULT9X9MAC pin functions:

Function	Pins
input data A and B	A[8:0], B[8:0]
signed input (0 = unsigned, 1 = signed)	SIGNEDAB
add/subtract (0 = add, 1 = subtract)	ADDNSUB
Accumulate (HIGH) /Load (LOW) Mode	ACCUMSLOAD
clock enable	CE[0:3]
clock input	CLK[0:3]
reset	RST[0:3]
shifted input A and B (from previous stage)	SRIA[8:0], SRIB[8:0]
shifted output A and B (from previous stage)	SROA[8:0], SROB[8:0]
output data	ACCUM[33:0]
overflow	OVERFLOW

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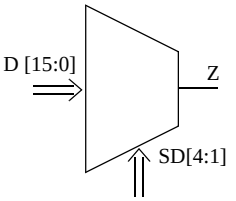
MUX161

16-Input Mux within the PFU (4 Slices)

Lattice FPGA		
SC	XP	EC
✓	✓	✓



MUX161

NOTE: The graphic is shown in bus notation for convenience. This element must be instantiated in expanded bus notation format with each individual bit as given below.

INPUTS: D0, D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, SD1, SD2, SD3, SD4
OUTPUTS: Z
PINORDER: D0, D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, SD1, SD2, SD3, SD4, Z

Truth Table:

INPUTS	OUTPUTS
SD[4:1]	Z
0000	D0
0001	D1
0010	D2
0011	D3
0100	D4
0101	D5
0110	D6
0111	D7

INPUTS	OUTPUTS
SD[4:1]	Z
1000	D8
1001	D9
1010	D10
1011	D11
1100	D12
1101	D13
1110	D14
1111	D15

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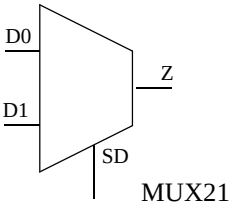
MUX21

2 to 1 Mux

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



MUX21

INPUTS: D0,D1,SD
OUTPUTS: Z
PINORDER: D0 D1 SD Z
MINIMUM CELL AREA (Series 2): 0.125
MINIMUM CELL AREA (Series 3 and 4): 0.047

Truth Table:

INPUTS			OUTPUTS
D0	D1	SD	Z
0	X	0	0
1	X	0	1
X	0	1	0
X	1	1	1

X = Don’t care

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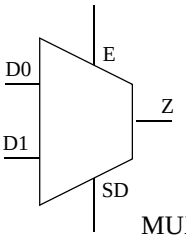
MUX21E

2 to 1 Mux with Enable

ORCA Series		
2	3	4
✓	✓	✓



MUX21E

INPUTS: D0,D1,SD,E
OUTPUTS: Z
PINORDER: D0 D1 SD E Z
MINIMUM CELL AREA (2A/2T): 0.125
MINIMUM CELL AREA (Series 3): 0.0625

Truth Table:

INPUTS				OUTPUTS
D0	D1	SD	E	Z
X	X	X	0	0
1	X	0	1	1
0	X	0	1	0
X	1	1	1	1
X	0	1	1	0

X = Don’t care

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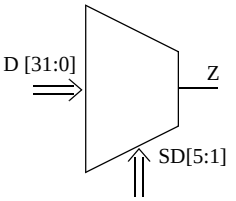
MUX321

32-Input Mux within the PFU (8 Slices)

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



MUX321

NOTE: The graphic is shown in bus notation for convenience. This element must be instantiated in expanded bus notation format with each individual bit as given below.

INPUTS: D0, D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, D16, D17, D18, D19, D20, D21, D22, D23, D24, D25, D26, D27, D28, D29, D30, D31, SD1, SD2, SD3, SD4, SD5
OUTPUTS: Z
PINORDER: D0, D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, D16, D17, D18, D19, D20, D21, D22, D23, D24, D25, D26, D27, D28, D29, D30, D31, SD1, SD2, SD3, SD4, SD5, Z
MINIMUM CELL AREA: 0.047

Truth Table:

INPUTS	OUTPUTS
SD[5:1]	Z
00000	D0
00001	D1
00010	D2
00011	D3
00100	D4
00101	D5
00110	D6
00111	D7
01000	D8
01001	D9

INPUTS	OUTPUTS
SD[5:1]	Z
10000	D16
10001	D17
10010	D18
10011	D19
10100	D20
10101	D21
10110	D22
10111	D23
11000	D24
11001	D25

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INPUTS	OUTPUTS
SD[5:1]	Z
01010	D10
01011	D11
01100	D12
01101	D13
01110	D14
01111	D15

INPUTS	OUTPUTS
SD[5:1]	Z
11010	D26
11011	D27
11100	D28
11101	D29
11110	D30
11111	D31

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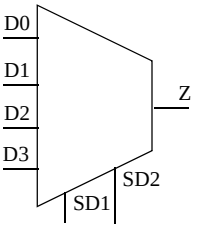
MUX41

4 to 1 Mux

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



MUX41

INPUTS: D0,D1,D2,D3,SD1,SD2
OUTPUTS: Z
PINORDER: D0 D1 D2 D3 SD1 SD2 Z
MINIMUM CELL AREA (2A/2T): 0.25
MINIMUM CELL AREA (Series 3): 0.125

Truth Table:

INPUTS						OUTPUTS
D0	D1	D2	D3	SD1	SD2	Z
0	X	X	X	0	0	0
1	X	X	X	0	0	1
X	0	X	X	1	0	0
X	1	X	X	1	0	1
X	X	0	X	0	1	0
X	X	1	X	0	1	1
X	X	X	0	1	1	0
X	X	X	1	1	1	1

X = Don’t care

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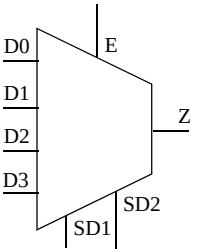
MUX41E

4 to 1 Mux with Enable

ORCA Series		
2	3	4
✓	✓	✓



MUX41E

INPUTS: D0,D1,D2,D3,SD1,SD2,E
OUTPUTS: Z
PINORDER: D0 D1 D2 D3 SD1 SD2 E Z
MINIMUM CELL AREA (2A/2T): 0.25
MINIMUM CELL AREA (Series 3): 0.125

Truth Table:

INPUTS							OUTPUTS
D0	D1	D2	D3	SD1	SD2	E	Z
X	X	X	X	X	X	0	0
0	X	X	X	0	0	1	0
1	X	X	X	0	0	1	1
X	0	X	X	1	0	1	0
X	1	X	X	1	0	1	1
X	X	0	X	0	1	1	0
X	X	1	X	0	1	1	1
X	X	X	0	1	1	1	0
X	X	X	1	1	1	1	1

X = Don’t care

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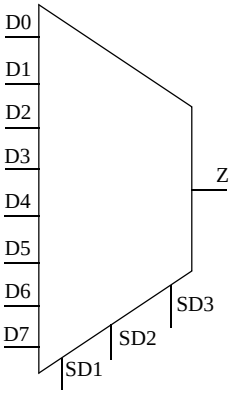
MUX81

8 to 1 Mux

ORCA Series/Lattice FPGA				
2	4	SC	XP	EC
✓	✓	✓	✓	✓



MUX81

INPUTS: D0,D1,D2,D3,D4,D5,D6,D7,SD1,SD2,SD3
OUTPUTS: Z
PINORDER:
D0 D1 D2 D3 D4 D5 D6 D7 SD1 SD2 SD3 Z
MINIMUM CELL AREA: 0.5

continued

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Truth Table:

INPUTS									OUTPUTS
D0	D1	D2	D3	D4	D5	D6	D7	SD[1:3]	Z
0	X	X	X	X	X	X	X	0 0 0	0
1	X	X	X	X	X	X	X	0 0 0	1
X	0	X	X	X	X	X	X	1 0 0	0
X	1	X	X	X	X	X	X	1 0 0	1
X	X	0	X	X	X	X	X	0 1 0	0
X	X	1	X	X	X	X	X	0 1 0	1
X	X	X	0	X	X	X	X	1 1 0	0
X	X	X	1	X	X	X	X	1 1 0	1
X	X	X	X	0	X	X	X	0 0 1	0
X	X	X	X	1	X	X	X	0 0 1	1
X	X	X	X	X	0	X	X	1 0 1	0
X	X	X	X	X	1	X	X	1 0 1	1
X	X	X	X	X	X	0	X	0 1 1	0
X	X	X	X	X	X	1	X	0 1 1	1
X	X	X	X	X	X	X	0	1 1 1	0
X	X	X	X	X	X	X	1	1 1 1	1

X = Don’t care

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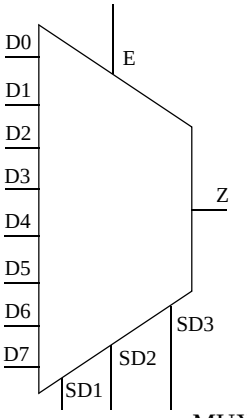
MUX81E

8 to 1 Mux with Enable

ORCA Series			
2	3	4	5
✓			



MUX81E

INPUTS: D0,D1,D2,D3,D4,D5,D6,D7,SD1,SD2,SD3,E
OUTPUTS: Z
PINORDER:
D0 D1 D2 D3 D4 D5 D6 D7 SD1 SD2 SD3 E Z
MINIMUM CELL AREA: 0.5

continued

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Truth Table:

INPUTS										OUTPUTS
D0	D1	D2	D3	D4	D5	D6	D7	SD[1:3]	E	Z
X	X	X	X	X	X	X	X	X X X	0	0
0	X	X	X	X	X	X	X	0 0 0	1	0
1	X	X	X	X	X	X	X	0 0 0	1	1
X	0	X	X	X	X	X	X	1 0 0	1	0
X	1	X	X	X	X	X	X	1 0 0	1	1
X	X	0	X	X	X	X	X	0 1 0	1	0
X	X	1	X	X	X	X	X	0 1 0	1	1
X	X	X	0	X	X	X	X	1 1 0	1	0
X	X	X	1	X	X	X	X	1 1 0	1	1
X	X	X	X	0	X	X	X	0 0 1	1	0
X	X	X	X	1	X	X	X	0 0 1	1	1
X	X	X	X	X	0	X	X	1 0 1	1	0
X	X	X	X	X	1	X	X	1 0 1	1	1
X	X	X	X	X	X	0	X	0 1 1	1	0
X	X	X	X	X	X	1	X	0 1 1	1	1
X	X	X	X	X	X	X	0	1 1 1	1	0
X	X	X	X	X	X	X	1	1 1 1	1	1

X = Don’t care

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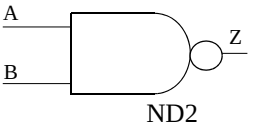
ND2

2 Input NAND Gate

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



INPUTS: A,B
OUTPUTS: Z
PINORDER: A B Z
MINIMUM CELL AREA (2A/2T): 0.125
MINIMUM CELL AREA (Series 3): 0.031

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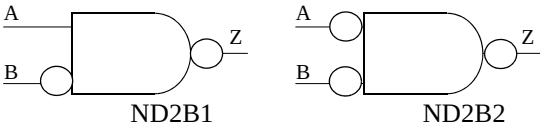
ND2B*x*

2 Input NAND Gates with *x* Inputs Inverting

ORCA Series		
2	3	4
✓		



INPUTS: A,B
OUTPUTS: Z
PINORDER: A B Z
MINIMUM CELL AREA: 0.125

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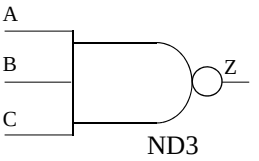
ND3

3 Input NAND Gate

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



INPUTS: A,B,C
OUTPUTS: Z
PINORDER: A B C Z
MINIMUM CELL AREA (2A/2T): 0.125
MINIMUM CELL AREA (Series 3): 0.047

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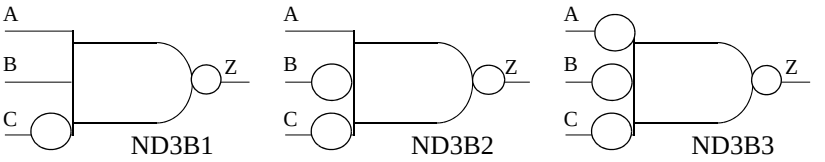
ND3B*x*

3 Input NAND Gates with *x* Inputs Inverting

ORCA Series		
2	3	4
✓		



INPUTS: A,B,C
OUTPUTS: Z
PINORDER: A B C Z
MINIMUM CELL AREA: 0.125

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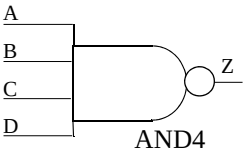
ND4

4 Input NAND Gate

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



INPUTS: A,B,C,D
OUTPUTS: Z
PINORDER: A B C D Z
MINIMUM CELL AREA (2A/2T): 0.175
MINIMUM CELL AREA (Series 3): 0.0625

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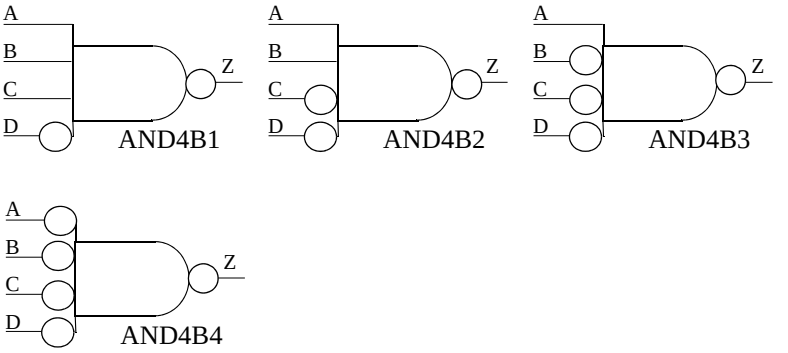
ND4B*x*

4 Input NAND Gates with *x* Inputs Inverting

ORCA Series		
2	3	4
✓		



INPUTS: A,B,C,D
OUTPUTS: Z
PINORDER: A B C D Z
MINIMUM CELL AREA: 0.175

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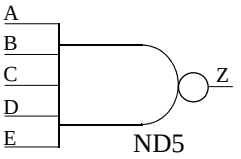
ND5

5 Input NAND Gate

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



INPUTS: A,B,C,D,E
OUTPUTS: Z
PINORDER: A B C D E Z
MINIMUM CELL AREA (2A/2T): 0.25
MINIMUM CELL AREA (Series 3): 0.125

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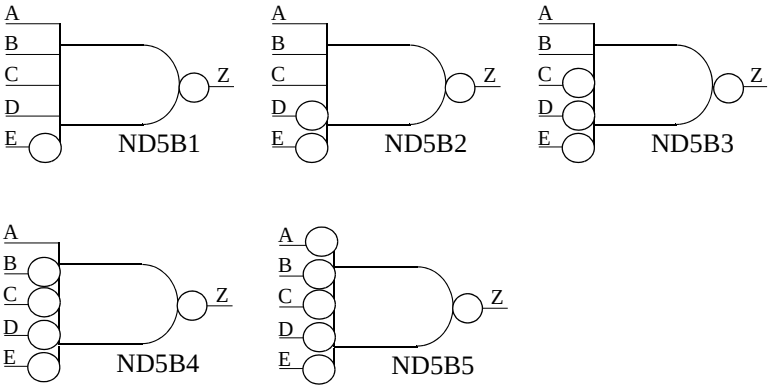
ND5B*x*

5 Input NAND Gates with *x* Inputs Inverting

ORCA Series		
2	3	4
✓		



INPUTS: A,B,C,D,E
OUTPUTS: Z
PINORDER: A B C D E Z
MINIMUM CELL AREA: 0.25

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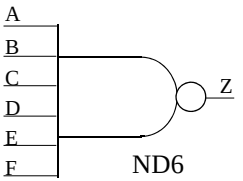
ND6

6 Input NAND Gate

ORCA Series		
2	3	4
✓		



INPUTS: A,B,C,D,E,F
OUTPUTS: Z
PINORDER: A B C D E F Z
MINIMUM CELL AREA: 0.5

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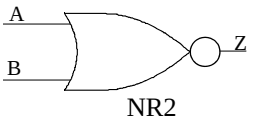
NR2

2 Input NOR Gate

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



NR2

INPUTS: A,B
OUTPUTS: Z
PINORDER: A B Z
MINIMUM CELL AREA (2A/2T) 0.125
MINIMUM CELL AREA (Series 3): 0.031

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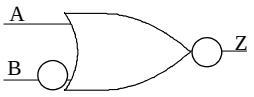
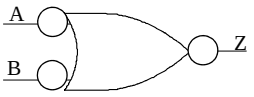
NR2B*x*

2 Input NOR Gates with *x* Inputs Inverting

ORCA Series		
2	3	4
✓		



NR2B1



NR2B2

INPUTS: A,B
OUTPUTS: Z
PINORDER: A B Z
MINIMUM CELL AREA: 0.125

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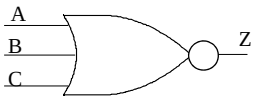
NR3

3 Input NOR Gate

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



NR3

INPUTS: A,B,C
OUTPUTS: Z
PINORDER: A B C Z
MINIMUM CELL AREA (2A/2T): 0.125
MINIMUM CELL AREA (Series 3): 0.047

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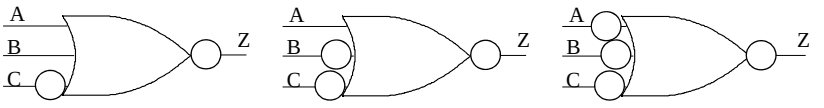
NR3B*x*

3 Input NOR Gates with *x* Inputs Inverting

ORCA Series		
2	3	4
✓		



NR3B1 NR3B2 NR3B3

INPUTS: A,B,C
OUTPUTS: Z
PINORDER: A B C Z
MINIMUM CELL AREA: 0.125

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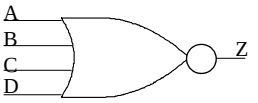
NR4

4 Input NOR Gate

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



NR4

INPUTS: A,B,C,D
OUTPUTS: Z
PINORDER: A B C D Z
MINIMUM cell AREA (2A/2T): 0.175
MINIMUM CELL AREA (Series 3): 0.0625

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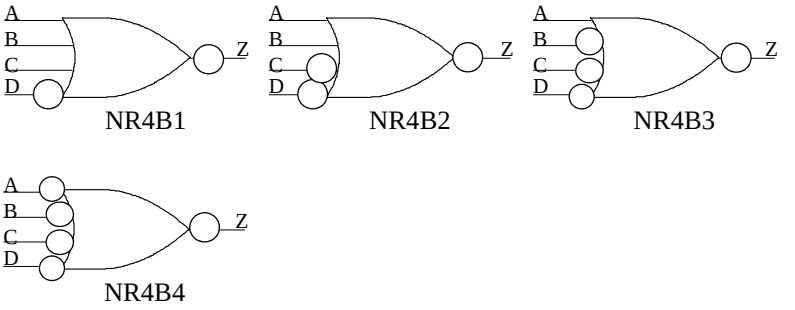
NR4B*x*

4 Input NOR Gates with *x* Inputs Inverting

ORCA Series		
2	3	4
✓		



INPUTS: A,B,C,D
OUTPUTS: Z
PINORDER: A B C D Z
MINIMUM CELL AREA: 0.175

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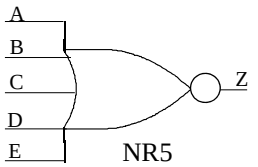
NR5

5 Input NOR Gate

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



INPUTS: A,B,C,D,E
OUTPUTS: Z
PINORDER: A B C D E Z
MINIMUM CELL AREA (2A/2T): 0.25
MINIMUM CELL AREA (Series 3): 0.125

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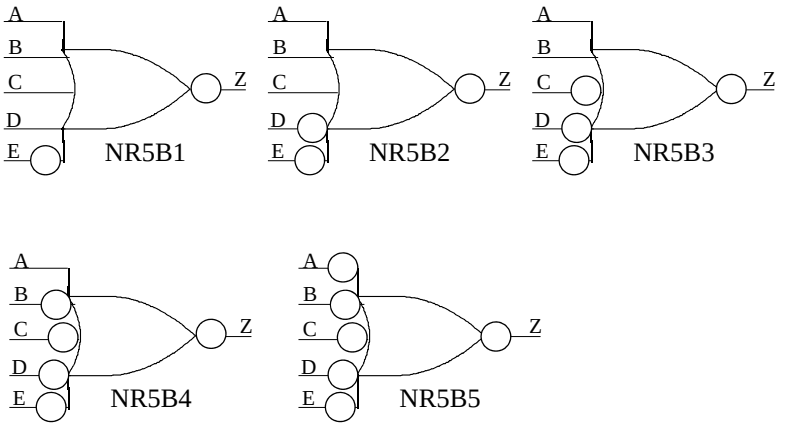
NR5B*x*

5 Input NOR Gates with *x* Inputs Inverting

ORCA Series		
2	3	4
✓		



INPUTS: A,B,C,D,E
OUTPUTS: Z
PINORDER: A B C D E Z
MINIMUM CELL AREA: 0.25

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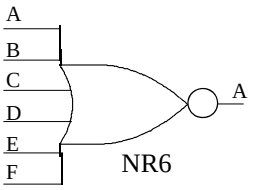
NR6

6 Input NOR Gate

ORCA Series		
2	3	4
✓		



INPUTS: A,B,C,D,E,F
OUTPUTS: Z
PINORDER: A B C D E F Z
MINIMUM CELL AREA: 0.5

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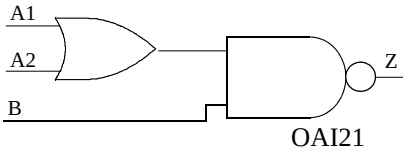
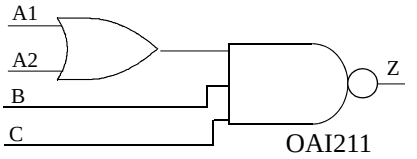
OAI

OR Array to AND Inverted

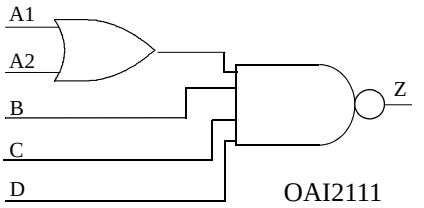
ORCA Series		
2	3	4
✓		



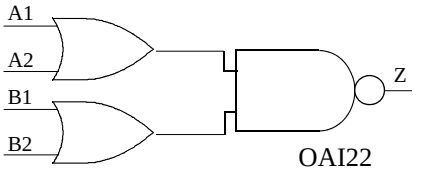
INPUTS: A1,A2,B
OUTPUTS: Z
PINORDER: A1 A2 B Z
MINIMUM CELL AREA: 0.125



INPUTS: A1,A2,B,C
OUTPUTS: Z
PINORDER: A1 A2 B C Z
MINIMUM CELL AREA: 0.175



INPUTS: A1,A2,B,C,D
OUTPUTS: Z
PINORDER: A1 A2 B C D Z
MINIMUM CELL AREA: 0.25



INPUTS: A1,A2,B1,B2
OUTPUTS: Z
PINORDER: A1 A2 B1 B2 Z
MINIMUM CELL AREA: 0.175

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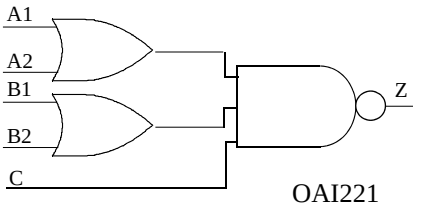
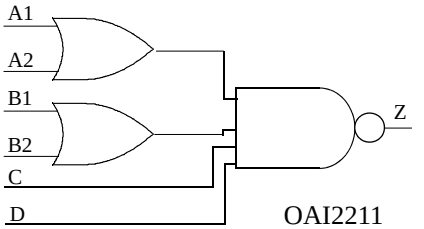


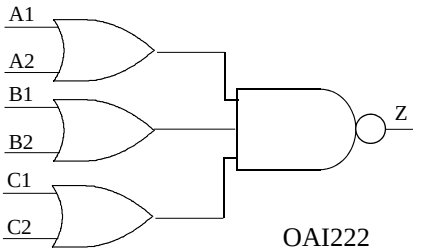
OAI221

INPUTS: A1,A2,B1,B2,C
OUTPUTS: Z
PINORDER: A1 A2 B1 B2 C Z
MINIMUM CELL AREA: 0.25



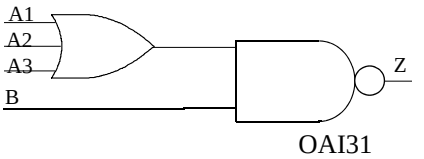
OAI2211

INPUTS: A1,A2,B1,B2,C,D
OUTPUTS: Z
PINORDER: A1 A2 B1 B2 C D Z
MINIMUM CELL AREA: 0.5



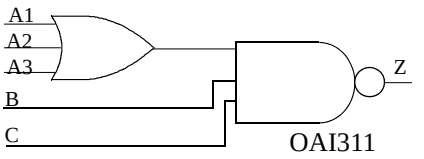
OAI222

INPUTS: A1,A2,B1,B2,C1,C2
OUTPUTS: Z
PINORDER:A1 A2 B1 B2 C1 C2 Z
MINIMUM CELL AREA: 0.5



OAI31

INPUTS: A1,A2,A3,B
OUTPUTS: Z
PINORDER: A1 A2 A3 B Z
MINIMUM CELL AREA: 0.175



OAI311

INPUTS: A1,A2,A3,B,C
OUTPUTS: Z
PINORDER: A1 A2 A3 B C Z
MINIMUM CELL AREA: 0.25

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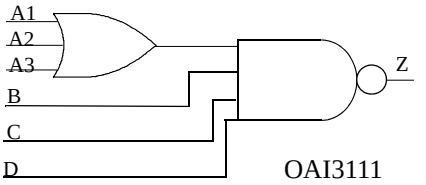
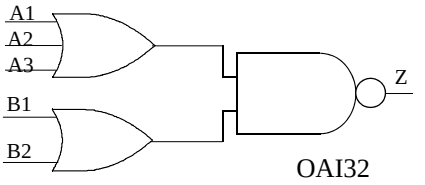
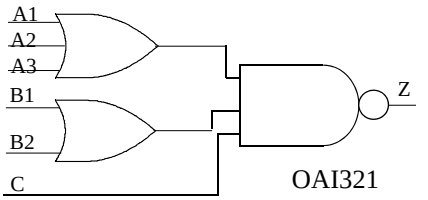


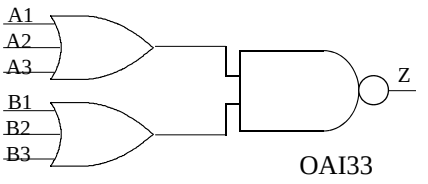
INPUTS: A1,A2,A3,B,C,D
OUTPUTS: Z
PINORDER: A1 A2 A3 B C D Z
MINIMUM CELL AREA: 0.5



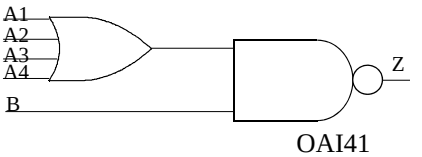
INPUTS: A1,A2,A3,B1,B2
OUTPUTS: Z
PINORDER: A1 A2 A3 B1 B2 Z
MINIMUM CELL AREA: 0.25



INPUTS: A1,A2,A3,B1,B2,C
OUTPUTS: Z
PINORDER: A1 A2 A3 B1 B2 C Z
MINIMUM CELL AREA: 0.5



INPUTS: A1,A2,A3,B1,B2,B3
OUTPUTS: Z
PINORDER:A1 A2 A3 B1 B2 B3 Z
MINIMUM CELL AREA: 0.5



INPUTS: A1,A2,A3,A4,B
OUTPUTS: Z
PINORDER: A1 A2 A3 A4 B Z
MINIMUM CELL AREA: 0.25

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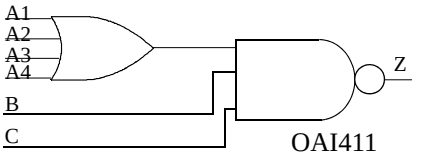
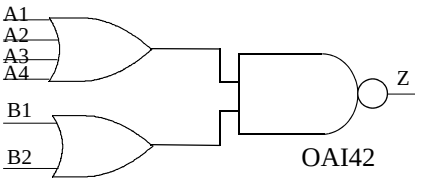


INPUTS: A1,A2,A3,A4,B,C
OUTPUTS: Z
PINORDER: A1 A2 A3 A4 B C Z
MINIMUM CELL AREA: 0.5



INPUTS: A1,A2,A3,A4,B1,B2
OUTPUTS: Z
PINORDER:A1 A2 A3 A4 B1 B2 Z
MINIMUM CELL AREA: 0.5

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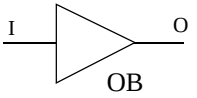
OB

Output Buffer

Lattice FPGA		
SC	XP	EC
✓	✓	✓



INPUTS: I
OUTPUTS: O
PINORDER: I O
MINIMUM CELL AREA: 0
ATTRIBUTES (LatticeSC)
IO_TYPE: LVDS, BLVDS25, MLVDS25, HYPT, LVPECL25, LVPECL33, LVCMOS25, LVCMOS25D, LVCMOS33, LVCMOS33D, LVCMOS18, LVCMOS18D, LVCMOS15, LVCMOS15D, LVCMOS12, LVCMOS12D, HSTL15_I, HSTL15_II, HSTL15D_I, HSTL15D_II, HSTL18_I, HSTL18_II, HSTL18D_I, HSTL18D_II, SSTL25_I, SSTL25_II, SSTL25D_I, SSTL25D_II, SSTL33_I, SSTL33_II, SSTL33D_I, SSTL33D_II, SSTL18_I, SSTL18_II, SSTL18D_I, SSTL18D_II, LVTTL33, LVTTL33D, PCI33, PCIX33, PCIX15, AGP1X33, AGP2X33
DRIVE: NA, 2, 4, 6, 8, 12, 16, 18, 20, 24
IMPEDANCEVCCIO: OFF (default), 20, 25, 33, 50, 100 (Impedance up)
IMPEDANCEGND: OFF (default), 20, 25, 33, 50, 100 (Impedance down)
TERMINATEVCCIO: OFF (default), 33, 50, 100 (Termination Up)
TERMINATEGND: OFF (default), 33, 50, 100 (Termination Down)
REFCIRCUIT: OFF, INTERNAL, EXTERNAL (for differential buffer)
DIFFRESISTOR: OFF(default), 100, 150, 200 (Only for differential buf
PULLMODE: UP, DOWN, NONE, KEEPER, PCICLAMP

Truth Table:

INPUTS	OUTPUTS
I	O
1	1
0	0

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INPUTS	OUTPUTS
I	O
Z	U

U = Unknown

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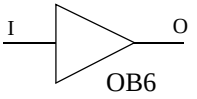
OB6

6mA Sink 3mA Source Sinklim Output Buffer

ORCA Series		
2	3	4
✓	✓	✓



INPUTS: I
OUTPUTS: O
PINORDER: I O
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVTTL, LVCMOS2 (default), LVDS, LVDSE, LVPECL, LVCMOS18, PCI, PECL, SSTL2, SSTL3, HSTL1, HSTL3, GTL, GTLPLUS
BUFMODE: SLEW (default), FAST
AMPSMODE: 6 (default), 12, 24
RESISTOR: OFF (default), ON (only for LVDS and LVPECL)

Note: BUFMODE and AMPSMODE are only supported when LEVELMODE = “LVTTL” or “LVCMOS2”.

Note: In Series 4, you can take the clock off-chip through a faster route by passing the attributes CKLMODE: SCLK, ECLK;

Truth Table:

INPUTS	OUTPUTS
I	O
1	1
0	0

When TSALL=0, O=Z

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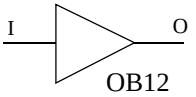
OB12

12mA Sink 6mA Source Slewlim Output Buffer

ORCA Series		
2	3	4
✓	✓	✓



INPUTS: I
OUTPUTS: O
PINORDER: I O
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVCMOS2
BUFMODE: SLEW
AMPSMODE: 12

Truth Table:

INPUTS	OUTPUTS
I	O
1	1
0	0

When TSALL=0, O=Z

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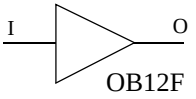
OB12F

12mA Sink 6mA Source Fast Output Buffer

ORCA Series		
2	3	4
✓	✓	✓



INPUTS: I
OUTPUTS: O
PINORDER: I O
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVCMOS2
BUFMODE: FAST
AMPSMODE: 12

Truth Table:

INPUTS	OUTPUTS
I	O
1	1
0	0

When TSALL=0, O=Z

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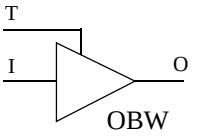
OBW

Output Buffer with Tristate

Lattice FPGA		
SC	XP	EC
✓	✓	✓



INPUTS: I, T
OUTPUTS: O
PINORDER: I O
MINIMUM CELL AREA: 0
ATTRIBUTES (LatticeSC)
IO_TYPE: LVDS, BLVDS25, MLVDS25, HYPT, LVPECL25, LVPECL33, LVCMOS25, LVCMOS25D, LVCMOS33, LVCMOS33D, LVCMOS18, LVCMOS18D, LVCMOS15, LVCMOS15D, LVCMOS12, LVCMOS12D, HSTL15_I, HSTL15_II, HSTL15D_I, HSTL15D_II, HSTL18_I, HSTL18_II, HSTL18D_I, HSTL18D_II, SSTL25_I, SSTL25_II, SSTL25D_I, SSTL25D_II, SSTL33_I, SSTL33_II, SSTL33D_I, SSTL33D_II, SSTL18_I, SSTL18_II, SSTL18D_I, SSTL18D_II, LVTTL33, LVTTL33D, PCI33, PCIX33, PCIX15, AGP1X33, AGP2X33
DRIVE: NA, 2, 4, 6, 8, 12, 16, 18, 20, 24
IMPEDANCEVCCIO: OFF (default), 20, 25, 33, 50, 100 (Impedance up)
IMPEDANCEGND: OFF (default), 20, 25, 33, 50, 100 (Impedance down)
TERMINATEVCCIO: OFF (default), 33, 50, 100 (Termination Up)
TERMINATEGND: OFF (default), 33, 50, 100 (Termination Down)
REFCIRCUIT: OFF, INTERNAL, EXTERNAL (for differential buffer)
DIFFRESISTOR: OFF(default), 100, 150, 200 (Only for differential buf
PULLMODE: UP, DOWN, NONE, KEEPER, PCICLAMP

Truth Table:

INPUTS		OUTPUTS
I	T	O
0	1	weak 0
1	1	weak 1

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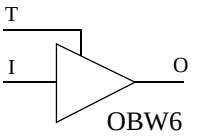
OBW6

6mA Sink 3mA Source Sinklim Output Buffer with Tristate

ORCA Series		
2	3	4
		✓



INPUTS: I, T
OUTPUTS: O
PINORDER: I O
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVTTL, LVCMOS2 (default)
BUFMODE: SLEW (default), FAST
AMPSMODE: 6 (default, 12, 24
SLKMODE: SCLK (default, ECLK

Note: BUFMODE and AMPSMODE are only supported when LEVELMODE = “LVTTL” or “LVCMOS2”.

Truth Table:

INPUTS		OUTPUTS
I	T	O
0	1	weak 0
1	1	weak 1

X = Don’t care
U = Unknown

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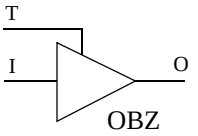
OBZ

Output Buffer with Tristate

Lattice FPGA		
SC	XP	EC
✓	✓	✓



INPUTS: I,T
OUTPUTS: O
PINORDER: I T O
MINIMUM CELL AREA: 0
ATTRIBUTES (LatticeSC)
IO_TYPE: LVDS, BLVDS25, MLVDS25, HYPT, LVPECL25, LVPECL33, LVCMOS25, LVCMOS25D, LVCMOS33, LVCMOS33D, LVCMOS18, LVCMOS18D, LVCMOS15, LVCMOS15D, LVCMOS12, LVCMOS12D, HSTL15_I, HSTL15_II, HSTL15D_I, HSTL15D_II, HSTL18_I, HSTL18_II, HSTL18D_I, HSTL18D_II, SSTL25_I, SSTL25_II, SSTL25D_I, SSTL25D_II, SSTL33_I, SSTL33_II, SSTL33D_I, SSTL33D_II, SSTL18_I, SSTL18_II, SSTL18D_I, SSTL18D_II, LVTTL33, LVTTL33D, PCI33, PCIX33, PCIX15, AGP1X33, AGP2X33
DRIVE: NA, 2, 4, 6, 8, 12, 16, 18, 20, 24
IMPEDANCEVCCIO: OFF (default), 20, 25, 33, 50, 100
IMPEDANCEGND: OFF (default), 20, 25, 33, 50, 100
TERMINATEVCCIO: OFF (default), 33, 50, 100
TERMINATEGND: OFF (default), 33, 50, 100
REFCIRCUIT: OFF, INTERNAL, EXTERNAL
PULLMODE: UP, DOWN, NONE, KEEPER, PCICLAMP

Truth Table:

INPUTS		OUTPUTS
I	T	O
X	1	Z
0	0	0
1	0	1

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X = Don’t care
When TSALL=0, O=Z
Note: For PU/PD buffers, when TSALL=0, O will be pulled up or pulled down, respectively. The letters PU (PD) in the buffer name indicate that a pull-up (pull-down) element is available. This is used to generate a logic high level (low level) for nodes that may be floating.

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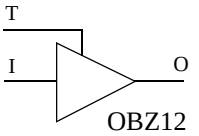
OBZ12

12mA Sink 6mA Source Slewlim Output Buffer with Tristate

ORCA Series		
2	3	4
✓	✓	✓



INPUTS: I,T
OUTPUTS: O
PINORDER: I T O
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVCMOS2
BUFMODE: SLEW
AMPSMODE: 12

Truth Table:

INPUTS		OUTPUTS
I	T	O
X	1	Z
0	0	0
1	0	1

X = Don’t care
When TSALL=0, O=Z
Note: For PU/PD buffers, when TSALL=0, O will be pulled up or pulled down, respectively. The letters PU (PD) in the buffer name indicate that a pull-up (pull-down) element is available. This is used to generate a logic high level (low level) for nodes that may be floating.

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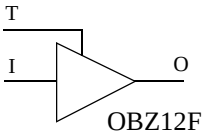
OBZ12F

12mA Sink 6mA Source Fast Output Buffer with Tristate

ORCA Series		
2	3	4
✓	✓	✓



INPUTS: I,T
OUTPUTS: O
PINORDER: I T O
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVCMOS2
BUFMODE: FAST
AMPSMODE: 12

Truth Table:

INPUTS		OUTPUTS
I	T	O
X	1	Z
0	0	0
1	0	1

X = Don’t care
When TSALL=0, O=Z
Note: For PU/PD buffers, when TSALL=0, O will be pulled up or pulled down, respectively. The letters PU (PD) in the buffer name indicate that a pull-up (pull-down) element is available. This is used to generate a logic high level (low level) for nodes that may be floating.

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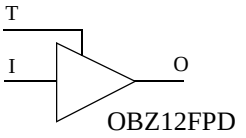
OBZ12FPD

12mA Sink 6mA Source Fast Output Buffer with Tristate and Pull-down

ORCA Series		
2	3	4
✓	✓	✓



INPUTS: I,T
OUTPUTS: O
PINORDER: I T O
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVCMOS2
BUFMODE: FAST
AMPSMODE: 12

Truth Table:

INPUTS		OUTPUTS
I	T	O
X	1	Z
0	0	0
1	0	1

X = Don't care
When TSALL=0, O=Z
Note: For PU/PD buffers, when TSALL=0, O will be pulled up or pulled down, respectively. The letters PU (PD) in the buffer name indicate that a pull-up (pull-down) element is available. This is used to generate a logic high level (low level) for nodes that may be floating.

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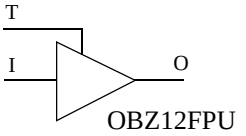
OBZ12FPU

12mA Sink 6mA Source Fast Output Buffer with Tristate and Pull-up

ORCA Series		
2	3	4
✓	✓	✓



INPUTS: I,T
OUTPUTS: O
PINORDER: I T O
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVCMOS2
BUFMODE: FAST
AMPSMODE: 12

Truth Table:

INPUTS		OUTPUTS
I	T	O
X	1	Z
0	0	0
1	0	1

X = Don’t care
When TSALL=0, O=Z
Note: For PU/PD buffers, when TSALL=0, O will be pulled up or pulled down, respectively. The letters PU (PD) in the buffer name indicate that a pull-up (pull-down) element is available. This is used to generate a logic high level (low level) for nodes that may be floating.

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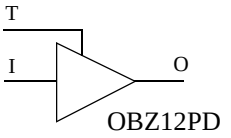
OBZ12PD

12mA Sink 6mA Source Slewlim Output Buffer with Tristate and Pull-down

ORCA Series		
2	3	4
✓	✓	✓



INPUTS: I,T
OUTPUTS: O
PINORDER: I T O
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVCMOS2
BUFMODE: SLEW
AMPSMODE: 12

Truth Table:

INPUTS		OUTPUTS
I	T	O
X	1	Z
0	0	0
1	0	1

X = Don’t care
When TSALL=0, O=Z
Note: For PU/PD buffers, when TSALL=0, O will be pulled up or pulled down, respectively. The letters PU (PD) in the buffer name indicate that a pull-up (pull-down) element is available. This is used to generate a logic high level (low level) for nodes that may be floating.

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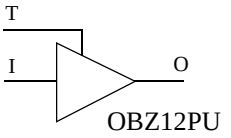
OBZ12PU

12mA Sink 6mA Source Slewlim Output Buffer with Tristate and Pull-up

ORCA Series		
2	3	4
✓	✓	✓



INPUTS: I,T
OUTPUTS: O
PINORDER: I T O
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVCMOS2
BUFMODE: SLEW
AMPSMODE: 12

Truth Table:

INPUTS		OUTPUTS
I	T	O
X	1	Z
0	0	0
1	0	1

X = Don’t care
When TSALL=0, O=Z
Note: For PU/PD buffers, when TSALL=0, O will be pulled up or pulled down, respectively. The letters PU (PD) in the buffer name indicate that a pull-up (pull-down) element is available. This is used to generate a logic high level (low level) for nodes that may be floating.

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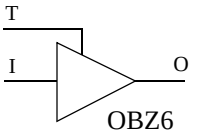
OBZ6

6mA Sink 3mA Source Sinklim Output Buffer with Tristate

ORCA Series		
2	3	4
✓	✓	✓



INPUTS: I,T
OUTPUTS: O
PINORDER: I T O
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVTTL, LVCMOS2 (default), LVCMOS18, PCI, PECL, SSTL2, SSTL3, HSTL1, HSTL3, GTL, GTLPLUS
BUFMODE: SLEW (default), FAST
AMPSMODE: 6 (default), 12, 24

Note: BUFMODE and AMPSMODE are only supported when LEVELMODE = “LVTTL” or “LVCMOS2”.

Truth Table:

INPUTS		OUTPUTS
I	T	O
X	1	Z
0	0	0
1	0	1

X = Don’t care
When TSALL=0, O=Z
Note: For PU/PD buffers, when TSALL=0, O will be pulled up or pulled down, respectively. The letters PU (PD) in the buffer name indicate that a pull-up (pull-down) element is available. This is used to generate a logic high level (low level) for nodes that may be floating.

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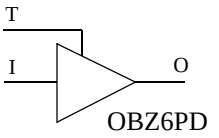
OBZ6PD

6mA Sink 3mA Source Sinklim Output Buffer with Tristate and Pull-down

ORCA Series		
2	3	4
✓	✓	✓



INPUTS: I,T
OUTPUTS: O
PINORDER: I T O
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVTTL, LVCMOS2 (default), LVCMOS18, PCI, PECL, SSTL2, SSTL3, HSTL1, HSTL3, GTL, GTLPLUS
BUFMODE: SLEW (default), FAST
AMPSMODE: 6 (default), 12, 24

Note: BUFMODE and AMPSMODE are only supported when LEVELMODE = “LVTTL” or “LVCMOS2”.

Truth Table:

INPUTS		OUTPUTS
I	T	O
X	1	Z
0	0	0
1	0	1

X = Don’t care
When TSALL=0, O=Z
Note: For PU/PD buffers, when TSALL=0, O will be pulled up or pulled down, respectively. The letters PU (PD) in the buffer name indicate that a pull-up (pull-down) element is available. This is used to generate a logic high level (low level) for nodes that may be floating.

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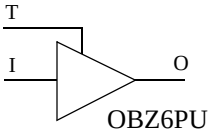
OBZ6PU

6mA Sink 3mA Source Sinklim Output Buffer with Tristate and Pull-up

ORCA Series		
2	3	4
✓	✓	✓



INPUTS: I,T
OUTPUTS: O
PINORDER: I T O
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
LEVELMODE: LVTTL, LVCMOS2 (default), LVCMOS18, PCI, PECL, SSTL2, SSTL3, HSTL1, HSTL3, GTL, GTLPLUS
BUFMODE: SLEW (default), FAST
AMPSMODE: 6 (default), 12, 24

Note: BUFMODE and AMPSMODE are only supported when LEVELMODE = “LVTTL” or “LVCMOS2”.

Truth Table:

INPUTS		OUTPUTS
I	T	O
X	1	Z
0	0	0
1	0	1

X = Don’t care
When TSALL=0, O=Z
Note: For PU/PD buffers, when TSALL=0, O will be pulled up or pulled down, respectively. The letters PU (PD) in the buffer name indicate that a pull-up (pull-down) element is available. This is used to generate a logic high level (low level) for nodes that may be floating.

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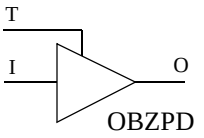
OBZPD

Output Buffer with Tristate and Pull-down

Lattice FPGA		
SC	XP	EC
✓	✓	✓



INPUTS: I,T
OUTPUTS: O
PINORDER: I T O
MINIMUM CELL AREA: 0
ATTRIBUTES (LatticeSC)
IO_TYPE: LVDS, BLVDS25, MLVDS25, HYPT, LVPECL25, LVPECL33, LVCMOS25, LVCMOS25D, LVCMOS33, LVCMOS33D, LVCMOS18, LVCMOS18D, LVCMOS15, LVCMOS15D, LVCMOS12, LVCMOS12D, HSTL15_I, HSTL15_II, HSTL15D_I, HSTL15D_II, HSTL18_I, HSTL18_II, HSTL18D_I, HSTL18D_II, SSTL25_I, SSTL25_II, SSTL25D_I, SSTL25D_II, SSTL33_I, SSTL33_II, SSTL33D_I, SSTL33D_II, SSTL18_I, SSTL18_II, SSTL18D_I, SSTL18D_II, LVTTL33, LVTTL33D, PCI33, PCIX33, PCIX15, AGP1X33, AGP2X33
DRIVE: NA, 2, 4, 6, 8, 12, 16, 18, 20, 24
IMPEDANCEVCCIO: OFF (default), 20, 25, 33, 50, 100
IMPEDANCEGND: OFF (default), 20, 25, 33, 50, 100
TERMINATEVCCIO: OFF (default), 33, 50, 100
TERMINATEGND: OFF (default), 33, 50, 100
REFCIRCUIT: OFF, INTERNAL, EXTERNAL
PULLMODE: UP, DOWN, NONE, KEEPER, PCICLAMP

Truth Table:

INPUTS		OUTPUTS
I	T	O
X	1	Z
0	0	0
1	0	1

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X = Don’t care
When TSALL=0, O=Z
Note: For PU/PD buffers, when TSALL=0, O will be pulled up or pulled down, respectively. The letters PU (PD) in the buffer name indicate that a pull-up (pull-down) element is available. This is used to generate a logic high level (low level) for nodes that may be floating.

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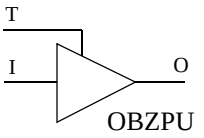
OBZPU

Output Buffer with Tristate and Pull-up

Lattice FPGA		
SC	XP	EC
✓	✓	✓



INPUTS: I,T
OUTPUTS: O
PINORDER: I T O
MINIMUM CELL AREA: 0
ATTRIBUTES (LatticeSC)
IO_TYPE: LVDS, BLVDS25, MLVDS25, HYPT, LVPECL25, LVPECL33, LVCMOS25, LVCMOS25D, LVCMOS33, LVCMOS33D, LVCMOS18, LVCMOS18D, LVCMOS15, LVCMOS15D, LVCMOS12, LVCMOS12D, HSTL15_I, HSTL15_II, HSTL15D_I, HSTL15D_II, HSTL18_I, HSTL18_II, HSTL18D_I, HSTL18D_II, SSTL25_I, SSTL25_II, SSTL25D_I, SSTL25D_II, SSTL33_I, SSTL33_II, SSTL33D_I, SSTL33D_II, SSTL18_I, SSTL18_II, SSTL18D_I, SSTL18D_II, LVTTL33, LVTTL33D, PCI33, PCIX33, PCIX15, AGP1X33, AGP2X33
DRIVE: NA, 2, 4, 6, 8, 12, 16, 18, 20, 24
IMPEDANCEVCCIO: OFF (default), 20, 25, 33, 50, 100
IMPEDANCEGND: OFF (default), 20, 25, 33, 50, 100
TERMINATEVCCIO: OFF (default), 33, 50, 100
TERMINATEGND: OFF (default), 33, 50, 100
REFCIRCUIT: OFF, INTERNAL, EXTERNAL
PULLMODE: UP, DOWN, NONE, KEEPER, PCICLAMP

Truth Table:

INPUTS		OUTPUTS
I	T	O
X	1	Z
0	0	0
1	0	1

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X = Don’t care
When TSALL=0, O=Z
Note: For PU/PD buffers, when TSALL=0, O will be pulled up or pulled down, respectively. The letters PU (PD) in the buffer name indicate that a pull-up (pull-down) element is available. This is used to generate a logic high level (low level) for nodes that may be floating.

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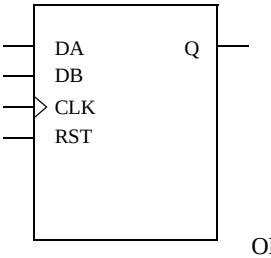
ODDRA

Output DDR

Lattice FPGA		
SC	XP	EC
✓		



ODDRA

INPUTS: DA, DB, CLK, RST
OUTPUTS: Q
PINORDER: D0, D1, CLK, RST, Q
ATTRIBUTES
LSRMODE: EDGE, LOCAL
CLKMODE: SCLK, ECLK
REGSET: RESET, SET

Description:

Output DDR data (positive edge and negative edge data) to the buffer.

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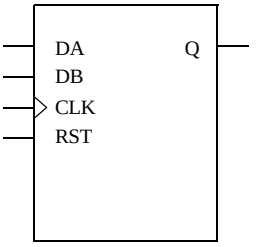
ODDRXA

Output DDR

Lattice FPGA		
SC	XP	EC
✓		



ODDRXA

INPUTS: DA, DB, CLK, RST
OUTPUTS: Q
PINORDER: DA, DB, CLK, RST, Q
ATTRIBUTES
LSRMODE: EDGE, LOCAL
CLKMODE: SCLK, ECLK
REGSET: RESET, SET

Description:

Output DDR data with half cycle clock domain transfer.

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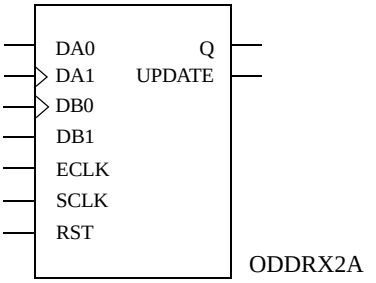
ODDRX2A

Output DDR

Lattice FPGA		
SC	XP	EC
✓		



ODDRX2A

INPUTS: DA0, DA1, DB0, DB1, ECLK, SCLK, RST
OUTPUTS: Q, UPDATE
PINORDER: DA0, DA1, DB0, DB1, ECLK, SCLK, RST, Q, UPDATE
MINIMUM CELL AREA: 0
ATTRIBUTES
LSRMODE: EDGE, LOCAL
UPDT : POS, NEG
REGSET: RESET, SET

Description:

Outputs DDR data to the buffer through the shift register and clock domain transfer from primary clock to edge clock.

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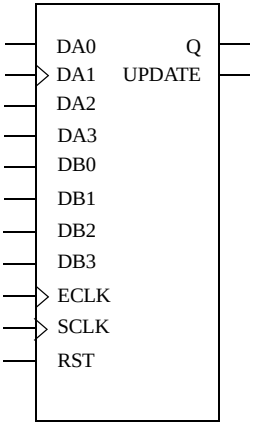
ODDRX4A

Output DDR

Lattice FPGA		
SC	XP	EC
✓		



ODDRX4A

INPUTS: DA0, DA1, DA2, DA3, DB0, DB1, DB2, DB3, ECLK, SCLK, RST
OUTPUTS: Q, UPDATE
PINORDER: DA0, DA1, DA2, DA3, DB0, DB1, DB2, DB3, ECLK, SCLK, RST, Q, UPDATE
MINIMUM CELL AREA: 0
ATTRIBUTES
LSRMODE: EDGE, LOCAL
UPDT : POS, NEG
REGSET: RESET, SET

Description:

Outputs DDR data to the buffer through the shift register and clock domain transfer from primary clock to edge clock.

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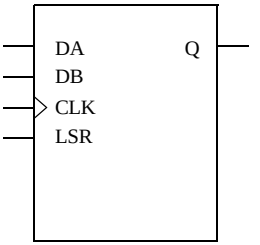
ODDRXB

Output DDR

Lattice FPGA		
SC	XP	EC
	✓	✓



ODDRXB

INPUTS: DA, DB, CLK, LSR
OUTPUTS: Q
PINORDER: DA, DB, CLK, LSR, Q
MINIMUM CELL AREA: 0
ATTRIBUTES

Description:

Output DDR data with half cycle clock domain transfer.

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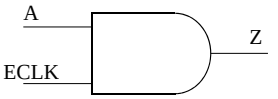
OEAND2

2 Input AND Gate with Express Clock (used in PIC area only)

ORCA Series		
2	3	4
	✓	✓



OEAND2

INPUTS: A,ECLK
OUTPUTS: Z
PINORDER: A ECLK Z
MINIMUM CELL AREA: 0

Note: This element must be paired with an output or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

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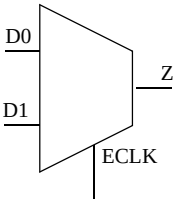
OEMUX21

2 to 1 Mux with Express Clock (used in PIC area only)

ORCA Series		
2	3	4
	✓	✓



OEMUX21

INPUTS: D0,D1,ECLK
OUTPUTS: Z
PINORDER: D0 D1 ECLK Z
MINIMUM CELL AREA: 0

Note: This element must be paired with an output or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element. In 4E designs, this element must be paired with a flip-flop or a latch in addition to the output/bidirectional buffer.

Truth Table:

INPUTS			OUTPUTS
D0	D1	ECLK	Z
0	X	0	0
1	X	0	1
X	0	1	0
X	1	1	1

X = Don’t care

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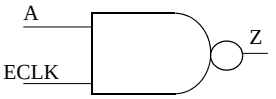
OEND2

2 Input NAND Gate with Express Clock (used in PIC area only)

ORCA Series		
2	3	4
	✓	✓



OEND2

INPUTS: A,ECLK
OUTPUTS: Z
PINORDER: A ECLK Z
MINIMUM CELL AREA: 0

Note: This element must be paired with an output or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

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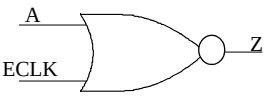
OENR2

2 Input NOR Gate with Express Clock (used in PIC area only)

ORCA Series		
2	3	4
	✓	✓



OENR2

INPUTS: A,ECLK
OUTPUTS: Z
PINORDER: A ECLK Z
MINIMUM CELL AREA: 0

Note: This element must be paired with an output or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

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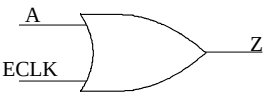
OEOR2

2 Input OR Gate with Express Clock (used in PIC area only)

ORCA Series		
2	3	4
	✓	✓



OEOR2

INPUTS: A,ECLK
OUTPUTS: Z
PINORDER: A ECLK Z
MINIMUM CELL AREA: 0

Note: This element must be paired with an output or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

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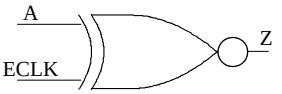
OEXNOR2

2 Input Exclusive NOR Gate with Express Clock (used in PIC area only)

ORCA Series		
2	3	4
	✓	✓



OEXNOR2

INPUTS: A,ECLK
OUTPUTS: Z
PINORDER: A ECLK Z
MINIMUM CELL AREA: 0

Note: This element must be paired with an output or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

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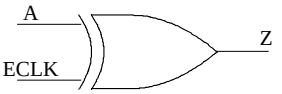
OEXOR2

2 Input Exclusive OR Gate with Express Clock (used in PIC area only)

ORCA Series		
2	3	4
	✓	✓



OEXOR2

INPUTS: A,ECLK
OUTPUTS: Z
PINORDER: A ECLK Z
MINIMUM CELL AREA: 0

Note: This element must be paired with an output or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

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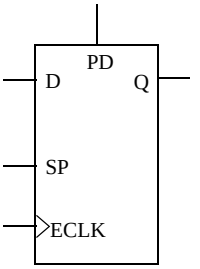
OFE1P3BX

Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Asynchronous Preset, and Express Clock (used in output PIC area only)

ORCA Series/Lattice FPGA				
3	4	SC	XP	EC
✓	✓	✓	✓	✓



OFE1P3BX

INPUTS: D,SP,ECLK,PD
OUTPUTS: Q
PINORDER: D SP ECLK PD Q
MINIMUM CELL AREA: 0

Note: This element must be paired with an output or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

Truth Table:

INPUTS				OUTPUTS
D	SP	ECLK	PD	Q
X	0	X	0	Q
X	X	X	1	1
0	1	↑	0	0
1	1	↑	0	1

X = Don’t care
When GSR=0, Q=1 (D=SP=ECLK=PD=X)

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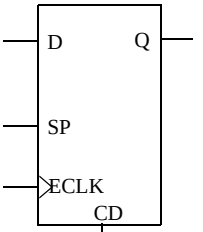
OFE1P3DX

Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Asynchronous Clear, and Express Clock (used in output PIC area only)

ORCA Series/Lattice FPGA				
3	4	SC	XP	EC
✓	✓	✓	✓	✓



OFE1P3DX

INPUTS: D,SP,ECLK,CD
OUTPUTS: Q
PINORDER: D SP ECLK CD Q
MINIMUM CELL AREA: 0

Note: This element must be paired with an output or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

Truth Table:

INPUTS				OUTPUTS
D	SP	ECLK	CD	Q
X	0	X	0	Q
X	X	X	1	0
0	1	↑	0	0
1	1	↑	0	1

X = Don’t care
When GSR=0, Q=0 (D=SP=ECLK=CD=X)

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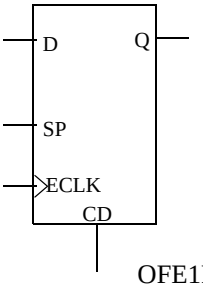
OFE1P3IX

Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Clear, Positive Level Enable (Clear overrides Enable), and Express Clock (used in output PIC area only)

ORCA Series/Lattice FPGA				
3	4	SC	XP	EC
✓	✓	✓	✓	✓



OFE1P3IX

INPUTS: D,SP,ECLK,CD
OUTPUTS: Q
PINORDER: D SP ECLK CD Q
MINIMUM CELL AREA: 0

Note: This element must be paired with an output or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

Truth Table:

INPUTS				OUTPUTS
D	SP	ECLK	CD	Q
X	0	X	0	Q
X	X	↑	1	0
0	1	↑	0	0
1	1	↑	0	1

X = Don’t care
When GSR=0, Q=0 (D=SP=ECLK=CD=X)

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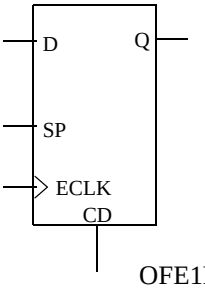
OFE1P3IZ

Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Synchronous Clear, and Express Clock (used in output PIC area only)

ORCA Series		
2	3	4
	✓	✓



OFE1P3IZ

INPUTS: D,SP,ECLK,CD
OUTPUTS: Q
PINORDER: D SP ECLK CD Q
MINIMUM CELL AREA: 0

Note: This element must be paired with an output or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

Truth Table:

INPUTS				OUTPUTS
D	SP	ECLK	CD	Q
X	0	X	X	Q
X	1	↑	1	0
0	1	↑	0	0
1	1	↑	0	1

X = Don’t care
When GSR=0, Q=0 (D=SP=ECLK=CD=X)

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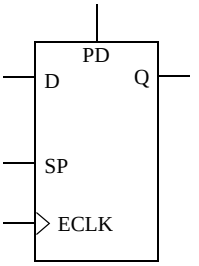
OFE1P3JX

Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Preset, Positive Level Enable (Preset overrides Enable), and Express Clock (used in output PIC area only)

ORCA Series/Lattice FPGA				
3	4	SC	XP	EC
✓	✓	✓	✓	✓



OFE1P3JX

INPUTS: D,SP,ECLK,PD
OUTPUTS: Q
PINORDER: D SP ECLK PD Q
MINIMUM CELL AREA: 0

Note: This element must be paired with an output or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

Truth Table:

INPUTS				OUTPUTS
D	SP	ECLK	PD	Q
X	0	X	0	Q
X	X	↑	1	1
0	1	↑	0	0
1	1	↑	0	1

X = Don’t care
When GSR=0, Q=1 (D=SP=ECLK=PD=X)

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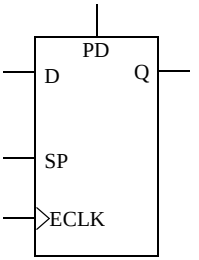
OFE1P3JZ

Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Synchronous Preset, and Express Clock (used in output PIC area only)

ORCA Series		
2	3	4
	✓	✓



OFE1P3JZ

INPUTS: D,SP,ECLK,PD
OUTPUTS: Q
PINORDER: D SP ECLK PD Q
MINIMUM CELL AREA: 0

Note: This element must be paired with an output or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

Truth Table:

INPUTS				OUTPUTS
D	SP	ECLK	PD	Q
X	0	X	X	Q
X	1	↑	1	1
0	1	↑	0	0
1	1	↑	0	1

X = Don’t care
When GSR=0, Q=1 (D=SP=ECLK=PD=X)

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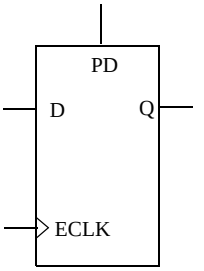
OFE1S1B

Output Positive Level Data Latch with Positive Level Asynchronous Preset and Express Clock (used in input PIC area only)

ORCA Series		
2	3	4
	✓	✓



OFE1S1B

Note: This element must be paired with an output or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

INPUTS: D,ECLK,PD
OUTPUTS: Q
PINORDER: D ECLK PD Q
MINIMUM CELL AREA: 0

Truth Table:

INPUTS			OUTPUTS
D	ECLK	PD	Q
X	0	0	Q
X	X	1	1
0	1	0	0
1	1	0	1

X= Don’t care
When GSR=0, Q=1 (D=ECLK=PD=X)

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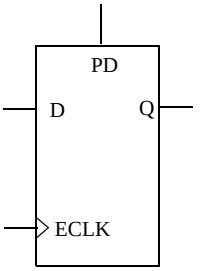
OFE1S1D

Output Positive Level Data Latch with Positive Level Asynchronous Clear and Express Clock (used in input PIC area only)

ORCA Series		
2	3	4
	✓	✓



OFE1S1D

Note: This element must be paired with an output or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

INPUTS: D,ECLK,PD
OUTPUTS: Q
PINORDER: D ECLK PD Q
MINIMUM CELL AREA: 0

Truth Table:

INPUTS			OUTPUTS
D	ECLK	PD	Q
X	0	0	Q
X	X	1	1
0	1	0	0
1	1	0	1

X= Don’t care
When GSR=0, Q=1 (D=ECLK=PD=X)

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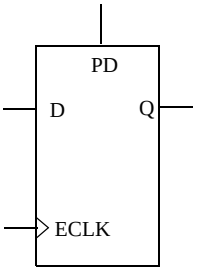
OFE1S1I

Output Positive Level Data Latch with Positive Level Asynchronous Preset and Express Clock (used in input PIC area only)

ORCA Series		
2	3	4
	✓	✓



OFE1S1I

Note: This element must be paired with an output or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

INPUTS: D,ECLK,PD
OUTPUTS: Q
PINORDER: D ECLK PD Q
MINIMUM CELL AREA: 0

Truth Table:

INPUTS			OUTPUTS
D	ECLK	PD	Q
X	0	0	Q
X	X	1	1
0	1	0	0
1	1	0	1

X= Don’t care
When GSR=0, Q=1 (D=ECLK=PD=X)

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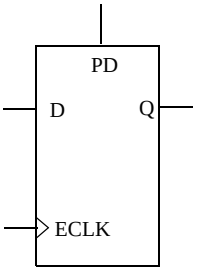
OFE1S1J

Output Positive Level Data Latch with Positive Level Asynchronous Preset and Express Clock (used in input PIC area only)

ORCA Series		
2	3	4
	✓	✓



OFE1S1J

Note: This element must be paired with an output or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

INPUTS: D,ECLK,PD
OUTPUTS: Q
PINORDER: D ECLK PD Q
MINIMUM CELL AREA: 0

Truth Table:

INPUTS			OUTPUTS
D	ECLK	PD	Q
X	0	0	Q
X	X	1	1
0	1	0	0
1	1	0	1

X= Don’t care
When GSR=0, Q=1 (D=ECLK=PD=X)

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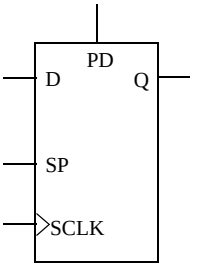
OFS1P3BX

Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Asynchronous Preset, and System Clock (used in output PIC area only)

ORCA Series/Lattice FPGA				
3	4	SC	XP	EC
✓	✓	✓	✓	✓



OFS1P3BX

INPUTS: D, SP,SCLK,PD
OUTPUTS: Q
PINORDER: D SP SCLK PD Q
MINIMUM CELL AREA: 0

Note: This element must be paired with an output or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

Truth Table:

INPUTS				OUTPUTS
D	SP	SCLK	PD	Q
X	0	X	0	Q
X	X	X	1	1
0	1	↑	0	0
1	1	↑	0	1

X = Don’t care
When GSR=0, Q=1 (D=SP=SCLK=PD=X)

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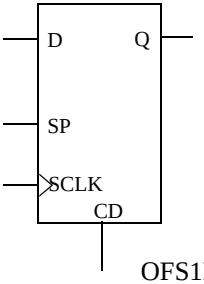
OFS1P3DX

Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Asynchronous Clear, and System Clock (used in output PIC area only)

ORCA Series/Lattice FPGA				
3	4	SC	XP	EC
✓	✓	✓	✓	✓



OFS1P3DX

INPUTS: D, SP,SCLK,CD
OUTPUTS: Q
PINORDER: D SP SCLK CD Q
MINIMUM CELL AREA: 0

Note: This element must be paired with an output or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

Truth Table:

INPUTS				OUTPUTS
D	SP	SCLK	CD	Q
X	0	X	0	Q
X	X	X	1	0
0	1	↑	0	0
1	1	↑	0	1

X = Don’t care
When GSR=0, Q=0 (D=SP=SCLK=CD=X)

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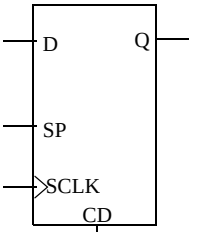
OFS1P3IX

Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Clear, Positive Level Enable (Clear overrides Enable), and System Clock (used in output PIC area only)

ORCA Series/Lattice FPGA				
3	4	SC	XP	EC
✓	✓	✓	✓	✓



OFS1P3IX

INPUTS: D, SP,SCLK,CD
OUTPUTS: Q
PINORDER: D SP SCLK CD Q
MINIMUM CELL AREA: 0

Note: This element must be paired with an output or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

Truth Table:

INPUTS				OUTPUTS
D	SP	SCLK	CD	Q
X	0	X	0	Q
X	X	↑	1	0
0	1	↑	0	0
1	1	↑	0	1

X = Don’t care
When GSR=0, Q=0 (D=SP=SCLK=CD=X)

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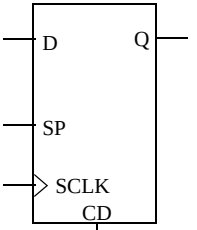
OFS1P3IZ

Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Synchronous Clear, and System Clock (used in output PIC area only)

ORCA Series		
2	3	4
	✓	✓



OFS1P3IZ

INPUTS: D, SP,SCLK,CD
OUTPUTS: Q
PINORDER: D SP SCLK CD Q
MINIMUM CELL AREA: 0

Note: This element must be paired with an output or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

Truth Table:

INPUTS				OUTPUTS
D	SP	SCLK	CD	Q
X	0	X	X	Q
X	1	↑	1	0
0	1	↑	0	0
1	1	↑	0	1

X = Don’t careOFS1P3JX

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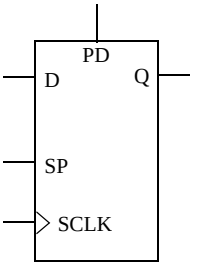
OFS1P3JX

Positive Edge Triggered D Flip-Flop with Positive Level Synchronous Preset, Positive Level Enable (Preset overrides Enable), and System Clock (used in output PIC area only)

ORCA Series/Lattice FPGA				
3	4	SC	XP	EC
✓	✓	✓	✓	✓



OFS1P3JX

INPUTS: D, SP,SCLK,PD
OUTPUTS: Q
PINORDER: D SP SCLK PD Q
MINIMUM CELL AREA: 0

Note: This element must be paired with an output or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

Truth Table:

INPUTS				OUTPUTS
D	SP	SCLK	PD	Q
X	0	X	0	Q
X	X	↑	1	1
0	1	↑	0	0
1	1	↑	0	1

X = Don’t care
When GSR=0, Q=1 (D=SP=SCLK=PD=X)

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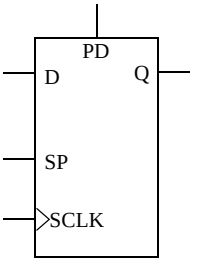
OFS1P3JZ

Positive Edge Triggered D Flip-Flop with Positive Level Enable, Positive Level Synchronous Preset, and System Clock (used in output PIC area only)

ORCA Series		
2	3	4
	✓	✓



OFS1P3JZ

INPUTS: D, SP,SCLK,PD
OUTPUTS: Q
PINORDER: D SP SCLK PD Q
MINIMUM CELL AREA: 0

Note: This element must be paired with an output or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

Truth Table:

INPUTS				OUTPUTS
D	SP	SCLK	PD	Q
X	0	X	X	Q
X	1	↑	1	1
0	1	↑	0	0
1	1	↑	0	1

X = Don’t care
When GSR=0, Q=1 (D=SP=SCLK=PD=X)

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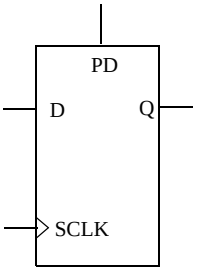
OFS1S1B

Output Positive Level Data Latch with Positive Level Asynchronous Preset and System Clock (used in output PIC area only)

ORCA Series		
2	3	4
	✓	✓



OFS1S1B

Note: This element must be paired with an output or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

INPUTS: D, SCLK,PD
OUTPUTS: Q
PINORDER: D SCLK PD Q
MINIMUM CELL AREA: 0

Truth Table:

INPUTS			OUTPUTS
D	SCLK	PD	Q
X	0	0	Q
X	X	1	1
0	1	0	0
1	1	0	1

X= Don’t care
When GSR=0, Q=1 (D=SCLK=PD=X)

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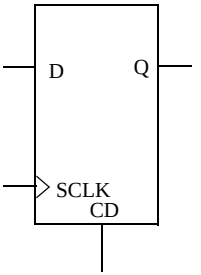
OFS1S1D

Output Positive Level Data Latch with Positive Level Asynchronous Clear and System Clock (used in output PIC area only)

ORCA Series		
2	3	4
	✓	✓



OFS1S1D

Note: This element must be paired with an output or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

INPUTS: D, SCLK,CD
OUTPUTS: Q
PINORDER: D SCLK CD Q
MINIMUM CELL AREA: 0

Truth Table:

INPUTS			OUTPUTS
D	SCLK	CD	Q
X	0	0	Q
X	X	1	0
0	1	0	0
1	1	0	1

X = Don’t care
When GSR=0, Q=0 (D=SCLK=CD=X)

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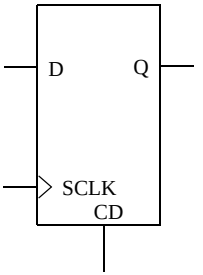
OFS1S1I

Output Positive Level Data Latch with Positive Level Synchronous Clear and System Clock (used in output PIC area only)

ORCA Series		
2	3	4
	✓	✓



OFS1S1I

Note: This element must be paired with an output or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

INPUTS: D, SCLK,CD
OUTPUTS: Q
PINORDER: D SCLK CD Q
MINIMUM CELL AREA: 0

Truth Table:

INPUTS			OUTPUTS
D	SCLK	CD	Q
X	0	0	Q
X	1	1	0
0	1	0	0
1	1	0	1

X = Don’t care
When GSR=0, Q=0 (D=SCLK=CD=X)

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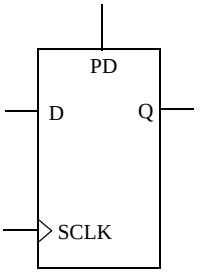
OFS1S1J

Output Positive Level Data Latch with Positive Level Synchronous Preset and System Clock (used in output PIC area only)

ORCA Series		
2	3	4
	✓	✓



OFS1S1J

Note: This element must be paired with an output or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

INPUTS: D, SCLK,PD
OUTPUTS: Q
PINORDER: D SCLK PD Q
MINIMUM CELL AREA: 0

Truth Table:

INPUTS			OUTPUTS
D	SCLK	CD	Q
X	0	0	Q
X	1	1	0
0	1	0	0
1	1	0	1

X = Don’t care
When GSR=0, Q=0 (D=SCLK=CD=X)

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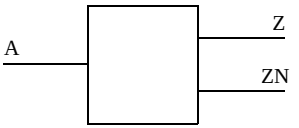
OLVDS

LVDS Output Buffer

ORCA Series/Lattice			
2	3	4	SC
		✓	✓



OLVDS

INPUTS: A
OUTPUTS: Z, ZN
PINORDER: A, Z, ZN
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 4 only)
RESISTOR: OFF (default), ON

Note: If you wish to use the LVPECL or LVDSE buffer, pass the property "LEVELMODE=LVPECL | LVDSE" in both ILVDS and OLVDS elements.

Truth Table:

INPUTS	OUPUTS	
A	Z	ZN
0	0	1
1	1	0

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OPAD

Output PAD

ORCA Series		
2	3	4
✓		

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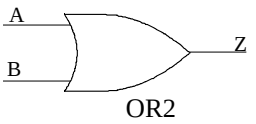
OR2

2 Input OR Gate

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



OR2

INPUTS: A,B
OUTPUTS: Z
PINORDER: A B Z
MINIMUM CELL AREA (Series 2): 0.125
MINIMUM CELL AREA (Series 3): 0.031

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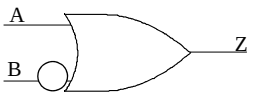
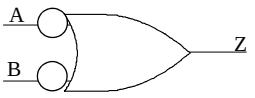
OR2B*x*

2 Input OR Gates with *x* Inputs Inverting

ORCA Series		
2	3	4
✓		



OR2B1



OR2B2

INPUTS: A,B
OUTPUTS: Z
PINORDER: A B Z
MINIMUM CELL AREA: 0.125

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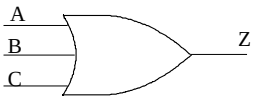
OR3

3 Input OR Gate

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



OR3

INPUTS: A,B,C
OUTPUTS: Z
PINORDER: A B C Z
MINIMUM CELL AREA (Series 2): 0.125
MINIMUM CELL AREA (Series 3 and Series 4): 0.047

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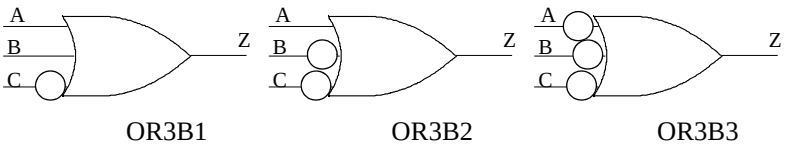
OR3B*x*

3 Input OR Gates with *x* Inputs Inverting

ORCA Series		
2	3	4
✓		



OR3B1 OR3B2 OR3B3

INPUTS: A,B,C
OUTPUTS: Z
PINORDER: A B C Z
MINIMUM CELL AREA: 0.125

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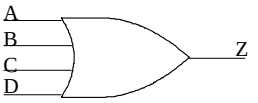
OR4

4 Input OR Gate

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



OR4

INPUTS: A,B,C,D
OUTPUTS: Z
PINORDER: A B C D Z
MINIMUM CELL AREA (Series 2): 0.175
MINIMUM CELL AREA (Series 3 and Series 4): 0.0625

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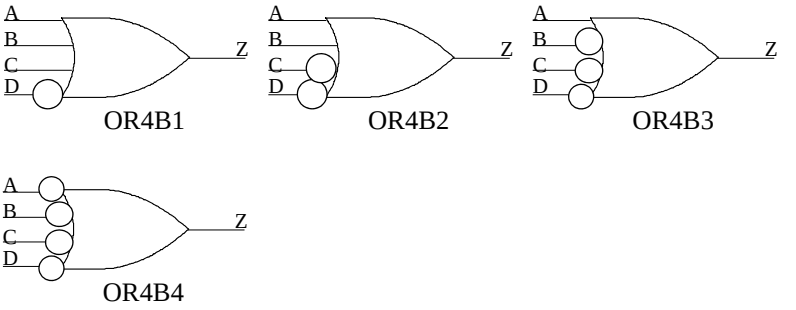
OR4B*x*

4 Input OR Gates with *x* Inputs Inverting

ORCA Series		
2	3	4
✓		



INPUTS: A,B,C,D
OUTPUTS: Z
PINORDER: A B C D Z
MINIMUM CELL AREA: 0.175

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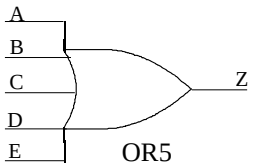
OR5

5 Input OR Gate

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



INPUTS: A,B,C,D,E
OUTPUTS: Z
PINORDER: A B C D E Z
MINIMUM CELL AREA (Series 2): 0.25
MINIMUM CELL AREA (Series 3 and Series 4): 0.125

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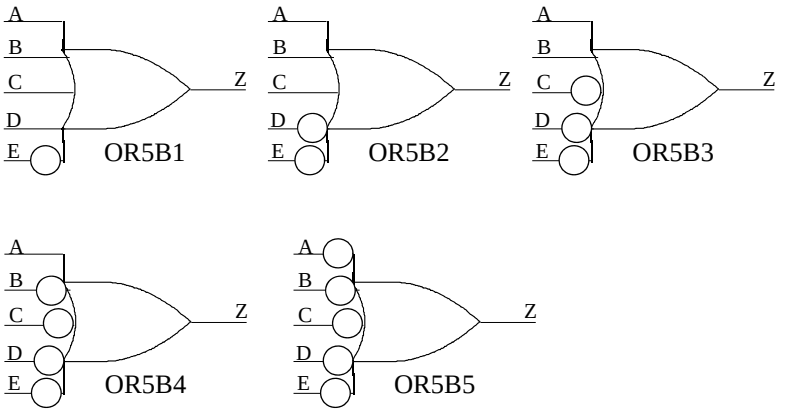
OR5B*x*

5 Input OR Gates with *x* Inputs Inverting

ORCA Series		
2	3	4
✓		



INPUTS: A,B,C,D,E
OUTPUTS: Z
PINORDER: A B C D E Z
MINIMUM CELL AREA: 0.25

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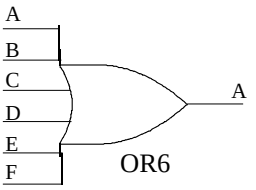
OR6

6 Input OR Gate

ORCA Series		
2	3	4
✓		



INPUTS: A,B,C,D,E,F
OUTPUTS: Z
PINORDER: A B C D E F Z
MINIMUM CELL AREA: 0.5

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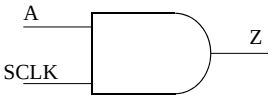
OSAND2

2 Input AND Gate with System Clock (used in PIC area only)

ORCA Series		
2	3	4
	✓	✓



OSAND2

INPUTS: A,SCLK
OUTPUTS: Z
PINORDER: A SCLK Z
MINIMUM CELL AREA: 0

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OSCA

Internal Oscillator

Lattice FPGA		
SC	XP	EC
✓		

OSCA

OUTPUTS: OSC
PINORDER: TEST OSC
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES
DIV: 1, 2, 4, 8, 16, 32, 64, 128

Description:

The OSCA is the source of the internal clock for configuration. After configuration, an internal oscillator is available within the FPGA. Normally this oscillator is disabled by default and must be enabled by a bitstream option. It may also be used after configuration as a general-purpose clock.

The clock frequency division varies from the time of start-up to the time of entering user mode. The internal clock frequency can be one of eight choices, 1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, or 1/128 of the oscillator frequency. During start-up, the clock frequency uses the slowest 1/128 (about1.0MHz), while during initialization; the clock uses 1/8 (about 20MHz ~ 13MHz).

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OSCC

Internal Oscillator

Lattice FPGA		
MX	XP	EC
✓		

OSCC

OUTPUTS: OSC
PINORDER: OSC
MINIMUM CELL AREA (All Series): 0

Description:

The OSCC is the source of the internal clock for configuration. After configuration, an internal oscillator is available within the FPGA. Normally this oscillator is disabled by default and must be enabled by a bitstream option. It may also be used after configuration as a general-purpose clock. OSCC has a frequency of approximately 20 MHz.

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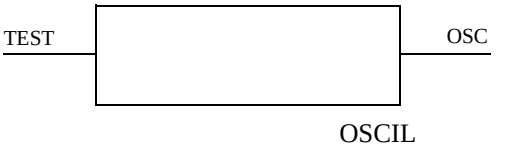
OSCIL

Internal Oscillator

ORCA Series		
2	3	4
✓	✓	✓



INPUTS: TEST
OUTPUTS: OSC
PINORDER: TEST OSC
MINIMUM CELL AREA (All Series): 0
ATTRIBUTES (Series 5 only)
DIV: 1, 2, 4, 8, 16, 32, 64, 128

Description:

After configuration, an internal oscillator is available within the ORCA FPGA. Normally this oscillator is disabled by default and must be enabled by a bitstream option.

TEST: This input is used purely for simulation purposes. It has no physical meaning and is used as a means of trouble-shooting.

OSC: In Series 4,this is the output of the oscillator which offers two choices of clock frequencies: 1.25 Mhz and 10 Mhz, which are also selected by a bitstream option.

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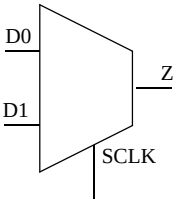
OSMUX21

2 to 1 Mux with System Clock (used in PIC area only)

ORCA Series		
2	3	4
	✓	✓



OSMUX21

INPUTS: D0,D1,SCLK
OUTPUTS: Z
PINORDER: D0 D1 SCLK Z
MINIMUM CELL AREA: 0

Note: This element must be paired with an output or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element. In 4E designs, this element must be paired with a flip-flop or a latch in addition to the output/bidirectional buffer.

Truth Table:

INPUTS			OUTPUTS
D0	D1	SCLK	Z
0	X	0	0
1	X	0	1
X	0	1	0
X	1	1	1

X = Don’t care

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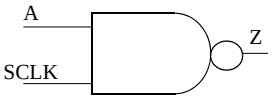
OSND2

2 Input NAND Gate with System Clock (used in PIC area only)

ORCA Series		
2	3	4
	✓	✓



OSND2

INPUTS: A,SCLK
OUTPUTS: Z
PINORDER: A SCLK Z
MINIMUM CELL AREA: 0

Note: This element must be paired with an output or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

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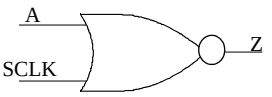
OSNR2

2 Input NOR Gate with System Clock (used in PIC area only)

ORCA Series		
2	3	4
	✓	✓



OSNOR2

INPUTS: A,SCLK
OUTPUTS: Z
PINORDER: A SCLK Z
MINIMUM CELL AREA: 0

Note: This element must be paired with an output or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

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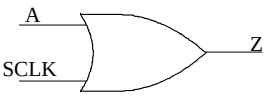
OSOR2

2 Input OR Gate with System Clock (used in PIC area only)

ORCA Series		
2	3	4
	✓	✓



OSOR2

INPUTS: A,SCLK
OUTPUTS: Z
PINORDER: A SCLK Z
MINIMUM CELL AREA: 0

Note: This element must be paired with an output or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

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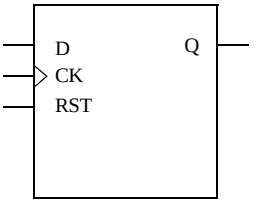
OSRX1A

Output 1-Bit Shift Register

Lattice FPGA		
SC	XP	EC
✓		



OSRX1A

INPUTS: D, CK, RST
OUTPUTS: Q
PINORDER: D, CK, Q
MINIMUM CELL AREA: 0

Description:

Outputs data through the shift register to the output data.

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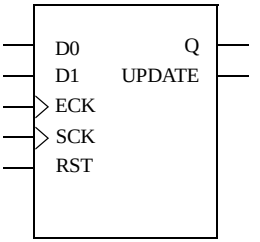
OSRX2A

Output 2-Bit Shift Register

Lattice FPGA		
SC	XP	EC
✓		



OSRX2XA

INPUTS: D0, D1, ECK, SCK, RST
OUTPUTS: Q, UPDATE
PINORDER: D0, D1, ECK, SCK, RST, Q, UPDATE
MINIMUM CELL AREA: 0
ATTRIBUTES
LSRMODE: EDGE, LOCAL
UPDT: POS, NEG

Description:

Outputs data through the shift register to the output data.

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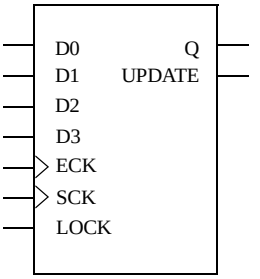
OSRX4A

Output 4-Bit Shift Register

Lattice FPGA		
SC	XP	EC
✓		



OSRX4A

INPUTS: D0, D1, D2, D3, ECK, SCK, LSR
OUTPUTS: Q, UPDATE
PINORDER: D0, D1, D2, D3, ECK, SCK, LSR, Q, UPDATE
MINIMUM CELL AREA: 0
ATTRIBUTES
LSRMODE: EDGE, LOCAL
UPDT: POS, NEG

Description:

Outputs data through the shift register to the output data.

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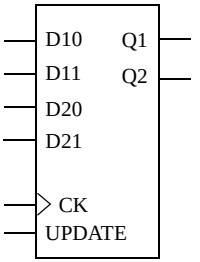
OSR2X2

Output Dual 2-Bit Shift Register

ORCA Series		
2	3	4
		✓



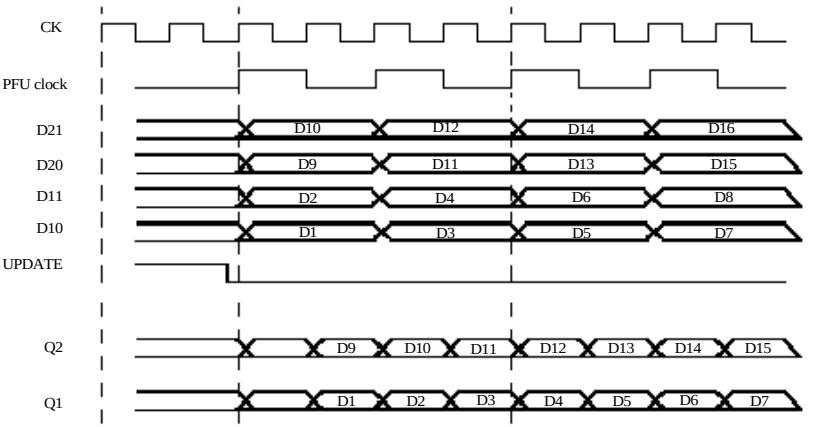
OSR2X2

INPUTS: D10,D11,D20,D21,CK,UPDATE
OUTPUTS: Q1,Q2
PINORDER: I O
MINIMUM CELL AREA (All Series): 0

Description:

D10 and D11 are the inputs and Q1 is the output of shift register 1. D20 and D21 are the inputs and Q2 is the output of shift register 2.

Below is a waveform showing the inputs/outputs of the OSR2X2 element.



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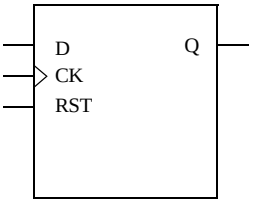
OSRX1A

Output 1-Bit Shift Register

Lattice FPGA		
SC	XP	EC
✓		



OSRX1A

INPUTS: D, CK, RST
OUTPUTS: Q
PINORDER: D, CK, Q
MINIMUM CELL AREA: 0

Description:

Output 1-bit shift register.

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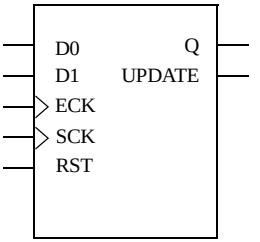
OSRX2A

Output 2-Bit Shift Register

Lattice FPGA		
SC	XP	EC
✓		



OSRX2XA

INPUTS: D0, D1, ECK, SCK, RST
OUTPUTS: Q, UPDATE
PINORDER: D0, D1, ECK, SCK, RST, Q, UPDATE
MINIMUM CELL AREA: 0
ATTRIBUTES
LSRMODE: EDGE, LOCAL
UPDT: POS, NEG

Description:

Output 2-bit shift register.

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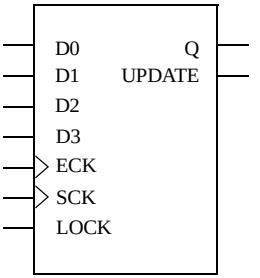
OSRX4A

Output 4-Bit Shift Register

Lattice FPGA		
SC	XP	EC
✓		



OSRX4A

INPUTS: D0, D1, D2, D3, ECK, SCK, LSR
OUTPUTS: Q, UPDATE
PINORDER: D0, D1, D2, D3, ECK, SCK, LSR, Q, UPDATE
MINIMUM CELL AREA: 0
ATTRIBUTES
  LSRMODE: EDGE, LOCAL
  UPDT: POS, NEG

Description:

Output 4-bit shift register.

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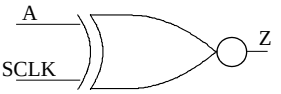
OSXNOR2

2 Input Exclusive NOR Gate with System Clock (used in PIC area only)

ORCA Series		
2	3	4
	✓	✓



OSXNOR2

INPUTS: A,SCLK
OUTPUTS: Z
PINORDER: A SCLK Z
MINIMUM CELL AREA: 0

Note: This element must be paired with an output or bidirectional buffer. The mapper automatically assigns the element and its buffer to the same PIC. Use the PIN or LOC properties, or the LOCATE COMP preference, on the buffer per normal use, but not on this element.

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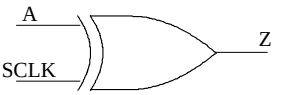
OSXOR2

2 Input Exclusive OR Gate with System Clock (used in PIC area only)

ORCA Series		
2	3	4
	✓	✓



OSXOR2

INPUTS: A,SCLK
OUTPUTS: Z
PINORDER: A SCLK Z
MINIMUM CELL AREA: 0

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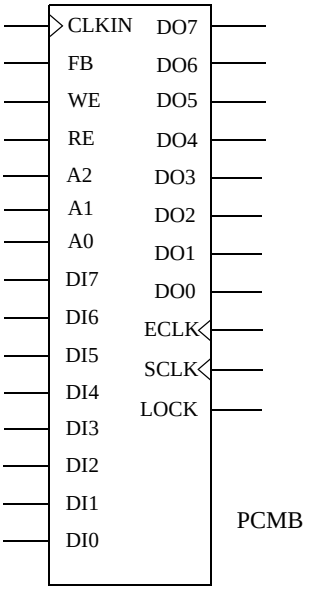
PCMB

Programmable Clock Manager – Bottom

ORCA Series		
2	3	4
	✓	✓



INPUTS: CLKIN,FB,WE,RE, A2,A1,A0,DI7,DI6,DI5,DI4,DI3,DI2,DI1,DI0
OUTPUTS: DO7,DO6,DO5,DO4,DO3,DO2,DO1,DO0,ECLK,SCLK,LOCK
PINORDER: CLKIN FB WE RE A2 A1 A0 DI7 DI6 DI5 DI4 DI3 DI2 DI1 DI0 DO7 DO6 DO5 DO4 DO3 DO2 DO1 DO0 ECLK SCLK LOCK
MINIMUM CELL AREA: 0

Description:

This is a fully functional PCM model which can be configured through configuration bitstream or can be programmed during operation through a read/write interface.

The LOCK output is asserted high when the ECLK and SCLK outputs are valid.

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For Express clock (ECLK) feedback:

Feclk = Fin*(DIV1/DIV0)
Fsclk = Fin*[(DIV1/DIV0)*DIV2]

For System clock (SCLK) feedback:

Fsclk = Fin*[(DIV1/DIV0)
Feclk = Fin*(DIV1/DIV0*DIV2)

PCM = Property of different modes of operation
DUTY = Attribute to control the duty cycle (default 50)
CLKIN = Clock in
ECLK = Express clock out
SCLK = System clock out
LOCK = Lock output
DIV0= Property to divide the input clock frequency (default 1)
DIV1= Property to divide the feedback clock frequency (default 1)
DIV2= Property to divide the express clock frequency (default 1)
DISABLED_GSR= Property to program bit7 of register7
DISABLED_DONE= Property to program bit6 of register7
PWRON= Property to program bit0 or register 7
FBDELAY= Feedback delay

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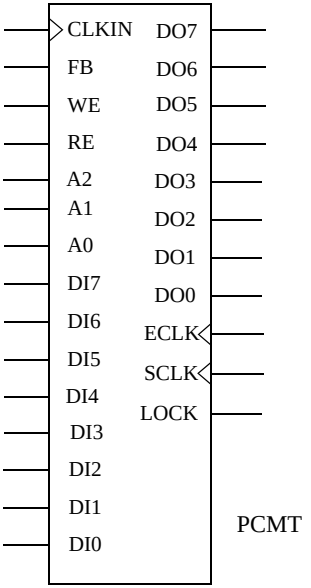
PCMT

Programmable Clock Manager – Top

ORCA Series		
2	3	4
	✓	✓



INPUTS: CLKIN,FB,WE,RE, A2,A1,A0,DI7,DI6,DI5,DI4,DI3,DI2,DI1,DI0
OUTPUTS: DO7,DO6,DO5,DO4,DO3,DO2,DO1,DO0,ECLK,SCLK,LOCK
PINORDER: CLKIN FB WE RE A2 A1 A0 DI7 DI6 DI5 DI4 DI3 DI2 DI1 DI0 DO7 DO6 DO5 DO4 DO3 DO2 DO1 DO0 ECLK SCLK LOCK
MINIMUM CELL AREA: 0

Description:

This is a fully functional PCM model which can be configured through configuration bitstream or can be programmed during operation through a read/write interface.

The LOCK output is asserted high when the ECLK and SCLK outputs are valid.

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For Express clock (ECLK) feedback:

Feclk = Fin*(DIV1/DIV0)
Fsclk = Fin*[(DIV1/DIV0)*DIV2]

For System clock (SCLK) feedback:

Fsclk = Fin*[(DIV1/DIV0)
Feclk = Fin*(DIV1/DIV0*DIV2)

PCM = Property of different modes of operation
DUTY = Attribute to control the duty cycle (default 50)
CLKIN = Clock in
ECLK = Express clock out
SCLK = System clock out
LOCK = Lock output
DIV0= Property to divide the input clock frequency (default 1)
DIV1= Property to divide the feedback clock frequency (default 1)
DIV2= Property to divide the express clock frequency (default 1)
DISABLED_GSR= Property to program bit7 of register7
DISABLED_DONE= Property to program bit6 of register7
PWRON= Property to program bit0 or register 7
FBDELAY= Feedback delay

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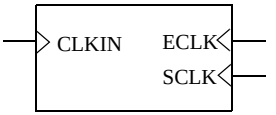
PCMBUFB

Programmable Clock Manager in Bypass Mode – Bottom

ORCA Series		
2	3	4
	✓	✓



PCMBUFB

INPUTS: CLKIN
OUTPUTS: ECLK,SCLK
PINORDER: CLKIN ECLK SCLK
MINIMUM CELL AREA: 0

Description:

The PCMBUFB generates output signals ECLK and SCLK, which are the buffered input clock.

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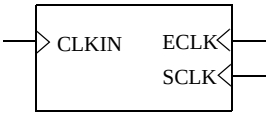
PCMBUFT

Programmable Clock Manager in Bypass Mode – Top

ORCA Series		
2	3	4
	✓	✓



PCMBUFT

INPUTS: CLKIN
OUTPUTS: ECLK,SCLK
PINORDER: CLKIN ECLK SCLK
MINIMUM CELL AREA: 0

Description:

The PCMBUFT generates output signals ECLK and SCLK, which are the buffered input clock.

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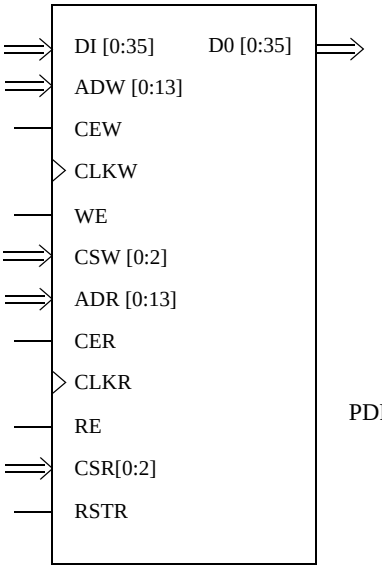
PDP16KA

16K Pseudo Dual Port Block RAM

Lattice FPGA		
SC	XP	EC
✓		



NOTE: The graphic is shown in bus notation for convenience. This element must be instantiated in expanded bus notation format with each individual bit as given below.

INPUT : DI0, DI1, DI2, DI3, DI4, DI5, DI6, DI7, DI8, DI9, DI10, DI11, DI12, DI13, DI14, DI15, DI16, DI17, DI18, DI19, DI20, DI21, DI22, DI23, DI24, DI25, DI26, DI27, DI28, DI29, DI30, DI31, DI32, DI33, DI34, DI35, ADW0, ADW1, ADW2, ADW3, ADW4, ADW5, ADW6, ADW7, ADW8, ADW9, ADW10, ADW11, ADW12, ADW13, CEW, CLKW, WE, CSW0, CSW1, CSW2, ADR0, ADR1, ADR2, ADR3, ADR4, ADR5, ADR6, ADR7, ADR8, ADR9, ADR10, ADR11, ADR12, ADR13, CER, CLKR, RE, CSR0, CSR1, CSR2, RSTR

OUTPUT : DO0, DO1, DO2, DO3, DO4, DO5, DO6, DO7, DO8, DO9, DO10, DO11, DO12, DO13, DO14, DO15, DO16, DO17, DO18, DO19, DO20, DO21, DO22, DO23, DO24, DO25, DO26, DO27, DO28, DO29, DO30, DO31, DO32, DO33, DO34, DO35

PINORDER: DI0, DI1, DI2, DI3, DI4, DI5, DI6, DI7, DI8, DI9, DI10, DI11, DI12, DI13, DI14, DI15, DI16, DI17, DI18, DI19, DI20, DI21, DI22, DI23, DI24, DI25, DI26, DI27, DI28, DI29, DI30, DI31, DI32, DI33, DI34, DI35, ADW0, ADW1, ADW2, ADW3, ADW4, ADW5, ADW6, ADW7, ADW8, ADW9, ADW10, ADW11, ADW12, ADW13, CEW, CLKW, WE, CSW0, CSW1, CSW2, ADR0, ADR1, ADR2, ADR3, ADR4, ADR5, ADR6, ADR7, ADR8, ADR9, ADR10, ADR11, ADR12, ADR13, CER, CLKR, RE, CSR0, CSR1, CSR2, RSTR, DO0, DO1, DO2, DO3, DO4, DO5, DO6, DO7, DO8, DO9, DO10, DO11, DO12, DO13, DO14, DO15, DO16, DO17, DO18, DO19, DO20, DO21, DO22, DO23, DO24, DO25, DO26, DO27, DO28, DO29, DO30, DO31, DO32, DO33, DO34, DO35

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ATTRIBUTES (Series 5-HSI only)
DATA_WIDTH_W : 1, 2, 4, 9, 18, 36
DATA_WIDTH_R : 1, 2, 4, 9, 18, 36
REGMODE : NOREG, OUTREG
RESETMODE : ASYNC, SYNC
CSDECODE_W : 000, 001, 010, 011, 100, 101, 110, 111
CSDECODE_R : 000, 001, 010, 011, 100, 101, 110, 111
DISABLED_GSR : 0, 1
INIT : DISABLED, ENABLED
INIT_RECFG : DISABLED, ENABLED
INIT_ID : "0000000000"

Description:

Pseudo Dual Port RAM. See “Pseudo Dual Port RAM Port Definitions” on page 3.

Note: When the write data width (DATA_WIDTH_W) is set to 36, the WE port is invalid, that is, it has no effect on the data output.

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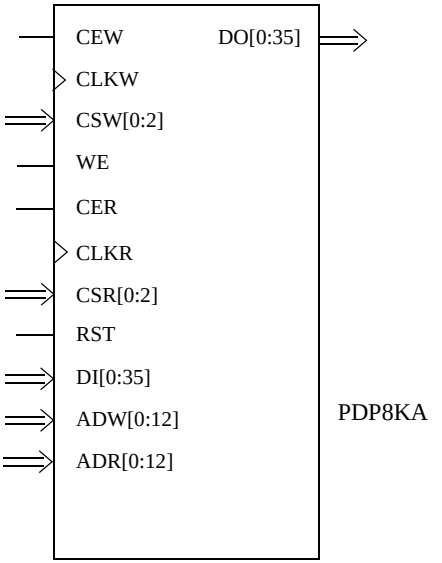
PDP8KA

8K Pseudo Dual Port Block RAM

Lattice FPGA		
SC	XP	EC
	✓	✓



NOTE: The graphic is shown in bus notation for convenience. This element must be instantiated in expanded bus notation format with each individual bit as given below.

INPUT : CEW, CLKW, CSW0, CSW1, CSW2, WE, CER, CLKR, CSR0, CSR1, CSR2, RST, DI0, DI1, DI2, DI3, DI4, DI5, DI6, DI7, DI8, DI9, DI10, DI11, DI12, DI13, DI14, DI15, DI16, DI17, DI18, DI19, DI20, DI21, DI22, DI23, DI24, DI25, DI26, DI27, DI28, DI29, DI30, DI31, DI32, DI33, DI34, DI35, ADW0, ADW1, ADW2, ADW3, ADW4, ADW5, ADW6, ADW7, ADW8, ADW9, ADW10, ADW11, ADW12, ADR0, ADR1, ADR2, ADR3, ADR4, ADR5, ADR6, ADR7, ADR8, ADR9, ADR10, ADR11, ADR12

OUTPUT : DO0, DO1, DO2, DO3, DO4, DO5, DO6, DO7, DO8, DO9, DO10, DO11, DO12, DO13, DO14, DO15, DO16, DO17, DO18, DO19, DO20, DO21, DO22, DO23, DO24, DO25, DO26, DO27, DO28, DO29, DO30, DO31, DO32, DO33, DO34, DO35

PINORDER:CEW, CLKW, CSW0, CSW1, CSW2, WE, CER, CLKR, CSR0, CSR1, CSR2, RST, DI0, DI1, DI2, DI3, DI4, DI5, DI6, DI7, DI8, DI9, DI10, DI11, DI12, DI13, DI14, DI15, DI16, DI17, DI18, DI19, DI20, DI21, DI22, DI23, DI24, DI25, DI26, DI27, DI28, DI29, DI30, DI31, DI32, DI33, DI34, DI35, ADW0, ADW1, ADW2, ADW3, ADW4, ADW5, ADW6, ADW7, ADW8, ADW9, ADW10, ADW11, ADW12, ADR0, ADR1, ADR2, ADR3, ADR4, ADR5, ADR6, ADR7, ADR8, ADR9, ADR10, ADR11, ADR12, DO0, DO1, DO2, DO3, DO4, DO5, DO6, DO7, DO8, DO9, DO10, DO11, DO12, DO13, DO14, DO15, DO16, DO17, DO18, DO19, DO20, DO21, DO22, DO23, DO24, DO25, DO26, DO27, DO28, DO29, DO30, DO31, DO32, DO33, DO34, DO35

ATTRIBUTES (LatticeXP/EC)

DATA_WIDTH_W : 1, 2 , 4, 9, 18, 36

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DATA_WIDTH_R : 1, 2 , 4, 9, 18, 36
REGMODE : NOREG, OUTREG
RESETMODE : ASYNC, SYNC
CSDECODE_W : 000, 001, 010, 011, 100, 101, 110, 111
CSDECODE_R : 000, 001, 010, 011, 100, 101, 110, 111
DISABLED_GSR: TRUE, FALSE
WRITEMODE : NORMAL, WRITETHROUGH, READBEFOREWRITE
INITVAL_00 to _3F : 0xXX….X (80 hex characters)

Description:

Pseudo Dual Port RAM. See “Pseudo Dual Port RAM Port Definitions” on page 3.

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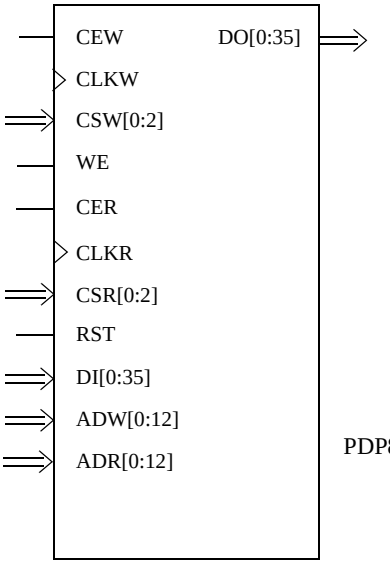
PDP8KB

8K Pseudo Dual Port Block RAM



Lattice FPGA			
SC	XP	EC	MX
	✓	✓	✓

NOTE: The graphic is shown in bus notation for convenience. This element must be instantiated in expanded bus notation format with each individual bit as given below.

INPUT : CEW, CLKW, CSW0, CSW1, CSW2, WE, CER, CLKR, CSR0, CSR1, CSR2, RST, DI0, DI1, DI2, DI3, DI4, DI5, DI6, DI7, DI8, DI9, DI10, DI11, DI12, DI13, DI14, DI15, DI16, DI17, DI18, DI19, DI20, DI21, DI22, DI23, DI24, DI25, DI26, DI27, DI28, DI29, DI30, DI31, DI32, DI33, DI34, DI35, ADW0, ADW1, ADW2, ADW3, ADW4, ADW5, ADW6, ADW7, ADW8, ADW9, ADW10, ADW11, ADW12, ADR0, ADR1, ADR2, ADR3, ADR4, ADR5, ADR6, ADR7, ADR8, ADR9, ADR10, ADR11, ADR12

INPUT : CEW, CLKW, CSW0, CSW1, CSW2, WE, CER, CLKR, CSR0, CSR1, CSR2, RST, DI0, DI1, DI2, DI3, DI4, DI5, DI6, DI7, DI8, DI9, DI10, DI11, DI12, DI13, DI14, DI15, DI16, DI17, DI18, DI19, DI20, DI21, DI22, DI23, DI24, DI25, DI26, DI27, DI28, DI29, DI30, DI31, DI32, DI33, DI34, DI35, ADW0, ADW1, ADW2, ADW3, ADW4, ADW5, ADW6, ADW7, ADW8, ADW9, ADW10, ADW11, ADW12, ADR0, ADR1, ADR2,ADR3,ADR4,ADR5,ADR6,ADR7,ADR8,ADR9,ADR10,ADR11,ADR12

OUTPUT : DO0, DO1, DO2, DO3, DO4, DO5, DO6, DO7, DO8, DO9, DO10, DO11, DO12, DO13, DO14, DO15, DO16, DO17, DO18, DO19, DO20, DO21, DO22, DO23, DO24, DO25, DO26, DO27, DO28, DO29, DO30, DO31, DO32, DO33, DO34, DO35

PINORDER:CEW, CLKW, CSW0, CSW1, CSW2, WE, CER, CLKR, CSR0, CSR1, CSR2, RST, DI0, DI1, DI2, DI3, DI4, DI5, DI6, DI7, DI8, DI9, DI10, DI11, DI12, DI13, DI14, DI15, DI16, DI17, DI18, DI19, DI20, DI21, DI22, DI23, DI24, DI25, DI26, DI27, DI28, DI29, DI30, DI31, DI32, DI33, DI34, DI35, ADW0, ADW1, ADW2, ADW3, ADW4, ADW5, ADW6, ADW7, ADW8, ADW9, ADW10, ADW11, ADW12, ADR0,

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ADR1, ADR2, ADR3, ADR4, ADR5, ADR6, ADR7, ADR8, ADR9, ADR10, ADR11, ADR12, DO0, DO1, DO2, DO3, DO4, DO5, DO6, DO7, DO8, DO9, DO10, DO11, DO12, DO13, DO14, DO15, DO16, DO17, DO18, DO19, DO20, DO21, DO22, DO23, DO24, DO25, DO26, DO27, DO28, DO29, DO30, DO31, DO32, DO33, DO34, DO35

ATTRIBUTES (LatticeXP/EC)

DATA_WIDTH_W : 1, 2 , 4, 9, 18, 36
DATA_WIDTH_R : 1, 2 , 4, 9, 18, 36
REGMODE : NOREG, OUTREG
RESETMODE : ASYNC, SYNC
CSDECODE_W : 000, 001, 010, 011, 100, 101, 110, 111
CSDECODE_R : 000, 001, 010, 011, 100, 101, 110, 111
DISABLED_GSR: TRUE, FALSE
GSR : ENABLED, DISABLED (same as above)
WRITEMODE : NORMAL, WRITETHROUGH, READBEFOREWRITE
INITVAL_00 to _3F : 0xXX….X (80 hex characters)

Description:

Pseudo Dual Port RAM. See “Pseudo Dual Port RAM Port Definitions” on page 3. PDP8KB is available in the MachXO library.

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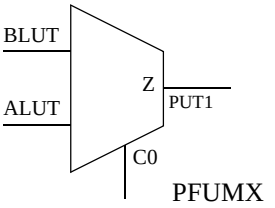
PFUMX

2-Input Mux within the PFU, C0 used for Selection with Positive Select

ORCA Series/Lattice			
2	3	4	SC
✓	✓	✓	✓



INPUTS: ALUT,BLUT,C0
OUTPUTS: Z
PINORDER: ALUT BLUT C0 Z
MINIMUM CELL AREA (Series 2): 0
MINIMUM CELL AREA (Series 3 and Series 4): 0.03

Truth Table:

INPUTS			OUTPUTS
BLUT	ALUT	C0	Z
X	1	1	1
X	0	1	0
1	X	0	1
0	X	0	0

X = Don’t care

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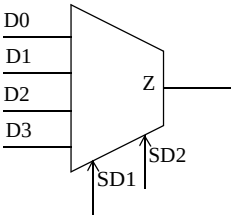
PFUMX41

4-Input Mux within the PFU

ORCA Series /Lattice		
4	XP	EC
✓	✓	✓



PFUMX41

INPUTS: D0,D1,D2,D3,SD1,SD2
OUTPUTS: Z
PINORDER: D0 D1 D2 D3 SD1 SD2 Z
MINIMUM CELL AREA (Series 2): 0
MINIMUM CELL AREA (Series 3 and Series 4): 0.03

Truth Table:

INPUTS						OUTPUTS
D0	D1	D2	D3	SD1	SD2	Z
0	X	X	X	0	0	0
1	X	X	X	0	0	1
X	0	X	X	1	0	0
X	1	X	X	1	0	1
X	X	0	X	0	1	0
X	X	1	X	0	1	1
X	X	X	0	1	1	0
X	X	X	1	1	1	1

X = Don’t care

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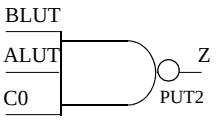
PFUND

3-Input NAND Element within the PFU

ORCA Series		
2	3	4
✓		

For EXPERTS only!



PFUND

INPUTS: ALUT,BLUT,C0
OUTPUTS: Z
PINORDER: ALUT BLUT C0 Z
MINIMUM CELL AREA: 0

Truth Table:

INPUTS			OUTPUTS
BLUT	ALUT	C0	Z
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

X = Don’t care

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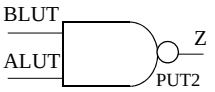
PFUND0

2-Input NAND Element within the PFU

ORCA Series		
2	3	4
✓		

For EXPERTS only!



PFUND0

INPUTS: ALUT,BLUT
OUTPUTS: Z
PINORDER: ALUT BLUT Z
MINIMUM CELL AREA: 0

Truth Table:

INPUTS		OUTPUTS
BLUT	ALUT	Z
0	0	1
0	1	1
1	0	1
1	1	0

X = Don’t care

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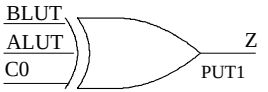
PFUXR

3-Input XOR Element within the PFU

ORCA Series		
2	3	4
✓		

For EXPERTS only!



PFUXR

INPUTS: ALUT,BLUT,C0
OUTPUTS: Z
PINORDER: ALUT BLUT C0 Z
MINIMUM CELL AREA: 0

Truth Table:

INPUTS			OUTPUTS
BLUT	ALUT	C0	Z
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

X = Don’t care

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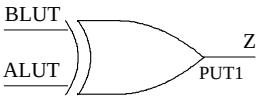
PFUXR0

2-Input XOR Element within the PFU

ORCA Series		
2	3	4
✓		

For EXPERTS only!



PFUXR0

INPUTS: ALUT,BLUT
OUTPUTS: Z
PINORDER: ALUT BLUT Z
MINIMUM CELL AREA: 0

Truth Table:

INPUTS		OUTPUTS
BLUT	ALUT	Z
0	0	0
0	1	1
1	0	1
1	1	0

X = Don’t care

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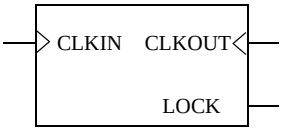
PLL1

Programmable Clock Manager (Phase Locked Loop) — Top-right and Bottom-left dedicated PLL for Clock Conditioning at 1.544 MHz and 2.048 MHz

ORCA Series		
2	3	4
		✓



PLL1

INPUTS: CLKIN
OUTPUTS: CLKOUT,LOCK
PINORDER: CLKIN CLKOUT LOCK
MINIMUM CELL AREA: 0

Description:

The phase locked loop is one of the functions performed by the PCM which is user selectable through configuration logic and/or a PCM_FPGA interface.

***Note*:** The PLL1 and PLL2 elements should be instantiated through SCUBA. Refer to the appropriate topic in the online help system for details.

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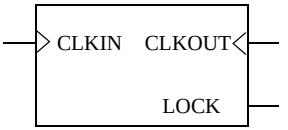
PLL2

Programmable Clock Manager (Phase Locked Loop) — Top-left and Bottom-right dedicated PLL for Clock Conditioning at 155.52 MHz

ORCA Series		
2	3	4
		✓



PLL2

INPUTS: CLKIN
OUTPUTS: CLKOUT,LOCK
PINORDER: CLKIN CLKOUT LOCK
MINIMUM CELL AREA: 0

Description:

The phase locked loop is one of the functions performed by the PCM which is user selectable through configuration logic and/or a PCM_FPGA interface.

***Note*:** The PLL1 and PLL2 elements should be instantiated through SCUBA. Refer to the appropriate topic in the online help system for details.

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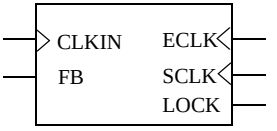
PLLB

Programmable Clock Manager (Phase Locked Loop) — Bottom

ORCA Series		
2	3	4
	✓	✓



PLLB

INPUTS: CLKIN, FB
OUTPUTS: ECLK,SCLK,LOCK
PINORDER: CLKIN FB ECLK SCLK LOCK
MINIMUM CELL AREA: 0
ATTRIBUTES: DIV0,DIV1,DIV2,FBDELAY

Description:

The phase locked loop is one of the functions performed by the PCM which is user selectable through configuration logic and/or a PCM_FPGA interface.

PLLB cell generates output signals ECLK and SCLK, whose frequency are a fraction of the input clock frequency.

The LOCK output is asserted high when the ECLK and SCLK outputs are valid.

continued

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For Express clock (ECLK) feedback:

Feclk = Fin*(DIV1/DIV0)
Fsclk = Fin*[(DIV1/DIV0)*DIV2]

For System clock (SCLK) feedback:

Fsclk = Fin*[(DIV1/DIV0)
Feclk = Fin*(DIV1/DIV0*DIV2)

DIV0= Property to divide the input clock frequency (default 1)
DIV1= Property to divide the feedback clock frequency (default 1)
DIV2= Property to divide the express clock frequency (default 1)
DISABLED_GSR= Property to disable global set/reset
CLKIN = Clock in
ECLK = Express clock out
SCLK = System clock out
LOCK = Lock output
FBDELAY = Feedback delay

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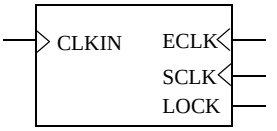
PLLDFB

Programmable Clock Manager (Phase Locked Loop) — Dedicated Feedback Bottom

ORCA Series		
2	3	4
	✓	



PLLDFB

INPUTS: CLKIN
OUTPUTS: ECLK,SCLK,LOCK
PINORDER: CLKIN ECLK SCLK LOCK
MINIMUM CELL AREA: 0
ATTRIBUTES: DIV0,DIV1,DIV2,FBDELAY

Description:

The dedicated feedback to this element comes from the output of the bottom center CLKCNTL (CLKCNTHB or CLKCNTLB). The phase locked loop is one of the functions performed by the PCM which is user selectable through configuration logic and/or a PCM_FPGA interface.

PLLDFB cell generates output signals ECLK and SCLK, whose frequency are a fraction of the input clock frequency.

The LOCK output is asserted high when the ECLK and SCLK outputs are valid.

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For Express clock (ECLK) feedback:

Feclk = Fin*(DIV1/DIV0)
Fsclk = Fin*[(DIV1/DIV0)*DIV2]

For System clock (SCLK) feedback:

Fsclk = Fin*[(DIV1/DIV0)
Feclk = Fin*(DIV1/DIV0*DIV2)

DIV0= Property to divide the input clock frequency (default 1)
DIV1= Property to divide the feedback clock frequency (default 1)
DIV2= Property to divide the express clock frequency (default 1)
DISABLED_GSR= Property to disable global set/reset
CLKIN = Clock in
ECLK = Express clock out
SCLK = System clock out
LOCK = Lock output
FBDELAY = Feedback delay

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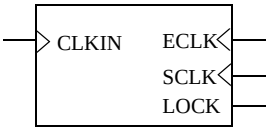
PLLDFT

Programmable Clock Manager (Phase Locked Loop) — Dedicated Feedback Top

ORCA Series		
2	3	4
	✓	



PLLDFT

INPUTS: CLKIN
OUTPUTS: ECLK,SCLK,LOCK
PINORDER: CLKIN ECLK SCLK LOCK
MINIMUM CELL AREA: 0
ATTRIBUTES: DIV0,DIV1,DIV2,FBDELAY

Description:

The dedicated feedback to this element comes from the output of the top center CLKCNTL (CLKCNTHT or CLKCNTLT). The phase locked loop is one of the functions performed by the PCM which is user selectable through configuration logic and/or a PCM_FPGA interface.

PLLDFT cell generates output signals ECLK and SCLK, whose frequency are a fraction of the input clock frequency.

The LOCK output is asserted high when the ECLK and SCLK outputs are valid.

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For Express clock (ECLK) feedback:

Feclk = Fin*(DIV1/DIV0)
Fsclk = Fin*[(DIV1/DIV0)*DIV2]

For System clock (SCLK) feedback:

Fsclk = Fin*[(DIV1/DIV0)
Feclk = Fin*(DIV1/DIV0*DIV2)

DIV0= Property to divide the input clock frequency (default 1)
DIV1= Property to divide the feedback clock frequency (default 1)
DIV2= Property to divide the express clock frequency (default 1)
DISABLED_GSR= Property to disable global set/reset
CLKIN = Clock in
ECLK = Express clock out
SCLK = System clock out
LOCK = Lock output
FBDELAY = Feedback delay

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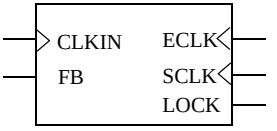
PLLT

Programmable Clock Manager (Phase Locked Loop) — Top

ORCA Series		
2	3	4
	✓	✓



PLLT

INPUTS: CLKIN, FB
OUTPUTS: ECLK,SCLK,LOCK
PINORDER: CLKIN FB ECLK SCLK LOCK
MINIMUM CELL AREA: 0
ATTRIBUTES: DIV0,DIV1,DIV2,FBDELAY

Description:

The phase locked loop is one of the functions performed by the PCM which is user selectable through configuration logic and/or a PCM_FPGA interface.

PLLT cell generates output signals ECLK and SCLK, whose frequency are a fraction of the input clock frequency.

The LOCK output is asserted high when the ECLK and SCLK outputs are valid.

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For Express clock (ECLK) feedback:

Feclk = Fin*(DIV1/DIV0)
Fsclk = Fin*[(DIV1/DIV0)*DIV2]

For System clock (SCLK) feedback:

Fsclk = Fin*[(DIV1/DIV0)
Feclk = Fin*(DIV1/DIV0*DIV2)

DIV0= Property to divide the input clock frequency (default 1)
DIV1= Property to divide the feedback clock frequency (default 1)
DIV2= Property to divide the express clock frequency (default 1)
DISABLED_GSR= Property to disable global set/reset
CLKIN = Clock in
ECLK = Express clock out
SCLK = System clock out
LOCK = Lock output
FBDELAY = Feedback delay

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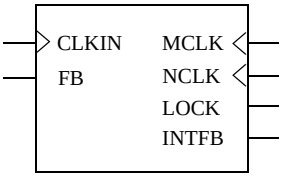
PPLL

Programmable Clock Manager (Programmable general purpose Phase Locked Loop)

ORCA Series		
2	3	4
		✓



PPLL

INPUTS: CLKIN,FB
OUTPUTS: MCLK,NCLK,LOCK,INTFB
PINORDER: CLKIN FB MCLK NCLK LOCK INTFB
MINIMUM CELL AREA: 0
ATTRIBUTES (Series 4 only)
DIV0: 1, 2, 3, 4, 5, 6, 7, 8
DIV1: 1, 2, 3, 4, 5, 6, 7, 8
DIV2: 1, 2, 3, 4, 5, 6, 7, 8
DIV3: 1, 2, 3, 4, 5, 6, 7, 8
MCLKMODE: BYPASS, DUTYCYCLE, PHSHIFT, DELAY
NCLKMODE: BYPASS, DUTYCYCLE, PHSHIFT, DELAY
VCOTAP: 0, 1, 2, 3, 4, 5, 6, 7
DISABLED_GSR: 0, 1
FB_PDEL: DEL0, DEL1, DEL2, DEL3

Description:

The phase locked loop is one of the functions performed by the PCM which is user selectable through configuration logic and/or a PCM_FPGA interface.

***Note*:** The PPLL element should be instantiated through SCUBA. Refer to the appropriate topic in the online help system for details. In addition, the FB_PDEL property should be used only if the FB port is driven from external routing (e.g., MCLK or NCLK).

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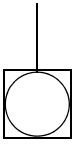
PUR

Power Up Set/Reset (Registers in Microprocessor Interface)

ORCA Series			
2	3	4	SC
✓	✓	✓	✓



PUR

INPUTS: PUR
PINORDER: PUR
MINIMUM CELL AREA (Series 2): 0
MINIMUM CELL AREA (Series 3 and Series 4): 0

Description:

PUR is used to reset or set all register elements in your microprocessor interface (MPI) component. The PUR component can be connected to a net from an input buffer or an internally generated net. It is active LOW and when pulsed will set or reset all register bits to the same state as the local set or reset functionality.

It is not necessary to connect signals for PUR to any register elements explictly. The function will be implicitly connected globally.

PUR will initially only be used with the MPI cells. GSR will not function with MPI cells.

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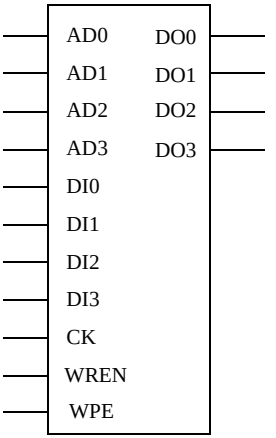
RCE16X4

16 Word by 4 Bit Positive Edge Triggered Write Synchronous Single Port Memory with Positive Write Enable and Positive Write Port Enable

ORCA Series		
2	3	4
✓		



RCE16X4

INPUTS: AD0,AD1,AD2,AD3,DI0,DI1,DI2,DI3, CK,WREN,WPE
OUTPUTS: DO0,DO1,DO2,DO3
PINORDER: AD0 AD1 AD2 AD3 DI0 DI1 DI2 DI3 CK WREN WPE DO0 DO1 DO2 DO3
MINIMUM CELL AREA: 1.0

Description:

The RCE16x4 symbol represents a 16 word by 4 bit synchronous single port RAM. It has four data inputs DI[3:0], a positive Write Enable (WREN), and a positive Write Port Enable (WPE).

Writing to the RAM does not occur until *both* the WREN and WPE signals are enabled. If both the WREN and WPE signals are HIGH, the data is written into the locations specified by address lines AD[3:0] on the next positive clock (CK) edge. If *either one* or *both* of the WREN or WPE signals are LOW, an asynchronous data read operation is performed, with the memory contents output on the signals DO[3:0].

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In other words, the read operation is asynchronous and is always active. The write operation is synchronous and only occurs when there is a rising edge of the clock and the write enables are high prior to that rising edge.

If desired, the contents of the RCE16x4 can be assigned an initial value, which will be loaded into the RAM during configuration. The INITVAL=<*value*> parameter is used to assign the initial value. The <*value*> should consist of sixteen 4 bit binary or hexadecimal data written into the RAM from the highest address to the lowest address. For example, if the following attribute is specified:

`INITVAL=0000000100100011010001010110011110001001101010111001101111011111` (in binary)
or
`INITVAL=0x0123456789ABCDEF` (in hex)

it implies that the above data is loaded sequentially from location FH to 0H (where FH would contain the 0 and 0H the F). If no INITVAL= parameter is specified, the RAM is initialized with zeros on configuration.

Truth Table:

INPUTS					OUTPUTS	OPERATION
DI[3:0]	WREN	WPE	CK	AD[3:0]	DO[3:0]	
DI[3:0]	1	1	↑	AD[3:0]	MEM[AD[3:0]]	Write DI[3:0] into AD[3:0]
X	X	X	X	AD[3:0]	MEM[AD[3:0]]	Read MEM[AD[3:0]]

X = Don’t care

Note: The memory is always being read. New data is read out after a write.

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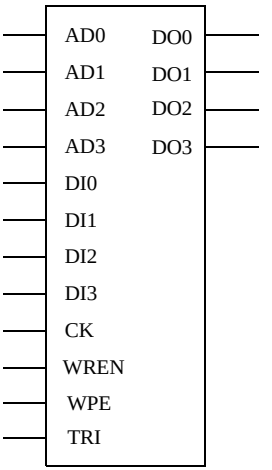
RCE16X4Z

16 Word by 4 Bit Positive Edge Triggered Write Synchronous Single Port Memory with Positive Write Enable, Positive Write Port Enable, and Positive Tristate Control

ORCA Series		
2	3	4
✓		



RCE16X4Z

INPUTS: AD0,AD1,AD2,AD3,DI0,DI1,DI2,DI3, CK,WREN,WPE,TRI
OUTPUTS: DO0,DO1,DO2,DO3
PINORDER: AD0 AD1 AD2 AD3 DI0 DI1 DI2 DI3 CK WREN WPE TRI DO0 DO1 DO2 DO3
MINIMUM CELL AREA: 1.0

Description:

The RCE16x4Z symbol represents a 16 word by 4 bit synchronous single port RAM. It has four data inputs DI[3:0], a positive Write Enable (WREN), and a positive Write Port Enable (WPE).

Writing to the RAM does not occur until *both* the WREN and WPE signals are enabled. If both the WREN and WPE signals are HIGH, the data is written into the locations specified by address lines AD[3:0] on the next positive clock (CK) edge. If *either one* or *both* of the WREN or WPE signals are LOW, an asynchronous data read operation is performed, with the memory contents output on the signals DO[3:0].

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In other words, the read operation is asynchronous and is always active. The write operation is synchronous and only occurs when there is a rising edge of the clock and the write enables are high prior to that rising edge.

The outputs can be tristated by enabling the TRI control signal HIGH. This is to enable the use of the outputs in a bus format and to drive the outputs into a high impedance state.

If desired, the contents of the RCE16x4Z can be assigned an initial value, which will be loaded into the RAM during configuration. The INITVAL=<*value*> parameter is used to assign the initial value. The <*value*> should consist of sixteen 4 bit binary or hexadecimal data written into the RAM from the highest address to the lowest address. For example, if the following attribute is specified

`INITVAL=0000000100100011010001010110011110001001101010111100110111101111` (in binary)
or
`INITVAL=0x0123456789ABCDEF` (in hex)

it implies that the above data is loaded sequentially from location FH to 0H (where FH would contain the 0 and 0H the F). If no INITVAL= parameter is specified, the RAM is initialized with zeros on configuration.

Truth Table:

INPUTS						OUTPUTS	OPERATION
DI[3:0]	WREN	WPE	TRI	CK	AD[3:0]	DO[3:0]	
DI[3:0]	1	1	1	↑	AD[3:0]	Z	Tristate outputs, but write DI[3:0] into AD[3:0]
DI[3:0]	1	1	0	↑	AD[3:0]	MEM[AD[3:0]]	Write DI[3:0] into AD[3:0]
DI[3:0]	X	X	1	X	AD[3:0]	Z	Tristate
X	X	X	0	X	AD[3:0]	MEM[AD[3:0]]	Read MEM[AD[3:0]]

X = Don’t care

Note: The memory is always being read. New data is read out after a write, except when in tristate.

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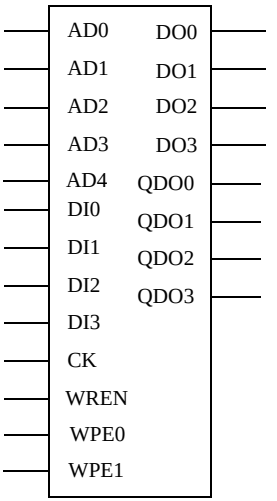
RCE32X4

32 Word by 4 Bit Negative Edge Triggered Write Synchronous Single Port Memory with Positive Write Enable and Two Positive Write Port Enables

ORCA Series		
2	3	4
	✓	✓



RCE32X4

INPUTS: AD0,AD1,AD2,AD3,AD4,DI0,DI1,DI2,DI3,CK,WREN,WPE0,WPE1
OUTPUTS: DO0,DO1,DO2,DO3,QDO0,QDO1,QDO2,QDO3
PINORDER: AD0 AD1 AD2 AD3 AD4 DI0 DI1 DI2 DI3 CK WREN WPE0 WPE1 DO0 DO1 DO2 DO3 QDO0 QDO1 QDO2 QDO3
MINIMUM CELL AREA: 1.0

Description:

The RCE32x4 symbol represents a 32 word by 4 bit synchronous single port RAM. It has four data inputs DI[3:0], a postive Write Enable (WREN), and two positive Write Port Enables (WPE0 and WPE1).

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Writing to the RAM does not occur until *both* the WREN and WPE signals are enabled. If both the WREN and WPE signals are HIGH, the data is written into the locations specified by address lines AD[4:0] on the next negative clock (CK) edge. If *any* of the WREN or WPE signals are LOW, an asynchronous data read operation is performed, with the memory contents output on the signals DO[3:0].

In other words, the read operation is asynchronous and is always active. The write operation is synchronous and only occurs when there is a falling edge of the clock and the write enables are high prior to that falling edge.

This RAM also has registered data outputs (QDO[0:3]), which are registered on the rising edge of the clock.

If desired, the contents of the RCE32x4 can be assigned an initial value, which will be loaded into the RAM during configuration. The INITVAL=<*value*> parameter is used to assign the initial value. The <*value*> should consist of 32 4-bit binary or hexadecimal data written into the RAM from the highest address to the lowest address. For example, if the following attribute is specified:

```
INITVAL=00000001001000110100010101100111100010011010101111001
1011110111100000001001000110100010101100111100010011010101111
1100110111101111 (in binary)
```
or
```
INITVAL=0x0123456789ABCDEF0123456789ABCDEF (in hex)
```

it implies that the above data is loaded sequentially from location 1FH to 0H (where 1FH would contain the 0 and 0H the F). If no INITVAL= parameter is specified, the RAM is initialized with zeros on configuration.

For simulation with a 3C RAM or ROM cell, you must instantiate a GSR in your netlist, and pulse the GSR high to low at the beginning of the simulation.

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Truth Table:

INPUTS						OUTPUTS		OPERATION
DI[3:0]	WREN	WPE0	WPE1	CK	AD[4:0]	DO[3:0]	QDO[3:0]	
DI[3:0]	1	1	1	↓	AD[4:0]	MEM[AD[4:0]]	QDO[3:0]	Write DI[3:0] into AD[4:0]
X	X	X	X	X	AD[4:0]	MEM[AD[4:0]]	QDO[3:0]	Read MEM[AD[4:0]]
X	X	X	X	↑	AD[4:0]	MEM[AD[4:0]]	MEM[AD[4:0]]	Read MEM[AD[4:0]] Register data outputs

X = Don’t care
When GSR=0, AD[0:4]=WREN=WPE0=WPE1=DO[0:3]=QDO[0:3]=0

Note: The memory is always being read. New data is read out after a write.

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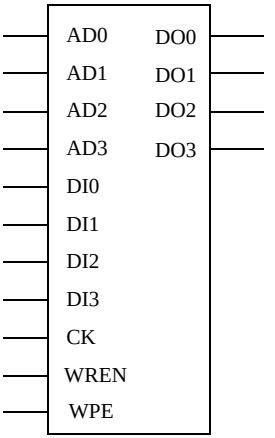
RCF16X4

16 Word by 4 Bit Fast Positive Edge Triggered Write Synchronous Single Port Memory with Positive Write Enable and Positive Write Port Enable

ORCA Series		
2	3	4
✓		



RCF16X4

INPUTS: AD0,AD1,AD2,AD3,DI0,DI1,DI2,DI3, CK,WREN,WPE
OUTPUTS: DO0,DO1,DO2,DO3
PINORDER: AD0 AD1 AD2 AD3 DI0 DI1 DI2 DI3 CK WREN WPEDO0 DO1 DO2 DO3
MINIMUM CELL AREA: 1.0

Note

This RAM cell is used in the fast mode. It allows for greater performance (clock speeds) when compared to RCE16X4. Please refer to your datasheet for the appropriate timing information. This RAM cell is not supported when using the Readback capability.

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Description:

The RCF16x4 symbol represents a 16 word by 4 bit synchronous single port fast RAM. It has four data inputs DI[3:0], a positive Write Enable (WREN), and a positive Write Port Enable (WPE).

Writing to the RAM does not occur until *both* the WREN and WPE signals are enabled. If both the WREN and WPE signals are HIGH, the data is written into the locations specified by the address lines AD[3:0] on the next positive clock (CK) edge. If *either one* or *both* of the WREN or WPE signals are LOW, an asynchronous data read operation is performed, with the memory contents output on the read/write data output signals DO[3:0].

In other words, the read operation is asynchronous and is always active. The write operation is synchronous and only occurs when there is a rising edge of the clock and the write enables are high prior to that rising edge.

If desired, the contents of the RCF16x4 can be assigned an initial value, which will be loaded into the RAM during configuration. The INITVAL=<*value*> parameter is used to assign the initial value. The <*value*> should consist of sixteen 4 bit binary or hexadecimal data written into the RAM from the highest address to the lowest address. For example, if the following attribute is specified:

`INITVAL=0000000100100011010001010110011110001001101010111001101111011111` (in binary)
or
`INITVAL=0x0123456789ABCDEF` (in hex)

it implies that the above data is loaded sequentially from location FH to 0H (where FH would contain the 0 and 0H the F). If no INITVAL= parameter is specified, the RAM is initialized with zeros on configuration.

This RAM cell is used in the fast mode. It is not supported when using the Readback capability. Please refer to your datasheet for the appropriate timing information.

continued

Truth Table:

INPUTS					OUTPUTS	OPERATION
DI[3:0]	WREN	WPE	CK	AD[3:0]	DO[3:0]	
DI[3:0]	1	1	↑	AD[3:0]	MEM[AD[3:0]]	Write DI[3:0] into AD[3:0]

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INPUTS					OUTPUTS	OPERATION
DI[3:0]	WREN	WPE	CK	AD[3:0]	DO[3:0]	
X	X	X	X	AD[3:0]	MEM[AD[3:0]]	Read MEM[AD[3:0]]

X = Don’t care

Note: The memory is always being read. New data is read out after a write.

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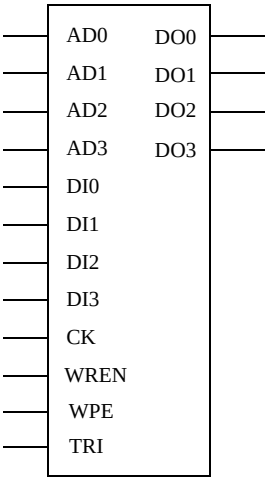
RCF16X4Z

16 Word by 4 Bit Fast Positive Edge Triggered Write Synchronous Single Port Memory with Positive Write Enable, Positive Write Port Enable, and Positive Tristate Control

ORCA Series		
2	3	4
✓		



RCF16X4Z

INPUTS: AD0,AD1,AD2,AD3,DI0,DI1,DI2,DI3, CK,WREN,WPE,TRI
OUTPUTS: DO0,DO1,DO2,DO3
PINORDER: AD0 AD1 AD2 AD3 DI0 DI1 DI2 DI3 CK WREN WPE TRI DO0 DO1 DO2 DO3
MINIMUM CELL AREA: 1.0

Note

This RAM cell is used in the fast mode. It allows for greater performance (clock speeds) when compared to RCE16X4Z. Please refer to your datasheet for the appropriate timing information. This RAM cell is not supported when using the Readback capability.

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Description:

The RCF16x4Z symbol represents a 16 word by 4 bit synchronous single port fast RAM. It has four data inputs DI[3:0], a positive Write Enable (WREN), and a positive Write Port Enable (WPE).

Writing to the RAM does not occur until *both* the WREN and WPE signals are enabled. If both the WREN and WPE signals are HIGH, the data is written into the locations specified by the address lines AD[3:0] on the next positive clock (CK) edge. If *either one* or *both* of the WREN or WPE signals are LOW, an asynchronous data read operation is performed, with the memory contents output on the read/write data output signals DO[3:0].

In other words, the read operation is asynchronous and is always active. The write operation is synchronous and only occurs when there is a rising edge of the clock and the write enables are high prior to that rising edge.

The outputs can be tristated by enabling the TRI control signal HIGH. This is to enable the use of the outputs in a bus format and to drive the outputs into a high impedance state.

If desired, the contents of the RCF16x4Z can be assigned an initial value, which will be loaded into the RAM during configuration. The INITVAL=<*value*> parameter is used to assign the initial value. The <*value*> should consist of sixteen 4 bit binary or hexadecimal data written into the RAM from the highest address to the lowest address. For example, if the following attribute is specified

`INITVAL=0000000100100011010001010110011110001001101010111100110111101111` (in binary)
or
`INITVAL=0x0123456789ABCDEF` (in hex)

it implies that the above data is loaded sequentially from location FH to 0H (where FH would contain the 0 and 0H the F). If no INITVAL= parameter is specified, the RAM is initialized with zeros on configuration.

This RAM cell is used in the fast mode. It is not supported when using the Readback capability. Please refer to your datasheet for the appropriate timing information.

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Truth Table:

INPUTS						OUTPUTS	OPERATION
DI[3:0]	WREN	WPE	TRI	CK	AD[3:0]	DO[3:0]	
DI[3:0]	1	1	1	↑	AD[3:0]	Z	Tristate outputs, but write DI[3:0] into AD[3:0]
DI[3:0]	1	1	0	↑	AD[3:0]	MEM[AD[3:0]]	Write DI[3:0] into AD[3:0]
DI[3:0]	X	X	1	X	AD[3:0]	Z	Tristate
X	X	X	0	X	AD[3:0]	MEM[AD[3:0]]	Read MEM[AD[3:0]]

X = Don’t care

Note: The memory is always being read. New data is read out after a write, except when in tristate.

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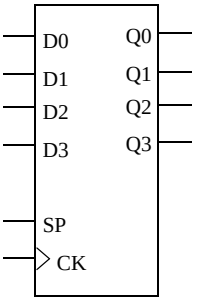
RD4P3A

Positive Edge Triggered 4 Bit Data Register with Positive Level Enable

ORCA Series		
2	3	4
✓		



RD4P3A

INPUTS: D0,D1,D2,D3,SP,CK
OUTPUTS: Q0,Q1,Q2,Q3
PINORDER: D0 D1 D2 D3 SP CK Q0 Q1 Q2 Q3
MINIMUM CELL AREA: 0.5

Truth Table:

INPUTS			OUTPUTS
D[0:3]	SP	CK	Q[0:3]
X	0	X	Q[0:3]
D[0:3]	1	↑	D[0:3]

X = Don’t care
When GSR=0, Q[0:3]=0 (D[0:3]=SP=CK=X)

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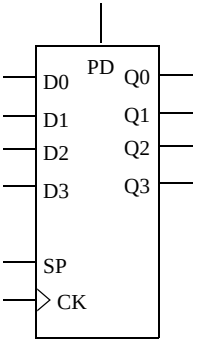
RD4P3B

Positive Edge Triggered 4 Bit Data Register with Positive Level Enable and Positive Level Asynchronous Preset

ORCA Series		
2	3	4
✓		



RD4P3B

INPUTS: D0,D1,D2,D3,SP,CK,PD
OUTPUTS: Q0,Q1,Q2,Q3
PINORDER: D0 D1 D2 D3 SP CK PD Q0 Q1 Q2 Q3
MINIMUM CELL AREA: 0.5

Truth Table:

INPUTS				OUTPUTS
D[0:3]	SP	CK	PD	Q[0:3]
X	X	X	1	1 1 1 1
X	0	X	0	Q[0:3]
D[0:3]	1	↑	0	D[0:3]

X = Don’t care
When GSR=0, Q[0:3]=1 (D[0:3]=SP=CK=X)

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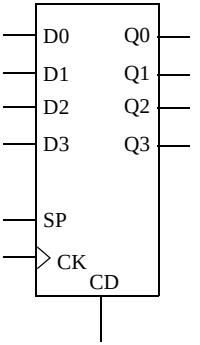
RD4P3D

Positive Edge Triggered 4 Bit Data Register with Positive Level Enable and Positive Level Asynchronous Clear

ORCA Series		
2	3	4
✓		



RD4P3D

INPUTS: D0,D1,D2,D3,SP,CK,CD
OUTPUTS: Q0,Q1,Q2,Q3
PINORDER:
D0 D1 D2 D3 SP CK CD Q0 Q1 Q2 Q3
MINIMUM CELL AREA: 0.5

Truth Table:

INPUTS				OUTPUTS
D[0:3]	SP	CK	CD	Q[0:3]
X	X	X	1	0 0 0 0
X	0	X	0	Q[0:3]
D[0:3]	1	↑	0	D[0:3]

X = Don’t care
When GSR=0, Q[0:3]=0 (D[0:3]=SP=CK=X)

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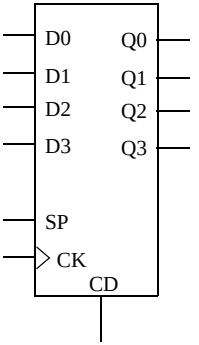
RD4P3I

Positive Edge Triggered 4 Bit Data Register with Positive Level Enable and Positive Level Synchronous Clear

ORCA Series		
2	3	4
✓		



RD4P3I

INPUTS: D0,D1,D2,D3,SP,CK,CD
OUTPUTS: Q0,Q1,Q2,Q3
PINORDER:
D0 D1 D2 D3 SP CK CD Q0 Q1 Q2 Q3
MINIMUM CELL AREA: 0.5

Truth Table:

INPUTS				OUTPUTS
D[0:3]	SP	CK	CD	Q[0:3]
X	0	X	X	Q[0:3]
X	1	↑	1	0 0 0 0
D[0:3]	1	↑	0	D[0:3]

X = Don’t care
When GSR=0, Q[0:3]=0 (D[0:3]=SP=CK=X)

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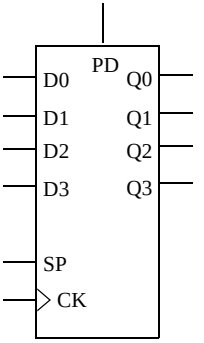
RD4P3J

Positive Edge Triggered 4 Bit Data Register with Positive Level Enable and Positive Level Synchronous Preset

ORCA Series		
2	3	4
✓		



RD4P3J

INPUTS: D0,D1,D2,D3,SP,CK,PD
OUTPUTS: Q0,Q1,Q2,Q3
PINORDER: D0 D1 D2 D3 SP CK PD Q0 Q1 Q2 Q3
MINIMUM CELL AREA: 0.5

Truth Table:

INPUTS				OUTPUTS
D[0:3]	SP	CK	PD	Q[0:3]
X	0	X	X	Q[0:3]
X	1	↑	1	1 1 1 1
D[0:3]	1	↑	0	D[0:3]

X = Don’t care
When GSR=0, Q[0:3]=1 (D[0:3]=SP=CK=X)

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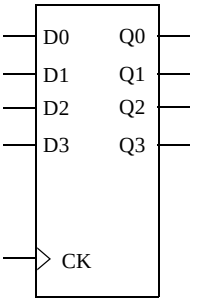
RD4S3A

Positive Edge Triggered 4 Bit Data Register

ORCA Series		
2	3	4
✓		



RD4S3A

INPUTS: D0,D1,D2,D3,CK
OUTPUTS: Q0,Q1,Q2,Q3
PINORDER: D0 D1 D2 D3 CK Q0 Q1 Q2 Q3
MINIMUM CELL AREA: 0.5

Truth Table:

INPUTS		OUTPUTS
D[0:3]	CK	Q[0:3]
D[0:3]	↑	D[0:3]

X = Don’t care
When GSR=0, Q[0:3]=0 (D[0:3]=CK=X)

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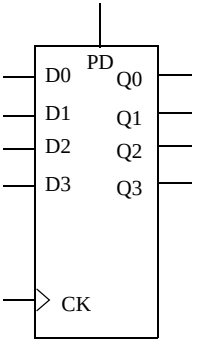
RD4S3B

Positive Edge Triggered 4 Bit Data Register with Positive Level Asynchronous Preset

ORCA Series		
2	3	4
✓		



RD4S3B

INPUTS: D0,D1,D2,D3,CK,PD
OUTPUTS: Q0,Q1,Q2,Q3
PINORDER: D0 D1 D2 D3 CK PD Q0 Q1 Q2 Q3
MINIMUM CELL AREA: 0.5

Truth Table:

INPUTS			OUTPUTS
D[0:3]	CK	PD	Q[0:3]
X	X	1	1 1 1 1
D[0:3]	↑	0	D[0:3]

X = Don’t care
When GSR=0, Q[0:3]=1 (D[0:3]=CK=X)

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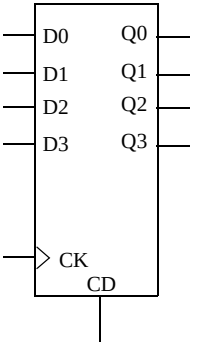
RD4S3D

Positive Edge Triggered 4 Bit Data Register with Positive Level Asynchronous Clear

ORCA Series		
2	3	4
✓		



RD4S3D

INPUTS: D0,D1,D2,D3,CK,CD
OUTPUTS: Q0,Q1,Q2,Q3
PINORDER: D0 D1 D2 D3 CK CD Q0 Q1 Q2 Q3
MINIMUM CELL AREA: 0.5

Truth Table:

INPUTS			OUTPUTS
D[0:3]	CK	CD	Q[0:3]
X	X	1	0 0 0 0
D[0:3]	↑	0	D[0:3]

X = Don’t care
When GSR=0, Q[0:3]=0 (D[0:3]=CK=X)

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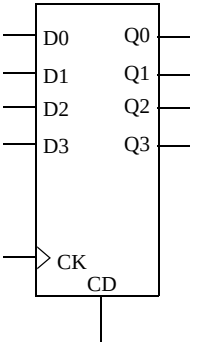
RD4S3I

Positive Edge Triggered 4 Bit Data Register with Positive Level Synchronous Clear

ORCA Series		
2	3	4
✓		



RD4S3I

INPUTS: D0,D1,D2,D3,CK,CD
OUTPUTS: Q0,Q1,Q2,Q3
PINORDER: D0 D1 D2 D3 CK CD Q0 Q1 Q2 Q3
MINIMUM CELL AREA: 0.5

Truth Table:

INPUTS			OUTPUTS
D[0:3]	CK	CD	Q[0:3]
X	↑	1	0 0 0 0
D[0:3]	↑	0	D[0:3]

X = Don’t care
When GSR=0, Q[0:3]=0 (D[0:3]=CK=X)

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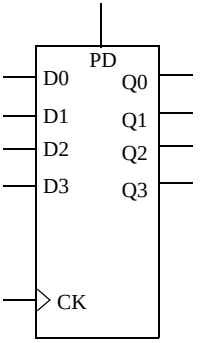
RD4S3J

Positive Edge Triggered 4 Bit Data Register with Positive Level Synchronous Preset

ORCA Series		
2	3	4
✓		



RD4S3J

INPUTS: D0,D1,D2,D3,CK,PD
OUTPUTS: Q0,Q1,Q2,Q3
PINORDER: D0 D1 D2 D3 CK PD Q0 Q1 Q2 Q3
MINIMUM CELL AREA: 0.5

Truth Table:

INPUTS			OUTPUTS
D[0:3]	CK	PD	Q[0:3]
X	↑	1	1 1 1 1
D[0:3]	↑	0	D[0:3]

X = Don’t care
When GSR=0, Q[0:3]=1 (D[0:3]=CK=X)

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RDBK

Readback Controller

Lattice FPGA		
SC	XP	EC
✓		

RDBK

INPUTS: RDCFGN
OUTPUTS: PRDDATA
PINORDER: RDCFGN PRDDATA
MINIMUM CELL AREA: 0

Description:

RDBK is used to read back the configuration data and optionally the state of the PFU outputs. RDBK can be done while the FPGA is in normal system operation. To use RDBK, select options in the bit stream generator within the place and route tool.

- You can choose the option to prohibit readback, allow a single readback, or allow unrestricted readback. For more information on RDBK, refer to applicable application notes or contact technical support.

RDCFGN: A high-to-low transition on this input initiates a readback operation. This pin must remain low during the readback operation.

PRDDATA: Readback data is available at this output, which in turn is connected to the same pad as that used by TDO for boundary scan.

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READBK

Readback Controller

ORCA Series		
2	3	4
✓	✓	✓

READBK

INPUTS: RDCFGN,CAPT
OUTPUTS: PRDDATA,RDBO
PINORDER: RDCFGN CAPT PRDDATA RDBO
MINIMUM CELL AREA (All Series): 0

Description:

Readback is used to read back the configuration data and optionally the state of the PFU outputs. Readback can be done while the FPGA is in normal system operation. To use readback, select options in the bit stream generator within the place and route tool.

- You can choose the option to prohibit readback, allow a single readback, or allow unrestricted readback. For more information on Readback, refer to an available data book or contact technical support.

RDCFGN: A high-to-low transition on this input initiates a readback operation. This pin must remain low during the readback operation.

CAPT: When a capture of PFU outputs is desired, three options are available: capture data upon entering readback, capture data based upon a configurable signal internal to the FPGA (CAPT), and capture data on either of the former two options. A low-to-high transition on CAPT enables the capture of PFU outputs at a given time.

PRDDATA: Readback data is available at this output, which in turn is connected to the same pad as that used by TDO for boundary scan.

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RDBO: On occasions when readback is used along with boundary scan, the pad which is dedicated to TDO for boundary scan cannot be used to obtain readback data. Thus, the readback data is available at the RDBO output, which can be connected to any I/O pad to obtain the readback data. (Note: This output is always available, not just in the case that TDO is used by boundary scan.)

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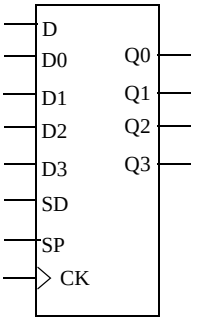
RLS4P3A

Positive Edge Triggered 4 Bit Loadable Shift Register with Positive Level Enable

ORCA Series		
2	3	4
✓		



RLS4P3A

INPUTS: D,D0,D1,D2,D3,SP,CK,SD
OUTPUTS: Q0,Q1,Q2,Q3
PINORDER: D D0 D1 D2 D3 SP CK SD Q0 Q1 Q2 Q3
MINIMUM CELL AREA: 0.5

Truth Table:

INPUTS					OUTPUTS			
D	D[0:3]	SD	SP	CK	Q0	Q1	Q2	Q3
X	X	X	0	X	Q0	Q1	Q2	Q3
X	D[0:3]	1	1	↑	D0	D1	D2	D3
0	X	0	1	↑	0	Q0	Q1	Q2
1	X	0	1	↑	1	Q0	Q1	Q2

X = Don’t care
When GSR=0, Q[0:3]=0 (D=D[0:3]=SD=SP=CK=X)

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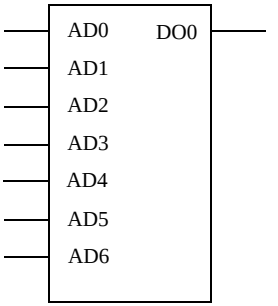
ROM128X1

128 Word by 1 Bit Positive Edge Triggered Read-Only Memory with Registered Data Outputs

Lattice FPGA		
SC	XP	EC
✓	✓	✓



ROM128X1

INPUTS: AD0, AD1, AD2, AD3, AD4, AD5, AD6
OUTPUTS: DO0
PINORDER: AD0, AD1, AD2, AD3, AD4, AD5, AD6, DO0

Description:

The ROM128X1 symbol represents a 128 word by1-bit read-only memory. The read operation is asynchronous and is always active.

The INITVAL=<*value*> parameter is used to initialize the ROM. The <*value*> should consist of 64 one-bit binary or hexadecimal data written into the ROM from the highest address to the lowest address. For example, if the following attribute is specified:

`INITVAL=0x0123456789ABCDEF0123456789ABCDEF` (in hex)

it implies that the above data is loaded sequentially from location 1FH to 0H (where 1FH would contain the 0 and 0H the F).

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Truth Table:

INPUTS	OUTPUTS	OPERATION
AD[5:0]	DO0	
AD[5:0]	MEM[AD[5:0]]	Read MEM[AD[5:0]]

Note: The memory is always being read.

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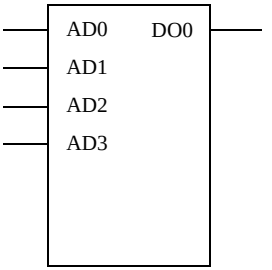
ROM16X1

16 Word by 1 Bit Read-Only Memory

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



ROM16X1

INPUTS: AD0,AD1,AD2,AD3
OUTPUTS: DO0
PINORDER: AD0 AD1 AD2 AD3 DO0
MINIMUM CELL AREA: 1.0 (All Series)

Description:

The ROM16x1 symbol represents a 16 word by 1 bit read-only memory. This ROM can be used to implement a ORCALUT4 in a design.

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The INITVAL=<*value*> parameter is used to initialize the ROM. The <*value*> should consist of 16 one-bit binary or 4 hexadecimal data written into the ROM from the highest address to the lowest address. For example, if the following attribute is specified:

`INITVAL=1111001100001010` (in binary)

or

`INITVAL=0xF30A` (in hex)

it implies that the above data is loaded sequentially from location FH to 0H (where FH would contain the F and 0H the A).

Truth Table:

INPUTS	OUTPUTS	OPERATION
AD[3:0]	DO0	
AD[3:0]	MEM[AD[3:0]]	Read MEM[AD[3:0]]

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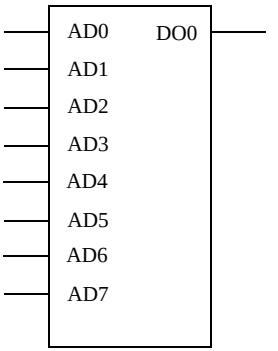
ROM256X1

256 Word by 1 Bit Positive Edge Triggered Read-Only Memory with Registered Data Outputs

ORCA Series/Lattice FPGA				
3	4	SC	XP	EC
✓	✓	✓	✓	✓



ROM256X1

INPUTS: AD0, AD1, AD2, AD3, AD4, AD5, AD6, AD7
OUTPUTS: DO0
PINORDER: AD0, AD1, AD2, AD3, AD4, AD5, AD6, AD7, DO0

Description:

The ROM256X1 symbol represents a 256 word by1-bit read-only memory. The read operation is asynchronous and is always active.

The INITVAL=<*value*> parameter is used to initialize the ROM. The <*value*> should consist of 64 one-bit binary or hexadecimal data written into the ROM from the highest address to the lowest address. For example, if the following attribute is specified:

`INITVAL=0x0123456789ABCDEF0123456789ABCDEF` (in hex)

it implies that the above data is loaded sequentially from location 1FH to 0H (where 1FH would contain the 0 and 0H the F).

continued

Truth Table:

INPUTS	OUTPUTS	OPERATION
AD[5:0]	DO0	
AD[5:0]	MEM[AD[5:0]]	Read MEM[AD[5:0]]

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Note: The memory is always being read.

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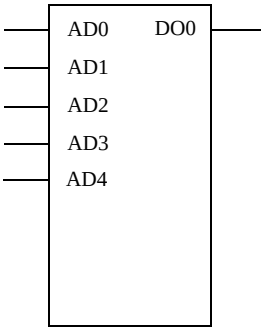
ROM32X1

32 Word by 1 Bit Read-Only Memory

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



ROM32X1

INPUTS: AD0,AD1,AD2,AD3,AD4
OUTPUTS: DO0
PINORDER: AD0 AD1 AD2 AD3 AD4 DO0
MINIMUM CELL AREA (All Series): 1.0

Description:

The ROM32x1 symbol represents a 32 word by 1 bit read-only memory. This ROM can be used to implement a ORCALUT5 in a design.

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The INITVAL=<*value*> parameter is used to initialize the ROM. The <*value*> should consist of 32 one-bit binary or 8 hexadecimal data written into the ROM from the highest address to the lowest address. For example, if the following attribute is specified:

`INITVAL=11110011000010100001001000011110001` (in binary)

or

`INITVAL=0x0F30A1234` (in hex)

it implies that the above data is loaded sequentially from location 1FH to 0H (where 1FH would contain the F and 0H the 4).

Truth Table:

INPUTS	OUTPUTS	OPERATION
AD[4:0]	DO0	
AD[4:0]	MEM[AD[4:0]]	Read MEM[AD[4:0]]

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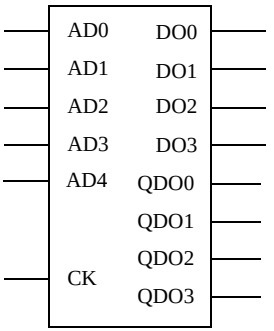
ROM32X4

32 Word by 4 Bit Positive Edge Triggered Read-Only Memory with Registered Data Outputs

ORCA Series		
2	3	4
	✓	✓



ROM32X4

INPUTS: AD0,AD1,AD2,AD3,AD4,CK
OUTPUTS: DO0,DO1,DO2,DO3,QDO0,QDO1,QDO2,QDO3
PINORDER: AD0 AD1 AD2 AD3 CK DO0 DO1 DO2 DO3 QDO0 QDO1 QDO2 QDO3
MINIMUM CELL AREA (All Series): 1.0

Description:

The ROM32x4 symbol represents a 32 word by 4 bit read-only memory.

The read operation is asynchronous and is always active.

This ROM also has registered data outputs (QDO[0:3]), which are registered on the rising edge of the clock.

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The INITVAL=<*value*> parameter is used to initialize the ROM. The <*value*> should consist of 32 four-bit binary or hexadecimal data written into the ROM from the highest address to the lowest address. For example, if the following attribute is specified:

```
INITVAL=00000001001000110100010101100111100010011010101111001101111011111000000010010001101000101011001111000100110101011
1100110111101111 (in binary)
```

or

```
INITVAL=0x0123456789ABCDEF0123456789ABCDEF (in hex)
```

it implies that the above data is loaded sequentially from location 1FH to 0H (where 1FH would contain the 0 and 0H the F).

For simulation with a 3C RAM or ROM cell, you must instantiate a GSR in your netlist, and pulse the GSR high to low at the beginning of the simulation.

Truth Table:

INPUTS		OUTPUTS		OPERATION
AD[4:0]	CK	DO[3:0]	QDO[3:0]	
AD[4:0]	X	MEM[AD[4:0]]	QDO[3:0]	Read MEM[AD[4:0]]
AD[4:0]	↑	MEM[AD[4:0]]	MEM[AD[4:0]]	MEM[AD[4:0]] Register data outputs

X = Don’t care
When GSR=0, QDO[3:0]=0

Note: The memory is always being read.

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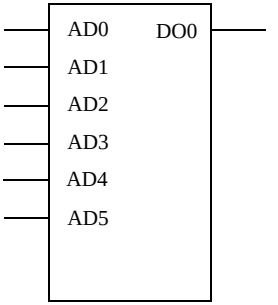
ROM64X1

64 Word by 1 Bit Positive Edge Triggered Read-Only Memory with Registered Data Outputs

Lattice FPGA		
SC	XP	EC
✓	✓	✓



ROM64X1

INPUTS: AD0, AD1, AD2, AD3, AD4, AD5
OUTPUTS: DO0
PINORDER: AD0, AD1, AD2, AD3, AD4, AD5, DO0

Description:

The ROM64X1 symbol represents a 64 word by 1-bit read-only memory. The read operation is asynchronous and is always active.

The INITVAL=<*value*> parameter is used to initialize the ROM. The <*value*> should consist of 64 one-bit binary or hexadecimal data written into the ROM from the highest address to the lowest address. For example, if the following attribute is specified:

`INITVAL=0x0123456789ABCDEF` (in hex)

it implies that the above data is loaded sequentially from location 64 to 1 (where location 64 would contain the 0 and location 1 the 1).

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Truth Table:

INPUTS	OUTPUTS	OPERATION
AD[5:0]	DO0	
AD[5:0]	MEM[AD[5:0]]	Read MEM[AD[5:0]]

Note: The memory is always being read.

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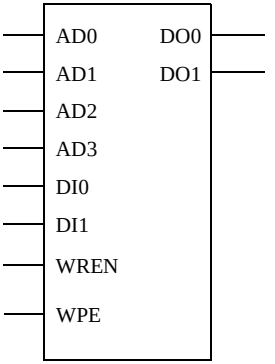
RPE16X2

16 Word by 2 Bit Static Memory with Positive Write Enable and Positive Write Port Enable

ORCA Series		
2	3	4
✓		



RPE16X2

INPUTS: AD0,AD1,AD2,AD3,DI0,DI1,WREN,WPE
OUTPUTS: DO0,DO1
PINORDER: AD0 AD1 AD2 AD3 DI0 DI1 WREN WPE DO0 DO1
MINIMUM CELL AREA: 1.0

Description:

The RPE16x2 symbol represents a 16 word by 2 bit static RAM. It has two data inputs DI[1:0], a positive Write Enable (WREN), and a positive Write Port Enable (WPE). Writing to the RAM does not occur until *both* the WREN and WPE signals are enabled. If the write enable(s) is HIGH the data is written into the locations specified by the address lines AD[3:0]. If the write enable(s) is LOW the data contents of the memory at the specified address appear at the data outputs DO[1:0].

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If desired, the contents of the RPE16x2 can be assigned an initial value, which is loaded into the RAM during configuration. The INITVAL=<*value*> parameter is used to assign the initial value. The <*value*> should consist of sixteen 2 bit binary or hexadecimal data written into the RAM from the highest address to the lowest address. For example, if the following attribute is specified:

`INITVAL=0001101100011011000110110001101 1` (in binary)
or
`INITVAL=0x0123012301230123` (in hex)

it implies that the above data is loaded sequentially from location FH to 0H (where FH would contain the 0 and 0H the 3). If no INITVAL= parameter is specified, the RAM is initialized with zeros on configuration.

If the INITVAL is specified as a hex string of 16 values, the values should not be greater than 3, since 3 is setting both memory locations to 1. If a value greater than 3 is used for synthesis/mapping, only the last two (least significant) bits are used for initialization by the mapper. For example,

`INITVAL=0x00000000ffffffff`
is equivalent to
`INITVAL=0x0000000033333333`

for mapping purposes, since the first two bits of the “f” are ingnored.

If a value other than 0,1,2 or 3 is used for simulation, the simulator will return undefined (‘U’) results for the data. Therefore, simulation results and actual mapped results could vary. For this reason, it is highly recommended to restrict initial hex strings to values of 0,1,2 or 3 for 2 bit wide memories.

RAM cells can be configured as ROM by connecting the WREN and WPE signals to ground (VLO) and supplying initial values to the memory element via the INITVAL attribute. To initialize the element for simulation, refer to the ORCA simulation tool’s interface manual.

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Truth Table:

INPUTS				OUTPUTS	OPERATION
DI[1:0]	WREN	WPE	AD[3:0]	DO[1:0]	
DI[1:0]	1	1	AD[3:0]	MEM[AD[3:0]]	Write DI[1:0] into AD[3:0]
X	X	X	AD[3:0]	MEM[AD[3:0]]	Read MEM[AD[3:0]]

X = Don’t care
Note: The memory is always being read. New data is read out after a write.

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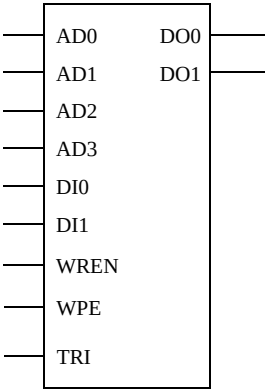
RPE16X2Z

16 Word by 2 Bit Static Memory with Positive Write Enable, Positive Write Port Enable, and Positive Tristate Control

ORCA Series		
2	3	4
✓		



RPE16X2Z

INPUTS: AD0,AD1,AD2,AD3,DI0,DI1,WREN,WPE,TRI
OUTPUTS: DO0,DO1
PINORDER: AD0 AD1 AD2 AD3 DI0 DI1 WREN WPE TRI DO0 DO1
MINIMUM CELL AREA: 1.0

Description:

The RPE16x2Z symbol represents a 16 word by 2 bit static RAM with tristated outputs. It has two data inputs DI[1:0], a positive Write Enable (WREN), a positive Write Port Enable (WPE), and a positive tristate control (TRI).

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Writing to the RAM does not occur until *both* the WREN and WPE signals are enabled. If the write enable(s) is HIGH the data is written into the locations specified by the address lines AD[3:0]. If the write enable(s) is LOW the data contents of the memory at the specified address appear at the data outputs DO[1:0]. The outputs can be tristated by enabling the TRI control signal HIGH. This is to enable the use of the outputs in a bus format and to drive the outputs into a high impedance state.

If desired, the contents of the RPE16x2Z can be assigned an initial value, which is loaded into the RAM during configuration. The INITVAL=<*value*> parameter is used to assign the initial value. The <*value*> should consist of sixteen 2 bit binary or hexadecimal data written into the RAM from the highest address to the lowest address. For example, if the following attribute is specified

`INITVAL=0001101100011011000110110011011` (in binary)
or
`INITVAL=0x0123012301230123` (in hex)

it implies that the above data is loaded sequentially from location FH to 0H (where FH would contain the 0 and 0H the 3). If no INITVAL= parameter is specified, the RAM is initialized with zeros on configuration.

If the INITVAL is specified as a hex string of 16 values, the values should not be greater than 3, since 3 is setting both memory locations to 1. If a value greater than 3 is used for synthesis/mapping, only the last two (least significant) bits are used for initialization by the mapper. For example,

`INITVAL=0x00000000ffffffff`
is equivalent to
`INITVAL=0x0000000033333333`

for mapping purposes, since the first two bits of the “f” are ingnored.

If a value other than 0,1,2 or 3 is used for simulation, the simulator will return undefined (‘U’) results for the data. Therefore, simulation results and actual mapped results could vary. For this reason, it is highly recommended to restrict initial hex strings to values of 0,1,2 or 3 for 2 bit wide memories.

RAM cells can be configured as ROM by connecting the WREN and WPE signals to ground (VLO) and supplying initial values to the memory element via the INITVAL attribute. To initialize the element for simulation, refer to the ORCA simulation tool’s interface manual.

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Truth Table:

INPUTS					OUTPUTS	OPERATION
DI[1:0]	WREN	WPE	TRI	AD[3:0]	DO[1:0]	
DI[1:0]	1	1	1	AD[3:0]	Z	Tristate outputs, but write DI[1:0] into AD[3:0]
DI[1:0]	1	1	0	AD[3:0]	MEM[AD[3:0]]	Write DI[1:0] into AD[3:0]
DI[1:0]	X	X	1	AD[3:0]	Z	Tristate
X	X	X	0	AD[3:0]	MEM[AD[3:0]]	Read MEM[AD[3:0]]

X = Don’t care

Note: The memory is always being read. New data is read out after a write, except when in tristate.

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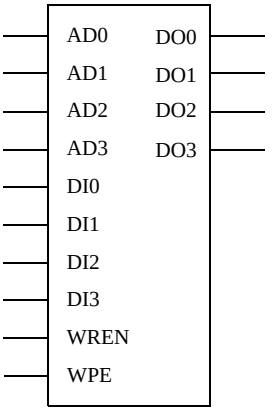
RPE16X4

16 Word by 4 Bit Static Memory with Positive Write Enable and Positive Write Port Enable

ORCA Series		
2	3	4
✓		



RPE16X4

INPUTS: AD0,AD1,AD2,AD3,DI0,DI1,DI2,DI3,WREN,WPE
OUTPUTS: DO0,DO1,DO2,DO3
PINORDER: AD0 AD1 AD2 AD3 DI0 DI1 DI2 DI3 WREN WPE DO0 DO1 DO2 DO3
MINIMUM CELL AREA: 1.0

Description:

The RPE16x4 symbol represents a 16 word by 4 bit static RAM. It has four data inputs DI[3:0], a positive Write Enable (WREN), and a positive Write Port Enable (WPE). Writing to the RAM does not occur until *both* the WREN and WPE signals are enabled. If the write enable(s) is HIGH the data is written into the locations specified by the address lines AD[3:0]. If the write enable(s) is LOW the data contents of the memory at the specified address appear at the data outputs DO[3:0].

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If desired, the contents of the RPE16x4 can be assigned an initial value, which will be loaded into the RAM during configuration. The INITVAL=<*value*> parameter is used to assign the initial value. The <*value*> should consist of sixteen 4 bit binary or hexadecimal data written into the RAM from the highest address to the lowest address. For example, if the following attribute is specified:

`INITVAL=0000000100100011010001010110011110001001101010111001101111101111` (in binary)

or

`INITVAL=0x0123456789ABCDEF` (in hex)

it implies that the above data is loaded sequentially from location FH to 0H (where FH would contain the 0 and 0H the F). If no INITVAL= parameter is specified, the RAM is initialized with zeros on configuration.

RAM cells can be configured as ROM by connecting the WREN and WPE signals to ground (VLO) and supplying initial values to the memory element via the INITVAL attribute. To initialize the element for simulation, refer to the ORCA simulation tool's interface manual.

Truth Table:

INPUTS				OUTPUTS	OPERATION
DI[3:0]	WREN	WPE	AD[3:0]	DO[3:0]	
DI[3:0]	1	1	AD[3:0]	MEM[AD[3:0]]	Write DI[3:0] into AD[3:0]
X	X	X	AD[3:0]	MEM[AD[3:0]]	Read MEM[AD[3:0]]

X = Don't care

Note: The memory is always being read. New data is read out after a write.

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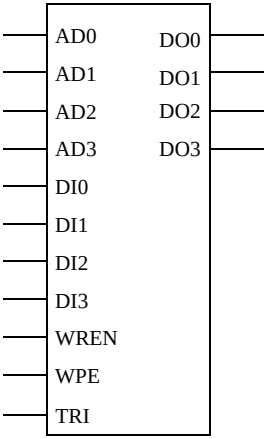
RPE16X4Z

16 Word by 4 Bit Static Memory with Positive Write Enable, Positive Write Port Enable, and Positive Tristate Control

ORCA Series		
2	3	4
✓		



RPE16X4Z

INPUTS: AD0,AD1,AD2,AD3,DI0,DI1,DI2,DI3, WREN,WPE,TRI
OUTPUTS: DO0,DO1,DO2,DO3
PINORDER: AD0 AD1 AD2 AD3 DI0 DI1 DI2 DI3 WREN WPE TRI DO0 DO1 DO2 DO3
MINIMUM CELL AREA: 1.0

Description:

The RPE16x4Z symbol represents a 16 word by 4 bit static RAM with tristated outputs. It has four data inputs DI[3:0], a positive Write Enable (WREN), a positive Write Port Enable (WPE), and a positive tristate control (TRI).

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Writing to the RAM does not occur until *both* the WREN and WPE signals are enabled. If the write enable(s) is HIGH the data is written into the locations specified by the address lines AD[3:0]. If the write enable(s) is LOW the data contents of the memory at the specified address appear at the data outputs DO[3:0]. The outputs can be tristated by enabling the TRI control signal HIGH. This is to enable the use of the outputs in a bus format and to drive the outputs into a high impedance state.

If desired, the contents of the RPE16x4Z can be assigned an initial value, which will be loaded into the RAM during configuration. The INITVAL=<*value*> parameter is used to assign the initial value. The <*value*> should consist of sixteen 4 bit binary or hexadecimal data written into the RAM from the highest address to the lowest address. For example, if the following attribute is specified

`INITVAL=0000000100100011010001010110011110001001101010111100110111101111` (in binary)

or

`INITVAL=0x0123456789ABCDEF` (in hex)

it implies that the above data is loaded sequentially from location FH to 0H (where FH would contain the 0 and 0H the F). If no INITVAL= parameter is specified, the RAM is initialized with zeros on configuration.

RAM cells can be configured as ROM by connecting the WREN and WPE signals to ground (VLO) and supplying initial values to the memory element via the INITVAL attribute. To initialize the element for simulation, refer to the ORCA simulation tool's interface manual.

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Truth Table:

INPUTS					OUTPUTS	OPERATION
DI[3:0]	WREN	WPE	TRI	AD[3:0]	DO[3:0]	
DI[3:0]	1	1	1	AD[3:0]	Z	Tristate outputs, but write DI[3:0] into AD[3:0]
DI[3:0]	1	1	0	AD[3:0]	MEM[AD[3:0]]	Write DI[3:0] into AD[3:0]
DI[3:0]	X	X	1	AD[3:0]	Z	Tristate
X	X	X	0	AD[3:0]	MEM[AD[3:0]]	Read MEM[AD[3:0]]

X = Don’t care

Note: The memory is always being read. New data is read out after a write, except when in tristate.

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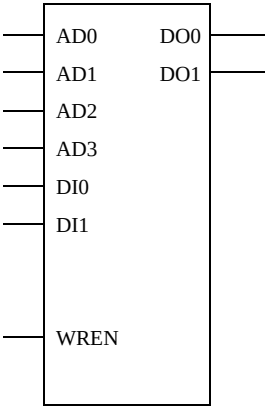
RPP16X2

16 Word by 2 Bit Static Memory with Positive Write Enable

ORCA Series		
2	3	4
✓		



RPP16X2

INPUTS: AD0,AD1,AD2,AD3,DI0,DI1,WREN
OUTPUTS: DO0,DO1
PINORDER: AD0 AD1 AD2 AD3 DI0 DI1 WREN DO0 DO1
MINIMUM CELL AREA: 1.0

Description:

The RPP16x2 symbol represents a 16 word by 2 bit static RAM. It has two data inputs DI[1:0], a positive Write Enable (WREN), four address inputs AD[0:3], and two data outputs DO[1:0]. If the WREN signal is HIGH, the data at inputs DI[1:0] are written into the locations specified by address lines AD[0:3]. When the WREN signal is LOW the data at the contents of the memory at the specified address appear at the data output.

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If desired, the contents of the RPP16x2 can be assigned an initial value, which is loaded into the RAM during configuration. The INITVAL=<*value*> parameter is used to assign the initial value. The <*value*> should consist of sixteen 2 bit binary or hexadecimal data written into the RAM from the highest address to the lowest address. For example, if the following attribute is specified:

`INITVAL=0001101100011011000110110001101l` (in binary)
or
`INITVAL=0x0123012301230123` (in hex)

it implies that the above data is loaded sequentially from location FH to 0H (where FH would contain the 0 and 0H the 3). If no INITVAL= parameter is specified, the RAM is initialized with zeros on configuration.

If the INITVAL is specified as a hex string of 16 values, the values should not be greater than 3, since 3 is setting both memory locations to 1. If a value greater than 3 is used for synthesis/mapping, only the last two (least significant) bits are used for initialization by the mapper. For example,

`INITVAL=0x00000000ffffffff`
is equivalent to
`INITVAL=0x0000000033333333`

for mapping purposes, since the first two bits of the “f” are ingnored.

If a value other than 0,1,2 or 3 is used for simulation, the simulator will return undefined (‘U’) results for the data. Therefore, simulation results and actual mapped results could vary. For this reason, it is highly recommended to restrict initial hex strings to values of 0,1,2 or 3 for 2 bit wide memories.

RAM cells can be configured as ROM by connecting the WREN signal to ground (VLO) and supplying initial values to the memory element via the INITVAL attribute. To initialize the element for simulation, refer to the ORCA simulation tool’s interface manual.

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Truth Table:

INPUTS			OUTPUTS	OPERATION
DI[1:0]	WREN	AD[3:0]	DO[1:0]	
DI[1:0]	1	AD[3:0]	MEM[AD[3:0]]	Write DI[1:0] into AD[3:0]
X	0	AD[3:0]	MEM[AD[3:0]]	Read MEM[AD[3:0]]

X = Don’t care
Note: The memory is always being read. New data is read out after a write.

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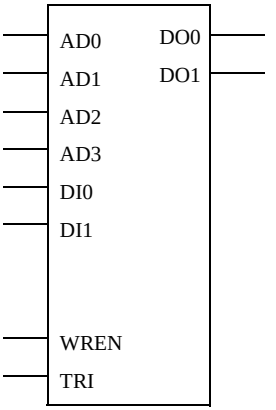
RPP16X2Z

16 Word by 2 Bit Static Memory with Tristated Outputs, Positive Write Enable and Positive Tristate Control

ORCA Series		
2	3	4
✓		



RPP16X2Z

INPUTS: AD0,AD1,AD2,AD3,DI0,DI1,WREN,TRI
OUTPUTS: DO0,DO1
PINORDER: AD0 AD1 AD2 AD3 DI0 DI1 WREN TRI DO0 DO1
MINIMUM CELL AREA: 1.0

Description:

The RPP16x2Z symbol represents a 16 word by 2 bit static RAM with tristated outputs. It has two data inputs DI[1:0], a positive Write Enable (WREN), four address inputs AD[0:3], two data outputs DO[1:0], and a positive tristate control signal TRI.

If the WREN signal is HIGH, the data at inputs DI[1:0] are written into the locations specified by address lines AD[0:3]. When the WREN signal is LOW the data at the contents of the memory at the specified address appear at the data output. The outputs can be tristated by enabling the TRI control signal HIGH. This is to enable the use of the outputs in a bus format.

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If desired, the contents of the RPP16x2Z can be assigned an initial value, which is loaded into the RAM during configuration. The INITVAL=<*value*> parameter is used to assign the initial value. The <*value*> should consist of sixteen 2 bit binary or hexadecimal data written into the RAM from the highest address to the lowest address. For example, if the following attribute is specified:

`INITVAL=00011011000110110001101100011011` (in binary)
or
`INITVAL=0x0123012301230123` (in hex)

it implies that the above data is loaded sequentially from location FH to 0H (where FH would contain the 0 and 0H the 3). If no INITVAL= parameter is specified, the RAM is initialized with zeros on configuration.

If the INITVAL is specified as a hex string of 16 values, the values should not be greater than 3, since 3 is setting both memory locations to 1. If a value greater than 3 is used for synthesis/mapping, only the last two (least significant) bits are used for initialization by the mapper. For example,

`INITVAL=0x00000000ffffffff`
is equivalent to
`INITVAL=0x0000000033333333`

for mapping purposes, since the first two bits of the “f” are ingnored.

If a value other than 0,1,2 or 3 is used for simulation, the simulator will return undefined (‘U’) results for the data. Therefore, simulation results and actual mapped results could vary. For this reason, it is highly recommended to restrict initial hex strings to values of 0,1,2 or 3 for 2 bit wide memories.

RAM cells can be configured as ROM by connecting the WREN signal to ground (VLO) and supplying initial values to the memory element via the INITVAL attribute. To initialize the element for simulation, refer to the ORCA simulation tool’s interface manual.

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Truth Table:

INPUTS				OUTPUTS	OPERATION
DI[1:0]	WREN	TRI	AD[3:0]	DO[1:0]	
DI[1:0]	1	1	AD[3:0]	Z	Tristate outputs, but write DI[1:0] into AD[3:0]
DI[1:0]	1	0	AD[3:0]	MEM[AD[3:0]]	Write DI[1:0] into AD[3:0]
DI[1:0]	0	1	AD[3:0]	Z	Tristate
X	0	0	AD[3:0]	MEM[AD[3:0]]	Read MEM[AD[3:0]]

X = Don’t care
Note: The memory is always being read. New data is read out after a write, except when in tristate.

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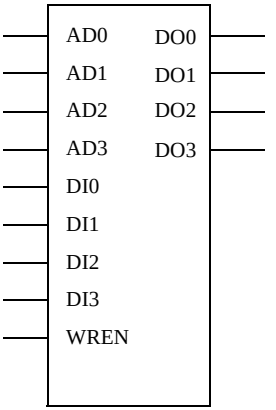
RPP16X4

16 Word by 4 Bit Static Memory with Positive Write Enable

ORCA Series		
2	3	4
✓		



RPP16X4

INPUTS: AD0,AD1,AD2,AD3,DI0,DI1,DI2,DI3,WREN
OUTPUTS: DO0,DO1,DO2,DO3
PINORDER: AD0 AD1 AD2 AD3 DI0 DI1 DI2 DI3 WREN DO0 DO1 DO2 DO3
MINIMUM CELL AREA: 1.0

Description:

The RPP16x4 symbol represents a 16 word by 4 bit static RAM. It has four data inputs DI[0:3], a positive Write Enable (WREN), four address inputs AD[0:3], and four data outputs DO[0:3]. If the WREN signal is HIGH, the data at inputs DI[0:3] is written into the locations specified by address lines AD[0:3]. When the WREN signal is LOW the data at the contents of the memory at the specified address appears at the data output.

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If desired, the contents of the RPP16x4 can be assigned an initial value, which will be loaded into the RAM during configuration. The INITVAL=<*value*> parameter is used to assign the initial value. The <*value*> should consist of sixteen 4 bit binary or hexadecimal data written into the RAM from the highest address to the lowest address. For example, if the following attribute is specified:

`INITVAL=0000000100100011010001010110011110001001101010111001101111101111` (in binary)

or

`INITVAL=0x0123456789ABCDEF` (in hex)

it implies that the above data is loaded sequentially from location FH to 0H (where FH would contain the 0 and 0H the F). If no INITVAL= parameter is specified, the RAM is initialized with zeros on configuration.

RAM cells can be configured as ROM by connecting the WREN signal to ground (VLO) and supplying initial values to the memory element via the INITVAL attribute. To initialize the element for simulation, refer to the ORCA simulation tool's interface manual.

Truth Table:

INPUTS			OUTPUTS	OPERATION
DI[3:0]	WREN	AD[3:0]	DO[3:0]	
DI[3:0]	1	AD[3:0]	MEM[AD[3:0]]	Write DI[3:0] into AD[3:0]
X	0	AD[3:0]	MEM[AD[3:0]]	Read MEM[AD[3:0]]

X = Don't care
Note: The memory is always being read. New data is read out after a write.

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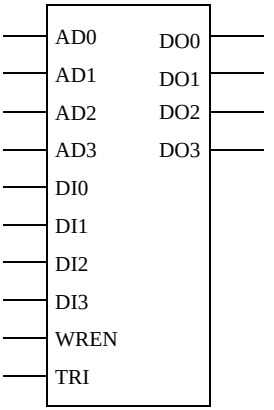
RPP16X4Z

16 Word by 4 Bit Static Memory with Tristated Outputs, Positive Write Enable and Positive Tristate Control

ORCA Series		
2	3	4
✓		



RPP16X4Z

INPUTS: AD0,AD1,AD2,AD3,DI0,DI1,DI2,DI3,WREN,TRI
OUTPUTS: DO0,DO1,DO2,DO3
PINORDER: AD0 AD1 AD2 AD3 DI0 DI1 DI2 DI3 WREN TRI DO0 DO1 DO2 DO3
MINIMUM CELL AREA: 1.0

Description:

The RPP16x4Z symbol represents a 16 word by 4 bit static RAM with tristated outputs. It has four data inputs DI[0:3], a positive Write Enable (WREN), four address inputs AD[0:3], four data outputs DO[0:3], and a positive tristate control signal TRI.

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If the WREN signal is HIGH, the data at inputs DI[0:3] is written into the locations specified by address lines AD[0:3]. When the WREN signal is LOW the data at the contents of the memory at the specified address appears at the data output. The outputs can be tristated by enabling the TRI control signal HIGH. This is to enable the use of the outputs in a bus format and to drive the outputs into a high impedance state.

If desired, the contents of the RPP16x4Z can be assigned an initial value, which will be loaded into the RAM during configuration. The INITVAL=<*value*> parameter is used to assign the initial value. The <*value*> should consist of sixteen 4 bit binary or hexadecimal data written into the RAM from the highest address to the lowest address. For example, if the following attribute is specified:

`INITVAL=0000000100100011010001010110011110001001101010111001101111101111` (in binary)

or

`INITVAL=0x0123456789ABCDEF` (in hex)

it implies that the above data is loaded sequentially from location FH to 0H (where FH would contain the 0 and 0H the F). If no INITVAL= parameter is specified, the RAM is initialized with zeros on configuration.

RAM cells can be configured as ROM by connecting the WREN signal to ground (VLO) and supplying initial values to the memory element via the INITVAL attribute. To initialize the element for simulation, refer to the ORCA simulation tool's interface manual.

continued

Truth Table:

INPUTS				OUTPUTS	OPERATION
DI[3:0]	WREN	TRI	AD[3:0]	DO[3:0]	
DI[3:0]	1	1	AD[3:0]	Z	Tristate outputs, but write DI[3:0] into AD[3:0]

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INPUTS				OUTPUTS	OPERATION
DI[3:0]	WREN	TRI	AD[3:0]	DO[3:0]	
DI[3:0]	1	0	AD[3:0]	MEM[AD[3:0]]	Write DI[3:0] into AD[3:0]
DI[3:0]	0	1	AD[3:0]	Z	Tristate
X	0	0	AD[3:0]	MEM[AD[3:0]]	Read MEM[AD[3:0]]

X = Don’t care

Note: The memory is always being read. New data is read out after a write, except when in tristate.

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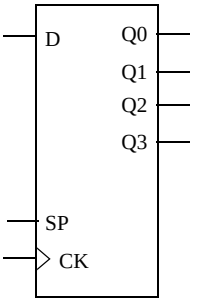
RS4P3A

Positive Edge Triggered 4 Bit Shift Register with Positive Level Enable

ORCA Series		
2	3	4
✓		



RS4P3A

Truth Table:

INPUTS			OUTPUTS			
D	SP	CK	Q0	Q1	Q2	Q3
X	0	X	Q0	Q1	Q2	Q3
0	1	↑	0	Q0	Q1	Q2
1	1	↑	1	Q0	Q1	Q2

X = Don’t care
When GSR=0, Q[0:3]=0 (D=SP=CK=X)

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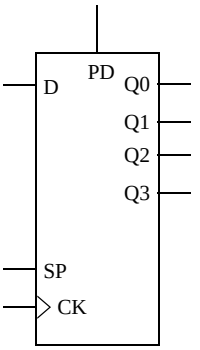
RS4P3B

Positive Edge Triggered 4 Bit Shift Register with Positive Level Enable and Positive Level Asynchronous Preset

ORCA Series		
2	3	4
✓		



RS4P3B

INPUTS: D,SP,CK,PD
OUTPUTS: Q0,Q1,Q2,Q3
PINORDER: D SP CK PD Q0 Q1 Q2 Q3
MINIMUM CELL AREA: 1.0

Truth Table:

INPUTS				OUTPUTS			
D	SP	CK	PD	Q0	Q1	Q2	Q3
X	X	X	1	1	1	1	1
X	0	X	0	Q0	Q1	Q2	Q3
0	1	↑	0	0	Q0	Q1	Q2
1	1	↑	0	1	Q0	Q1	Q2

X = Don’t care
When GSR=0, Q[0:3]=1 (D=SP=CK=X)

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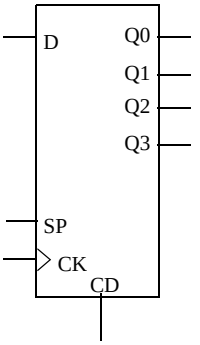
RS4P3D

Positive Edge Triggered 4 Bit Shift Register with Positive Level Enable and Positive Level Asynchronous Clear

ORCA Series		
2	3	4
✓		



RS4P3D

INPUTS: D,SP,CK,CD
OUTPUTS: Q0,Q1,Q2,Q3
PINORDER: D SP CK CD Q0 Q1 Q2 Q3
MINIMUM CELL AREA: 1.0

Truth Table:

INPUTS				OUTPUTS			
D	SP	CK	CD	Q0	Q1	Q2	Q3
X	X	X	1	0	0	0	0
X	0	X	0	Q0	Q1	Q2	Q3
0	1	↑	0	0	Q0	Q1	Q2
1	1	↑	0	1	Q0	Q1	Q2

X = Don’t care
When GSR=0, Q[0:3]=0 (D=SP=CK=X)

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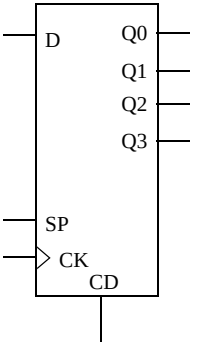
RS4P3I

Positive Edge Triggered 4 Bit Shift Register with Positive Level Enable and Positive Level Synchronous Clear

ORCA Series		
2	3	4
✓		



RS4P3I

INPUTS: D,SP,CK,CD
OUTPUTS: Q0,Q1,Q2,Q3
PINORDER: D SP CK CD Q0 Q1 Q2 Q3
MINIMUM CELL AREA: 1.0

Truth Table:

INPUTS				OUTPUTS			
D	SP	CK	CD	Q0	Q1	Q2	Q3
X	0	X	X	Q0	Q1	Q2	Q3
X	1	↑	1	0	0	0	0
0	1	↑	0	0	Q0	Q1	Q2
1	1	↑	0	1	Q0	Q1	Q2

X = Don’t care
When GSR=0, Q[0:3]=0 (D=SP=CK=X)

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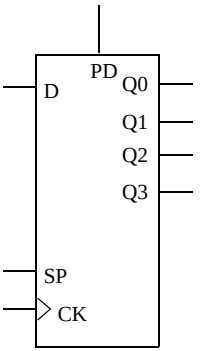
RS4P3J

Positive Edge Triggered 4 Bit Shift Register with Positive Level Enable and Positive Level Synchronous Preset

ORCA Series		
2	3	4
✓		



RS4P3J

INPUTS: D,SP,CK,PD
OUTPUTS: Q0,Q1,Q2,Q3
PINORDER: D SP CK PD Q0 Q1 Q2 Q3
MINIMUM CELL AREA: 1.0

Truth Table:

INPUTS				OUTPUTS			
D	SP	CK	PD	Q0	Q1	Q2	Q3
X	0	X	X	Q0	Q1	Q2	Q3
X	1	↑	1	1	1	1	1
0	1	↑	0	0	Q0	Q1	Q2
1	1	↑	0	1	Q0	Q1	Q2

X = Don’t care
When GSR=0, Q[0:3]=1 (D=SP=CK=X)

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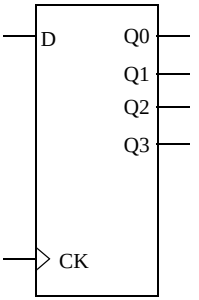
RS4S3A

Positive Edge Triggered 4 Bit Shift Register

ORCA Series		
2	3	4
✓		



RS4S3A

INPUTS: D,CK
OUTPUTS: Q0,Q1,Q2,Q3
PINORDER: D CK Q0 Q1 Q2 Q3
MINIMUM CELL AREA: 1.0

Truth Table:

INPUTS		OUTPUTS			
D	CK	Q0	Q1	Q2	Q3
0	↑	0	Q0	Q1	Q2
1	↑	1	Q0	Q1	Q2

X = Don’t care
When GSR=0, Q[0:3]=0 (D=CK=X)

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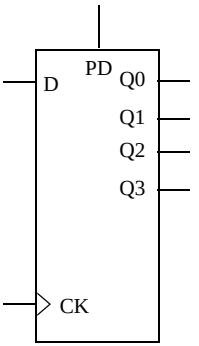
RS4S3B

Positive Edge Triggered 4 Bit Shift Register with Positive Level Asynchronous Preset

ORCA Series		
2	3	4
✓		



RS4S3B

INPUTS: D,CK,PD
OUTPUTS: Q0,Q1,Q2,Q3
PINORDER: D CK PD Q0 Q1 Q2 Q3
MINIMUM CELL AREA: 1.0

Truth Table:

INPUTS			OUTPUTS			
D	CK	PD	Q0	Q1	Q2	Q3
X	X	1	1	1	1	1
0	↑	0	0	Q0	Q1	Q2
1	↑	0	1	Q0	Q1	Q2

X = Don’t care
When GSR=0, Q[0:3]=1 (D=CK=X)

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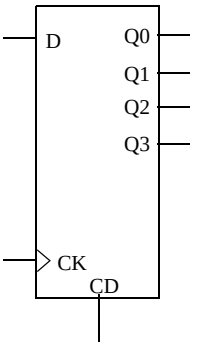
RS4S3D

Positive Edge Triggered 4 Bit Shift Register with Positive Level Asynchronous Clear

ORCA Series		
2	3	4
✓		



RS4S3D

INPUTS: D,CK,CD
OUTPUTS: Q0,Q1,Q2,Q3
PINORDER: D CK CD Q0 Q1 Q2 Q3
MINIMUM CELL AREA: 1.0

Truth Table:

INPUTS			OUTPUTS			
D	CK	CD	Q0	Q1	Q2	Q3
X	X	1	0	0	0	0
0	↑	0	0	Q0	Q1	Q2
1	↑	0	1	Q0	Q1	Q2

X = Don’t care
When GSR=0, Q[0:3]=0 (D=CK=X)

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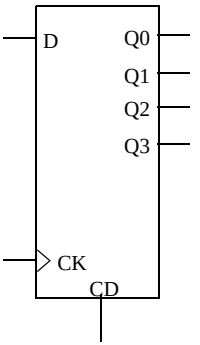
RS4S3I

Positive Edge Triggered 4 Bit Shift Register with Positive Level Synchronous Clear

ORCA Series		
2	3	4
✓		



RS4S3I

INPUTS: D,CK,CD
OUTPUTS: Q0,Q1,Q2,Q3
PINORDER: D CK CD Q0 Q1 Q2 Q3
MINIMUM CELL AREA: 1.0

Truth Table:

INPUTS			OUTPUTS			
D	CK	CD	Q0	Q1	Q2	Q3
X	↑	1	0	0	0	0
0	↑	0	0	Q0	Q1	Q2
1	↑	0	1	Q0	Q1	Q2

X = Don’t care
When GSR=0, Q[0:3]=0 (D=CK=X)

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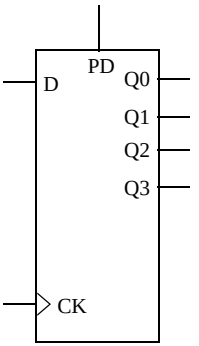
RS4S3J

Positive Edge Triggered 4 Bit Shift Register with Positive Level Synchronous Preset

ORCA Series		
2	3	4
✓		



RS4S3J

INPUTS: D,CK,PD
OUTPUTS: Q0,Q1,Q2,Q3
PINORDER: D CK PD Q0 Q1 Q2 Q3
MINIMUM CELL AREA: 1.0

Truth Table:

INPUTS			OUTPUTS			
D	CK	PD	Q0	Q1	Q2	Q3
X	↑	1	1	1	1	1
0	↑	0	0	Q0	Q1	Q2
1	↑	0	1	Q0	Q1	Q2

X = Don’t care
When GSR=0, Q[0:3]=1 (D=CK=X)

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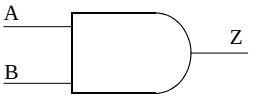
SAND2

2 Input AND Gate (used in SLIC area only)

ORCA Series		
2	3	4
	✓	✓



SAND2

INPUTS: A,B
OUTPUTS: Z
PINORDER: A B Z
MINIMUM CELL AREA: 0

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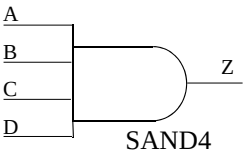
SAND4

4 Input AND Gate (used in SLIC area only)

ORCA Series		
2	3	4
	✓	✓



INPUTS: A,B,C,D
OUTPUTS: Z
PINORDER: A B C D Z
MINIMUM CELL AREA: 0

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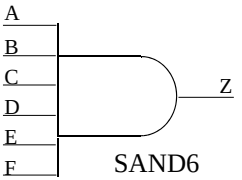
SAND6

6 Input AND Gate (used in SLIC area only)

ORCA Series		
2	3	4
	✓	✓



INPUTS: A,B,C,D,E,F
OUTPUTS: Z
PINORDER: A B C D E F Z
MINIMUM CELL AREA: 0

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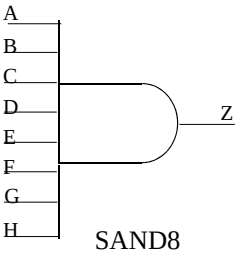
SAND8

8 Input AND Gate (used in SLIC area only)

ORCA Series		
2	3	4
	✓	✓



SAND8

INPUTS: A,B,C,D,E,F,G,H
OUTPUTS: Z
PINORDER: A B C D E F G H Z
MINIMUM CELL AREA: 0

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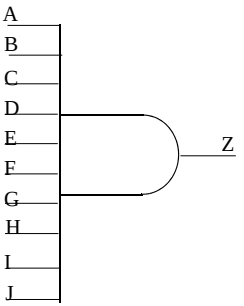
SAND10

10 Input AND Gate (used in SLIC area only)

ORCA Series		
2	3	4
	✓	✓



SAND10

INPUTS: A,B,C,D,E,F,G,H,I,J
OUTPUTS: Z
PINORDER: A B C D E F G H I J Z
MINIMUM CELL AREA: 0

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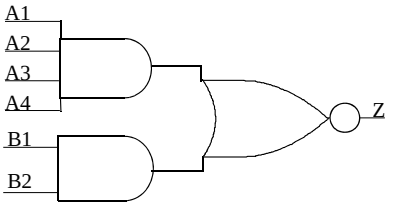
SAOI42

AND Array to OR Inverted (used in SLIC area only)

ORCA Series		
2	3	4
	✓	✓



SAOI42

INPUTS: A1,A2,A3,A4,B1,B2
OUTPUTS: Z
PINORDER: A1 A2 A3 A4 B1 B2 Z
MINIMUM CELL AREA: 0

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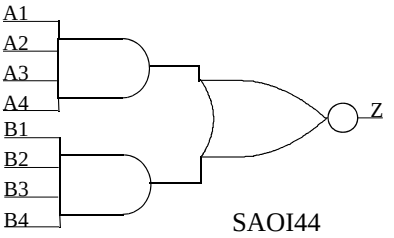
SAOI44

AND Array to OR Inverted (used in SLIC area only)

ORCA Series		
2	3	4
	✓	✓



SAOI44

INPUTS: A1,A2,A3,A4,B1,B2,B3,B4
OUTPUTS: Z
PINORDER: A1 A2 A3 A4 B1 B2 B3 B4 Z
MINIMUM CELL AREA: 0

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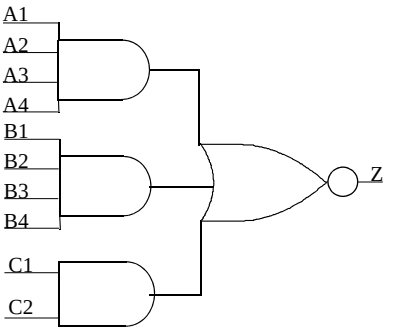
SAOI442

AND Array to OR Inverted (used in SLIC area only)

ORCA Series		
2	3	4
	✓	✓



SAOI442

INPUTS: A1,A2,A3,A4,B1,B2,B3,B4,C1,C2
OUTPUTS: Z
PINORDER: A1 A2 A3 A4 B1 B2 B3 B4 C1 C2 Z
MINIMUM CELL AREA: 0

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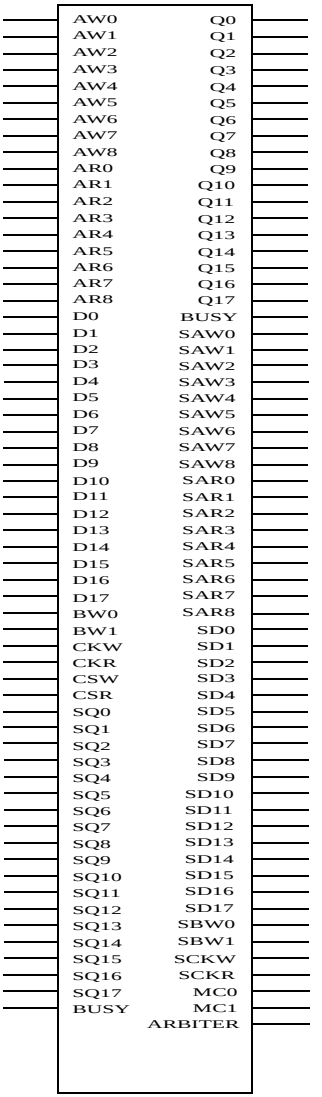
SBR512X18

512 Word by 18 Bit System Bus RAM

ORCA Series		
2	3	4
		✓



SBR512X18

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INPUTS: AW0, AW1, AW2, AW3, AW4, AW5, AW6, AW7, AW8, AR0, AR1, AR2, AR3, AR4, AR5, AR6, AR7, AR8, D0, D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, D16, D17, BW0, BW1, CKW, CKR, CSW, CSR, SQ0, SQ1, SQ2, SQ3, SQ4, SQ5, SQ6, SQ7, SQ8, SQ9, SQ10, SQ11, SQ12, SQ13, SQ14, SQ15, SQ16, SQ17, SBUSY

OUTPUTS: Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8, Q9, Q10, Q11, Q12, Q13, Q14, Q15, Q16, Q17, BUSY, SAW0, SAW1, SAW2, SAW3, SAW4, SAW5, SAW6, SAW7, SAW8, SAR0, SAR1, SAR2, SAR3, SAR4, SAR5, SAR6, SAR7, SAR8, SD0, SD1, SD2, SD3, SD4, SD5, SD6, SD7, SD8, SD9, SD10, SD11, SD12, SD13, SD14, SD15, SD16, SD17, SBW0, SBW1, SCKW, SCKR, SCSW, SCSR, MC0, MC1, ARBITER

PINORDER: AW0 AW1 AW2 AW3 AW4 AW5 AW6 AW7 AW8 AR0 AR1 AR2 AR3 AR4 AR5 AR6 AR7 AR8 D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16 D17 BW0 BW1 CKW CKR CSW CSR SQ0 SQ1 SQ2 SQ3 SQ4 SQ5 SQ6 SQ7 SQ8 SQ9 SQ10 SQ11 SQ12 SQ13 SQ14 SQ15 SQ16 SQ17 SBUSY Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 Q10 Q11 Q12 Q13 Q14 Q15 Q16 Q17 BUSY SAW0 SAW1 SAW2 SAW3 SAW4 SAW5 SAW6 SAW7 SAW8 SAR0 SAR1 SAR2 SAR3 SAR4 SAR5 SAR6 SAR7 SAR8 SD0 SD1 SD2 SD3 SD4 SD5 SD6 SD7 SD8 SD9 SD10 SD11 SD12 SD13 SD14 SD15 SD16 SD17 SBW0 SBW1 SCKW SCKR SCSW SCSR MC0 MC1 ARBITER

ATTRIBUTES (Series 4 only)
BRAMMODE: NOREG, INREG, OUTREG, IOREG
ARBITERMODE : TRUE, FALSE

Description:

There is one write port (AW[0:8]) and one read port (AR[0:8]).

Example pin functions:

Function	Pins
write address	AW0, AW1,...AW8
read address	AR0, AR1,...AR8
data (18-bit)	D0, D1,...D17
port-1 byte enable	BW0, BW1

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Function	Pins
write clock	CKW
read clock	CKR
write enable	CSW
read enable	CSR

Data can be written into the memory at the rising edge of the write clock when write enable is HIGH and byte enable is HIGH.

Attribute	
BRRAMODE[*]	“INREG” - Read address is registered. “OUTREG” - Data out is registered. “IOREG” - Both read address and data out are registered. “NOREG” - (default) Nothing is registered.

When ARBITERMODE is “TRUE,” then the arbitration function is enabled.

Function	Pins
output	Q0, Q1,...Q17

***Note*:** The SBR512X18 element should be instantiated through SCUBA. Refer to the appropriate topic in the online help system for details.

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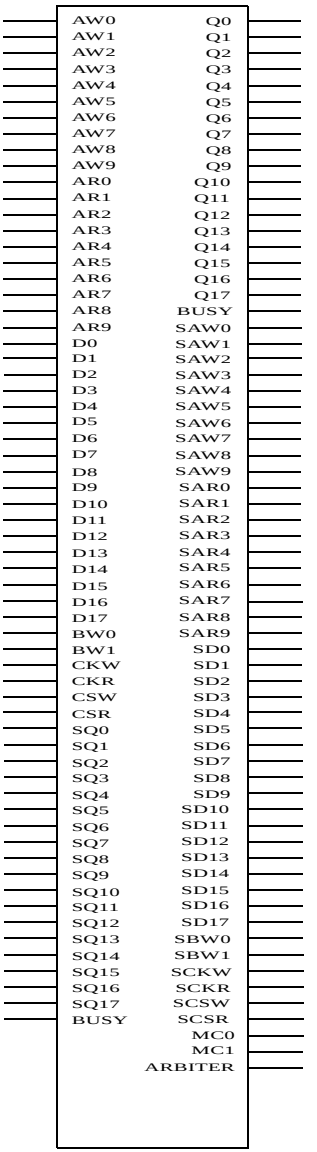
SBR1024X18

1024 Word by 18 Bit System Bus RAM

ORCA Series		
2	3	4
		✓



SBR1024X18

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INPUTS: AW0, AW1, AW2, AW3, AW4, AW5, AW6, AW7, AW8, AW9, AR0, AR1, AR2, AR3, AR4, AR5, AR6, AR7, AR8, AR9, D0, D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, D16, D17, BW0, BW1, CKW, CKR, CSW, CSR, SQ0, SQ1, SQ2, SQ3, SQ4, SQ5, SQ6, SQ7, SQ8, SQ9, SQ10, SQ11, SQ12, SQ13, SQ14, SQ15, SQ16, SQ17, SBUSY

OUTPUTS: Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8, Q9, Q10, Q11, Q12, Q13, Q14, Q15, Q16, Q17, BUSY, SAW0, SAW1, SAW2, SAW3, SAW4, SAW5, SAW6, SAW7, SAW8, SAW9, SAR0, SAR1, SAR2, SAR3, SAR4, SAR5, SAR6, SAR7, SAR8, SAR9, SD0, SD1, SD2, SD3, SD4, SD5, SD6, SD7, SD8, SD9, SD10, SD11, SD12, SD13, SD14, SD15, SD16, SD17, SBW0, SBW1, SCKW, SCKR, SCSW, SCSR, MC0, MC1, ARBITER

PINORDER: AW0 AW1 AW2 AW3 AW4 AW5 AW6 AW7 AW8 AW9 AR0 AR1 AR2 AR3 AR4 AR5 AR6 AR7 AR8 AR9 D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16 D17 BW0 BW1 CKW CKR CSW CSR SQ0 SQ1 SQ2 SQ3 SQ4 SQ5 SQ6 SQ7 SQ8 SQ9 SQ10 SQ11 SQ12 SQ13 SQ14 SQ15 SQ16 SQ17 SBUSY Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 Q10 Q11 Q12 Q13 Q14 Q15 Q16 Q17 BUSY SAW0 SAW1 SAW2 SAW3 SAW4 SAW5 SAW6 SAW7 SAW8 SAW9 SAR0 SAR1 SAR2 SAR3 SAR4 SAR5 SAR6 SAR7 SAR8 SAR9 SD0 SD1 SD2 SD3 SD4 SD5 SD6 SD7 SD8 SD9 SD10 SD11 SD12 SD13 SD14 SD15 SD16 SD17 SBW0 SBW1 SCKW SCKR SCSW SCSR MC0 MC1 ARBITER

ATTRIBUTES (Series 4 only)

BRAMMODE: NOREG, INREG, OUTREG, IOREG

ARBITERMODE: TRUE, FALSE

Description:

There is one write port (AW[9:0]) and one read port (AR[9:0]).

Example pin functions:

Function	Pins
write address	AW0, AW1,...AW9
read address	AR0, AR1,...AR9
data (18-bit)	D0, D1,...D17
port-1 byte enable	BW0, BW1

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Function	Pins
write clock	CKW
read clock	CKR
write enable	CSW
read enable	CSR

Data can be written into the memory at the rising edge of the write clock when write enable is HIGH and byte enable is HIGH.

Attribute	
BRRAMODE[*]	“INREG” - Read address is registered. “OUTREG” - Data out is registered. “IOREG” - Both read address and data out are registered. “NOREG” - (default) Nothing is registered.

When ARBITERMODE is “TRUE,” then the arbitration function is enabled.

Function	Pins
output	Q0, Q1,...Q17

***Note*:** The SBR1024X18 element should be instantiated through SCUBA. Refer to the appropriate topic in the online help system for details.

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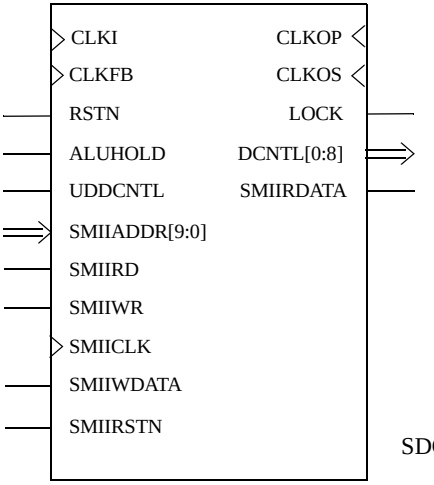
SDCDLLA

Single Delay Cell DLL



SDCDLLA

Lattice FPGA		
SC	XP	EC
✓		

NOTE: The graphic is shown in bus notation for convenience. This element must be instantiated in expanded bus notation format with each individual bit as given below

INPUTS: CLKI, CLKFB, RSTN, ALUHOLD, UDDCNTL, SMIADDR9, SMIADDR8, SMIADDR7, SMIADDR6, SMIADDR5, SMIADDR4, SMIADDR3, SMIADDR2, SMIADDR1, SMIADDR0, SMIRD, SMIWR, SMICLK, SMIWDATA, SMIRSTN
OUTPUTS: CLKOP, CLKOS, LOCK, DCNTL0, DCNTL1, DCNTL2, DCNTL3, DCNTL4, DCNTL5, DCNTL6, DCNTL7, DCNTL8, SMIRDATA
PINORDER: CLKI, CLKFB, RSTN, ALUHOLD, UDDCNTL, SMIADDR9, SMIADDR8, SMIADDR7, SMIADDR6, SMIADDR5, SMIADDR4, SMIADDR3, SMIADDR2, SMIADDR1, SMIADDR0, SMIRD, SMIWR, SMICLK, SMIWDATA, SMIRSTN, CLKOP, CLKOS, LOCK, DCNTL0, DCNTL1, DCNTL2, DCNTL3, DCNTL4, DCNTL5, DCNTL6, DCNTL7, DCNTL8, SMIRDATA
CELL AREA: One Slice
ATTRIBUTES:
CLKOS_FPHASE: 0, 11.25, 22.5, 45
CLKOS_DIV: 1, 2, 3,...63, 64
DISABLED_GSR: 1, 0
PHASELOCK: DISABLED, ENABLED
CLKOS_FDEL_ADJ: DISABLED, ENABLED
ALU_LOCK_CNT: 3, 4, 5,...15
ALU_UNLOCK_CNT: 3, 4, 5,...15
GLITCH_TOLERANCE: 0, 1, 2,...7
DCNTL_ADJVAL: -127, -126, ..., -1, 0, 1, ..., 126, 127
ALU_INIT_CNTVAL: 0, 4, 8, 12, 16, 32, 48, 64, 72
SMI_OFFSET: 12'h410 (default hexidecimal value)
SMI_ADDR_DIS: 10'b0000000000 (default hexidecimal value)

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Description:

The single delay cell corrects for clock injection and enables the 9-bit ALU output. The element features a single clock output, lock achieved starting from minimum delay, output control bits, and allows +/- delay on output control bits. Its requirementsa maximum frequency of 700MHz and a minimum frequency of 300MHz.

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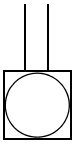
SGSR

Synchronous Release Global Set/Reset Interface

Lattice FPGA		
SC	XP	EC
✓		



SGSR

INPUTS: GSR, CK
PINORDER: GSR, CK
MINIMUM CELL AREA (All Series): 0

Description:

SGSR is used to reset or set all register elements in your design. The SGSR component can be connected to a net from an input buffer or an internally generated net. It is active LOW and when pulsed will set or reset all flip-flops, latches, registers, and counters to the same state as the local set or reset functionality. When input GSR is HIGH, the global siganl is released at the positive edge of the clock (CK).

It is not necessary to connect signals for SGSR to any register elements explictly. The function will be implicitly connected globally. The functionality of the SGSR for sequential cells without a local set or reset are described in the appropriate library manual page.

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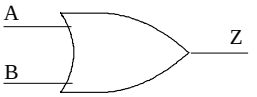
SOR2

2 Input OR Gate (used in SLIC area only)

ORCA Series		
2	3	4
	✓	✓



SOR2

INPUTS: A,B
OUTPUTS: Z
PINORDER: A B Z
MINIMUM CELL AREA: 0

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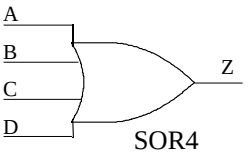
SOR4

4 Input OR Gate (used in SLIC area only)

ORCA Series		
2	3	4
	✓	✓



INPUTS: A,B,C,D
OUTPUTS: Z
PINORDER: A B C D Z
MINIMUM CELL AREA: 0

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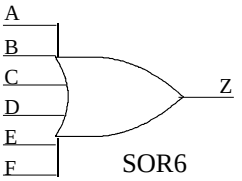
SOR6

6 Input OR Gate (used in SLIC area only)

ORCA Series		
2	3	4
	✓	✓



INPUTS: A,B,C,D,E,F
OUTPUTS: Z
PINORDER: A B C D E F Z
MINIMUM CELL AREA: 0

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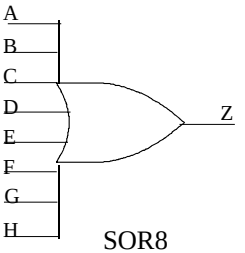
SOR8

8 Input OR Gate (used in SLIC area only)

ORCA Series		
2	3	4
	✓	✓



SOR8

INPUTS: A,B,C,D,E,F,G,H
OUTPUTS: Z
PINORDER: A B C D E F G H Z
MINIMUM CELL AREA: 0

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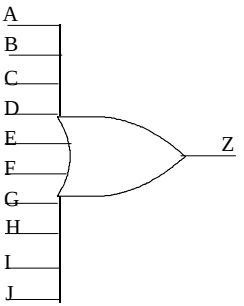
SOR10

10 Input OR Gate (used in SLIC area only)

ORCA Series		
2	3	4
	✓	✓



SOR10

INPUTS: A,B,C,D,E,F,G,H,I,J
OUTPUTS: Z
PINORDER: A B C D E F G H I J Z
MINIMUM CELL AREA: 0

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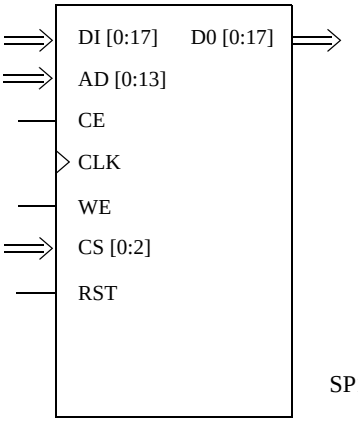
SP16KA

16K Single Port Block RAM

Lattice FPGA		
SC	XP	EC
✓		



SP16KA

NOTE: The graphic is shown in bus notation for convenience. This element must be instantiated in expanded bus notation format with each individual bit as given below.

INPUT: DI0, DI1, DI2, DI3, DI4, DI5, DI6, DI7, DI8, DI9, DI10, DI11, DI12, DI13, DI14, DI15, DI16, DI17, AD0, AD1, AD2, AD3, AD4, AD5, AD6, AD7, AD8, AD9, AD10, AD11, AD12, AD13, CE, CLK, WE, CS0, CS1, CS2, RST
OUTPUT: DO0, DO1, DO2, DO3, DO4, DO5, DO6, DO7, DO8, DO9, DO10, DO11, DO12, DO13, DO14, DO15, DO16, DO17
PINORDER: DI0, DI1, DI2, DI3, DI4, DI5, DI6, DI7, DI8, DI9, DI10, DI11, DI12, DI13, DI14, DI15, DI16, DI17, AD0, AD1, AD2, AD3, AD4, AD5, AD6, AD7, AD8, AD9, AD10, AD11, AD12, AD13, CE, CLK, WE, CS0, CS1, CS2, RST, DO0, DO1, DO2, DO3, DO4, DO5, DO6, DO7, DO8, DO9, DO10, DO11, DO12, DO13, DO14, DO15, DO16, DO17
ATTRIBUTES (Series 5-HSI only)
DATA_WIDTH: 1, 2, 4, 9, 18
REGMODE : NOREG, OUTREG
RESETMODE : ASYNC, SYNC
CSDECODE : 000, 001, 010, 011, 100, 101, 110, 111
WRITEMODE : NORMAL, WRITETHROUGH, READBEFOREWRITE
DISABLED_GSR: 0, 1
INIT: DISABLED, ENABLED
INIT_RECFG: DISABLED, ENABLED
INIT_ID: "0000000000"

Description:

Single Port RAM. See “Single Port RAM Port Definitions” on page 2.

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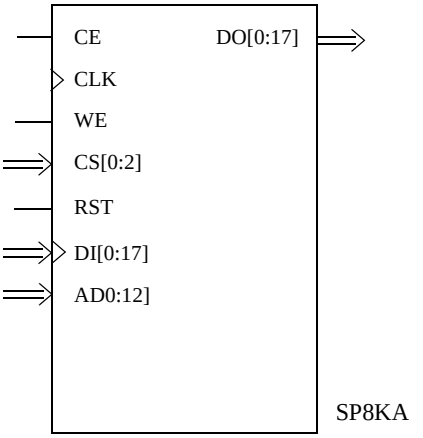
SP8KA

8K Single Port Block RAM

Lattice FPGA		
SC	XP	EC
	✓	✓



NOTE: The graphic is shown in bus notation for convenience. This element must be instantiated in expanded bus notation format with each individual bit as given below.

INPUT : CE, CLK, WE, CS0, CS1, CS2, RST, DI0, DI1, DI2, DI3, DI4, DI5, DI6, DI7, DI8, DI9, DI10, DI11, DI12, DI13, DI14, DI15, DI16, DI17, AD0, AD1, AD2, AD3, AD4, AD5, AD6, AD7, AD8, AD9, AD10, AD11, AD12
OUTPUT : DO0, DO1, DO2, DO3, DO4, DO5, DO6, DO7, DO8, DO9, DO10, DO11, DO12, DO13, DO14, DO15, DO16, DO17
PINORDER:CE, CLK, WE, CS0, CS1, CS2, RST, DI0, DI1, DI2, DI3, DI4, DI5, DI6, DI7, DI8, DI9, DI10, DI11, DI12, DI13, DI14, DI15, DI16, DI17, AD0, AD1, AD2, AD3, AD4, AD5, AD6, AD7, AD8, AD9, AD10, AD11, AD12, DO0, DO1, DO2, DO3, DO4, DO5, DO6, DO7, DO8, DO9, DO10, DO11, DO12, DO13, DO14, DO15, DO16, DO17
ATTRIBUTES (LatticeXP/EC)
DATA_WIDTH_W : 1, 2 , 4, 9, 18
DATA_WIDTH_R : 1, 2 , 4, 9, 18
REGMODE : NOREG, OUTREG
RESETMODE : ASYNC, SYNC
CSDECODE : 000, 001, 010, 011, 100, 101, 110, 111
GSR: ENABLED, DISABLED
WRITEMODE : NORMAL, WRITETHROUGH, READBEFOREWRITE
INITVAL_00 to _3F : 0xXX….X (80 hex characters)

Description:

Single Port RAM. See “Single Port RAM Port Definitions” on page 2.

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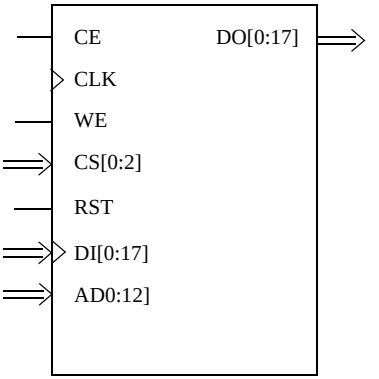
SP8KB

8K Single Port Block RAM



SP8KB

Lattice FPGA			
SC	XP	EC	MX
			✓

NOTE: The graphic is shown in bus notation for convenience. This element must be instantiated in expanded bus notation format with each individual bit as given below.

INPUT : CE, CLK, WE, CS0, CS1, CS2, RST, DI0, DI1, DI2, DI3, DI4, DI5, DI6, DI7, DI8, DI9, DI10, DI11, DI12, DI13, DI14, DI15, DI16, DI17, AD0, AD1, AD2, AD3, AD4, AD5, AD6, AD7, AD8, AD9, AD10, AD11, AD12
OUTPUT : DO0, DO1, DO2, DO3, DO4, DO5, DO6, DO7, DO8, DO9, DO10, DO11, DO12, DO13, DO14, DO15, DO16, DO17
PINORDER:CE, CLK, WE, CS0, CS1, CS2, RST, DI0, DI1, DI2, DI3, DI4, DI5, DI6, DI7, DI8, DI9, DI10, DI11, DI12, DI13, DI14, DI15, DI16, DI17, AD0, AD1, AD2, AD3, AD4, AD5, AD6, AD7, AD8, AD9, AD10, AD11, AD12, DO0, DO1, DO2, DO3, DO4, DO5, DO6, DO7, DO8, DO9, DO10, DO11, DO12, DO13, DO14, DO15, DO16, DO17
ATTRIBUTES (LatticeXP/EC/MACHxo)
DATA_WIDTH_W : 1, 2 , 4, 9, 18
DATA_WIDTH_R : 1, 2 , 4, 9, 18
REGMODE : NOREG, OUTREG
RESETMODE : ASYNC, SYNC
CSDECODE : 000, 001, 010, 011, 100, 101, 110, 111
GSR: ENABLED, DISABLED
WRITEMODE : NORMAL, WRITETHROUGH, READBEFOREWRITE
INITVAL_00 to _3F : 0xXX….X (80 hex characters)

Description:

Single Port RAM. See “Single Port RAM Port Definitions” on page 2.

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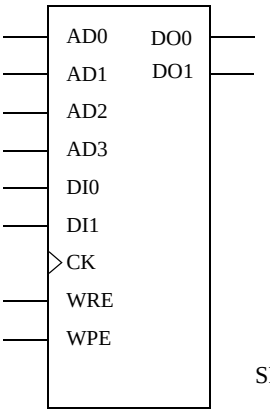
SPR16X2

16 Word by 2 Bit Positive Edge Triggered Write Synchronous Single Port RAM Memory with Positive Write Enable and Positive Write Port Enable (1-Slice)

Lattice FPGA		
SC	XP	EC
✓		



SPR16X2

INPUTS: AD0, AD1, AD2, AD3, DI0, DI1, CK, WRE, WPE
OUTPUTS: DO0, DO1
PINORDER: AD0, AD1, AD2, AD3, DI0, DI1, CK, WRE, WPE, DO0, DO1
MINIMUM CELL AREA: 1.0
ATTRIBUTES (Series 5-HSI only)
INITVAL: 0x0000000000000000
DISABLED_GSR : 0, 1

Description:

The SPR16X2 symbol represents a 16 word by 2 bit asynchronous single port RAM. It has two data inputs DI[1:0], a positive Write Enable (WRE), one positive Write Port Enables (WPE), and one set of address inputs.

The WRE and WPE must be HIGH for the rising clock edge if the write to the RAM is occurring on the falling edge. The data is written into the locations specified by the write address lines AD[3:0] on the next negative clock (CK) edge. The data read operation is always performed asynchronously, with the memory contents specified by the address inputs AD[3:0] output on the data output signals DO[1:0].

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In other words, the read operation is asynchronous and is always active. The write operation is synchronous and only occurs when there is a falling edge of the clock and the write enables are high prior to that falling edge.

If desired, the contents of the SPR16X2 can be assigned an initial value, which is loaded into the RAM during configuration. The INITVAL=<*value*> parameter is used to assign the initial value. The <*value*> should consist of 16 hexadecimal data written into the RAM from the highest address to the lowest address. For example, if the following attribute is specified:

`INITVAL=0x0123012301230123` (in hex)

it implies that the above data is loaded sequentially from location FH to 0H (where FH would contain the 0 and 0H the 3). If no INITVAL= parameter is specified, the RAM is initialized with zeros on configuration.

If the INITVAL is specified as a hex string of 16 values, the values should not be greater than 3, since 3 is setting both memory locations to 1. If a value greater than 3 is used for synthesis/mapping, only the last two (least significant) bits are used for initialization by the mapper. For example,

`INITVAL=0x00000000ffffffff`
is equivalent to
`INITVAL=0x0000000033333333`

for mapping purposes, since the first two bits of the “f” are ingnored.

See “Single Port RAM Port Definitions” on page 2.

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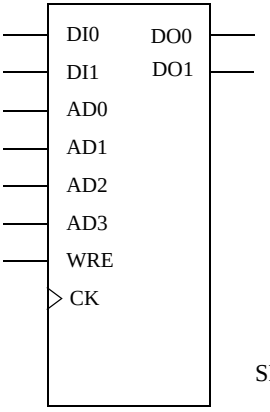
SPR16X2B

16 Word by 2 Bit Positive Edge Triggered Write Synchronous Single Port RAM Memory with Positive Write Enable and Positive Write Port Enable (1-Slice)

Lattice FPGA			
SC	XP	EC	MX
	✓	✓	✓



SPR16X2B

INPUTS: DI0, DI1, AD0, AD1, AD2, AD3, WRE, CK
OUTPUTS: DO0, DO1
PINORDER: DI0, DI1, AD0, AD1, AD2, AD3, WRE, CK, DO0, DO1
ATTRIBUTES
INITVAL: [63:0] 64'h0000000000000000

Description:

Refer to the SPR16X2 for functionality. See “Single Port RAM Port Definitions” on page 2.

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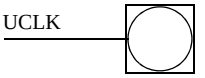
STRTUP

Startup Controller

ORCA Series/Lattice			
2	3	4	SC
✓	✓	✓	✓



STRTUP

INPUTS: UCLK
PINORDER: UCLK
MINIMUM CELL AREA (2A/2T): 0
MINIMUM CELL AREA (Series 3): 0

Description:

After configuration, the FPGA enters the start-up phase, which is the transition between the configuration and operational states. Normally, the relative timing of the following three events is triggered by the configuration clock (CCLK): DONE going high, release of the set/reset of internal FFs, and activation of user I/Os. The three events can also be triggered by a user clock, UCLK. This allows the start-up to be synchronized by a known system clock. For more detailed information refer to an available data book or contact technical support.

Another set of bitstream options for the STRTUP block allows the DONE pin to be held low and then released to be used with either CCLK or UCLK to control the release of the set/reset of internal FFs and the activation of user I/Os. This allows the synchronization of the start-up of multiple FPGAs.

UCLK: User defined clock to trigger DONE going high, release of set/reset of internal FFs, and activation of user I/Os.

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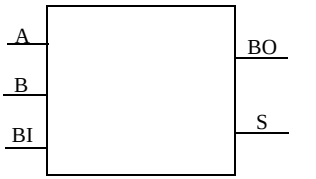
SUB

1 Bit Subtracter (two's complement)

ORCA Series		
2	3	4
✓		



SUB

INPUTS: A,B,BI
OUTPUTS: BO,S
PINORDER: A B BI BO S
MINIMUM CELL AREA: 0.5

Truth Table:

INPUTS			OUTPUTS	
A	B	BI	BO	S
0	0	0	0	1
1	0	0	1	0
0	1	0	0	0
1	1	0	0	1
0	0	1	1	0
1	0	1	1	1
0	1	1	0	1
1	1	1	1	0

Note: BI and BO are inverse from standard two's complement behavior.

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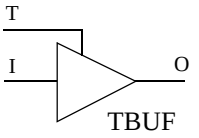
TBUF

Internal Buffer with Tristate

ORCA Series/Lattice FPGA						
2	3	4	SC	XP	EC	MX
✓	✓	✓	✓	✓	✓	✓



INPUTS: I,T
OUTPUTS: O
PINORDER: I T O
MINIMUM CELL AREA (2A/2T): 0.375
MINIMUM CELL AREA (Series 3): 0

Truth Table:

INPUTS		OUTPUTS
I	T	O
X	1	Z
0	0	0
1	0	1

X = Don’t care

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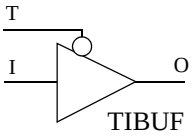
TIBUF

Internal Buffer with Inverted Tristate (used in SLIC area only, for Series 3)

ORCA Series		
2	3	4
✓	✓	✓



INPUTS: I,T
OUTPUTS: O
PINORDER: I T O
MINIMUM CELL AREA (2A/2T): 0.375
MINIMUM CELL AREA (Series 3): 0

Truth Table:

INPUTS		OUTPUTS
I	T	O
X	0	Z
0	1	0
1	1	1

X = Don’t care

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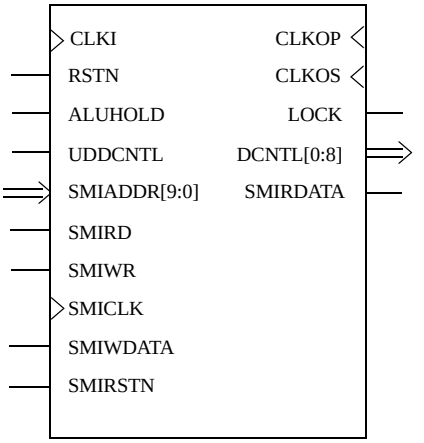
TRDLLA

Time Reference Delay

Lattice FPGA		
SC	XP	EC
✓		



TRDLLA

NOTE: The graphic is shown in bus notation for convenience. This element must be instantiated in expanded bus notation format with each individual bit as given below

INPUTS: CLKI, RSTN, ALUHOLD, UDDCNTL, SMIADDR9, SMIADDR8, SMIADDR7, SMIADDR6, SMIADDR5, SMIADDR4, SMIADDR3, SMIADDR2, SMIADDR1, SMIADDR0, SMIRD, SMIWR, SMICLK, SMIWDATA, SMIRSTN
OUTPUTS: CLKOP, CLKOS, LOCK, DCNTL0, DCNTL1, DCNTL2, DCNTL3, DCNTL4, DCNTL5, DCNTL6, DCNTL7, DCNTL8, SMIRDATA
PINORDER: CLKI, RSTN, ALUHOLD, UDDCNTL, SMIADDR9, SMIADDR8, SMIADDR7, SMIADDR6, SMIADDR5, SMIADDR4, SMIADDR3, SMIADDR2, SMIADDR1, SMIADDR0, SMIRD, SMIWR, SMICLK, SMIWDATA, SMIRSTN, CLKOP, CLKOS, LOCK, DCNTL0, DCNTL1, DCNTL2, DCNTL3, DCNTL4, DCNTL5, DCNTL6, DCNTL7, DCNTL8, SMIRDATA
CELL AREA: One Slice
ATTRIBUTES:
CLKI_PDEL: "DEL0", "DEL1", "DEL2", "DEL3"
CLKOP_PHASE: "0", "90", "180", "270", "360"
CLKOS_PHASE: "0", "90", "180", "270", "360"
CLKOS_FPHASE: "0", "11.25", "22.5", "45"
CLKOS_DIV: 1, 2, 4,
DISABLED_GSR: 0, 1
PHASELOCK: DISABLED, ENABLED
CLKOS_FDEL_ADJVAL: 0, 1, 2, ... 143
CLKOS_FPHASE_ADJVAL: -127, -126, ..., -1, 0, 1, ..., 126, 127
ALU_LOCK_CNT: 3, 4, ... 15
ALU_UNLOCK_CNT: 3, 4, ... 15

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GLITCH_TOLERANCE: 0, 1, ... 7
DCNTL_ADJ: -127, -126, ..., -1, 0, 1, ..., 126, 127
SMI_ID: 000000, 000001, ... 111111
ADDR_DIS: 0000000000, 0000000001, ... 1111111111

Description:

TRDLLA will generate four phases of the clock, 0, 90, 180, 270 degrees, along with the control setting used to generate these phases. This mode features registered control bit output with separate enable, addition and subtraction on the outgoing control bits, lock achieved starting from minimum delay which guarantees lock to first harmonic (fundamental frequency), and four available output phases (0, 90, 180, 270) degrees. This requires internal feedback only, a maximum frequency 700MHz, and a minimum frequency 100MHz.

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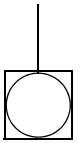
TSALL

Global Tristate Interface

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



TSALL

INPUTS: TSALL
PINORDER: TSALL
MINIMUM CELL AREA (2A/2T): 0
MINIMUM CELL AREA (Series 3): 0

Description:

TSALL is used to tristate buffers in your design. The TSALL component is connected to a net to drive all output and bidirectional buffers into a HIGH impedence state when active LOW.

It is not necessary to connect signals to buffers explictly. The function will be implictly connected globally.

Note: The TSALL component may be driven by general FPGA logic or by the read-configuration block. In the latter case, the TSALL block must be driven by a buffer located at the RDCGFN pin. When locating the TSALL to the RDCFGN, you must do this by explicitly designating “RDCFGN” in the attribute. In the ORCA 2002 release or prior, default pin numbers cannot be substituted for RDCFGN. The use of default pin numbers may be available in later releases. Check with customer support or with FAEs for more details.

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ULIM

System Bus User Logic Interface Master

ORCA Series		
2	3	4
		✓

INPUTS: ADDR0, ADDR1, ADDR2, ADDR3, ADDR4, ADDR5, ADDR6, ADDR7, ADDR8, ADDR9, ADDR10, ADDR11, ADDR12, ADDR13, ADDR14, ADDR15, ADDR16, ADDR17, WDATA0, WDATA1, WDATA2, WDATA3, WDATA4, WDATA5, WDATA6, WDATA7, WDATA8, WDATA9, WDATA10, WDATA11, WDATA12, WDATA13, WDATA14, WDATA15, WDATA16, WDATA17, WDATA18, WDATA19, WDATA20, WDATA21, WDATA22, WDATA23, WDATA24, WDATA25, WDATA26, WDATA27, WDATA28, WDATA29, WDATA30, WDATA31, WDATA32, WDATA33, WDATA34, WDATA35, CLK, RESET, WRITE, READ, BURST, RDY, SIZE0, SIZE1, LOCK, IRQ, SRDATA0, SRDATA1, SRDATA2, SRDATA3, SRDATA4, SRDATA5, SRDATA6, SRDATA7, SRDATA8, SRDATA9, SRDATA10, SRDATA11, SRDATA12, SRDATA13, SRDATA14, SRDATA15, SRDATA16, SRDATA17, SRDATA18, SRDATA19, SRDATA20, SRDATA21, SRDATA22, SRDATA23, SRDATA24, SRDATA25, SRDATA26, SRDATA27, SRDATA28, SRDATA29, SRDATA30, SRDATA31, SRDATA32, SRDATA33, SRDATA34, SRDATA35, SGRANTED, SACK, SRETRY, SERR

OUTPUTS: RDATA0, RDATA1, RDATA2, RDATA3, RDATA4, RDATA5, RDATA6, RDATA7, RDATA8, RDATA9, RDATA10, RDATA11, RDATA12, RDATA13, RDATA14, RDATA15, RDATA16, RDATA17, RDATA18, RDATA19, RDATA20, RDATA21, RDATA22, RDATA23, RDATA24, RDATA25, RDATA26, RDATA27, RDATA28, RDATA29, RDATA30, RDATA31, RDATA32, RDATA33, RDATA34, RDATA35, GRANTED, ACK, RETRY, ERR, SADDR0, SADDR1, SADDR2, SADDR3, SADDR4, SADDR5, SADDR6, SADDR7, SADDR8, SADDR9, SADDR10, SADDR11, SADDR12, SADDR13, SADDR14, SADDR15, SADDR16, SADDR17, SWDATA0, SWDATA1, SWDATA2, SWDATA3, SWDATA4, SWDATA5, SWDATA6, SWDATA7, SWDATA8, SWDATA9, SWDATA10, SWDATA11, SWDATA12, SWDATA13, SWDATA14, SWDATA15, SWDATA16, SWDATA17, SWDATA18, SWDATA19, SWDATA20, SWDATA21, SWDATA22, SWDATA23, SWDATA24, SWDATA25, SWDATA26, SWDATA27, SWDATA28, SWDATA29, SWDATA30, SWDATA31, SWDATA32, SWDATA33, SWDATA34, SWDATA35, SCLK, SRESET, SWRITE, SREAD, SBURST, SRDY, SSIZE0, SSIZE1, SLOCK, SIRQ

Note: The system bus user logic interface slave element should be instantiated using the Module/IP Manager. Refer to the appropriate topic in the online help system for details.

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ULIS

System Bus User Logic Interface Slave

ORCA Series		
2	3	4
		✓

INPUTS: RDATA0, RDATA1, RDATA2, RDATA3, RDATA4, RDATA5, RDATA6, RDATA7, RDATA8, RDATA9, RDATA10, RDATA11, RDATA12, RDATA13, RDATA14, RDATA15, RDATA16, RDATA17, RDATA18, RDATA19, RDATA20, RDATA21, RDATA22, RDATA23, RDATA24, RDATA25, RDATA26, RDATA27, RDATA28, RDATA29, RDATA30, RDATA31, RDATA32, RDATA33, RDATA34, RDATA35, CLK, RESET, ACK, RETRY, ERR, IRQ, SWDATA0, SWDATA1, SWDATA2, SWDATA3, SWDATA4, SWDATA5, SWDATA6, SWDATA7, SWDATA8, SWDATA9, SWDATA10, SWDATA11, SWDATA12, SWDATA13, SWDATA14, SWDATA15, SWDATA16, SWDATA17, SWDATA18, SWDATA19, SWDATA20, SWDATA21, SWDATA22, SWDATA23, SWDATA24, SWDATA25, SWDATA26, SWDATA27, SWDATA28, SWDATA29, SWDATA30, SWDATA31, SWDATA32, SWDATA33, SWDATA34, SWDATA35, SADDR0, SADDR1, SADDR2, SADDR3, SADDR4, SADDR5, SADDR6, SADDR7, SADDR8, SADDR9, SADDR10, SADDR11, SADDR12, SADDR13, SADDR14, SADDR15, SADDR16, SADDR17, SBURST, SRDY, SWR, SSIZE0, SSIZE1

OUTPUTS: WDATA0, WDATA1, WDATA2, WDATA3, WDATA4, WDATA5, WDATA6, WDATA7, WDATA8, WDATA9, WDATA10, WDATA11, WDATA12, WDATA13, WDATA14, WDATA15, WDATA16, WDATA17, WDATA18, WDATA19, WDATA20, WDATA21, WDATA22, WDATA23, WDATA24, WDATA25, WDATA26, WDATA27, WDATA28, WDATA29, WDATA30, WDATA31, WDATA32, WDATA33, WDATA34, WDATA35, ADDR0, ADDR1, ADDR2, ADDR3, ADDR4, ADDR5, ADDR6, ADDR7, ADDR8, ADDR9, ADDR10, ADDR11, ADDR12, ADDR13, ADDR14, ADDR15, ADDR16, ADDR17, BURST, RDY, WR, SIZE0, SIZE1, SRDATA0, SRDATA1, SRDATA2, SRDATA3, SRDATA4, SRDATA5, SRDATA6, SRDATA7, SRDATA8, SRDATA9, SRDATA10, SRDATA11, SRDATA12, SRDATA13, SRDATA14, SRDATA15, SRDATA16, SRDATA17, SRDATA18, SRDATA19, SRDATA20, SRDATA21, SRDATA22, SRDATA23, SRDATA24, SRDATA25, SRDATA26, SRDATA27, SRDATA28, SRDATA29, SRDATA30, SRDATA31, SRDATA32, SRDATA33, SRDATA34, SRDATA35, SCLK, SRESET, SACK, SRETRY, SERR, SIRQ

Note: The system bus user logic interface slave element should be instantiated using the Module/IP Manager. Refer to the appropriate topic in the online help system for details.

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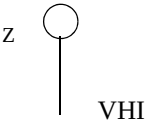
VHI

Logic High Generator

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



OUTPUTS: Z
PINORDER: Z
MINIMUM CELL AREA (2A/2T): 0.094
MINIMUM CELL AREA (Series 3): 0.047

Note: It is possible that this element will be optimized by the back-end tool before place and route.

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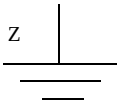
VLO

Logic Low Generator

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



VLO

OUTPUTS: Z
PINORDER: Z
MINIMUM CELL AREA (2A/2T): 0.094
MINIMUM CELL AREA (Series 3): 0.047

Note: It is possible that this element will be optimized by the back-end tool before place and route.

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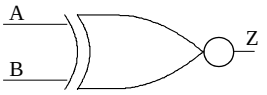
XNOR2

2-Input Exclusive NOR Gate

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



XNOR2

INPUTS: A,B
OUTPUTS: Z
PINORDER: A B Z
MINIMUM CELL AREA (2A/2T): 0.125
MINIMUM CELL AREA (Series 3): 0.031

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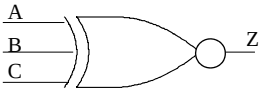
XNOR3

3-Input Exclusive NOR Gate

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



XNOR3

INPUTS: A,B,C
OUTPUTS: Z
PINORDER: A B C Z
MINIMUM CELL AREA (2A/2T): 0.125
MINIMUM CELL AREA (Series 3): 0.047

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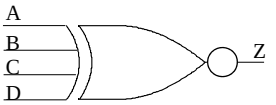
XNOR4

4-Input Exclusive NOR Gate

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



XNOR4

INPUTS: A,B,C,D
OUTPUTS: Z
PINORDER: A B C D Z
MINIMUM CELL AREA (2A/2T): 0.175
MINIMUM CELL AREA (Series 3): 0.0625

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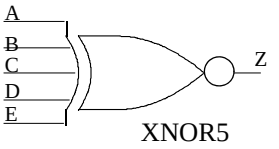
XNOR5

5-Input Exclusive NOR Gate

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



XNOR5

INPUTS: A,B,C,D,E
OUTPUTS: Z
PINORDER: A B C D E Z
MINIMUM CELL AREA (2A/2T): 0.25
MINIMUM CELL AREA (Series 3): 0.125

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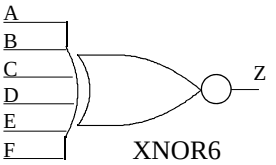
XNOR6

6-Input Exclusive NOR Gate

ORCA Series		
2	3	4
✓		



INPUTS: A,B,C,D,E,F
OUTPUTS: Z
PINORDER: A B C D E F Z
MINIMUM CELL AREA: 0.5

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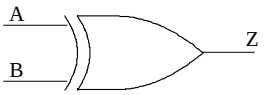
XOR2

2-Input Exclusive OR Gate

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



XOR2

INPUTS: A,B
OUTPUTS: Z
PINORDER: A B Z
MINIMUM CELL AREA (2A/2T): 0.125
MINIMUM CELL AREA (Series 3): 0.031

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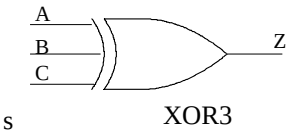
XOR3

3-Input Exclusive OR Gate

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



INPUTS: A,B,C
OUTPUTS: Z
PINORDER: A B C Z
MINIMUM CELL AREA (2A/2T): 0.125
MINIMUM CELL AREA (Series 3): 0.047

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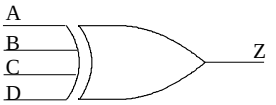
XOR4

4-Input Exclusive OR Gate

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



XOR4

INPUTS: A,B,C,D
OUTPUTS: Z
PINORDER: A B C D Z
MINIMUM CELL AREA (2A/2T): 0.175
MINIMUM CELL AREA (Series 3): 0.0625

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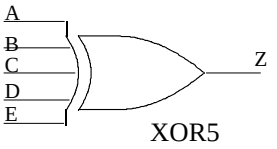
XOR5

5-Input Exclusive OR Gate

ORCA Series/Lattice FPGA					
2	3	4	SC	XP	EC
✓	✓	✓	✓	✓	✓



XOR5

INPUTS: A,B,C,D,E
OUTPUTS: Z
PINORDER: A B C D E Z
MINIMUM CELL AREA (2A/2T): 0.25
MINIMUM CELL AREA (Series 3): 0.125

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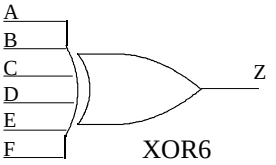
XOR6

6-Input Exclusive OR Gate

ORCA Series		
2	3	4
✓	✓	✓



INPUTS: A,B,C,D,E,F
OUTPUTS: Z
PINORDER: A B C D E F Z
MINIMUM CELL AREA: 0.5

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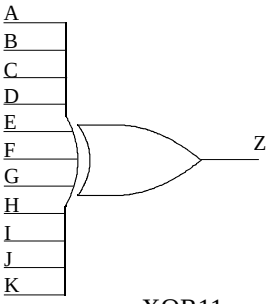
XOR11

11-Input Exclusive OR Gate

ORCA Series			
2	3	4	SC
	✓	✓	✓



XOR11

INPUTS: A,B,C,D,E,F,G,H,I,J,K
OUTPUTS: Z
PINORDER: A B C D E F G H I J K Z
MINIMUM CELL AREA: 0.5

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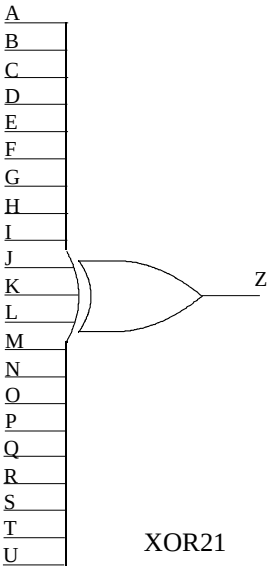
XOR21

21-Input Exclusive OR Gate

ORCA Series			
2	3	4	SC
	✓	✓	✓



XOR21

INPUTS: A,B,C,D,E,F,G,H,I,J,K,L,M,N,O,P,Q,R,S,T,U
OUTPUTS: Z
PINORDER: A B C D E F G H I J K L M N O P Q R S T U Z
MINIMUM CELL AREA: 1.0