Thermal Management

Technical Note

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
BBG	Wirebond BGA (0.8 mm Pitch)
BGA	Ball Grid Array
caBGA	Chip Array BGA
CERDIP	Ceramic Dual Inline Package
ckfBGA	Chip-Scale Flip-Chip BGA (7.00 mm × 7.00 mm)
CLPD	Complex Programmable Logic Device
csBGA	Chip-Scale BGA
CPGA	Ceramic Pin Grid Array
csfBGA	Chip-Scale Flip-Chip BGA
fcBGA	Flip Chip BGA
FOWLCSP	Fan Out Wafer Level Chip Scale Package
FPGA	Field-Programmable Gate Array
fpBGA	Fine Pitch BGA
fpSBGA	Fine Pitch SBGA
ftBGA	Thin BGA
GAL	Generic Array Logic
IPC	Association Connecting Electronics Industries
JEDEC	JEDEC Solid State Technology Association
JLCC	J-Lead Chip Carrier
LCC	Leadless Chip Carrier
MQFP	Metric Quad Flat Package
NSMD	Non-Solder Mask Defined
PBGA	Plastic BGA
PCB	Printed circuit board
PDIP	Plastic Dual In-Line Package
PLCC	Plastic Leaded Chip Carrier
PQFP	Plastic Quad Flat Pack
QFNS	Quad Flat Pack Saw-Singulated
SBGA	Super BGA
SMD	Solder Mask Defined
SSOP	Shrink Small Outline Package
TQFP	Thin Quad Flat Pack
ucBGA	Ultra Chip-Scale BGA
WLCSP	Wafer Level Chip Scale Package

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1. Introduction

Thermal Management is recommended as part of any sound Complex Programmable Logic Device (CPLD) and Field-Programmable Gate Array (FPGA) design methodology. To properly assess the thermal characteristics of the system, Lattice Semiconductor specifies a maximum allowable junction temperature in all device data sheets. The system designer should always complete a thermal analysis of the design to ensure that the device and package do not exceed the junction temperature requirements.

The data shown in this Thermal Management document is relative and actual values depend on a variety of factors such as: die size, paddle size, airflow, power applied, printed circuit board design, proximity of other devices and user applications. The Legacy Products Package Thermal Resistance section specifies the generic package thermal resistance for legacy Generic Array Logic (GAL), CPLD, FPGA and Expanded Programmable Logic Device (XPLD) devices. The tables in the Device/Package Thermal Resistance section specify the device/package specific thermal resistance for newer FPGA products. These values are based upon JEDEC standards. If specified, the device/package specific thermal value supersedes the generic package thermal data contained in the Legacy Products Package Thermal Resistance section.

In addition to the device and package, the thermal characteristics of a circuit depend on the operating temperature, device power consumption, and the ability of the system to dissipate heat. The maximum junction temperature of a device can be calculated using the equation below that corresponds to the type of thermal management utilized in the design. Equation 1.1 is for a simple system that dissipates heat directly from the device to the ambient air, as shown in Figure 1.1. Equation 1.2 is for a system that has a heat sink located on the top of the device, as shown in Figure 1.2. Finally, Equation 1.3 is used for a system that dissipates the device heat into the PCB, as shown in Figure 1.2.

$$T_J = T_A + Power * \theta_{JA} \quad \text{(Equation 1.1)}$$

or

$$T_J = T_A + Power * (\theta_{JC} + \theta_{CS} + \theta_{SA}) \quad \text{(Equation 1.2)}$$

or

$$T_J = T_A + Power * (\theta_{JB} + \theta_{BA}) \quad \text{(Equation 1.3)}$$

Where:

T_J	=	Junction Temperature of the device.
T_A	=	Ambient Temperature
θ_{BA}	=	Thermal resistance of PCB to ambient air; property of user board geometry.
θ_{CS}	=	Thermal resistance of thermal interface material between device case and heat sink; typically thermal pad, grease, or glue as shown in Figure 1.2.
θ_{SA}	=	Thermal resistance of heat sink to ambient air (specified in heat sink data sheet).
θ_{JA}	=	Junction-to-Ambient thermal resistance as shown in Figure 1.1 (see the Legacy Products Package Thermal Resistance and Device/Package Thermal Resistance sections.
θ_{JB}	=	Junction-to-Board Thermal Resistance as shown in Figure 1.2 (see the Legacy Products Package Thermal Resistance and Device/Package Thermal Resistance sections).
θ_{JC}	=	Junction-to-Case thermal resistance as shown in Figure 1.2 (see the Legacy Products Package Thermal Resistance and Device/Package Thermal Resistance sections).
Power	=	$I_{CC} * V_{CC}$ (Maximum values for maximum power)

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I_{CC} may be estimated as shown in the Power Consumption section of the DC and Switching Characteristics section of each individual device data sheet. The parameters in the I_{CC} equation may be found in the report file from the Lattice Diamond® compiler. For predicting power, the best resource is to use Lattice Diamond design tools. For additional information on power calculations and considerations, refer to the referenced technical note in the For Further Information section of each individual data sheet.

If the calculated T_J exceeds the maximum specified limits, refer to the following section on how to reduce the overall power dissipation and package temperature.

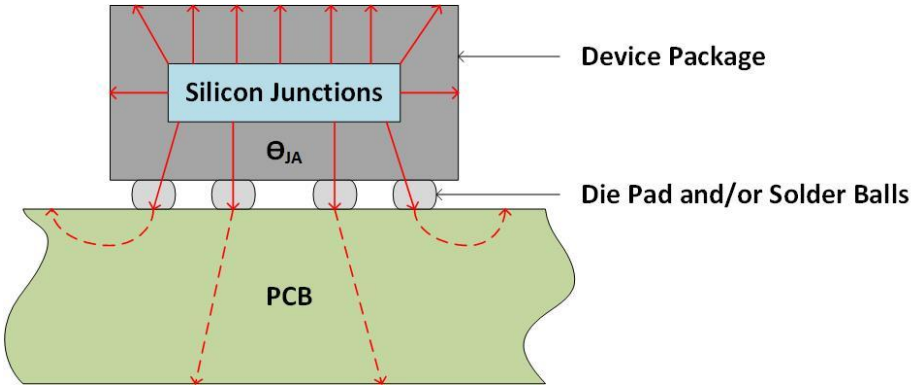

Figure 1.1. Thermal Resistance Path from Silicon Junctions to Ambient Air

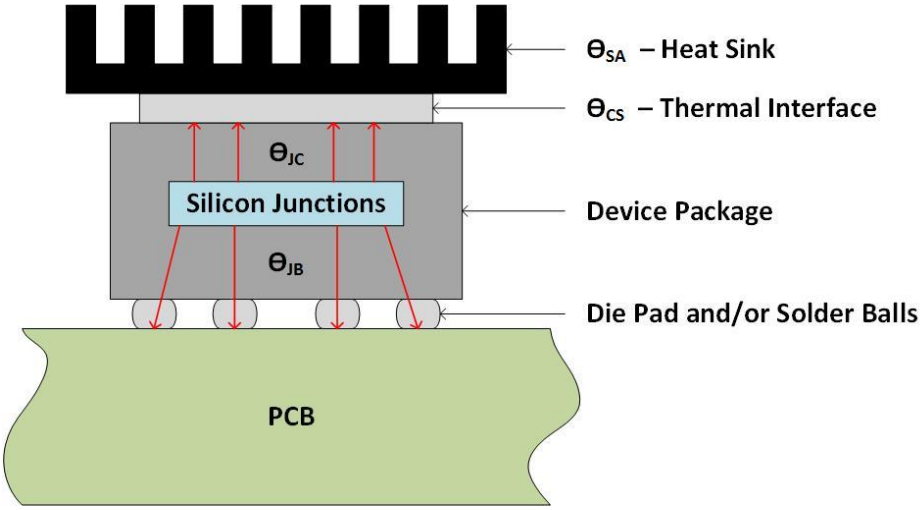

Figure 1.2. Thermal Resistance Path from Silicon Junctions to Package Top and to PCB

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2. Reducing Junction Temperature

The following are the ways to reduce junction temperature:

- Increase airflow in the system to reduce the case or ambient temperature.
- Reduce power in one of the following ways:
  - Reduce overall device utilization by combining common input functions. This is especially true when using wide input CPLD blocks. Even with the narrow FPGA logic blocks, careful partitioning of logic can reduce the overall net utilization.
  - Trade off net utilization with reducing the number of high frequency switching nets. By careful use of different encoding schemes, the high frequency switching nodes can be reduced. For example, using one-hot encoding can reduce the high frequency switching nodes compared to a binary encoding while increasing the logic utilization.
  - Reduce the frequency of operation. High-density architectures provide flexibility to control clock polarity to potentially reduce the overall clock speed.
- Where possible, make use of the output slew rate control to reduce the output switching current of the device.
- Make sure that programmable pull-ups are enabled to drive unused inputs to a proper logic level.
- Select an appropriate heat sink and thermal interface material for the package.

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3. Legacy Products Package Thermal Resistance

Table 3.1 is a general reference for all types of package thermal resistance. It is recommended for you to refer to Device/Package Thermal Resistance section for specific device package thermal resistance. This table specifies the generic package thermal resistance for legacy GAL, CPLD, FPGA and XPLD devices. These values are based upon JEDEC standards. If specified in the Device/Package Thermal Resistance section, the device/package specific thermal value supercedes the generic package thermal data contained in the tables.

Table 3.1. Package Thermal Resistance[1]

Package	Dimension	Pin Count	θ_{JA} (0lfm) °C/W	θ_{JA} (200lfm) °C/W	θ_{JC} °C/W
BBG	14 mm × 14 mm	256	39.9	36.0	20.7
	17 mm × 17 mm	400	32.5	28.6	16.4
	19 mm × 19 mm	484	24.4	21	9.4
caBGA	7 mm × 7 mm	49	74	68	15
	10 mm × 10 mm	100	48	39	12
	14 mm × 14 mm	256	40	35	10
CERDIP	—	20	62	52	10
	—	24	60	48	10
ckfBGA	7 mm × 7 mm	80	44.2	39.4	14.0
CPGA	—	84	38	21	3
	—	133	26	21	2
csBGA	5 mm × 5 mm	64	90	85	15
	6 mm × 6 mm	56	74	68	15
	7 mm × 7 mm	144	72	66	13
	8 mm × 8 mm	100	70	65	13
	8 mm × 8 mm	132	49	40	13
fpBGA	11 mm × 11 mm	100	40	32	11
	13 mm × 13 mm	144	29	25	11
	17 mm × 17 mm	208	24	20	10
	17 mm × 17 mm	256	20	16	10
	23 mm × 23 mm	388	18	15	6
	23 mm × 23 mm	484	18	15	6
	27 mm × 27 mm	416	17	14	5
	27 mm × 27 mm	672	16	13	5
	31 mm × 31 mm	516	14	12	4
	31 mm × 31 mm	676	14	12	4
	31 mm × 31 mm	900	14	12	4
	35 mm × 35 mm	680	14	12	3
	35 mm × 35 mm	1156	13	11	3
fpSBGA	40 mm × 40 mm	680	11	10	0.65
	45 mm × 45 mm	1036	10	9	0.65
ftBGA	17 mm × 17 mm	256	37	33	6
	19 mm × 19 mm	324	37	31	6
JLCC	—	44	69	38	4
	—	68	52	30	3
LCC	—	20	65	60	8
	—	28	62	49	7
LFG	—	672	20.2	16.6	5.5
	35 mm × 35 mm	1156	12.5	8.5	0.1

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Package	Dimension	Pin Count	θ_{JA} (0lfm) °C/W	θ_{JA} (200lfm) °C/W	θ_{JC} °C/W
PBGA	27 mm × 27 mm	272	20	17	6
	35 mm × 35 mm	388	16	13	3
	35 mm × 35 mm	492	16	13	3
PDIP	.300 wide	20	67	49	30
	.300 wide	24	64	35	25
	.300 wide	28	56	33	23
PLCC	—	20	64	58	22
	—	28	56	49	18
	—	44	35	31	16
	—	68	34	30	13
	—	84	33	29	12
PQFP/MQFP	14 mm × 20 mm	100	35	34	12
	28 mm × 28 mm	120	32	26	12
	28 mm × 28 mm	128	32	26	11
	28 mm × 28 mm	160	30	24	9
	28 mm × 28 mm	208	25	23	8
	32 mm × 32 mm	240	24	18	5
QFN	4 mm × 4 mm	24	42	32	16 (θ_{JB}) [2]
	5 mm × 5 mm	32	40	30	15 (θ_{JB}) [2]
	7 mm × 7 mm	48	39	29	15 (θ_{JB}) [2]
	9 mm × 9 mm	64	38	27	14 (θ_{JB}) [2]
SBGA	27 mm × 27 mm	256	15	12	0.65
	31 mm × 31 mm	320[3]	13	10	0.65
	35 mm × 35 mm	352	12	9	0.65
	40 mm × 40 mm	432[3]	11	8	0.65
	45 mm × 45 mm	600	10	7	0.65
SSOP	—	28	105	80	25
TQFP (1.0 mm thick)	7 mm × 7 mm	48	49	45	19
	10 mm × 10 mm	44	43	37	17
TQFP (1.4 mm thick)	10 mm × 10 mm	44	42	36	17
	7 mm × 7 mm	48	48	44	19
	14 mm × 14 mm	100	35	29	10
	14 mm × 14 mm	128	35	29	10
	20 mm × 20 mm	144	33	27	9
	24 mm × 24 mm	176	33	27	8
ucBGA	4 mm × 4 mm	64	77	70	20
	6 mm × 6 mm	132	61	53	16

Notes:

1. The data shown in this Thermal Management document is relative and actual values depend on a variety of factors such as die size, paddle size, airflow, power applied, printed circuit board design, proximity of other devices and user applications.
2. θ_{JB} (θ_{JB} = Junction-to-Board Thermal Resistance). θ_{JB} value shown is only applicable when the package thermal pad and/or solder balls are soldered directly onto user PCB (see Figure 1.2).
3. The 320-ball BGA and 432-ball BGA packages junction temperature must not exceed 140 °C.

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4. Device/Package Thermal Resistance

4.1. Avant™

Table 4.1. Avant Device/Package Thermal Resistance

Device	Package	Dimensions (mm)	Pin Count	θ_{JA} (0 lfm) °C/W	θ_{JA} (200 lfm) °C/W	θ_{JA} (500 lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
LAV-AT-E30	ASGA	11 mm × 9 mm	410	24.6	20.1	15.0	13.1	0.9
LAV-AT-E30	CBG	18 mm × 18 mm	484	20.70	16.50	15.20	9.70	1.00
LAV-AT-E70	CBG	18 mm × 18 mm	484	17.5	13.2	10.8	5.1	0.5
LAV-AT-E70	CSG	15 mm × 15 mm	841	18.7	14.4	12.0	3.8	2.3
LAV-AT-E/G/X70[1]	LFG	35 mm × 35 mm	1156	12.4	9.2	7.6	6.6	0.1
LAV-AT-E/G/X70	LFG	27mm × 27mm	676	16.2	13.1	11.1	9.8	0.9

Note:

1. LAV-AT-70 is formerly known as LAV-AT-500.

4.2. CrossLink™

Table 4.2. CrossLink Device/Package Thermal Resistance

Device	Package	Dimensions (mm)	Pin Count	θ_{JA} (0 lfm) °C/W	θ_{JA} (200 lfm) °C/W	θ_{JA} (500 lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
LIF-MD6000	WLCSP	2.46 mm × 2.46 mm	36	56.2	51.8	49.2	38.7	2.2
LIF-MD6000	ucfBGA	3.5 mm × 3.5 mm	64	53.2	47.4	44.6	40.9	23.0
LIF-MD6000	ctfBGA	6.5 mm × 6.5 mm	80	47.5	42.4	39.7	26.6	16.8
LIF-MD6000	ckfBGA	7 mm × 7 mm	80	44.2	39.4	36.8	33.7	14.0
LIF-MD6000	csfBGA	4.5 mm × 4.5 mm	81	49.3	43.4	40.7	30.3	18.9
LIA-MD6000	ctfBGA	6.5 mm × 6.5 mm	80	47.5	42.4	39.7	26.6	16.8
LIA-MD6000	ckfBGA	7 mm × 7 mm	80	44.2	39.4	36.8	33.7	14.0
LIA-MD6000	csfBGA	7 mm × 7 mm	81	49.3	43.4	40.7	30.3	18.9

4.3. CrossLinkPlus™

Table 4.3. CrossLinkPlus Device/Package Thermal Resistance

Device	Package	Dimensions (mm)	Pin Count	θ_{JA} (0 lfm) °C/W	θ_{JA} (200 lfm) °C/W	θ_{JA} (500 lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
LIF-MDF6000	ucfBGA	3.5 mm × 3.5 mm	64	54.6	48.5	45.6	38.4	16.8

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4.4. CrossLink™-NX

Table 4.4. CrossLink-NX Device/Package Thermal Resistance

Device	Package	Dimensions (mm)	Pin Count	θ_{JA} (0 lfm) °C/W	θ_{JA} (200 lfm) °C/W	θ_{JA} (500 lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
LIFCL-40	caBGA	17 mm × 17 mm	400	27.5	26.9	25.9	18.4	8.9
LIFCL-40	csBGA	9.5 mm × 9.5 mm	289	34.1	29.7	28.7	28.3	9.5
LIFCL-40	caBGA	14 mm × 14 mm	256	30.4	25.6	23.6	20.5	12.1
LIFCL-40	csfBGA	6 mm × 6 mm	121	33.2	28.5	26.1	18.4	14.9
LIFCL-40	QFN	10 mm × 10 mm	72	24.4	15.0	13.8	8.9	8.5
LIFCL-17	csfBGA	6 mm × 6 mm	121	35.4	30.6	28.2	20.5	15.6
LIFCL-17	WLCSP	3.8 mm × 4.1 mm	72	41.0	37.0	33.6	6.0	7.3
LIFCL-17	caBGA	14 mm × 14 mm	256	38.8	33.9	32.0	24.7	13.4
LIFCL-17	QFN	10 mm × 10 mm	72	25.1	15.7	14.5	9.6	9.3

4.5. CrossLink™-NX-33

Table 4.5. CrossLink-NX-33 Device/Package Thermal Resistance

Device	Package	Dimensions (mm)	Pin Count	θ_{JA} (0 lfm) °C/W	θ_{JA} (200 lfm) °C/W	θ_{JA} (500 lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
LIFCL-33	USG	7 mm × 3 mm	84	64.6	56.7	55.1	20.0	0.3

4.6. CrossLinkU™-NX

Table 4.6. CrossLinkU-NX Device/Package Thermal Resistance[1]

Device	Package	Dimensions (mm)	Pin Count	θ_{JA} (0 lfm) °C/W	θ_{JA} (200 lfm) °C/W	θ_{JA} (500 lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
LIFCL-33U	WLCSP	7 mm × 3 mm	84	51.7	46.4	42.0	19.9	0.3
LIFCL-33U	FCCSP	7 mm × 3 mm	104	50.1	44.9	41.2	34.1	6.0

Note:

1. Values are preliminary.

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4.7. Certus™-NX

Table 4.7. Certus-NX Device/Package Thermal Resistance

Device	Package	Dimensions (mm)	Pin Count	θ_{JA} (0 lfm) °C/W	θ_{JA} (200 lfm) °C/W	θ_{JA} (500 lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
LFD2NX-65	caBGA	19 mm × 19 mm	484	22.7	18.5	17.5	10.2	7.1
LFD2NX-40	caBGA	14 mm × 14 mm	256	30.4	25.6	23.6	20.5	12.1
LFD2NX-40	caBGA	12 mm × 12 mm	196	33.3	28.3	25.8	24.1	14.8
LFD2NX-40	csfBGA	6 mm × 6 mm	121	33.2	28.5	26.1	18.4	14.9
LFD2NX-35	caBGA	19 mm × 19 mm	484	22.7	18.5	17.5	10.2	7.1
LFD2NX-28	caBGA	14 mm × 14 mm	256	30.4	25.6	23.6	20.5	12.1
LFD2NX-28	caBGA	12 mm × 12 mm	196	33.3	28.3	25.8	24.1	14.8
LFD2NX-28	csfBGA	6 mm × 6 mm	121	33.2	28.5	26.1	18.4	14.9
LFD2NX-25	caBGA	17 mm × 17 mm	400	35.74	33.85	32.46	17.35	12.24
LFD2NX-15	caBGA	17 mm × 17 mm	400	35.74	33.85	32.46	17.35	12.24
LFD2NX-17	csfBGA	6 mm × 6 mm	121	35.4	30.6	28.2	20.5	15.6
LFD2NX-9	csfBGA	6 mm × 6 mm	121	35.4	30.6	28.2	20.5	15.6

4.8. CertusPro™-NX

Table 4.8. CertusPro-NX Device/Package Thermal Resistance

Device	Package	Dimensions (mm)	Pin Count	θ_{JA} (0 lfm) °C/W	θ_{JA} (200 lfm) °C/W	θ_{JA} (500 lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
LFCPNX	FOWLP	9 mm × 9 mm	256	29.1	24.5	22.7	18.2	10.2
LFCPNX	fcCSP	14 mm × 14 mm	256	22.5	21.1	20.1	14.9	10.2
LFCPNX	fpBGA	23 mm × 23 mm	484	19.7	15.2	14.3	9.9	6.3
LFCPNX	BBG	19 mm × 19 mm	484	24.4	21	19.2	12	9.4
LFCPNX	LFG	27 mm × 27 mm	672	20.2	16.6	15.5	11	5.5

4.9. LatticeECP™/LatticeEC™

Table 4.9. LatticeECP/LatticeEC Device/Package Thermal Resistance

Device	Package	Dimensions	Pin Count	θ_{JA} (0 lm) °C/W	θ_{JA} (200 lfm) °C/W	θ_{JA} (500 lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
LFEC1	TQFP	14 mm × 14 mm	100	36.9	33.0	30.4	23.6	12.4
LFEC1	TQFP	20 mm × 20 mm	144	28.8	26.1	24.0	19.1	9.4
LFEC1	PQFP	28 mm × 28 mm	208	40.2	37.0	34.2	30.5	18.5
LFEC3	TQFP	14 mm × 14 mm	100	36.9	33.0	30.4	23.6	12.4
LFEC3	TQFP	20 mm × 20 mm	144	28.8	26.1	24.0	19.1	9.4
LFEC3	PQFP	28 mm × 28 mm	208	30.2	27.8	25.7	22.9	13.9
LFEC3	fpBGA	17 mm × 17 mm	256	28.4	24.3	21.8	16.4	5.2
LFECP/EC6	TQFP	20 mm × 20 mm	144	27.8	25.0	23.1	17.8	7.2
LFECP/EC6	PQFP	28 mm × 28 mm	208	30.2	27.8	25.7	22.9	13.9
LFECP/EC6	fpBGA	17 mm × 17 mm	256	25.9	22.0	19.5	14.2	4.0
LFECP/EC6	fpBGA	23 mm × 23 mm	484	19.6	16.9	15.3	11.3	6.5
LFECP/EC10	PQFP	28 mm × 28 mm	208	30.2	27.8	25.7	22.9	13.9

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Device	Package	Dimensions	Pin Count	θ_{JA} (0 lm) °C/W	θ_{JA} (200 lfm) °C/W	θ_{JA} (500 lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
LFECP/EC10	fpBGA	17 mm × 17 mm	256	24.0	20.1	17.7	12.4	3.1
LFECP/EC10	fpBGA	23 mm × 23 mm	484	18.0	15.4	13.7	9.3	5.0
LFECP/EC15	fpBGA	17 mm × 17 mm	256	22.7	18.9	16.5	11.3	2.6
LFECP/EC15	fpBGA	23 mm × 23 mm	484	17.1	14.6	12.8	8.4	4.2
LFECP/EC20	fpBGA	23 mm × 23 mm	484	16.6	14.0	12.2	7.8	3.8
LFECP/EC20	fpBGA	27 mm × 27 mm	672	15.2	12.8	11.0	7.0	3.2
LFECP/EC33	fpBGA	23 mm × 23 mm	484	15.8	13.1	11.3	7.1	3.1
LFECP/EC33	fpBGA	27 mm × 27 mm	672	14.0	11.8	10.1	6.9	2.6

4.10. LatticeECP2™

Table 4.10. LatticeECP2 Device/Package Thermal Resistance

Device	Package	Dimensions	Pin Count	θ_{JA} (0 lfm) °C/W	θ_{JA} (200 lfm) °C/W	θ_{JA} (500 lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
LFE2-6E	TQFP	20 mm × 20 mm	144	28.8	26.1	24.0	19.1	9.4
LFE2-6E	fpBGA	17 mm × 17 mm	256	29.1	25.0	22.5	17.1	5.7
LFE2-12E	TQFP	20 mm × 20 mm	144	28.8	26.1	24.0	19.1	9.4
LFE2-12E	PQFP	28 mm × 28 mm	208	30.2	27.8	25.7	22.9	13.9
LFE2-12E	fpBGA	17 mm × 17 mm	256	26.7	22.7	20.2	14.9	4.3
LFE2-12E	fpBGA	23 mm × 23 mm	484	20.0	17.4	15.8	11.7	7.0
LFE2-20E	PQFP	28 mm × 28 mm	208	30.2	27.8	25.7	22.9	13.9
LFE2-20E	fpBGA	17 mm × 17 mm	256	24.9	21.0	18.5	13.2	3.5
LFE2-20E	fpBGA	23 mm × 23 mm	484	18.7	16.1	14.4	10.1	5.6
LFE2-20E	fpBGA	27 mm × 27 mm	672	17.4	15.1	13.0	10.2	4.8
LFE2-35E	fpBGA	23 mm × 23 mm	484	17.7	15.2	13.4	9.0	4.7
LFE2-35E	fpBGA	27 mm × 27 mm	672	16.4	14.0	12.1	8.5	4.0
LFE2-50E	fpBGA	23 mm × 23 mm	484	16.7	14.2	12.3	7.9	3.9
LFE2-50E	fpBGA	27 mm × 27 mm	672	15.3	13.0	11.2	7.2	3.3
LFE2-70E	fpBGA	27 mm × 27 mm	672	14.3	12.0	10.3	6.0	2.7
LFE2-70E	fpBGA	31 mm × 31 mm	900	12.6	10.5	9.2	6.3	2.0

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4.11. LatticeECP2M™

Table 4.11. LatticeECP2M Device/Package Thermal Resistance

Device	Package	Dimensions	Pin Count	θ_{JA} (0 lfm) °C/W	θ_{JA} (200 lfm) °C/W	θ_{JA} (500 lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
LFE2M20E	fpBGA	17 mm × 17 mm	256	24.2	20.2	17.8	12.6	3.2
LFE2M20E	fpBGA	23 mm × 23 mm	484	18.1	15.6	13.8	9.5	5.1
LFE2M35E	fpBGA	17 mm × 17 mm	256	22.4	18.5	16.2	11.0	2.5
LFE2M35E	fpBGA	23 mm × 23 mm	484	16.8	14.3	12.5	8.1	4.0
LFE2M35E	fpBGA	27 mm × 27 mm	672	15.5	13.0	11.1	5.9	3.1
LFE2M50E	fpBGA	23 mm × 23 mm	484	15.6	13.1	11.3	6.9	3.1
LFE2M50E	fpBGA	27 mm × 27 mm	672	14.2	11.9	10.2	5.9	2.6
LFE2M50E	fpBGA	31 mm × 31 mm	900	12.5	10.4	9.1	6.1	1.9
LFE2M70E	fpBGA	31 mm × 31 mm	900	11.7	9.5	8.1	5.3	1.5
LFE2M70E	fpBGA	35 mm × 35 mm	1152	13.7	12.0	11.0	6.5	2.0
LFE2M100E	fpBGA	31 mm × 31 mm	900	10.8	8.6	7.1	4.5	1.2
LFE2M100E	fpBGA	35 mm × 35 mm	1152	13.2	11.2	9.8	5.7	1.5

4.12. LatticeECP3™

Table 4.12. LatticeECP3 Device/Package Thermal Resistance

Device	Package	Dimensions	Pin Count	θ_{JA} (0 lfm) °C/W	θ_{JA} (200 lfm) °C/W	θ_{JA} (500 lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
LFE3-17	ftBGA	17 mm × 17 mm	256	24.5	20.6	18.2	12.9	3.3
LFE3-17	csBGA	10 mm × 10 mm	328	30.8	27.8	25.5	12.5	6.1
LFE3-17	fpBGA	23 mm × 23 mm	484	18.4	15.8	14.1	9.8	5.4
LFE3-35	ftBGA	17 mm × 17 mm	256	24.5	20.6	18.2	12.9	3.3
LFE3-35	fpBGA	23 mm × 23 mm	484	18.4	15.8	14.1	9.8	5.4
LFE3-35	fpBGA	27 mm × 27 mm	672	17.1	14.7	12.7	9.5	4.5
LFE3-70	fpBGA	23 mm × 23 mm	484	15.7	13.2	11.4	7	3.2
LFE3-70	fpBGA	27 mm × 27 mm	672	14.3	12	10.3	6	2.7
LFE3-70	fpBGA	35 mm × 35 mm	1156	12.9	11.5	10.6	7.3	2.3
LFE3-95	fpBGA	23 mm × 23 mm	484	15.7	13.2	11.4	7	3.2
LFE3-95	fpBGA	27 mm × 27 mm	672	14.3	12	10.3	6	2.7
LFE3-95	fpBGA	35 mm × 35 mm	1156	12.9	11.5	10.6	7.3	2.3
LFE3-150	fpBGA	27 mm × 27 mm	672	13.2	10.9	9.3	4.8	2.1
LFE3-150	fpBGA	35 mm × 35 mm	1156	12.2	10.5	9.2	6	1.6

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4.13. LatticeSC™/LatticeSCM™

Table 4.13. LatticeSC/LatticeSCM Device/Package Thermal Resistance

Device	Package	Dimensions	Pin Count	θ_{JA} (0 lfm) °C/W	θ_{JA} (200 lfm) °C/W	θ_{JA} (500 lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
LFSC/SCM15	fpBGA	17 mm × 17 mm	256	21.1	17.4	15.1	10.0	2.1
LFSC/SCM15	fpBGA	31 mm × 31 mm	900	12.9	10.8	9.6	6.6	2.1
LFSC/SCM25	fpBGA	31 mm × 31 mm	900	11.5	9.3	7.9	5.1	1.5
LFSC/SCM25	FFBGA	33 mm × 33 mm	1020	10.1	8.1	6.7	5.1	1.1
LFSC/SCM40	FFBGA	33 mm × 33 mm	1020	10.1	8.1	6.7	3.7	0.4
LFSC/SCM40	fcBGA	35 mm × 35 mm	1152	9.5	6.8	5.1	2.7	0.6
LFSC/SCM80	fcBGA	35 mm × 35 mm	1152	7.9	5.7	4.2	2.2	0.5
LFSC/SCM80	fcBGA	42.5 mm × 42.5 mm	1704	7.7	5.5	4.0	3.0	0.5
LFSC/SCM115	fcBGA	35 mm × 35 mm	1152	7.9	5.7	4.2	2.2	0.5
LFSC/SCM115	fcBGA	42.5 mm × 42.5 mm	1704	7.7	5.5	4.0	3.0	0.5

4.14. ECP5™

Table 4.14. ECP5 Device/Package Thermal Resistance

Device	Package	Dimensions	Pin Count	θ_{JA} (0 lfm) °C/W	θ_{JA} (200 lfm) °C/W	θ_{JA} (500 lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
LFE5U-12F	csfBGA	10 mm × 10 mm	285	33.1	26.8	24.3	20.7	12.5
LFE5U-12F	caBGA	17 mm × 17 mm	381	21.5	15.8	13.9	11.7	6.8
LAE5U-12F	caBGA	17 mm × 17 mm	381	21.5	15.8	13.9	11.7	6.8
LFE5U-25F	csfBGA	10 mm × 10 mm	285	33.1	26.8	24.3	20.7	12.5
LFE5U-25F	caBGA	14 mm × 14 mm	256	35.1	31.1	29.2	24.0	13.8
LFE5U-25F	caBGA	17 mm × 17 mm	381	21.5	15.8	13.9	11.7	6.8
LFE5UM-25F	csfBGA	10 mm × 10 mm	285	33.1	26.8	24.3	20.7	12.5
LFE5UM-25F	caBGA	17 mm × 17 mm	381	21.5	15.8	13.9	11.7	6.8
LAE5UM-25F	caBGA	17 mm × 17 mm	381	21.5	15.8	13.9	11.7	6.8
LFE5UM-45F	csfBGA	10 mm × 10 mm	285	29.6	23.2	20.8	17.2	9.6
LFE5UM-45F	caBGA	17 mm × 17 mm	381	20.5	14.6	12.8	10.6	5.7
LAE5UM-45F	caBGA	17 mm × 17 mm	381	20.5	14.6	12.8	10.6	5.7
LFE5UM-45F	caBGA	23 mm × 23 mm	554	20.3	15.1	13.4	9.3	2.9
LFE5U-45F	csfBGA	10 mm × 10 mm	285	29.6	23.2	20.8	17.2	9.6
LFE5U-45F	caBGA	14 mm × 14 mm	256	30.7	24.6	22.9	17.9	9.1
LFE5U-45F	caBGA	17 mm × 17 mm	381	20.5	14.6	12.8	10.6	5.7
LFE5U-45F	caBGA	23 mm × 23 mm	554	20.3	15.1	13.4	9.3	2.9
LFE5U-85F	csfBGA	10 mm × 10 mm	285	26.2	21.9	19.8	12.5	6.7
LFE5U-85F	caBGA	17 mm × 17 mm	381	19.0	13.5	11.7	9.4	4.1
LFE5U-85F	caBGA	23 mm × 23 mm	554	18.6	13.3	11.6	8.3	3.8
LFE5U-85F	caBGA	27 mm × 27 mm	756	17.1	11.8	10.2	8.1	2.1
LFE5UM-85F	csfBGA	10 mm × 10 mm	285	26.2	21.9	19.8	12.5	6.7
LFE5UM-85F	caBGA	17 mm × 17 mm	381	19.0	13.5	11.7	9.4	4.1
LFE5UM-85F	caBGA	23 mm × 23 mm	554	18.6	13.3	11.6	8.3	3.8
LFE5UM-85F	caBGA	27 mm × 27 mm	756	17.1	11.8	10.2	8.1	2.1

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4.15. ECP5-5G™

Table 4.15. ECP5-5G Device/Package Thermal Resistance

Device	Package	Dimensions	Pin Count	θ_{JA} (0 lfm) °C/W	θ_{JA} (200 lfm) °C/W	θ_{JA} (500 lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
LFE5UM5G-25F	csfBGA	10 mm × 10 mm	285	33.1	26.8	24.3	20.7	12.5
LFE5UM5G-25F	caBGA	17 mm × 17 mm	381	21.5	15.8	13.9	11.7	6.8
LFE5UM5G-45F	csfBGA	10 mm × 10 mm	285	29.6	23.2	20.8	17.2	9.6
LFE5UM5G-45F	caBGA	17 mm × 17 mm	381	20.5	14.6	12.8	10.6	5.7
LFE5UM5G-45F	caBGA	23 mm × 23 mm	554	20.3	15.1	13.4	9.3	2.9
LFE5UM5G-85F	csfBGA	10 mm × 10 mm	285	26.2	21.9	19.8	12.5	6.7
LFE5UM5G-85F	caBGA	17 mm × 17 mm	381	19.0	13.5	11.7	9.4	4.1
LFE5UM5G-85F	caBGA	23 mm × 23 mm	554	18.6	13.3	11.6	8.3	3.8
LFE5UM5G-85F	caBGA	27 mm × 27 mm	756	17.1	11.8	10.2	8.1	2.1

4.16. iCE40™ LP/HX/LM

Table 4.16. iCE40 LP/HX/LM Device/Package Thermal Resistance

Device	Package	Dimensions	Pin Count	θ_{JA} (0 lfm) °C/W	θ_{JA} (200 lfm) °C/W	θ_{JA} (500 lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
iCE40-LP384	QFN	5 mm × 5 mm	32	67.75	64.2	62.3	29.9	18.2
iCE40-LP384	ucBGA	2.5 mm × 2.5 mm	36	138.1	128.1	123.2	57.2	35.7
iCE40-LP384	ucBGA	3 mm × 3 mm	49	121.0	110.9	106.4	53.7	33.5
iCE40-LP640	WLCSP	1.40 mm × 1.48 mm	16	72.3	66.9	64.8	30.0	3.0
iCE40-LP1K	ucBGA	2.5 mm × 2.5 mm	36	119.3	109.7	105.2	51.9	32.5
iCE40-LP1K	ucBGA	3 mm × 3 mm	49	108.5	100.3	96.5	44.0	27.5
iCE40-LP1K	ucBGA	4 mm × 4 mm	81	83.9	72.6	69.9	33.6	24.6
iCE40-LP1K	csBGA	5 mm × 5 mm	81	72.7	60.1	56.3	32.5	20.3
iCE40-LP1K	QFN	7 mm × 7 mm	84	46.7	43.9	42.4	15.6	14.3
iCE40-LP1K	ucBGA	5 mm × 5 mm	121	79.6	74.3	71.9	45.2	22.0
iCE40-LP1K	csBGA	6 mm × 6 mm	121	70.6	64.7	60.7	61.6	18.0
iCE40-LP1K	WLCSP	1.48 mm × 1.40 mm	16	72.3	66.9	64.8	30.0	3.0
iCE40-LM1K	WLCSP	1.71 mm × 1.71 mm	25	57.8	52.6	50.9	29.0	4.4
iCE40-LM1K	ucBGA	2.5 mm × 2.5 mm	36	116.5	110.5	105.9	41.1	39.0
iCE40-LM1K	ucBGA	3 mm × 3 mm	49	104.5	98.9	94.7	33.9	27.2
iCE40-HX1K	TQFP	14 mm × 14 mm	100	44.2	40.4	37.8	26.7	14.2
iCE40-HX1K	csBGA	8 mm × 8 mm	132	67.7	61.2	59.2	55.5	27.3
iCE40-HX1K	TQFP	20 mm × 20 mm	144	38.5	35.4	33.3	19.8	10.0
iCE40-LM2K	WLCSP	1.71 mm × 1.71 mm	25	57.8	52.6	50.9	29.0	4.4
iCE40-LM2K	ucBGA	2.5 mm × 2.5 mm	36	116.5	110.5	105.9	41.1	39.0
iCE40-LM2K	ucBGA	3 mm × 3 mm	49	104.5	98.9	94.7	33.9	27.2
iCE40-LP4K	ucBGA	4 mm × 4 mm	81	77.0	64.3	60.6	32.8	20.5
iCE40-LP4K	ucBGA	5 mm × 5 mm	121	70.7	63.1	59.8	31.6	19.7
iCE40-LP4K	ucBGA	7 mm × 7 mm	225	66.7	61.1	57.4	58.0	16.9
iCE40-HX4K	caBGA	9 mm × 9 mm	121	53.4	49.3	46.8	31.0	20.8
iCE40-HX4K	csBGA	8 mm × 8 mm	132	60.2	55.2	51.8	52.3	15.3
iCE40-HX4K	TQFP	20 mm × 20 mm	144	38.3	35.2	33.1	19.7	9.9

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Device	Package	Dimensions	Pin Count	θ_{JA} (0 lfm) °C/W	θ_{JA} (200 lfm) °C/W	θ_{JA} (500 lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
iCE40-LM4K	WLCSP	1.71 mm × 1.71 mm	25	57.8	52.6	50.9	29.0	4.4
iCE40-LM4K	ucBGA	2.5 mm × 2.5 mm	36	116.5	110.5	105.9	41.1	39.0
iCE40-LM4K	ucBGA	3 mm × 3 mm	49	104.5	98.9	94.7	33.9	27.2
iCE40-LP8K	ucBGA	4 mm × 4 mm	81	77.0	64.3	60.6	32.8	20.5
iCE40-LP8K	ucBGA	5 mm × 5 mm	121	60.9	52.7	48.3	27.8	17.4
iCE40-LP8K	ucBGA	7 mm × 7 mm	225	55.1	49.3	47.3	46.5	16.5
iCE40-HX8K	caBGA	9 mm × 9 mm	121	53.4	49.3	46.8	31.0	20.8
iCE40-HX8K	csBGA	8 mm × 8 mm	132	54.3	50.1	47.4	42.8	12.5
iCE40-HX8K	ucBGA	7 mm × 7 mm	225	55.1	49.3	47.3	46.5	16.5
iCE40-HX8K	caBGA	14 mm × 14 mm	256	42.8	38.3	36.4	39.5	11.6

4.17. iCE40 Ultra™

Table 4.17. iCE40 Ultra Device/Package Thermal Resistance

Device	Package	Dimensions	Pin Count	θ_{JA} (0 lfm) °C/W	θ_{JA} (200 lfm) °C/W	θ_{JA} (500 lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
iCE5LP1K	WLCSP	2.078 mm × 2.078 mm	36	68.2	63.1	60.4	18.4	3.3
iCE5LP1K	UCFBGA	2.5 mm × 2.5 mm	36	117.9	105.1	100.2	42.9	24.3
iCE5LP1K	QFN	7 mm × 7 mm	48	37.1	33.0	30.7	11.5	14.3
iCE5LP2K	WLCSP	2.078 mm × 2.078 mm	36	68.2	63.1	60.4	18.4	3.3
iCE5LP2K	UCFBGA	2.5 mm × 2.5 mm	36	117.9	105.1	100.2	42.9	24.3
iCE5LP2K	QFN	7 mm × 7 mm	48	37.1	33.0	30.7	11.5	14.3
iCE5LP4K	WLCSP	2.078 mm × 2.078 mm	36	68.2	63.1	60.4	18.4	3.3
iCE5LP4K	UCFBGA	2.5 mm × 2.5 mm	36	117.9	105.1	100.2	42.9	24.3
iCE5LP4K	QFN	7 mm × 7 mm	48	37.1	33.0	30.7	11.5	14.3

4.18. iCE40 UltraLite™

Table 4.18. iCE40 UltraLite Device/Package Thermal Resistance

Device	Package	Dimensions	Pin Count	θ_{JA} (0 lfm) °C/W	θ_{JA} (200 lfm) °C/W	θ_{JA} (500 lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
iCE40UL640	WLCSP	1.409 mm × 1.409 mm	16	93.1	86.7	83.7	29.7	6.7
iCE40UL640	ucBGA	2.5 mm × 2.5 mm	36	125.3	119.0	113.7	59.8	40.6
iCE40UL1K	WLCSP	1.409 mm × 1.409 mm	16	93.1	86.7	83.7	29.7	6.7
iCE40UL1K	ucBGA	2.5 mm × 2.5 mm	36	125.3	119.0	113.7	59.8	40.6

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4.19. iCE40 UltraPlus™

Table 4.19. iCE40 UltraPlus Device/Package Thermal Resistance

Device	Package	Dimensions	Pin Count	θ_{JA} (0 lfm) °C/W	θ_{JA} (200 lfm) °C/W	θ_{JA} (500 lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
iCE40UP3K	WLCSP	2.15 mm × 2.55 mm	30	65.25	60.57	57.75	20.57	2.03
iCE40UP3K	QFN	7 mm × 7 mm	48	37.1	33	30.7	11.5	14.3
iCE40UP5K	WLCSP	2.15 mm × 2.55 mm	30	65.25	60.57	57.75	20.57	2.03
iCE40UP5K	QFN	7 mm × 7 mm	48	37.1	33	30.7	11.5	14.3

4.20. Mach™-NX

Table 4.20. Mach-NX Device/Package Thermal Resistance

Device	Package	Dimensions	Pin Count	θ_{JA} (0 lfm) °C/W	θ_{JA} (200 lfm) °C/W	θ_{JA} (500 lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
LFMNX-50	fcBGA	19 mm × 19 mm	484	23.3	12.1	10.4	17.5	0.7

4.21. MachXO™

Table 4.21. MachXO Device/Package Thermal Resistance

Device	Package	Dimensions	Pin Count	θ_{JA} (0 lfm) °C/W	θ_{JA} (200 lfm) °C/W	θ_{JA} (500 lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
LCMXO256C/E	csBGA	8 mm × 8 mm	100	85.4	79.4	74.4	62.8	31.9
LCMXO256C/E	TQFP	14 mm × 14 mm	100	36.9	33.0	30.4	23.6	12.4
LCMXO640C/E	csBGA	8 mm × 8 mm	100	75.1	69.5	65.9	57.5	18.5
LCMXO640C/E	TQFP	14 mm × 14 mm	100	36.9	33.0	30.4	23.6	12.4
LCMXO640C/E	csBGA	8 mm × 8 mm	132	67.6	62.3	58.5	50.4	16.7
LCMXO640C/E	TQFP	20 mm × 20 mm	144	28.8	26.1	24.0	19.1	9.4
LCMXO640C/E	caBGA	14 mm × 14 mm	256	47.8	43.8	41.1	46.1	15.1
LCMXO640C/E	ftBGA	17 mm × 17 mm	256	44.9	40.3	37.8	39.0	11.4
LCMXO1200C/E	TQFP	14 mm × 14 mm	100	36.9	33.0	30.4	23.6	12.4
LCMXO1200C/E	csBGA	8 mm × 8 mm	132	55.7	51.0	48.0	37.1	9.7
LCMXO1200C/E	TQFP	20 mm × 20 mm	144	28.8	26.1	24.0	19.1	9.4
LCMXO1200C/E	caBGA	14 mm × 14 mm	256	43.1	39.1	36.5	35.8	9.5
LCMXO1200C/E	ftBGA	17 mm × 17 mm	256	41.8	36.9	34.3	33.2	7.7
LCMXO2280C/E	TQFP	14 mm × 14 mm	100	36.9	33.0	30.4	23.6	12.4
LCMXO2280C/E	csBGA	8 mm × 8 mm	132	48.4	44.1	41.6	33.7	6.6
LCMXO2280C/E	TQFP	20 mm × 20 mm	144	28.8	26.1	24.0	19.1	9.4
LCMXO2280C/E	caBGA	14 mm × 14 mm	256	40.9	34.9	32.3	32.5	6.5
LCMXO2280C/E	ftBGA	17 mm × 17 mm	256	40.0	34.9	32.3	28.7	5.1
LCMXO2280C/E	ftBGA	19 mm × 19 mm	324	37.3	31.2	29.5	25.0	6.2

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4.22. MachXO2™

Table 4.22. MachXO2 Device/Package Thermal Resistance

Device	Package	Dimensions	Pin Count	θ_{JA} (0 lfm) °C/W	θ_{JA} (200 lfm) °C/W	θ_{JA} (500 lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
LCMXO2-256	QFN	5 mm × 5 mm	32	41.3	37.3	35.1	22.2	20.4
LCMXO2-256	QFN	7 mm × 7 mm	48	36.8	31.1	28.9	20.2	16.6
LCMXO2-256	ucBGA	4 mm × 4 mm	64	71.6	59.2	55.5	32.0	20.0
LCMXO2-256	TQFP	14 mm × 14 mm	100	40.8	35.5	33.3	23.6	12.4
LCMXO2-256	csBGA	8 mm × 8 mm	132	90.3	82.8	79.4	62.8	31.9
LCMXO2-640	QFN	7 mm × 7 mm	48	36	30.2	28.1	17.1	15.9
LCMXO2-640	TQFP	14 mm × 14 mm	100	36.9	33.0	30.4	23.6	12.4
LCMXO2-640	csBGA	8 mm × 8 mm	132	79.8	72.3	68.9	62.8	31.9
LCMXO2-640U	TQFP	20 mm × 20 mm	144	34.1	29.7	27.7	19.1	9.4
LCMXO2-1200	WLCSP	2.5 mm × 2.5 mm	25	42.4	36.8	33.5	30.5	5.8
LCMXO2-1200	QFN	5 mm × 5 mm	32	39.9	36.4	34.5	32.5	17.7
LCMXO2-1200	TQFP	14 mm × 14 mm	100	36.9	33.0	30.4	23.6	12.4
LCMXO2-1200	csBGA	8 mm × 8 mm	132	69.8	62.3	59.1	62.8	31.9
LCMXO2-1200	TQFP	20 mm × 20 mm	144	34.1	29.7	27.7	19.1	9.4
LCMXO2-1200U	ftBGA	17 mm × 17 mm	256	43.3	38.6	36.1	36.1	9.5
LCMXO2-2000	WLCSP	3.2 mm × 3.2 mm	49	31.4	27.6	25.5	24.5	4.8
LCMXO2-2000	TQFP	14 mm × 14 mm	100	36.9	33.0	30.4	23.6	12.4
LCMXO2-2000	csBGA	8 mm × 8 mm	132	60.7	55.8	52.5	57.5	18.5
LCMXO2-2000	TQFP	20 mm × 20 mm	144	28.8	26.1	24.0	19.1	9.4
LCMXO2-2000	ftBGA	17 mm × 17 mm	256	43.3	38.6	36.1	36.1	9.5
LCMXO2-2000	CABGA	14 mm × 14 mm	256	47.7	43.7	41.0	46.1	15.1
LCMXO2-2000U	fpBGA	23 mm × 23 mm	484	25.2	21.5	19.5	19.9	10.3
LCMXO2-4000	QFN	7 mm × 7 mm	84	37.9	33.8	31.6	22.8	14.0
LCMXO2-4000	csBGA	8 mm × 8 mm	132	52.8	48.3	45.5	37.1	9.7
LCMXO2-4000	csBGA	8 mm × 8 mm	184	40.0	34.7	32.4	13.7	9.8
LCMXO2-4000	TQFP	20 mm × 20 mm	144	28.8	26.1	24.0	19.1	9.4
LCMXO2-4000	ftBGA	17 mm × 17 mm	256	40.9	36.0	33.4	25.1	4.4
LCMXO2-4000	caBGA	14 mm × 14 mm	256	42.6	38.7	36.0	32.5	6.5
LCMXO2-4000	caBGA	17 mm × 17 mm	332	35.1	31.3	29.1	30.4	6.6
LCMXO2-4000	fpBGA	23 mm × 23 mm	484	25.2	21.5	19.5	19.9	10.3
LCMXO2-7000	TQFP	20 mm × 20 mm	144	28.8	26.1	24.0	19.1	9.4
LCMXO2-7000	ftBGA	17 mm × 17 mm	256	38.7	33.8	31.0	28.4	4.4
LCMXO2-7000	caBGA	14 mm × 14 mm	256	40.3	36.3	33.6	30.1	6.1
LCMXO2-7000	caBGA	17 mm × 17 mm	332	33.3	29.5	27.3	26.9	5.5
LCMXO2-7000	fpBGA	23 mm × 23 mm	484	23.4	19.8	17.8	18.6	7.5

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4.23. MachXO3™

Table 4.23. MachXO3 Device/Package Thermal Resistance

Device	Package	Dimensions	Pin Count	θ_{JA} (0 lfm) °C/W	θ_{JA} (200 lfm) °C/W	θ_{JA} (500 lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
LCMXO3L-640E	csfBGA	6 mm × 6 mm	121	52.4	49.5	46.8	35.4	18.3
LAMXO3LF-640E/C	TQFP	14 mm × 14 mm	100	36.9	33.0	30.4	23.6	12.4
LAMXO3LF-640E/C	csBGA	8 mm × 8 mm	132	79.8	72.3	68.9	62.8	31.9
LCMXO3LF-640E/C	TQFP	14 mm × 14 mm	100	36.9	33.0	30.4	23.6	12.4
LCMXO3LF-640E/C	csBGA	8 mm × 8 mm	132	79.8	72.3	68.9	62.8	31.9
LCMXO3L-1300E	WLCSP	2.487 mm × 2.541 mm	36	41.7	36.3	33.0	30.2	5.8
LCMXO3L-1300E	csfBGA	6 mm × 6 mm	121	52.4	49.5	46.8	35.4	18.3
LCMXO3L-1300E	csfBGA	9 mm × 9 mm	256	36.2	33.8	31.5	23.8	11.6
LCMXO3L-1300C	caBGA	14 mm × 14 mm	256	47.0	43.0	40.3	44.1	13.9
LAMXO3LF-1300E/C	TQFP	14 mm × 14 mm	100	36.9	33.0	30.4	23.6	12.4
LAMXO3LF-1300E/C	csBGA	8 mm × 8 mm	132	69.8	62.3	59.1	62.8	31.9
LCMXO3LF-1300E/C	TQFP	14 mm × 14 mm	100	36.9	33.0	30.4	23.6	12.4
LCMXO3LF-1300E/C	csBGA	8 mm × 8 mm	132	69.8	62.3	59.1	62.8	31.9
LCMXO3L-2100E	WLCSP	3.106 mm × 3.185 mm	49	31.4	27.6	25.5	24.5	4.8
LCMXO3L-2100E	csfBGA	6 mm × 6 mm	121	45.1	40.4	37.7	28.2	13.7
LCMXO3L-2100E	csfBGA	9 mm × 9 mm	256	36.2	33.8	31.5	23.8	11.6
LCMXO3L-2100E	csfBGA	10 mm × 10 mm	324	31.2	28.7	26.6	19.3	8.7
LCMXO3L-2100C	caBGA	14 mm × 14 mm	256	47.0	43.0	40.3	44.1	13.9
LCMXO3L-2100C	caBGA	15 mm × 15 mm	324	34.8	31.0	28.8	29.9	6.4
LAMXO3LF-2100C/E	TQFP	14 mm × 14 mm	100	36.9	33.0	30.4	23.6	12.4
LAMXO3LF-2100C/E	csBGA	8 mm × 8 mm	132	60.7	55.8	52.5	57.5	18.5
LCMXO3LF-2100C/E	TQFP	14 mm × 14 mm	100	36.9	33.0	30.4	23.6	12.4
LCMXO3LF-2100C/E	csBGA	8 mm × 8 mm	132	60.7	55.8	52.5	57.5	18.5
LCMXO3L-4300E	WLCSP	3.797 mm × 3.693 mm	81	21.6	19.4	18.3	19.1	3.8
LCMXO3L-4300E	csfBGA	6 mm × 6 mm	121	39.1	34.9	32.1	22.0	10.3
LCMXO3L-4300E	csfBGA	9 mm × 9 mm	256	33.2	30.9	28.5	20.9	9.5
LCMXO3L-4300E	csfBGA	10 mm × 10 mm	324	31.2	28.7	26.6	19.3	8.7
LCMXO3L-4300C	caBGA	14 mm × 14 mm	256	42.2	38.3	35.6	32.1	6.4
LCMXO3L-4300C	caBGA	15 mm × 15 mm	324	34.8	31.0	28.8	29.9	6.4
LCMXO3L-4300C	caBGA	17 mm × 17 mm	400	33.0	29.2	27.0	26.3	5.3
LAMXO3LF-4300C/E	csBGA	8 mm × 8 mm	132	52.8	48.3	45.5	37.1	9.7
LAMXO3LF-4300C/E	csBGA	8 mm × 8 mm	132	52.8	48.3	45.5	37.1	9.7

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Device	Package	Dimensions	Pin Count	θ_{JA} (0 lfm) °C/W	θ_{JA} (200 lfm) °C/W	θ_{JA} (500 lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
LCMXO3L-6900E	csfBGA	9 mm × 9 mm	256	30.5	28.0	25.7	18.1	7.7
LCMXO3L-6900E	csfBGA	9 mm × 9 mm	256	30.5	28.0	25.7	18.1	7.7
LCMXO3L-6900E	csfBGA	10 mm × 10 mm	324	29.1	26.7	24.4	17.1	7.3
LCMXO3L-6900C	caBGA	14 mm × 14 mm	256	39.9	35.9	33.2	29.7	6.0
LCMXO3L-6900C	caBGA	15 mm × 15 mm	324	33.1	29.5	27.4	29.8	6.0
LCMXO3L-6900C	caBGA	17 mm × 17 mm	400	33.0	29.2	27.0	26.3	5.3
LCMXO3L-9400E	csfBGA	9 mm × 9 mm	256	29.3	25.3	23.1	15.8	5.7
LCMXO3L-9400C	caBGA	14 mm × 14 mm	256	30.6	26.6	24.7	18.9	10.5
LCMXO3L-9400C	caBGA	17 mm × 17 mm	400	29.7	26.0	24.1	19.2	8.9
LCMXO3L-9400C	caBGA	19 mm × 19 mm	484	28.1	25.2	23.7	17.2	7.0
LCMXO3L-9400E	caBGA	14 mm × 14 mm	256	30.6	26.6	24.7	18.9	10.5
LCMXO3L-9400E	caBGA	17 mm × 17 mm	400	29.7	26.0	24.1	19.2	8.9
LCMXO3L-9400E	caBGA	19 mm × 19 mm	484	28.1	25.2	23.7	17.2	7.0

Note: XO3L and XO3LF use physically the same die size. All thermal data for the XO3L also applies to the XO3LF.

4.24. MachXO3D™

Table 4.24. MachXO3D Device/Package Thermal Resistance

Device	Package	Dimensions	Pin Count	θ_{JA} (0 lfm) °C/W	θ_{JA} (200 lfm) °C/W	θ_{JA} (500 lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
LCMXO3D-4300	QFN	10 mm × 10 mm	72	18.1	15.4	14.2	8.5	7.8
LCMXO3D-4300	caBGA	14 mm × 14 mm	256	30.7	26.4	24.5	19.7	9.3
LCMXO3D-4300	ftBGA	17 mm × 17 mm	256	26.1	22.5	20.3	17.9	4.9
LCMXO3D-9400	QFN	10 mm × 10 mm	72	17.7	14.0	12.9	8.2	7.3
LCMXO3D-9400	caBGA	19 mm × 19 mm	484	24.7	20.9	19.1	15.3	6.2
LCMXO3D-9400	caBGA	17 mm × 17 mm	400	25.3	21.7	19.9	15.8	6.5
LCMXO3D-9400	caBGA	14 mm × 14 mm	256	26.3	22.5	20.6	15.8	6.8
LCMXO3D-9400	WLCSP	5.192 mm × 6.218 mm	69	30.2	27.9	24.8	11.3	5.7

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4.25. MachXO4™

Table 4.25. MachXO4 Device/Package Thermal Resistance

Device	Package	Dimensions	Pin Count	θ_{JA} (0 lfm) °C/W	θ_{JA} (200 lfm) °C/W	θ_{JA} (500 lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
LFMXO4-010	TQFP	14 mm × 14 mm	100	35.5	33.5	31.6	25.5	13.6
LFMXO4-010	csBGA	8 mm × 8 mm	132	69.8	62.3	59.1	62.8	31.9
LFMXO4-010	TQFP	20 mm × 20 mm	144	34.1	29.7	27.7	19.1	9.4
LFMXO4-015	WLCSP	2.5 mm × 2.5 mm	36	41.7	36.3	33	30.2	5.8
LFMXO4-015	TQFP	14 mm × 14 mm	100	35.5	33.5	31.6	25.5	13.6
LFMXO4-015	csBGA	8 mm × 8 mm	132	69.8	62.3	59.1	62.8	31.9
LFMXO4-015	TQFP	20 mm × 20 mm	144	34.1	29.7	27.7	19.1	9.4
LFMXO4-015	caBGA	14 mm × 14 mm	256	47.7	43.7	41.0	46.1	15.1
LFMXO4-015	ftBGA	17 mm × 17 mm	256	43.3	38.6	36.1	36.1	9.5
LFMXO4-025	WLCSP	3.2 mm × 3.2 mm	49	31.4	27.6	25.5	24.5	4.8
LFMXO4-025	TQFP	14 mm × 14 mm	100	40.5	33.3	30.1	32.1	12.0
LFMXO4-025	csBGA	8 mm × 8 mm	132	60.7	55.8	52.5	57.5	18.5
LFMXO4-025	TQFP	20 mm × 20 mm	144	28.8	26.1	24	19.1	9.4
LFMXO4-025	caBGA	14 mm × 14 mm	256	47	43	40.3	44.1	13.9
LFMXO4-025	ftBGA	17 mm × 17 mm	256	43.3	38.6	36.1	36.1	9.5
LFMXO4-050	WLCSP	3.8 mm × 3.8 mm	81	21.6	19.4	18.3	19.1	3.8
LFMXO4-050	csBGA	8 mm × 8 mm	132	60.7	55.8	52.5	57.5	18.5
LFMXO4-050	TQFP	20 mm × 20 mm	144	28.8	26.1	24	19.1	9.4
LFMXO4-050	caBGA	14 mm × 14 mm	256	42.2	38.3	35.6	32.1	6.4
LFMXO4-050	caBGA	17 mm × 17 mm	400	33	29.2	27	26.3	5.3
LFMXO4-050	ftBGA	17 mm × 17 mm	256	25.0	20.5	18.2	13.6	6.8
LFMXO4-080	caBGA	14 mm × 14 mm	256	39.9	35.9	33.2	29.7	6
LFMXO4-080	caBGA	17 mm × 17 mm	400	33	29.2	27	26.3	5.3
LFMXO4-110	caBGA	14 mm × 14 mm	256	26.3	22.5	20.6	15.8	6.8
LFMXO4-110	caBGA	17 mm × 17 mm	400	25.3	21.7	19.9	15.8	6.5
LFMXO4-110	caBGA	19 mm × 19 mm	484	24.7	20.9	19.1	15.3	6.2
LFMXO4D-40	caBGA	14 mm × 14 mm	256	42.2	38.3	35.6	32.1	6.4
LFMXO4D-40	ftBGA	17 mm × 17 mm	256	25.0	20.5	18.2	13.6	6.8
LFMXO4D-50	caBGA	14 mm × 14 mm	256	42.2	38.3	35.6	32.1	6.4
LFMXO4D-50	ftBGA	17 mm × 17 mm	256	25.0	20.5	18.2	13.6	6.8
LFMXO4D-80	WLCSP	5.2 mm × 6.2 mm	69	30.2	27.9	24.8	11.3	5.7
LFMXO4D-80	caBGA	14 mm × 14 mm	256	26.3	22.5	20.6	15.8	6.8
LFMXO4D-80	caBGA	17 mm × 17 mm	400	25.3	21.7	19.9	15.8	6.5
LFMXO4D-110	WLCSP	5.2 mm × 6.2 mm	69	30.2	27.9	24.8	11.3	5.7
LFMXO4D-110	caBGA	14 mm × 14 mm	256	26.3	22.5	20.6	15.8	6.8
LFMXO4D-110	caBGA	17 mm × 17 mm	400	25.3	21.7	19.9	15.8	6.5
LFMXO4D-110	caBGA	19 mm × 19 mm	484	24.7	20.9	19.1	15.3	6.2

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4.26. MachXO5™-NX

Table 4.26. MachXO5-NX Device/Package Thermal Resistance

Device	Package	Dimensions	Pin Count	θ_{JA} (0 lfm) °C/W	θ_{JA} (200 lfm) °C/W	θ_{JA} (500 lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
LFMXO5-15D	caBGA	14 mm × 14mm	256	39.9	38.7	35.5	22.8	15.9
LFMXO5-15D	caBGA	17 mm × 17mm	400	35.7	33.9	32.5	17.4	12.2
LFMXO5-25	caBGA	14 mm × 14mm	256	39.9	38.7	35.5	22.8	15.9
LFMXO5-25	caBGA	17 mm × 17mm	400	35.7	33.9	32.5	17.4	12.2
LFMXO5-55T	caBGA	17 mm × 17mm	400	38.2	35.8	33.9	17.9	13.9
LFMXO5-55TD	caBGA	17 mm × 17mm	400	38.2	35.8	33.9	17.9	13.9
LFMXO5-55TDQ	caBGA	14 mm × 14mm	256	28.8	24.2	23.1	14.6	11.9
LFMXO5-55TDQ	caBGA	17 mm × 17mm	400	38.2	35.8	33.9	17.9	13.9
LFMXO5-65TDQ	caBGA	17 mm × 17mm	400	38.2	35.8	33.9	17.9	13.9
LFMXO5-100T	caBGA	17 mm × 17mm	400	38.2	35.8	33.9	17.9	13.9
LFMXO5-35/T	caBGA	14 mm × 14mm	256	23.1	19.1	17.8	9.0	6.5
LFMXO5-65/T	caBGA	14 mm × 14mm	256	23.1	19.1	17.8	9.0	6.5
LFMXO5-35/T	caBGA	17 mm × 17mm	400	22.4	18.4	17.1	6.1	10.1
LFMXO5-65/T	caBGA	17 mm × 17mm	400	22.4	18.4	17.1	6.1	10.1
LFMXO5-35/T	caBGA	19 mm × 19mm	484	22.7	18.5	17.5	10.2	7.1
LFMXO5-65/T	caBGA	19 mm × 19mm	484	22.7	18.5	17.5	10.2	7.1

4.27. Lattice Nexus™ 2

Table 4.27. Lattice Nexus 2 Device/Package Thermal Resistance

Device	Package	Dimensions	Pin Count	θ_{JA} (0 lfm) °C/W	θ_{JA} (200 lfm) °C/W	θ_{JA} (500 lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
LN2-CT16E	FOWLP	11 mm × 9 mm	410	23.8	19.9	16.9	13.1	9.4
LN2-CT16	FOWLP	11 mm × 9 mm	410	23.8	19.9	16.9	13.1	9.4
LN2-CT16	FCCSP	18 mm × 18 mm	484	21.1	17.0	15.7	9.6	3.1
LN2-CT16	FCBGA	27 mm × 27 mm	676	18.1	13.8	12.4	9.9	1.0
LN2-CT20E	FOWLP	11 mm × 9 mm	410	23.8	19.9	16.9	13.1	9.4
LN2-CT20	FOWLP	11 mm × 9 mm	410	23.8	19.9	16.9	13.1	9.4
LN2-CT20	FCCSP	18 mm × 18 mm	484	21.1	17.0	15.7	9.6	3.1
LN2-CT20	FCBGA	27 mm × 27 mm	676	18.1	13.8	12.4	9.9	1.0
LN2-MH16	FCCSP	18 mm × 18 mm	484	21.1	17.0	15.7	9.6	3.1
LN2-MH20	FCCSP	18 mm × 18 mm	484	21.1	17.0	15.7	9.6	3.1

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4.28. LatticeXP™

Table 4.28. LatticeXP Device/Package Thermal Resistance

Device	Package	Dimensions	Pin Count	θ_{JA} (0 lfm) °C/W	θ_{JA} (200 lfm) °C/W	θ_{JA} (500 lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
LFXP3C/E	TQFP	14 mm × 14 mm	100	31.0	27.1	24.6	16.9	8.1
LFXP3C/E	TQFP	20 mm × 20 mm	144	28.8	26.1	24.0	19.1	9.4
LFXP3C/E	PQFP	28 mm × 28 mm	208	29.5	27.0	24.7	21.5	13.2
LFXP6C/E	TQFP	20 mm × 20 mm	144	27.8	25.0	23.1	17.8	7.2
LFXP6C/E	PQFP	28 mm × 28 mm	208	30.2	27.8	25.7	22.9	13.9
LFXP6C/E	fpBGA	17 mm × 17 mm	256	25.7	21.6	19.4	14.1	5.3
LFXP10C/E	fpBGA	17 mm × 17 mm	256	23.4	19.5	17.2	11.9	2.9
LFXP10C/E	fpBGA	23 mm × 23 mm	388	17.6	15.0	13.2	8.9	4.6
LFXP15C/E	fpBGA	17 mm × 17 mm	256	21.6	18.1	15.6	11.6	1.5
LFXP15C/E	fpBGA	23 mm × 23 mm	388	16.1	13.5	11.9	7.6	3.8
LFXP15C/E	fpBGA	23 mm × 23 mm	484	16.3	14.0	12.0	7.3	3.7
LFXP20C/E	fpBGA	17 mm × 17 mm	256	21.9	17.8	15.6	9.6	2.8
LFXP20C/E	fpBGA	23 mm × 23 mm	388	16.2	13.7	11.8	7.4	3.5
LFXP20C/E	fpBGA	23 mm × 23 mm	484	16.2	13.7	11.8	7.4	3.5

4.29. LatticeXP2™

Table 4.29. LatticeXP2 Device/Package Thermal Resistance

Device	Package	Dimensions	Pin Count	θ_{JA} (0 lfm) °C/W	θ_{JA} (200 lfm) °C/W	θ_{JA} (500 lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
LFXP2-5E	csBGA	8 mm × 8 mm	132	47.2	43.0	40.5	32.7	6.1
LFXP2-5E	TQFP	20 mm × 20 mm	144	28.8	26.1	24.0	19.1	9.4
LFXP2-5E	PQFP	28 mm × 28 mm	208	30.2	27.8	25.7	22.9	13.9
LFXP2-5E	ftBGA	17 mm × 17 mm	256	39.1	34.1	31.4	29.4	6.1
LFXP2-8E	csBGA	8 mm × 8 mm	132	41.9	38.0	35.8	28.4	4.4
LFXP2-8E	TQFP	20 mm × 20 mm	144	28.8	26.1	24.0	19.1	9.4
LFXP2-8E	PQFP	28 mm × 28 mm	208	30.2	27.8	25.7	22.9	13.9
LFXP2-8E	ftBGA	17 mm × 17 mm	256	37.2	32.3	29.5	27.0	5.1
LFXP2-17E	PQFP	28 mm × 28 mm	208	30.2	27.8	25.7	22.9	13.9
LFXP2-17E	ftBGA	17 mm × 17 mm	256	33.9	29.1	26.2	23.7	4.3
LFXP2-17E	fpBGA	23 mm × 23 mm	484	18.6	16.0	14.3	10.0	5.5
LFXP2-30E	ftBGA	17 mm × 17 mm	256	32.0	27.1	24.2	20.7	3.0
LFXP2-30E	fpBGA	23 mm × 23 mm	484	17.3	14.8	13.0	8.6	4.4
LFXP2-30E	fpBGA	27 mm × 27 mm	672	16.0	13.6	11.7	7.9	3.7
LFXP2-40E	fpBGA	23 mm × 23 mm	484	16.5	14.0	12.1	7.7	3.7
LFXP2-40E	fpBGA	27 mm × 27 mm	672	15.1	12.7	10.9	6.8	3.1

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4.30. L-ASC10™

Table 4.30. L-ASC10 Device/Package Thermal Resistance

Device	Package	Dimensions	Pin Count	θ_{JA} (0 lfm) °C/W	θ_{JA} (200 lfm) °C/W	θ_{JA} (500 lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
L-ASC10	QFN	7 mm × 7 mm	48	35.33	31.19	28.95	11.15	12.98

4.31. Platform Manager™

Table 4.31. Platform Manager Device/Package Thermal Resistance

Device	Package	Dimensions	Pin Count	θ_{JA} (0 lfm) °C/W	θ_{JA} (200 lfm) °C/W	θ_{JA} (500 lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
LPTM10-1247	TQFP	14 mm × 14 mm	128	33.7	29.5	27.0	17.7	15.5
LPTM10-12107	ftBGA	17 mm × 17 mm	208	37.7	34.3	31.8	24.2	18.3

4.32. Platform Manager 2

Table 4.32. Platform Manager 2 Device/Package Thermal Resistance

Device	Package	Dimensions	Pin Count	θ_{JA} (0 lfm) °C/W	θ_{JA} (200 lfm) °C/W	θ_{JA} (500 lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
LPTM21	ftBGA	17 mm × 17 mm	237	36	33.1	30.2	24.7	15.5
LPTM21L	caBGA	10 mm × 10 mm	100	48.9	45.1	41.9	38.8	19.5

Note: The data shown in this Thermal Management document is relative and actual values depend on a variety of factors such as: die size, paddle size, airflow, power applied, printed circuit board design, proximity of other devices and user applications. This table specifies the device/package specific thermal resistance for newer FPGA products. These values are based upon JEDEC standards.

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Revision History

Revision 6.1, September 2026

Section	Change Summary
Device/Package Thermal Resistance	• Updated Table 4.25. MachXO4 Device/Package Thermal Resistance to add packages for LFMXO4D. • Updated Table 4.27. Lattice Nexus 2 Device/Package Thermal Resistance to add packages for LN2-CT16/E, LN2-CT20E, LN2-20 (FCBGA), LN2-MH16, and LN2-MH20 and updated dimension for LN2-CT20 FCCSP.

Revision 6.0, August 2026

Section	Change Summary
Device/Package Thermal Resistance	Updated Table 4.26. MachXO5-NX Device/Package Thermal Resistance to add BBG400 package for LFMXO5-65TDQ.

Revision 5.9, June 2026

Section	Change Summary
Device/Package Thermal Resistance	Updated Table 4.26. MachXO5-NX Device/Package Thermal Resistance to add CBG256 package for LFMXO5-55TDQ.

Revision 5.8, December 2025

Section	Change Summary
All	Made editorial fixes across the document.
Device/Package Thermal Resistance	Added MachXO4 section.

Revision 5.7, October 2025

Section	Change Summary
Legacy Products Package Thermal Resistance	Updated section content to change section name from Package Thermal Resistance to Legacy Products Package Thermal Resistance and move this text from the table note to the section description: *This table specifies the generic package thermal resistance for legacy GAL, CPLD, FPGA and XPLD devices. These values are based upon JEDEC standards. If specified in the Device/Package Thermal Resistance section, the device/package specific thermal value supercedes the generic package thermal data contained in the tables.*
Device/Package Thermal Resistance	Added LFMXO5-55TDQ device package in Table 4.25. MachXO5-NX Device/Package Thermal Resistance.

Revision 5.6, July 2025

Section	Change Summary
Device/Package Thermal Resistance	• Updated Table 4.1. Avant Device/Package Thermal Resistance to add ASGA410 and CBG484 packages for LAV-AT-E30, CBG484 and CSG841 packages for LAV-AT-E70, and update package name from FBGA to LFG. • Updated Table 4.7. Certus-NX Device/Package Thermal Resistance to add LFD2NX-15, LFD2NX-25, LFD2NX-35, and LFD2NX-65 device packages. • Updated Table 4.25. MachXO5-NX Device/Package Thermal Resistance to add • LFMXO5-35/T and LFMXO5-65/T device packages and update package name from BBG to *caBGA*.

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Revision 5.5, February 2025

Section	Change Summary
Device/Package Thermal Resistance	Updated 676 values in Table 4.1. Avant Device/Package Thermal Resistance.

Revision 5.4, December 2024

Section	Change Summary
Device/Package Thermal Resistance	• Updated Table 4.23. MachXO3D Device/Package Thermal Resistance to add LCMXO3D-4300 ftBGA package. • Added Lattice Nexus 2 section.

Revision 5.3, December 2024

Section	Change Summary
Device/Package Thermal Resistance	Updated θ_{JC} value for LAV-AT-E/G/X70 (1156 pin count) in Table 4.1. Avant Device/Package Thermal Resistance.

Revision 5.2, August 2024

Section	Change Summary
Device/Package Thermal Resistance	Updated Table 4.22. MachXO3 Device/Package Thermal Resistance to add LAMXO3LF-640/1300/2100/4300 device packages.

Revision 5.1, July 2024

Section	Change Summary
Device/Package Thermal Resistance	Updated Table 4.7. Certus-NX Device/Package Thermal Resistance to add LFD2NX-28 and LFD2NX-9 device packages.

Revision 5.0, June 2024

Section	Change Summary
Device/Package Thermal Resistance	Updated Table 4.25. MachXO5-NX Device/Package Thermal Resistance to add LFMXO5-15D and LFMXO5-55TD.

Revision 4.9, March 2024

Section	Change Summary
Package Thermal Resistance	This statement is added in the introduction to Section 3, "*The table below is a general reference for all types of package thermal resistance. It is recommended for you to refer to Section 4 for specific device package thermal resistance*."

Revision 4.8, December 2023

Section	Change Summary
Device/Package Thermal Resistance	• Updated Table 4.1. Avant Device/Package Thermal Resistance for Avant E/G/X. • Added the 676 package in Table 4.1 for Avant E/G/X.

Revision 4.7, October 2023

Section	Change Summary
Device/Package Thermal Resistance	• Updated the Theta values of Table 4.25. MachXO5-NX Device/Package Thermal Resistance. • Updated the Avant device name from LAV-AT-500 to LAV-AT-70 in Table 4.1. Avant Device/Package Thermal Resistance.
All	Changed product name from *CrossLink-NX-33U* to *CrossLinkU-NX*.

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Revision 4.6, September 2023

Section	Change Summary
Device/Package Thermal Resistance	• Updated values in Table 4.5. CrossLink-NX-33 Device/Package Thermal Resistance. • Added Table 4.6. CrossLinkU-NX Device/Package Thermal Resistance.

Revision 4.5, April 2023

Section	Change Summary
Device/Package Thermal Resistance	Added LFMXO5-55T and LFMXO5-100T information in Table 4.24. MachXO5-NX Device/Package Thermal Resistance.

Revision 4.4, November 2022

Section	Change Summary
Package Thermal Resistance	Added LFG 1156 to Table 3.1. Package Thermal Resistance1.
Device/Package Thermal Resistance	Added Avant™ device.

Revision 4.3, September 2022

Section	Change Summary
Device/Package Thermal Resistance	• Updated LIFCL-40 values and added LIFCL-17 values in Table 4.4. CrossLink-NX Device/Package Thermal Resistance. • Updated LFD2NX-40 and LFD2NX-17 values in Table 4.6. Certus-NX Device/Package Thermal Resistance. • Updated LFCPNX (FOWLP and fcCSP) values in Table 4.7. CertusPro-NX Device/Package Thermal Resistance. • Updated LCMXO3L-9400C/E caBGA400 values from “15 mm x 15 mm” to “17 mm x 17 mm” in Table 4.21. MachXO3 Device/Package Thermal Resistance. • Updated LCMXO3L-9400C/E caBGA484 values from “17 mm x 17 mm” to “19 mm x 19 mm” in Table 4.21. MachXO3 Device/Package Thermal Resistance.

Revision 4.2, June 2022

Section	Change Summary
Device/Package Thermal Resistance	• Added CrossLink™-NX-33 device. • Updated Table 4.6. CertusPro-NX Device/Package Thermal Resistance. Modified the values of the fpBGA 484 device package.

Revision 4.1, March 2022

Section	Change Summary
Acronyms in This Document	Added BBG.
Package Thermal Resistance	Updated Table 3.1. Package Thermal Resistance1. Added BBG256 and BBG400 packages.
Device/Package Thermal Resistance	Added MachXO5-NX device packages: BBG256 and BBG400.

Revision 4.0, December 2021

Section	Change Summary
Package Thermal Resistance	Updated Table 3.1. Package Thermal Resistance. Added BBG and LFG packages.
Device/Package Thermal Resistance	• Added CrossLink device packages: LIA-MD6000 ckfBGA80 and LIA-MD6000 csfBGA81. • Updated Table 4.5. CertusPro-NX Device/Package Thermal Resistance.

Revision 3.9, October 2021

Section	Change Summary
Acronyms in This Document	Added items to the acronyms table.

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Section	Change Summary
Package Thermal Resistance	Updated Table 3.1 Package Thermal Resistance. • Reordered packages. • Added ckfBGA package.
Device/Package Thermal Resistance	• Added CrossLink device package: LIF-MD6000 ckfBGA80. • Added MachXO3D device package: LCMXO3D-9400 WLCSP.
—	Minor style changes.

Revision 3.8, June 2021

Section	Change Summary
Device/Package Thermal Resistance	Added CertusPro-NX device.

Revision 3.7, February 2021

Section	Change Summary
Device/Package Thermal Resistance	Added Mach-NX device package: LFMNX-50 FCBGA484.

Revision 3.6, June 2020

Section	Change Summary
Device/Package Thermal Resistance	• Added Certus-NX device packages: LFD2NX-40-CABGA256, LFD2NX-40-CABGA196, LFD2NX-40-CSFBGA121, and LFD2NX-17-CSFBGA121 • Added CrossLink-NX device packages: LIFCL-40-CSBGA121 and LIFCL-40-CSBGA256.

Revision 3.5, November 2019

Section	Change Summary
Device/Package Thermal Resistance	Added CrossLink-NX device packages: LIFCL-40-CABGA400, LIFCL-40-CSBGA289, and LIFCL-40-QFN72.

Revision 3.4, September 2019

Section	Change Summary
Device/Package Thermal Resistance	• Added CrossLinkPlus device. • Added note referring to XO3LF device. • Added new packages to XO2: XO2-2000-WLCSP49, XO2-4000-QFN84, and XO2-4000-CSBGA184. • Added new packages to XO3D: XO3D-4300-QFN72, XO3D-4300-CABGA256, XO3D-9400-QFN72.

Revision 3.3, June 2019

Section	Change Summary
—	Added Disclaimers section.
Device/Package Thermal Resistance	Added MachXO3D device.

Revision 3.2, March 2019

Section	Change Summary
Acronyms in This Document	Added PCB.
Introduction	• Revised and added context information. • Revised equations. • Added Figure 1.1. Thermal Resistance Path from Silicon Junctions to Ambient Air and Figure 1.2. Thermal Resistance Path from Silicon Junctions to Package Top and to PCB.

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Section	Change Summary
Reducing Junction Temperature	Revised list format.
Device/Package Thermal Resistance	• Added Platform Manager device and moved LPTM10-1247 and LPTM10-12107 to this section. • Added Platform Manager 2 device.

Revision 3.1, September 2018

Section	Change Summary
All	• Changed document ID from “thermal” to FPGA-TN-02044. • Updated document template. • Added Acronyms in This Document section.
Device/Package Thermal Resistance	• Updated CrossLink thermal data based on new silicon design O1E. • Added automotive part LIA-MD6000 80 ctfBGA. • Added LFE5U-12F CSFBGA 285, LFE5U-12F CABGA 381, LFE5U-25F CABGA 256, LFE5U-45F CABGA 256, and LAE5U-12F CABGA 381. • Added automotive part LAE5UM-4F 381 CABGA. • Added iCE40 UltraPlus devices. • Updated LCMXO2-256 QFN 7 mm × 7 mm and LCMXO2-640 QFN 7 mm × 7 mm thermal data. • Added LCMXO2-1200 QFN 5 mm × 5 mm thermal data. • Added LCMXO3L-9400E devices. • Added L-ASC10 device. • Deleted obsolete packages.

Revision 3.0, March 2017

Section	Change Summary
Device/Package Thermal Resistance	Reverted the LCMXO3L-6900C 400 I/O data in Table 4.21. MachXO3 Device/Package Thermal Resistance.

Revision 2.9, March 2017

Section	Change Summary
Device/Package Thermal Resistance	• Added CrossLink packages. • Added MachXO2 QFN packages. • Added LCMXO3L-9400E and LCMXO3L-9400C values.

Revision 2.8, February 2015

Section	Change Summary
Device/Package Thermal Resistance	Added iCE40 UltraLite packages.

Revision 2.7, January 2015

Section	Change Summary

Device/Package Thermal Resistance	• Updated Package Thermal Resistance section.
	  • Added iCE40LP1K and iCE40LM4K WLCSP packages.
	• Updated Device/Package Thermal Resistance section.
	  • Added iCE40 UltraLite packages
	  • Updated iCE40 Ultra 36 WLCSP θ_{JB} and θ_{JC} data for all devices
	  • Removed iCE40 Ultra 20 WLCSP product.

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Revision 2.6, October 2014

Section	Change Summary
Device/Package Thermal Resistance	Added ECP5 packages.

Revision 2.5, September 2014

Section	Change Summary
Device/Package Thermal Resistance	Added MachXO3L packages.

Revision 2.4, June 2014

Section	Change Summary
Device/Package Thermal Resistance	Added iCE40 Ultra packages.

Revision 2.3, May 2014

Section	Change Summary
Device/Package Thermal Resistance	Changed LCMXO2-1200 TQFP package dimensions to 20 mm × 20 mm.

Revision 2.2, May 2014

Section	Change Summary
Device/Package Thermal Resistance	Added Platform Manager information.

Revision 2.1, August 2013

Section	Change Summary
Device/Package Thermal Resistance	Added iCE40 and MachXO2 information.

Revision 2.0, August 2012

Section	Change Summary
Device/Package Thermal Resistance	Added iCE40 information.

Revision 1.9, March 2012

Section	Change Summary
Device/Package Thermal Resistance	Updated MachXO2 and LatticeECP3 families to reflect current product availability.

Revision 1.8, February 2012

Section	Change Summary
All	Updated document with new corporate logo.

Revision 1.7, February 2011

Section	Change Summary
Device/Package Thermal Resistance	Added MachXO2 information.

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Revision 1.6, July 2009

Section	Change Summary
Package Thermal Resistance	Added new caBGA packaging.
Device/Package Thermal Resistance	• Added LatticeECP3 information. • Added θ_{JB} column in tables.

Revision 1.5, April 2009

Section	Change Summary
Package Thermal Resistance	Added new QFNS, ucBGA, csBGA, and caBGA packaging.

Revision 1.4, October 2008

Section	Change Summary
Package Thermal Resistance	Added units (°C/W).

Revision 1.3, April 2008

Section	Change Summary
Package Thermal Resistance	Added 64-ball csBGA and 144-ball csBGA packaging.

Revision 1.2, March 2008

Section	Change Summary
Introduction	Corrected equation on page 1.

Revision 1.1, January 2008

Section	Change Summary
Package Thermal Resistance	Updated this section for ftBGA 256 packaging information.

Revision 1.0, September 2007

Section	Change Summary
Package Thermal Resistance	Updated information
Device/Package Thermal Resistance	Added this section.

Previous Lattice releases

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