SERIAL MULTI-PROTOCOL TRANSMISSION WITH THE LatticeSC FPGA

A Lattice Semiconductor White Paper

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Introduction

The movement towards serial chip to chip and backplane interconnects continues at a frantic pace, particularly in the communications and storage arena. Standardization forums such as the OIF, RapidIO TA, PCI-SIG, OBSAI and CPRI have solidified their work and various packet-based protocols are in the process of being adopted by system and chip vendors.

In addition to these emerging protocols, there is also a broad installed base of more mature serial-based protocols such as GbE, 10G Ethernet, SONET and Fibre Channel that must be addressed as they undergo a facelift to accommodate the multi-protocol nature of the network.

As the PHY and protocol layers of these new standards are being established and work continues to upgrade existing technology in the field, system vendors now have to decide how best to transmit these various protocols over existing transmission infrastructures, both inter- and intra-board.

Although each protocol is unique, one thing that they all have in common is a layered protocol stack. However, all protocol stacks are not created equal: their implementation can vary greatly from one layer to the next. Typically, the physical layer consists of fixed functionality that is common to multiple packet-based protocols, while the upper layers tend to be more customizable. The dynamic of upper layer functionality is necessitated by both the natural evolution that takes place when dealing with an emerging standard as well as the desire of system vendors to create their own “value add” via proprietary functionality. In either case, the value of programmability for implementation of these serial standards means a SERDES-based FPGA solution will remain a necessity for the foreseeable future. Figure 1 shows the functional partitioning of the physical and the upper layers of the protocol stacks.

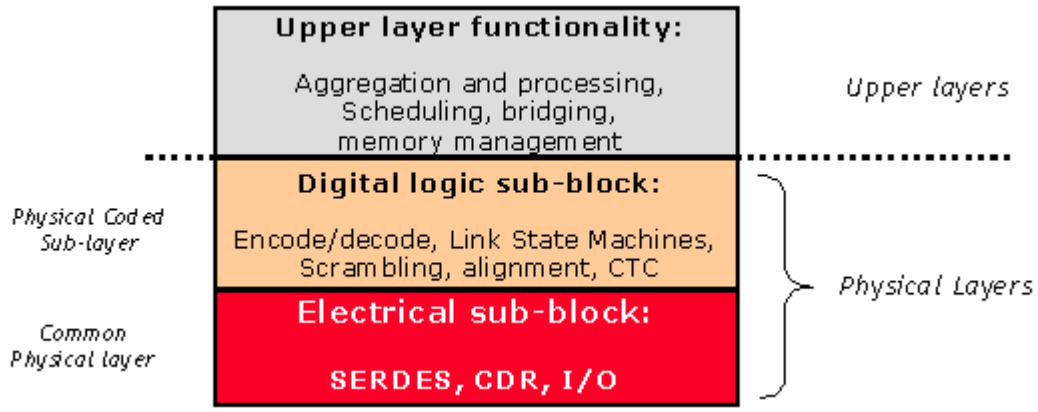

Figure 1 – Protocol stack functional partitioning

This white paper examines the implementation of these multi-protocol standards and their associated stacks, and discusses why they are ideally suited to an FPGA-based SERDES implementation such as the LatticeSC family of FPGA devices.

Physical Layer

As shown in Figure 1, many elements of the Physical Layer (PHY) are common across many of the packet-based protocols. The functionality is partitioned into the electrical sub-block and the digital logic sub-block.

The Importance of a Robust SERDES

System level designers are often faced with moving large blocks of data from one location to another over moderate distances and high rates of speed. Historically, this was accomplished by a source synchronous parallel interface, which required large banks of parallel line drivers and receivers. In addition, it has become more and more difficult to ensure the data integrity of these types of interfaces from board to board at the gigabit plus data rates that are required in systems today.

With the inception and growing acceptance of Serializer/Deserializer (SERDES) devices, designers can alleviate the concerns inherent in the implementation of a parallel interface. SERDES technology permits smaller, less expensive cables and connectors, while providing a more robust solution in terms of signal integrity when moving large blocks of data at rates of 3.125Gbps and beyond.

However, there is more to providing a robust SERDES solution than just the raw data rate. Physical layer parameters such as media type/drive length at high data rates, signal jitter and overall device power consumption must also be considered if one is to truly assess a SERDES capability.

Lattice SERDES is recognized as an industry leading technology for the following reasons:

- **Drive length** (across passive channel) - >60 inches of FR-4 backplane @ 3.125Gbps (aided by built-in Tx pre-emphasis and Rx equalization).
- **Tx/Rx jitter tolerance** - Tx/Rx jitter values (0.29UI at 3.125G for Tx, 0.8UI tolerance for Rx, typical) meets XAUI, PCI Express, GbE and FC jitter specifications.
- **Power** - 100 mW/channel (typical) @ 3.125Gbps, including I/O buffers and Rx equalization
- **Flexibility** - 600Mbps-3.4Gbps serial data rates (full and half rate data rates selectable per channel)
- **System Level Integration** - various status and interrupt capabilities to monitor the physical link.

Physical Coded Sublayer (PCS)

In addition to a quality SERDES, it is also essential to offer the associated Physical Coded Sublayer (PCS) functionality that is required in order to comply with existing packet-based industry standards such as PCI Express, Serial RapidIO, GbE, XAUI, Fibre Channel and emerging standards such as CPRI and OBSAI. The LatticeSC FPGA provides such a solution by coupling industry leading SERDES technology with associated higher layer PCS logic, called flexiPCS, which is implemented in ASIC technology. These embedded cores are integrated onto the same die with the FPGA fabric to create a high performance, low power and low cost system level solution that is unique to the industry.

What makes the Lattice flexiPCS unique is how feature rich and programmable the block is, supporting packet-based 8b10b and SONET-based protocols as well as a bypass mode for applications that do not require this functionality. Among the features supported in the PCS are

- Tx/Rx Link State Machines *(with programmable support for conversion to |A|, |K|, |R| and |Q| code groups)*
- CRC generation/ checking
- Encoding/Decoding, and/or TDM Scrambling/Descrambling
- Protocol specific clock tolerance compensation
- SONET framing and TOH generation
- MAC level scrambling *(for PCI Express)*
- Alignment/Bonding of multiple channels
- Packet buffers and FIFOs to support clock domain transfers

These blocks provide the foundation for implementing a multitude of existing and emerging serial packet protocols and TDM/SONET protocols. Some of these will be explored in greater detail below.

Upper Layers

The Value of Programmability

As with any emerging standard or technology, implementation begins long before the final version of the specifications is issued. Also, vendors rarely design chips targeted towards a single specification, choosing instead to architect their systems utilizing proprietary circuitry that augments the functionality called for in the specification…a way of adding their own personal touch to the final product.

The advantages of stand-alone ASSPs are well documented and understood. However, for applications involving emerging specifications or where custom logic is desired, programmability is a key advantage and necessity for the designer. Programmability offers system designers the luxury of an early start architecting and implementing their designs without having to wait for the final version of the specification. The ASIC portion of the LatticeSC offers performance and power advantages for the “fixed” portion of the design (i.e. PHY layer functionality), while the programmable nature of the LatticeSC device allows the upper layers of the design to evolve with the specifications and customer needs.

One example of this is PCI Express. The protocol stack consists of the Physical (PHY), Data Link and Transactions layers. The transaction layer can vary greatly, depending on factors such as end application, number of channels and other interfaces that need to be bridged to PCI Express. In this situation, the LatticeSC can provide an economical solution by virtue of 'hardening' the fixed portions of the stack while providing the flexibility of an FPGA fabric for custom or evolving logic.

The following sections will examine more closely this as well as various other protocol standards and applications that are well suited for a programmable platform that combines high performance, low power embedded ASIC technology with the flexibility of an FPGA fabric.

Wireline Networks: PCI Express, Serial RapidIO, Ethernet and Fibre Channel

These are four of the most popular serial protocols utilized in wireline applications. Figure 2 shows the PHY layer support offered by the LatticeSC flexiPCS. The following sections provide a more detailed look at each protocol and the inherent advantages the extreme performance of the LatticeSC programmable platform provides.

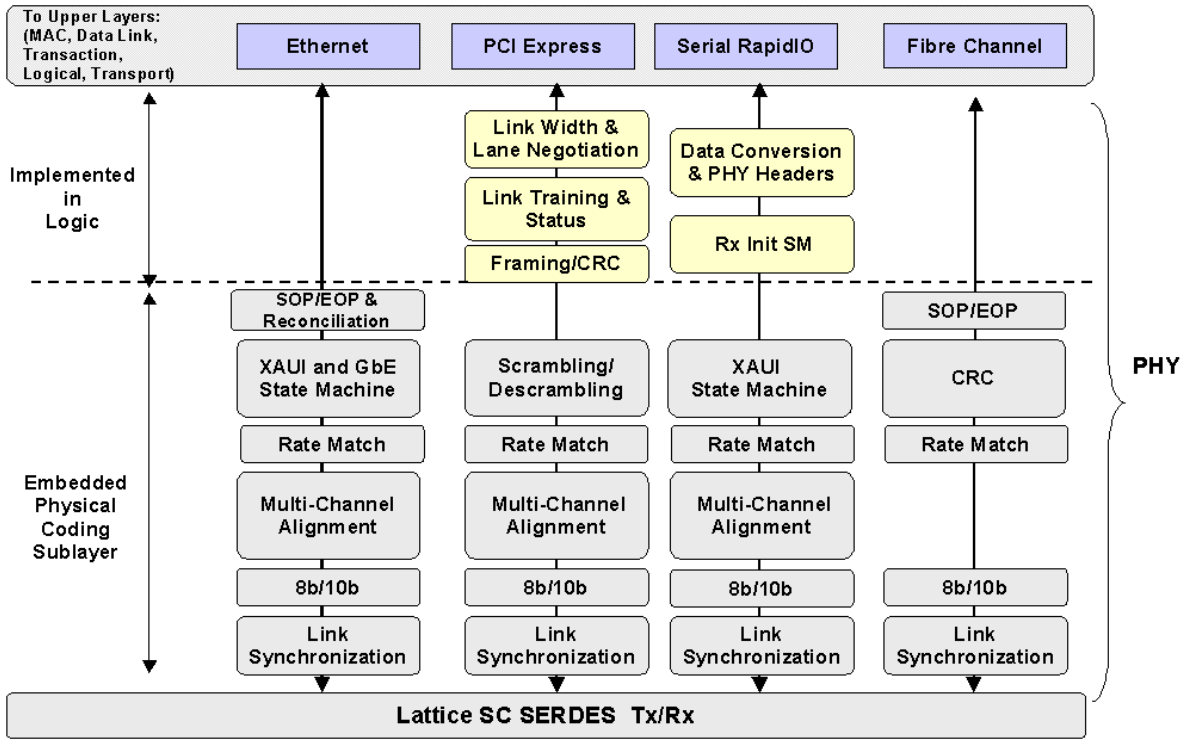

Figure 2 - Packet Protocols Supported by the LatticeSC flexiPCS

PCI Express

Conventional PCI, once the standard I/O bus with its roots in the early 90's, is now showing its age. This has led designers to implement newer versions such as PCI-x and PCI-x 2.0, allowing them to maintain the existing software base while achieving greater throughput. But even with these enhancements, processor throughput still outpaces I/O throughput.

PCI Express was conceived in order to address these ever increasing bandwidth needs by providing a scalable, point-to-point serial connection between chips, over cable or via connector slots for expansion cards, while maintaining compatibility with conventional PCI at the software layer.

A single PCI Express serial link is a dual-simplex connection, specified to speeds of up to 2.5Gbps per link that can be scaled in x1, x2, x4, x8, x12, x16 and x32 lane widths to achieve greater bandwidth. A serial implementation is cheaper, can be driven further distances and alleviates common mode noise and skew concerns inherent in existing source synchronous parallel interfaces (such as conventional PCI), as well as reducing the overall number of connections required. For practical purposes, this paper will discuss lane widths available for implementation on standard cable connectors.

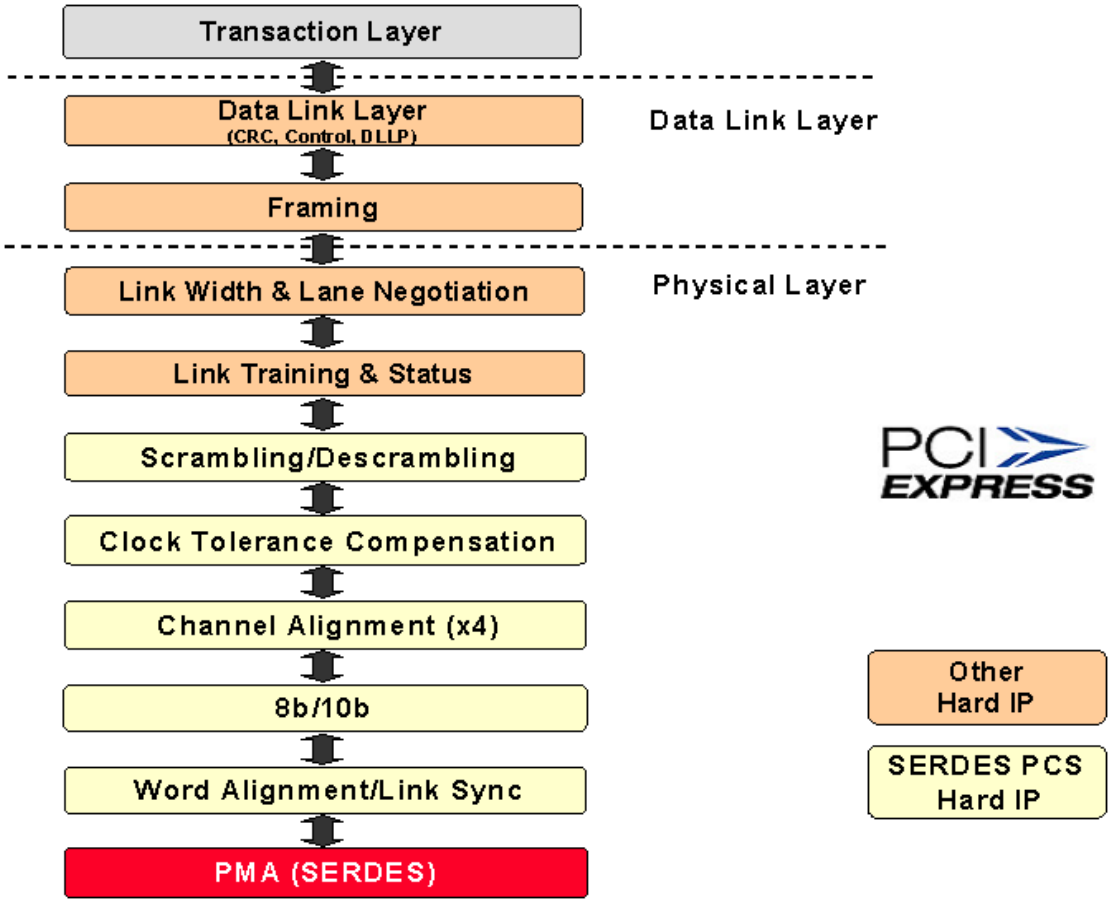

Figure 3 - LatticeSC PCI Express protocol stack implementation

As Figure 3 illustrates, PCI Express is a packetized and layered protocol structure. The stack consists of the Physical (PHY), Data Link and Transaction layers. This white paper has previously noted the value of a programmable solution when implementing the protocol stacks of these emerging standards and, in this case, both the data link layer and transaction layers of the PCI Express stack are good examples of functionality that takes advantage of programmability.

Depending upon the design, these layers can be customized to support an end point implementation, a switch or, in many cases in which an FPGA is involved, a bridging function to a legacy communications protocol such as conventional PCI.

With up to 32 SERDES channels available on a single device, the LatticeSC provides a highly integrated, configurable and economical PCI Express solution by “hardening”

the fixed portions of the protocol stack while leaving the customizable higher layer functionality to be implemented in FPGA gates.

Serial RapidIO

Another emerging serial standard is Serial RapidIO. Like PCI Express, Serial RapidIO has its roots in the source synchronous world. When combined with the existing RapidIO parallel specification, Serial RapidIO allows designers to standardize on a single interconnect technology for networking, telecommunications and other embedded applications.

Serial RapidIO is a scalable, point-to-point, low pin count interconnect designed to address increasing system bandwidth needs. Serial RapidIO leverages industry-standard signaling technology found in Fibre Channel, 10G Ethernet XAUI interfaces and Infiniband, and operates at 1.25, 2.5 and 3.125 Gigabaud per link, providing the required bandwidth for signal processors and backplane applications. The serial specification defines both a single differential link in each direction between devices and support for ganging four links together for higher throughput applications.

As illustrated in Figure 4, Serial RapidIO also has a layered protocol structure. Lattice Semiconductor also offers a family of devices that, when coupled with available embedded ASIC and soft IP cores, provides a low cost, low power and highly integrated solution that addresses the physical, with future support for the logical and transport, layers of the Serial RapidIO specification.

As with PCI Express, a Serial RapidIO implementation also benefits from the inherent flexibility that a programmable device provides. Here, the malleable logical and transport layer functionality can be implemented in FPGA gates, while the fixed functionality of the physical layer is dedicated to the ASIC portion of the device.

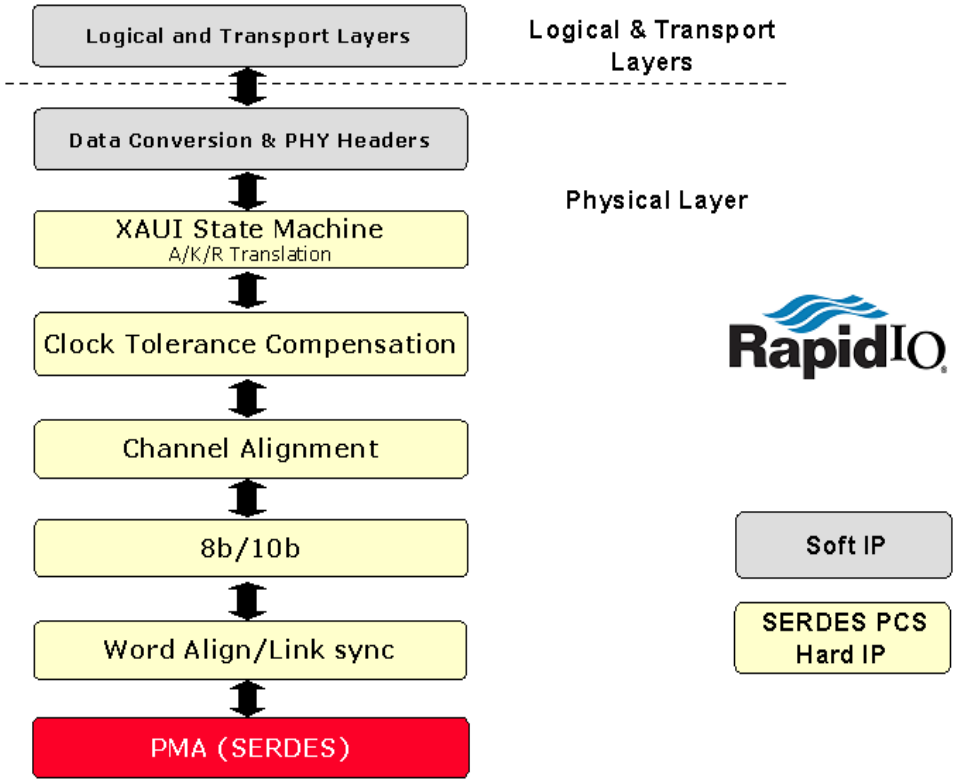

Figure 4 – Serial RapidIO protocol stack implementation

Ethernet

Gigabit Ethernet

Based on the volume of installed ports, Ethernet is the most dominant networking protocol by virtue of its cost performance relative to other solutions.

Gigabit Ethernet builds on top of the Ethernet protocol, but increases the speed tenfold over Fast Ethernet from 100Mbps to 1000 Mbps, or 1 gigabit per second (Gbps). By leveraging the Fast Ethernet protocol stack, GbE allows customers to migrate their Fast Ethernet solutions while maintaining software compatibility with existing products.

As Figure 5 shows, GbE is a layered protocol structure. The stack consists of the Physical (PHY) layers as well as the MAC, Logical Link and other customizable upper layers. Once again, there is value in a programmable solution for GbE applications. The LatticeSC family offers a fully compliant 802.3z implementation of a GbE PHY in

the PCS portion of our SERDES. This ASIC block provides functionality such as 8b/10 encode/decode, link state machine, auto-negotiation and clock tolerance compensation. When combined with available MAC layer IP and proprietary upper layer functionality, the LatticeSC allows the user to design a fully integrated GbE solution.

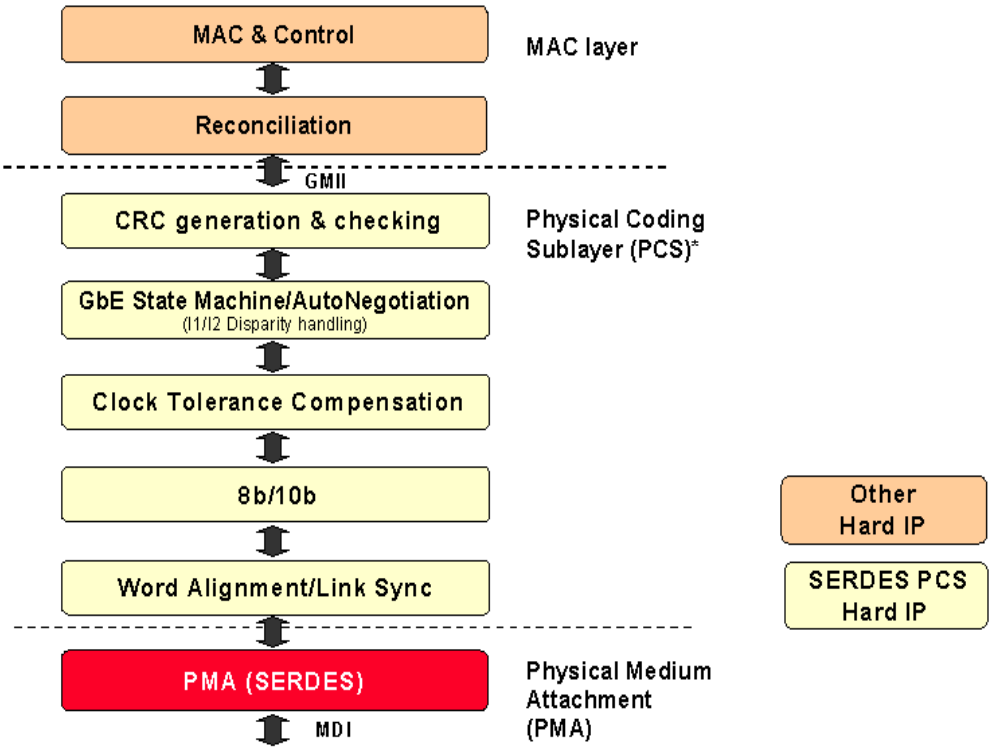

Figure 5 - LatticeSC GbE stack implementation

XAUI

XAUI transceivers are comprised of four 3.125-Gbit/s SERDES channels and employ the same 8B/10B-transmission code of GbE to provide the high level of signal integrity necessary to traverse both chip-to-chip and backplane interfaces. By virtue of its serial nature, XAUI reduces 10G Ethernet's 72-pin XGMII interface to 16 pins, simplifying and extending the reach of the interface. The same PCS block can also be used for 10G Fibre Channel applications with minor changes that can be implemented in the FPGA.

Figure 6 illustrates the XAUI interface and where it resides in the 10G Ethernet stack. The LatticeSC family of devices offer a fully compliant 802.3ae-2002 XAUI implementation, including ASIC block functionality such as 8b/10 encode/decode, Tx/Rx state machines with programmable |A|, |K|, |R| characters, lane alignment and deskew and clock tolerance compensation. This block also provides an XGMII to support interfacing with the Lattice 10G MAC IP that is also available. This Lattice IP, when combined with proprietary upper layer functionality, allows the LatticeSC to offer a fully integrated XAUI solution.

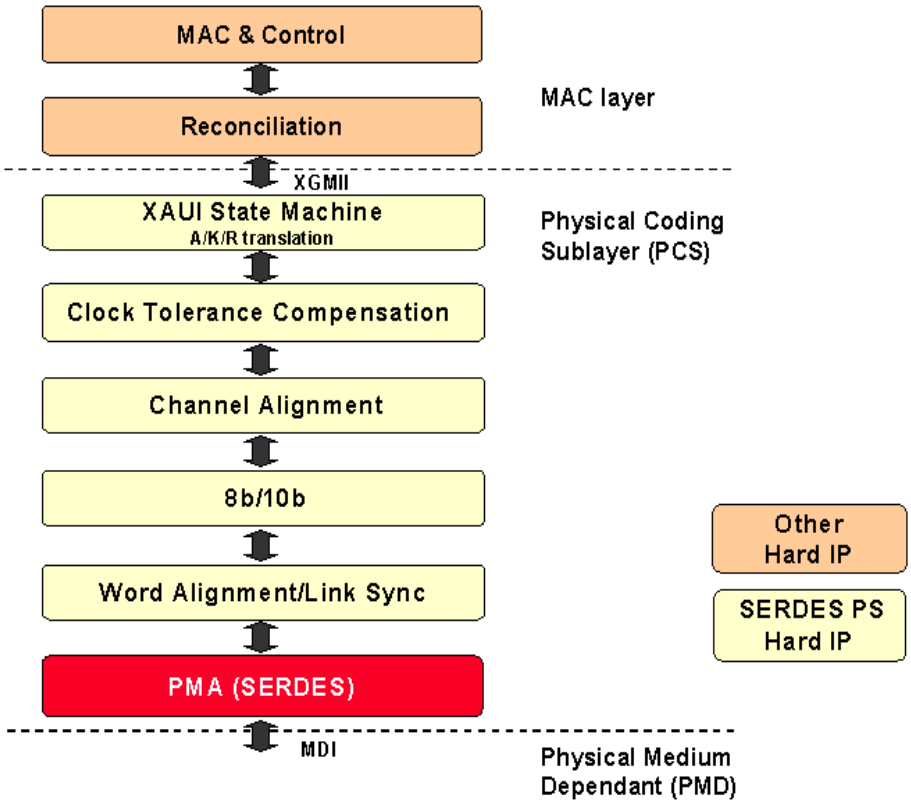

Figure 6 - LatticeSC XAUI implementation

Fibre Channel

Fibre Channel (FC) was developed as a practical, inexpensive and expendable means of quickly transferring data between workstations, mainframes, supercomputers, desktop computers, storage devices, displays and other peripherals. Fibre channel is a high performance serial link supporting its own, as well as other higher-level protocols, such as the FDDI, SCSI, HIPPI and IPI. The Fibre Channel standard addresses the need for very fast, reliable transfers of large

amounts of information. The bulk of current implementations operate at 1Gbps on a single serial channel; however, specifications exist for single channel data rates of 2G, 4G and 10Gbps as well.

The Fibre Channel mode of the LatticeSC SERDES/PCS block supports the 1G and 2G Fibre Channel protocol. FC-0, FC-1 and portions of the FC-2 layer are implemented in this embedded ASIC block, which includes capabilities such as Tx/Rx state machines, 8b/10b encode/decode, word alignment and CRC generation and checking. Figure 7 shows the Lattice implementation of the FC protocol stack. The remaining FC-2 functionality and any other customer specific upper layer functionality can be implemented in the FPGA portion of the device.

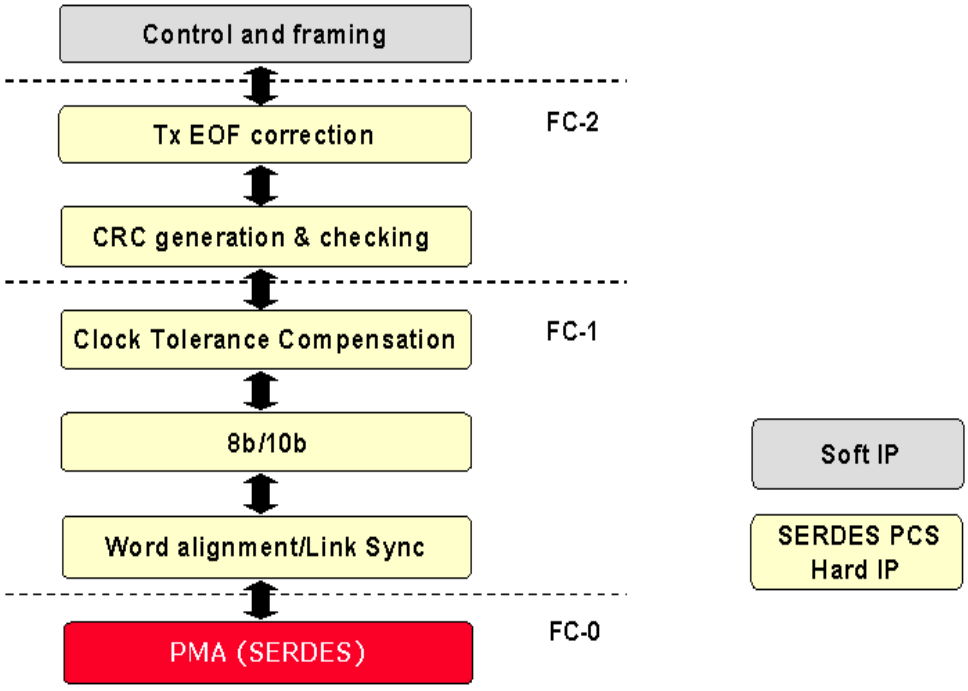

Figure 7- LatticeSC Fibre Channel stack implementation

SONET/SDH

The majority of worldwide telecom equipment is still based on legacy SONET/SDH protocols. Even though there is strong momentum to move to packet protocols, the

large installed base means SONET will still be a viable player in the foreseeable future. This maturity, as well as its inherent low overhead, makes SONET/SDH attractive to the backplane system designer.

The LatticeSC family offers a robust SONET mode in its SERDES/PCS block. This embedded ASIC core supports both STS-12/STM-4 and STS-48/STM16 standards, as well as options to implement major portions of the emerging TFI-5 standard. Some of the supported features in the embedded ASIC block include Tx scrambling and TOH generation/insertion, as well as frame detection/pulse generation, descrambling, AIS insertion/RDI detection and B1 BIP checking on the Rx side. Pointer monitoring/interpretation for the H1/H2 bytes is also provided to support floating payloads. These features are summarized in Figure 8.

Once again a programmable platform allows the design to support other higher layer functionality. An example of this flexibility is apparent in GbEoS applications, in which the Ethernet frames can be mapped in SONET payloads utilizing circuitry such as GFP and LCAS. Another example is when SONET is used as a low overhead backplane transport. The LatticeSC provides the user the physical layer SONET/SDH functionality in ASIC gates, while providing a robust FPGA fabric for integration of proprietary functionality onto a single platform.

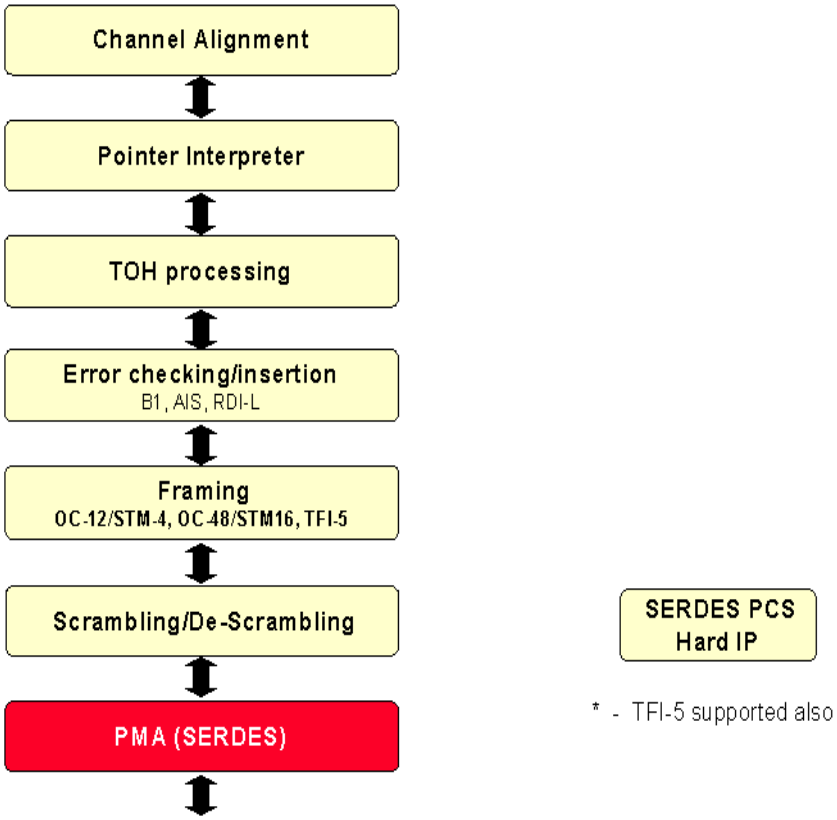

Figure 8 - LatticeSC SONET/SDH implementation

Wireless Networks

CPRI and OBSAI

In the wireless domain, two initiatives are currently competing to facilitate the more rapid development of cellular base stations. Both the CPRI and OBSAI standards focus on the standardization of serial transmission protocols, with the primary objective the reduction of overall system cost though the standardization of its components.

CPRI

The CPRI (Common Public Radio Interface) is an industry initiative with the intent to support a flexible basestation architecture by partitioning the base station into two basic building blocks, the radio equipment control (REC), which handles the base band functionality, and the Radio Equipment (RE), which provides the RF functionality.

Building blocks are interconnected by a serial data link that is 8b10b encoded and intended to utilize existing High Speed Serial standards such as Ethernet and Fibre Channel. Physical layer line rates of 614Mbs, 1.228Gbs or 2.456Gbps are supported with three different information flows (User Plane data, Control & Management (C&M) and Synchronization) multiplexed over a single serial interface.

Lattice Semiconductor offers a complete system solution for CPRI applications. The physical layer functionality is supported via the embedded ASIC core in the LatticeSC devices, with associated soft IP cores addressing data link layer functionality, as shown in Figure 9.

OBSAI

Similarly, OBSAI partitions the base station into baseband and RF blocks, but also defines an additional Transport and Control block. In contrast to CPRI, the interfaces between each of these are unique reference points, defined as RP1 (control plane), RP2 (user plane between transport to base band blocks) and RP3 (user plane between base band and RF blocks). These building blocks are specified as Ethernet interfaces, but for the purposes of this white paper the focus will be on the RP3 interface, since it is an 8b/10b encoded serial link similar to the CPRI specification mentioned above.

Physical layer line rates of 768Mb and 1.536Gbps are supported for the RP3 interface in support of high speed data transfer and associated control. The protocol stack is again a packet concept utilizing a layered protocol, as shown in Figure 9 below.

Again, the SERDES and 8b/10b-based nature of the LatticeSC devices provide an integrated platform in support of a complete OBSAI system solution. Physical layer functionality is supported via the embedded ASIC core of the devices, with associated soft IP core addressing data link layer functionality.

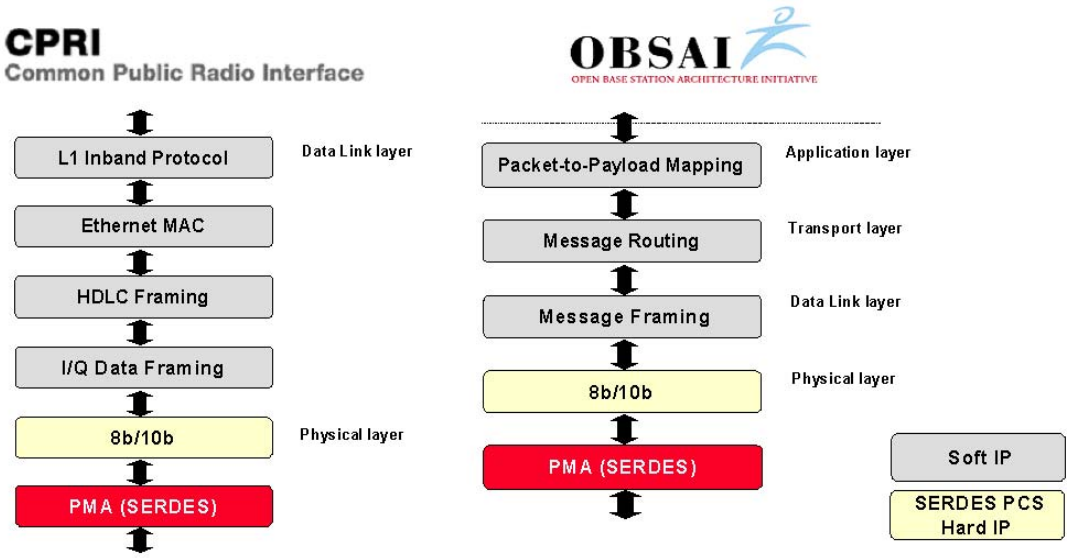

Figure 9 – LatticeSC CPRI/ OBSAI RP3 protocol stack implementation

Summary

As the communications and storage systems industries converge toward various packet-based serial I/O for high bandwidth and low pin count connectivity, system vendors will look toward silicon and infrastructure vendors to provide a one-stop, SERDES-based solution as they focus increasingly upon adding value to the overall system.

To achieve this, silicon suppliers must offer solutions that deliver robust signal integrity in addition to flexible silicon solutions. These needs are more prevalent than ever in order to support the myriad of designs that require the bridging of both serial and high-speed parallel interfaces for backplane and chip-to-chip applications.

In these situations a high quality, integrated SERDES solution mixed with pre-engineered “hard IP” for the mature portions of popular serial protocols offers the most robust, lowest power and lowest cost solution. Add a dose of high density, high performance programmable logic to the mix for implementation of proprietary circuitry, and you have the ideal solution.

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