



MANAGING POWER SEQUENCING FOR THE LatticeSC FPGA

A Lattice Semiconductor White Paper

February 2007

Lattice Semiconductor
5555 Northeast Moore Ct.
Hillsboro, Oregon 97124 USA
Telephone: (503) 268-8000
www.latticesemi.com

Introduction to the LatticeSC FPGA and Lattice Power Manager II Families

The LatticeSC (System Chip) FPGA family combines a high-performance FPGA fabric, 3.8Gbps SERDES and PCS, high-performance I/Os, large embedded RAM and embedded ASIC blocks in a single architecture. Because this device can interface with a number of logic standards, most designs require that multiple power supply voltages power up its I/O channels. The LatticeSC device also requires multiple power supply voltages to power its core, PLL, etc.

The Lattice Power Manager II family consists of in-system programmable mixed-signal devices that combine both programmable analog and programmable digital circuitry to provide a cost effective, flexible and programmable solution for integrating all board-level power supply management functions: power supply sequencing, voltage supervision, reset generation, hot-swap control, watchdog timer and power supply margining.

This white paper examines a Power Manager II device that provides safe turn-on for a LatticeSC FPGA across a wide range of applications, limiting current in-rush as well as monitoring and controlling the sequencing of multiple power supplies. For a detailed description of the LatticeSC power sequencing requirements and power supply trip point levels, please refer to the document TN (Technical Note) 1101 – “Power Calculations and Considerations for LatticeSC Devices,” available at <http://www.latticesemi.com/documents/tn1101.pdf>

A brief introduction to the LatticeSC and Power Manager architectures is provided to facilitate understanding of the LatticeSC FPGA power supply sequencing implementation using the Lattice Power Manager device.

LatticeSC FPGA Architecture

The LatticeSC FPGA is manufactured on Fujitsu's 90nm CMOS process technology which, combined with an optimized logic block and ample routing, yields an FPGA fabric easily capable of 500MHz performance (e.g., 64-bit address decode). The basic logic element of the array is the Programmable Function Unit (PFU), which can be configured for logic, arithmetic and distributed RAM/ROM functions. PFUs are divided into four slices, each containing two 4-input SRAM Look-up Tables (LUTs) plus registers. Slices are individually configurable and can be cascaded, as can the PFUs for larger functions. Densities in the family span 15K to 115K LUTs.

LatticeSC devices offer 1 to 7.8 Mbit embedded block RAM (EBR) capable of 500MHz operation. Each 18Kb sysMEM EBR block can implement single port, true dual port and pseudo-dual port or FIFO memories. Dedicated FIFO support logic allows the LatticeSC devices to efficiently implement FIFOs without consuming LUTs or routing resources for flag generation.

The LatticeSC FPGA also is packed with hierarchical clocking resources and, unlike competitive devices, provides both PLL and DLL resources to deliver a no-compromise solution for clock management.

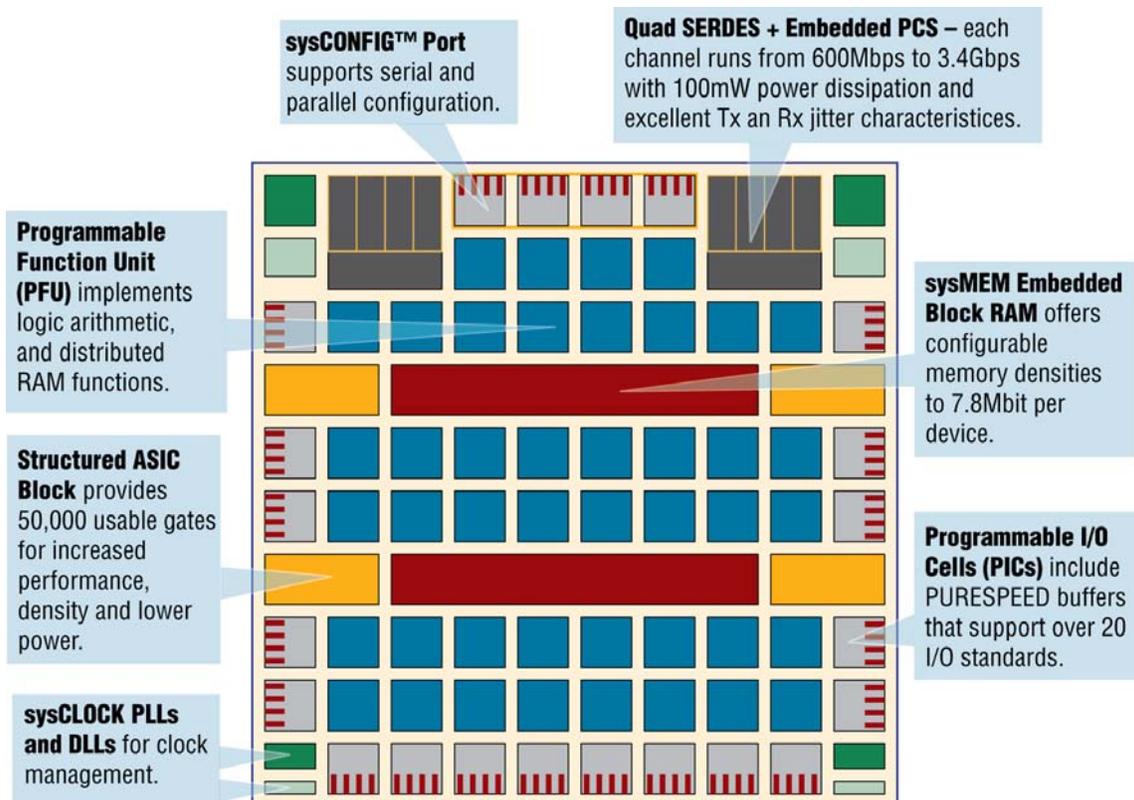


Figure 1 – LatticeSC Block Diagram

Power Manager Device Architecture

Figure 2 shows the block diagram of the Lattice Power Manager, a programmable mixed signal device. It consists of the following blocks

- Programmable Threshold Comparator – to monitor Power Supply voltages and feed the logic status to the PLD, which implements power management algorithms
- Digital Monitoring Inputs – To monitor digital inputs
- Programmable Timers – to control power supply sequencing and other delays as required by the power management algorithm
- Programmable Digital Outputs, driven by the on-chip PLD or by I²C interface, to control DC-DC converter enable signals as well as for the generation of control signals used on the circuit board
- Programmable MOSFET driver to control power supply feed through MOSFETs

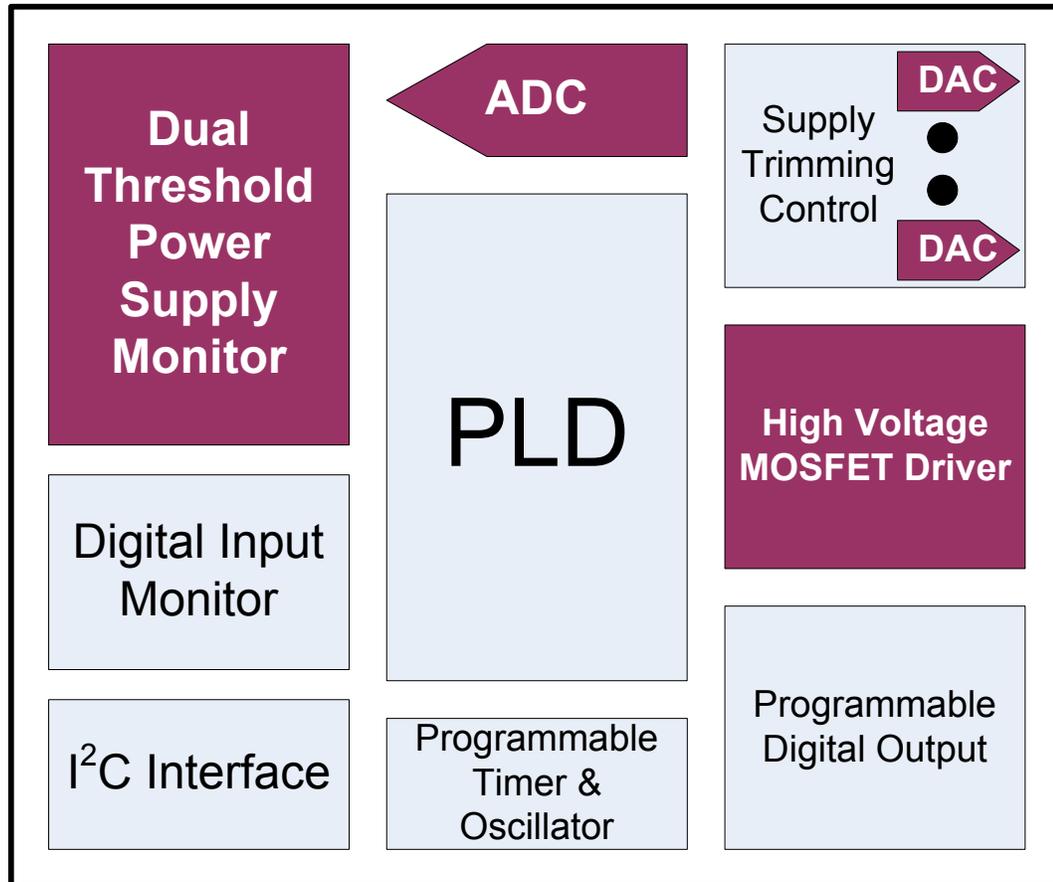


FIGURE 2 – Power Manager Block Diagram

- DACs to control power supply output voltages and maintain them within 1% of the preset value
- PLD based on Lattice Semiconductor’s ispMACH4000 CPLD architecture to implement the entire power management algorithm
- ADC to measure the monitored power supply voltage and enable an external processor to read the measured value through the I²C interface
- I²C interface to measure the power supply voltages, read digital input and output status and to enable a microprocessor on the I2C bus to control power supply algorithm

The power supply management algorithm is implemented using the software tool, PAC-Designer. The PAC-Designer provides intuitive and user-friendly graphical user interface. The on-board graphical stimulus editor and the simulator enable verification of the power management algorithm.

A verified design can be easily downloaded into a power manager device on an evaluation board through the PC Parallel port, for hardware verification.

LatticeSC FPGA Power Supply Sequence Control

Figure 3 illustrates the LatticeSC's seven power supplies on the right of the block diagram. They are:

1. V_{cc} – This is the core voltage this can be 1.0 or 1.2V depending on the type of FPGA used.
2. V_{cc12} – This is a 1.2V power supply powering the analog sections of the LatticeSC. This supply should be as quiet as possible. Designers can either use an LDO for this or, if the core voltage is 1.2V, use a passive filter to get a clean supply. Note: If the V_{cc12} is derived from the core supply, the V_{cc} must never (even during power up and down) be more than 300 mV above V_{cc12} .
3. V_{ccAUX} – This is a 2.5V supply. Note that if the device uses I/O power supplies less than 2.5V, then V_{ccAux} should be turned on before those I/O power supplies.
4. V_{ccJ} – This supply powers the JTAG circuitry.
5. V_{CCIO1} – This is a special I/O power supply. If this supply drops below its power up trip point, the LatticeSC device is reset.
6. $V_{ccIOs} > V_{ccAUX}$ – These I/O supplies are 2.5V and above and are turned on and off differently from the next set of V_{ccIO} supplies.
7. $V_{ccIOs} < V_{ccAUX}$ – These I/O supply voltages are less than 2.5V. These supplies should be turned on only after V_{ccAUX} .

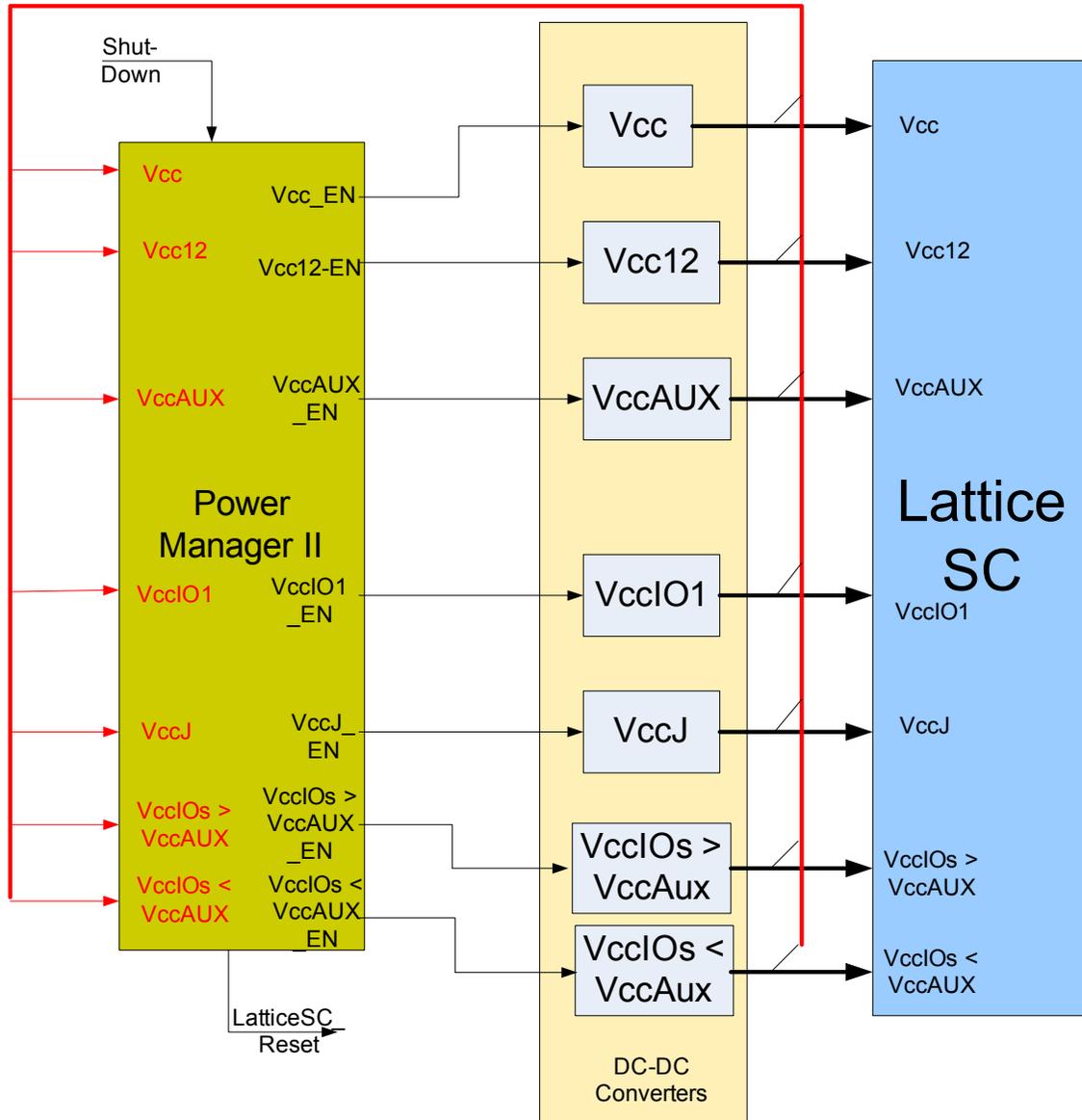


Figure 3 – LatticeSC Power Supply Sequence Control

All DC-DC converter output voltages are connected to the left side of the Power Manager II device. These voltages are monitored for preset voltage levels by the on-chip programmable threshold comparators of the Power Manager II. Each power supply is controlled by one of the open drain outputs of the Power Manager II. These open drain outputs are controlled by the logic implemented in the on-chip PLD. The inputs to this on-chip PLD are derived from the programmable threshold comparators and the digital input pins.

When a power supply voltage crosses its threshold, the on-chip programmable threshold comparator signals the state machine in the PLD, which in turn controls the power supply sequence.

Changes to the power sequencing order can be implemented easily by altering the logic in the state machine.

LatticeSC Power Sequencing Algorithm **Implemented in Power Manager II**

1. Turn on VCC12 supply, wait for it to reach Min Trip Point.
2. Simultaneously turn on all other supplies (VCC, VCCAUX, VCCIO1, VCCJ, VccIOs> VccAUX,).
3. Wait for VccAUX to reach its Min Trip Point and turn on VccIOs<VccAux supplies.
4. Wait for all supplies to reach their power up Min Trip Point.
5. Wait for all supplies to reach their operating range with a time-out of 75 ms.
6. If 75 ms time-out occurs, jump to power down sequencing.
If all supplies reach their operating values before timeout, continue.
7. Wait for the shutdown request.
8. Turn off VCC, VCC12 and VccIOs<VccAUX.
9. Wait for all three supplies to reach their respective power-down trip point.
10. Turn off all other supplies.

LatticeSC_Reset =
(VCC or VCC12 or VCC Aux, or VCC IO1) < Their respective Power Down Trip points

This logic signal can be used to alert the board management processor for further palliative action.

A Power Manager II device has up to 12 analog power supply voltage monitoring inputs, up to 20 control outputs as well as up to 6 digital inputs, and up to a 48-Macrocell CPLD. The power supply sequencing circuit uses fewer resources than those available on the Power1014 chip, one of the smaller members of the Power Manager II family. These additional programmable resources can be used to implement other board management functions.

Implementing Board Level Power Management in a POWR1014

Designers have to meet the combined power supply sequencing needs of all devices, including the LatticeSC FPGA, on the circuit board. Often these sequencing needs change during the prototype stage and again when one of the device's specification changes.

Overall board-level power management includes not only the power supply sequencing but also monitoring the output voltages of all power supplies for under and over voltage. Typically, the on-board CPU also requires the generation of a CPU reset signal.

The following screen shot shows the source code listing of a board-level design implemented in a Lattice's Power Manager II ispPAC-POWR1014 device.

The POWR1014 device implements not only the power supply sequencing required for the LatticeSC FPGA but also the sequencing needed for a CPU. In addition, the POWR1014 generates the following control signals:

- **CPU-Reset** – Integrates the function of a Reset Generator IC
- **Supply_Fault_Intr** – Integrates a Voltage Supervisor IC
- **WDT_Intr** – Integrates a Watchdog timer IC
- **VccCPU_Core_en** – Controls the sequencing on-board CPU core supply

Figure 4 shows the source code of the power management algorithm implemented within the POWR1014 device using the PAC-Designer Software Tool

Step	Sequencer Instruction	Comment
SMD Step 0	Begin Startup Sequence	ispPAC-POWR1014 reset
SMD Step 1	Wait for AGOOD	
SMD Step 2	Vcc12_En = 1, VccCPU_Core_En = 1,	Enable PLL Supply & CPU Core Voltage First
SMD Step 3	Wait for Vcc12_on_off_Trip_Point AND CPU_Core_1V0_...	PLL Voltage crosses turn on trip point, and CPU Core voltage is ON
SMD Step 4	VccAUX_En = 1, VCCIO33_En = 1, VccIO25_En = 1,	Turn on all supplies > VccAUX and VCCAUX on
SMD Step 5	Wait for VccAUX_On_Trip_Point	Wait for VccAUX to reach the trip point to turn all supplies lower than...
SMD Step 6	VCCIO18_En = 1, VCCIO15_En = 1,	VCC IOs lower than VccAUX are on
SMD Step 7	Wait for Vcc12_on_off_Trip_Point AND VccAUX_On_Trip_...	Wait for all supplies to reach their turn-on trip point
SMD Step 8	Wait for VCC_OK AND Vcc12_OK AND VccAUX_OK AND ...	All power supplies should be on within 65 ms otherwise jump to shut...
SMD Step 9	NOP	
SMD Step 10	Wait for 147.46ms using timer 3	All supplies are on, Hold reset active for another 150 ms
SMD Step 11	CPU_Reset = 1,	
SMD Step 12	Wait for NOT VCC_OK OR NOT Vcc12_OK OR NOT VccA...	Wait for any power supply fault
SMD Step 13	Supply_Fault_Intr = 0,	Flag supply fault
SMD Step 14	Supply_Fault_Intr = 1,	Reset the fault and get back to normal operation
SMD Step 15	Wait for 2.05ms using timer 4	Wait for processor complete interrupt processing
SMD Step 16	Begin Shutdown Sequence	
SMD Step 17	Vcc_En = 0, VCCIO18_En = 0, VCCIO15_En = 0, CPU_R...	Turn off VCC and the voltages lower than VCCAux
SMD Step 18	Wait for NOT VCC_PWR_On_Off_Trip AND NOT VCC_I...	Wait for core voltage and voltages lower than auxiliary voltages ar...
SMD Step 19	Vcc12_En = 0, VccAUX_En = 0, VccIO25_En = 0,	Turn off all supplies
SMD Step 20	Halt (end-of-program)	

Figure 4 – Board Level Power Management Algorithm

Because the entire algorithm is implemented in software, it can be modified easily to meet changing power management needs. The source code for this design can be obtained by contacting techsupport@latticesemi.com

Summary

POWR1014: The Ideal Power Supply Manager for the LatticeSC

FPGA & Circuit Board

The POWR1014 device is a single-chip solution for power supply sequencing, CPU-Reset generation, monitoring power supply voltages for fault and watchdog timer. Because all these functions are implemented in software, the POWR1014 device can be used across a wide variety of circuit boards with software changes to implement board-specific power management algorithm requirements.