



MachXO PLDs in System Control Designs

A Lattice Semiconductor White Paper
October 2009

Lattice Semiconductor
5555 Northeast Moore Ct.
Hillsboro, Oregon 97124 USA
Telephone: (503) 268-8000
www.latticesemi.com

Introduction

Temperature measurement, current monitoring, power supply sequencing, fan control and fault logging are typical board control functions used in complex circuit designs. System designers are faced with continual pressure to meet their development schedules, and need to implement control functions with minimal effort and risk while maintaining maximum flexibility. By using a programmable-based approach for their designs, designers can accelerate their time-to-market, address system cost and space reduction and ensure a high level of product differentiation.

The following are the general evolving trends in system control applications.

Thermal Management for Improved System Reliability

Due to environmental, cost and reliability concerns, designers need to minimize the total power dissipation of their system. Lower operating power requires fewer board components, which reduces the total system cost. However, as process geometries migrate to smaller nodes for faster performance and lower cost, the power consumption of the device increases. This causes total system power to increase, which in turn decreases the mean time between failures (MTBF) of other devices on the board, thereby affecting overall system reliability.

To address these concerns, designers are increasingly using sophisticated techniques to control power and temperature in their designs. Common approaches include dynamically adjusting the frequency, voltage and airflow dependent on the system load and operating conditions.

Environmental Monitoring for Early Device Failures

In addition to actively managing power, frequency and airflow, there are a number of benefits to monitoring and logging environmental conditions such as

temperature and voltage. Changes in these variables can provide an early warning of likely failures. After failure, this information can be useful in debug and repair. Many manufacturers also use this data to determine if a warranty placement is justified or not.

Enhanced Manufacturability and Testability

Boundary scan, as defined by the IEEE 1149.1 standard, is a standard method for testing interconnects, monitoring pin states, or testing the logic status of components on a PCB. It is a probeless technique that allows the testing of hardware via JTAG commands.

Generally, designers JTAG test one board at a time. However, as systems become more complex, with multiple boards to support high levels of functionality, testing long chains poses a number of challenges. A failure on one chain can cause the entire system to become non-testable as fault detection and isolation can be quite difficult. Also, physical routing while trying to balance skew and voltage translations between different devices can be challenging.

Reducing System Downtime

Updating logic while devices are deployed in the field continues to be important as it provides designers the flexibility to respond to changing standards, fix bugs, upgrade existing equipment and minimize system downtime. Systems are typically placed in a non-operational mode while the logic is being updated. However, system manufacturers are under increasing pressure to increase system up-time. In fact, in many system control applications, the demand for “5 nines” (99.999%) up-time is a common requirement.

Implementing System Control Using MachXO PLDs

Many designers are using MachXO™ PLDs to implement system control functions in their systems. Aspects of MachXO PLDs that make them particularly well suited for these applications include:

- Low cost
- Simple single chip solution with on-chip Flash
- Operation possible from a single 3.3-V power supply
- Distributed and block memory
- PLLs
- Flexible I/O supports common LVCMOS interface standards

The following sections discuss how MachXO PLDs can be used to address the trends outlined in the previous section.

Thermal Management for Improved System Reliability

MachXO PLDs are ideal for feedback control operations due to their key benefits:

- Ability to power up in less than 1ms, enabling precise control during system boot-up
- Single 3.3V core supply allows it to be run off an auxiliary power rail, which is typically the first rail to be brought up during a power cycle
- High I/O count for monitoring and controlling many signals to multiple devices

For example, to implement temperature-based fan control, the MachXO PLD, in conjunction with the I2C temperature, PWM controller reference designs and a MOSFET, can be used to control the speed of the fan, which enables temperature regulation within a system without the need for an external sensor.

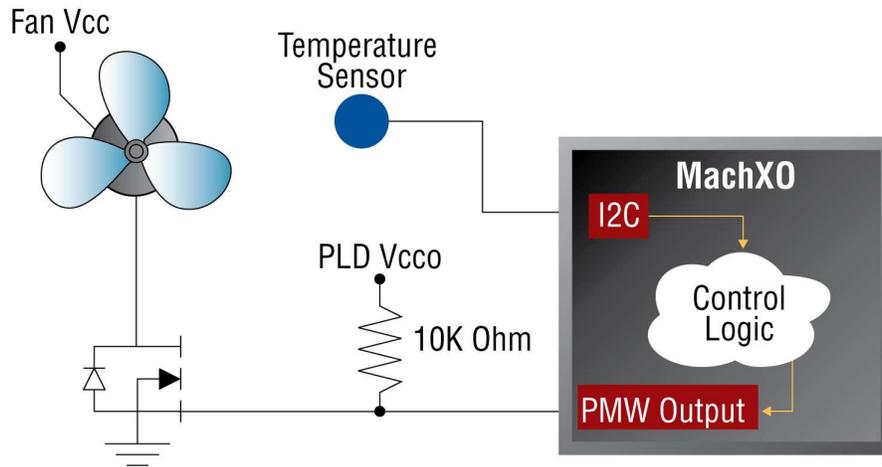


Figure 1 – Fan Control Using MachXO PLD

Using MachXO PLDs to Maintain Environmental Logging

MachXO PLDs, when used in conjunction with Power Manager II POWR1014A and SPI Flash memory, provide a solution for logging environmental variables such as temperature and voltage. Systems can be designed to continuously log data or to log data only when predefined limits have been exceeded. Figure 2 shows a block diagram of the fault logging design using the MachXO PLD. In this example, the fault log can be interrogated via the serial port.

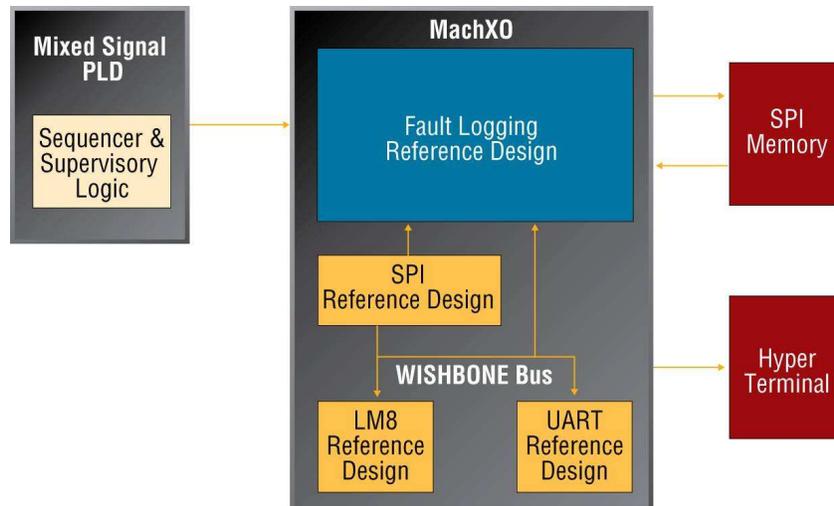


Figure 2 – Using MachXO PLD for Logging Environmental Data

Using MachXO PLDs to Improve JTAG Testability

By using the free downloadable BSCAN1 and BSCAN2 linker reference designs from the Lattice website, designers can break up long JTAG chains and isolate faults. Board routing is simplified, and voltage level translation between different chains can also be easily implemented. This allows for simpler testing of complex systems, resulting in a zero cost, risk free design.

Figure 3 shows an example of a JTAG chain partitioning using the BSCAN2 linker reference design in Lattice's MachXO PLD. In this example, an FPGA, CPLD and an ASIC device comprise one 3.3V chain. A lower voltage 1.8V chain is assembled in a second chain, consisting of an ASIC and another FPGA. A third chain contains processor devices, specifically separated from other components. The final chain in this example is used to isolate one ASIC device that has been determined to have some special requirements or restrictions. After defining the chain partitions and making connections accordingly, the overall chain is now configurable through the BSCAN2 register control. Any combination of sub-chains can now be enabled.

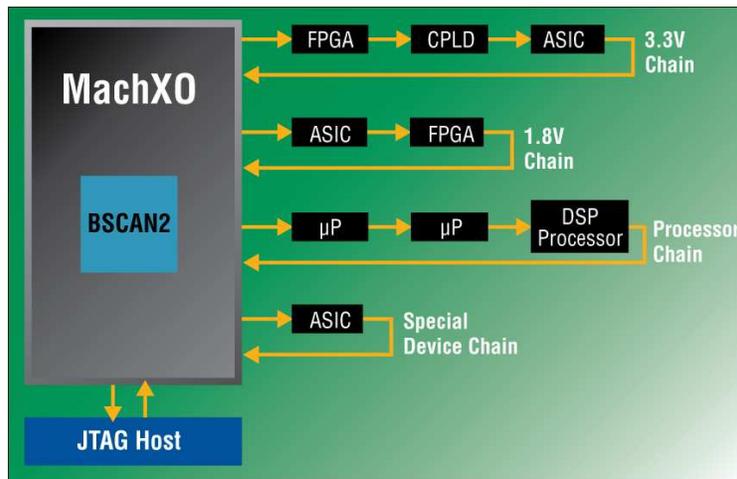


Figure 3 – Using MachXO PLD to Break Up Long JTAG Chains

Voltage Monitoring Using Delta Sigma ADC

Designers need to monitor various sensors and power rails of a system and typically use discrete ADCs to implement this function. Delta Sigma ADC is an efficient and cost effective way to replace discrete ADCs and monitor voltage fluctuations on a board. The Delta Sigma ADC can be implemented using an analog comparator, low pass RC filter, Successive Approximation Register (SAR) technique and a delta-sigma DAC. An analog input signal is tracked and converted to a digital value. The design can be implemented using the MachXO PLD. Designers can modify parameter values to define the bit precision and adjust the sampling rate of the ADC. Figure 4 shows how a MachXO PLD can be used to implement voltage monitoring using Delta Sigma ADC.

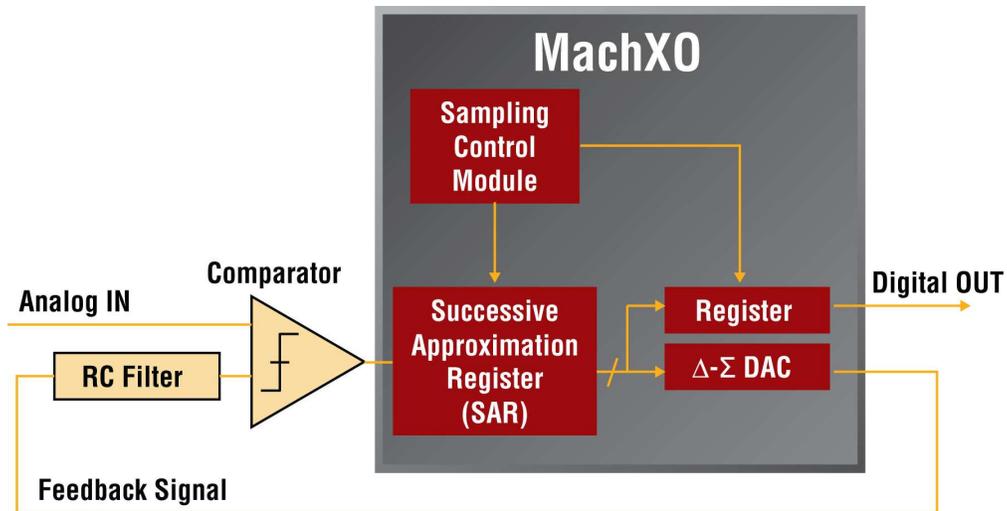


Figure 4 – Voltage Monitoring Using MachXO and Delta Sigma ADC implementation

Remote Field Upgrade

Using Lattice’s TransFR™ technology, the Flash memory in MachXO PLDs can be programmed in the background while the device continues to operate. The new configuration file can be loaded into the SRAM logic, enabling remote field upgrades and minimizing system downtime. Alternatively, toggling the sleep pin (SLEEPN) in MachXO PLDs can be used to load a new configuration file into the SRAM logic without having to cycle the power. The sleep pin is also useful in power sensitive applications, and controls the power down or sleep mode of the device. Using the sleep pin, the static power of the MachXO PLD is less than 100 microamps.

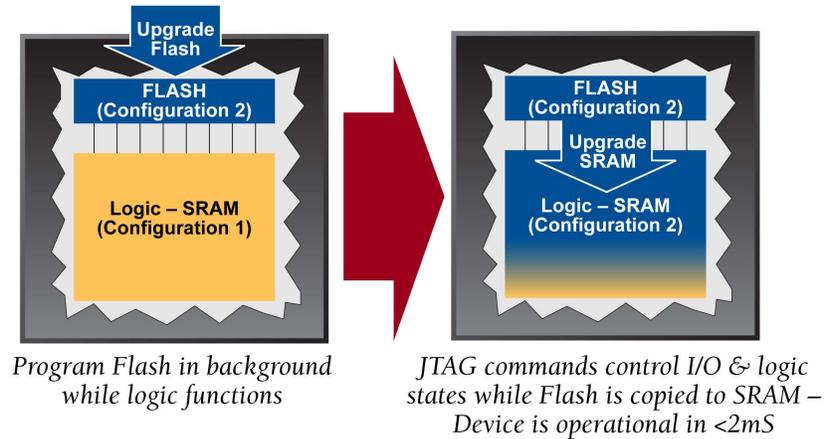


Figure 5 - TransFR operation using MachXO PLDs

MachXO Control Development Kit and Reference Designs

The MachXO Control Development Kit provides a complete platform for rapidly prototyping system control designs with MachXO PLDs. Using the pre-loaded control system-on-chip (Control SoC) design that demonstrates board control functions, including fan speed control based on temperature monitoring, LCD control and complete power supply monitoring and reset distribution in conjunction with the Power Manager II POWR1014A and 8-bit LatticeMico8™ microcontroller. It integrates several Lattice reference designs, including the LatticeMico8 microcontroller, PWM fan controller, LCD controller, SRAM controller, I2C controller, SPI Flash memory controller and a UART peripheral.

Using the Control SoC design, users test these functions within minutes and then build designs using the free downloadable reference design source codes, implementing these features in less than an hour. The board can be controlled with switches and a menu driven interface via a Windows or Linux terminal program over an RS-232/USB link.

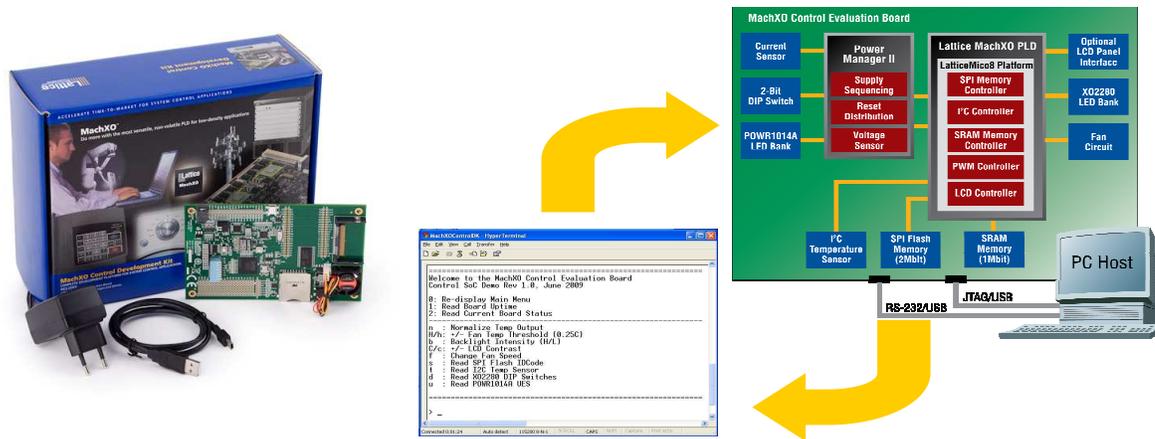


Figure 6 - MachXO Control Development Kit & Evaluation Board

A comprehensive suite of popular reference designs optimized for control and interface bridging applications can be downloaded for free from the Lattice website. The available reference designs include support for protocol and connectivity standards such as I2C, SPI, UART, PCI, power fault logger and delta sigma ADC. Table 2 shows the list of available reference designs for the MachXO PLD family.

#	RD Number	Name	WISHBONE Compatible	Format	
				Verilog	VHDL
1	RD1062	Power Manager Fault Logger		✓	
2	RD1063	Delta Sigma ADC		✓	
3	RD1040	Compact Flash Controller – WISHBONE Compatible	✓	✓	
4	RD1051	Control Link Serial Interface		✓	
5	RD1014	Fast Page Mode DRAM Controller		✓	
6	RD1038	HDLC Controller (NCD format)			
7	RD1006	I ² C Controller for Serial EEPROMs		✓	✓
8	RD1046	I ² C Bus Controller - WISHBONE Compatible	✓	✓	✓
9	RD1005	I ² C Master Controller			✓
10	RD1054	I ² C Slave / Peripheral		✓	
11	RD1026	LatticeMico8 Microcontroller		✓	✓
12	RD1043	LatticeMico8 to WISHBONE Interface Adapter	✓	✓	✓
13	RD1053	LCD Controller – WISHBONE Compatible	✓	✓	

14	RD1049	LPC Bus Controller		✓	
15	RD1001	Multiple Scan Port Addressable Buffer (BSCAN1)		✓	✓
16	RD1002	Multiple Scan Port Linker - BSCAN 2		✓	✓
17	RD1055	NAND Flash Memory Controller		✓	
18	RD1050	PCI to NOR Flash Interface		✓	
19	RD1008	PCI Target 32-bit/33MHz		✓	✓
20	RD1045	PCI/WISHBONE Bridge		✓	
21	RD1060	PWM Fan Controller		✓	
22	RD1041	Read and Write Usercode		✓	✓
23	RD1048	SD Flash Memory Controller – WISHBONE Compatible	✓	✓	
24	RD1010	SD SDRAM Controller		✓	
25	RD1044	SPI Controller - WISHBONE Compatible	✓	✓	✓
26	RD1011	UART Peripheral			✓
27	RD1042	UART Peripheral – WISHBONE Compatible	✓	✓	✓

Table 1 - Reference designs optimized for the MachXO PLD family

The reference design source, including HDL, firmware and design tools, can be modified depending on the application requirement. For more information about the reference designs, visit www.latticesemi.com/ip

Summary

MachXO PLDs are ideal for implementing system control functions such as temperature measurement, current monitoring, power supply sequencing, fan control and fault logging, commonly found in wireless infrastructure, high end computing, industrial and medical applications. They provide several key system integration benefits that ultimately reduce total system cost. The MachXO Control Development Kit and free downloadable reference designs provide designers a comprehensive and flexible solution to accelerate their system control designs quickly and effectively.

###