



Introducing the Lattice Avant™ Platform: Designed for the Mid-Range

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Intro

FPGA products are well known to the design engineer, having been part of their electronics arsenal for decades. FPGAs are generally differentiated in terms of logic density, using the basic unit of logic known as a logic cell (LC). The market can be viewed as stratified into three specific ranges roughly delineated by LC count, high-end, mid-range and small. Although the delineations slowly change over time, today many categorize the high-end as more than 500k LCs; the mid-range as 100k to 500k LCs; and small, with fewer than 100k LCs.

From an architectural perspective, the mid-range FPGA space has long been treated by many FPGA suppliers as an afterthought, which is surprising as it has become a sweet spot for countless embedded, industrial, automation, and robotics applications, just to name a few. An argument can be made that it has been nearly a decade since the last true mid-range FPGA has been released.

Recognizing the need for mid-range FPGAs, suppliers often use a “waterfall” concept to deliver these products. Basically, taking architectures optimized for the high-end and applying them to the mid-range. While these products do fill the mid-range gap, they are far from optimized for that space. They carry the baggage of an architecture that was designed to support up to 10x greater logic densities. While this strategy may be good for the FPGA supplier, that same argument can't be made for the mid-range FPGA customer.

Filling the Need

What's really needed is a mid-range FPGA architected for the mid-range, not some adaptation from above or below. Enter the Lattice Avant™ platform, architected from the ground up for the mid-range. As compared to existing FPGAs serving the mid-range FPGA segment, the Avant platform features:

- Lower power than similar class competitive devices
- Significantly smaller package footprints compared to similar class competitive devices
- Higher DSP performance, supporting the demands of the latest AI algorithms than similar class competitive devices
- 25 Gbps SERDES
- DDR3L/DDR4/LPDDR4 and DDR5 support
- Next-generation security
- Enhanced reliability

Lattice Semiconductor has a history of producing low power FPGAs that are optimized for the small density market. In fact, Lattice out-ships (in terms of unit volume) all other traditional FPGA vendors combined. Now, the company is making its mark at the mid-range with the Avant platform. With Avant, designers gain access to the same low power, density-optimized product concept they expect from Lattice, at a much higher capacity. The result is a device family with high-end features, but with mid-range (and low-end) form factors and power levels.

The potential application list for the Avant FPGA Platform is a lengthy one. In the Industrial space, it could include networking controllers, PLCs, Edge computers, machine vision, and Industrial robotics. It's also valuable for Automotive networking and software-defined radio, thanks to its DSP performance.

General wireless Communications, indoor 5G small cells, and 5G fronthaul applications are also potential landing places for this platform.

Avant implements a range of high-bandwidth I/O standards, such as PCIe® Gen4, and LPDDR4 and DDR5, and provides ample DSP and workload acceleration horsepower. Supported clock rates range up to 350 MHz for the FPGA fabric and 625 MHz for embedded RAM blocks and DSP multiply/accumulate blocks. The devices are the industry's smallest form factor FPGAs to offer 25 Gbps SERDES capability compared to similar class competitive devices.

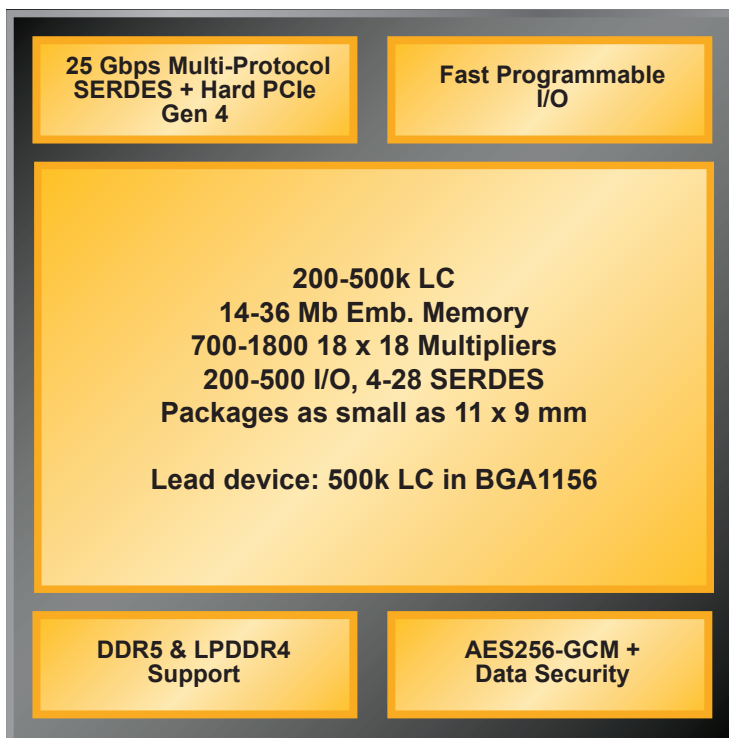


Figure 1

Sufficiently Secured

As with any new embedded design, security must be top-of-mind. To that end, the Lattice engineers were sure to include a wide range of security capabilities in the Avant platform, such as AES256-GCM, ECC, RSA, anti-tamper, and a Physically Unclonable Function (PUF). These capabilities enable configuration and user-data to be both encrypted and authenticated, providing a high level of assurance that the FPGA is safe from malicious attacks. Soft error detection and correction ensure that environmental effects that cause soft errors are detected quickly so appropriate actions can be initiated.

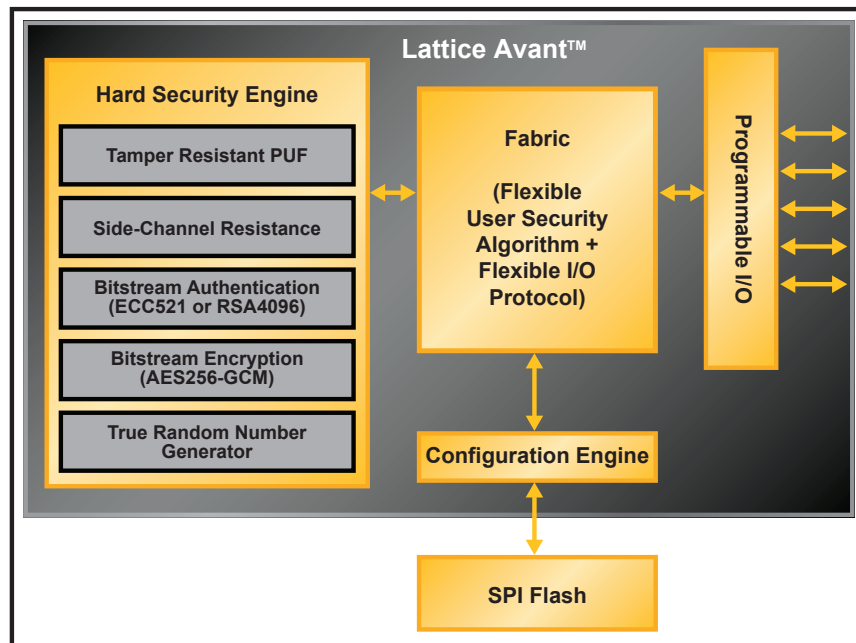


Figure 2

The FPGA's configuration bitstream is protected through authentication and encryption, and user-mode security is implemented through hardened crypto engines accessible as IP blocks embedded in the FPGA fabric. Anti-tamper features resistant to side-channel and fault-injection attacks are implemented through zeroization of keys and sensitive data.

In addition to the strong security, Lattice Avant devices are designed to be robust against transient soft-error failures that are sometimes induced by alpha particle emissions. Detection and recovery from a single-event upset needs to transpire quickly to maintain system up-time and reliability.

Minimizing Power Consumption

One strategy that was employed to reduce power consumption in the Lattice Avant platform was to use a four-input LUT as opposed to six-input LUT for logic implementation. The four-input LUT requires just 16 SRAM configuration bits to program the LUTs as opposed to the 64 SRAM configurations bits required by the six-input LUT.

Another area of power optimization comes through careful consideration in reducing high-capacitance nets. Higher fanout internal nets incur more capacitance through higher drive strength buffers connected to higher capacitance metal wiring. The Lattice Avant architecture utilizes small multiplexers and reduced fanout nets to decrease power consumption. It's also worth noting that the Lattice Avant devices are manufactured in a 16nm FinFET process technology that's optimized for low leakage.

Rich Architecture

Ample DSP blocks are paramount for a wide range of signal processing and AI functionality in mid-range FPGAs. The Lattice Avant devices offers up to 1800 18-by-18 multipliers operating fully pipelined at a frequency of 625 MHz. The DSP blocks can also operate as three 9-by-9 or four 8-by-8 multipliers, with an 18-bit pre-adder and 48-bit accumulator. These configuration modes easily outpace conventional offerings. In addition, multipliers can be cascaded in 27-by-18, 36-by-18, 27-by-27, or 36-by-36 configurations.

I/O flexibility is a cornerstone of the Lattice Avant architecture. The FPGA offers SERDES and parallel I/O standards that address a wide variety of applications. In terms of SERDES standards, the list includes PCIe Gen 4, 25G Ethernet, DP/eDP, SLVS-EC, CoaXPress, JESD204B/C, eCPRI/CPRI, RoE, and SyncE. In addition, to accelerate implementation of PCIe, a hardened PCIe controller is provided. The GPIO support a variety of interfaces including LVCMOS 0.9 to 3.3V, 1.8 Gbps MIPI D-PHY, 1.6 Gbps LVDS/subLVDS, I3C, SGMII, and LVDS 7:1.

Internal embedded memory is organized in 36-kbit blocks, and supports single port, pseudo dual port (1R1W), true dual port (2RW), and ROM configurations. Lattice Radiant® software memory compilers can assemble and place/route internal memory blocks as large as 64 kbits by 256 bits (16 Mbits total). Memory capacity up to 36 Mbits is provided.

External memory interfaces include DDR4, DDR5, and LPDDR4 (operating at up to 2.4 Gbits/s) along with legacy standards DDR3L (1.866 Gbits/s) and LPDDR2 (1.066 Gbits/s). These implementations are based on a hardened MEMPHY with flexible soft controller. Error correction code (ECC) is supported with a soft memory controller.

Smaller Die, Lower Cost Package

From a packaging perspective, the goal for the Lattice design team was to deliver a smaller die in a lower-cost package, and that's exactly what they achieved. Reaching that goal was made possible by the lower power requirement, which permits the use of the smaller die and lower-cost packaging, down to 11x9 mm for 200k logic cells and 15x13 mm for 500k logic cells.

The Lattice Radiant and Lattice Propel™ tools are powerful yet intuitive, and enable users to develop their FPGA applications efficiently and effectively with fast design starts and precise implementation. That includes compiler optimizations and analysis to achieve fast and predictable design convergence. This is achieved using a unified design database, design constraints flow, and timing analysis throughout the flow.

Lattice Avant offers a full suite of IPs to support the platform. Some are offered in hardened (custom logic) configurations for optimized area and performance, while others are offered in soft format (through the use of logic cells) for maximum flexibility. PCIe is an example of hardened IP, whereas external memory interfaces are partially hardened with the MEMPHY and a soft controller. And keep in mind that the soft cores don't consume any space if they aren't used.

Designed For the Midrange Out of the Chute

The Avant Platform has been designed from the start to service the mid-range FPGA market. Lattice's investment in this area has enabled a platform with power, size, and performance leadership. This leadership is further enhanced with a modernized set of features to enable connectivity using the latest interface standards. The platform is supported by Lattice's Radiant and Propel design tools that enable existing Lattice customers to leverage their tool usage knowledge. The platform is also supported by a wide range of IP and development boards.

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