



Tri-Rate SDI PHY IP Loopback and Passthrough Sample Designs

User's Guide

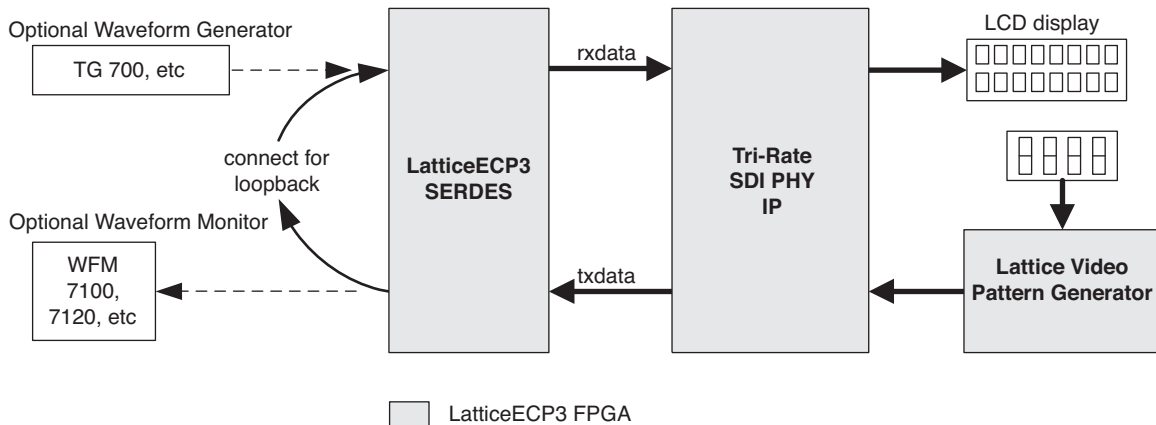
Introduction

When the Tri-Rate SDI PHY IP core is generated using IPexpress™, two sample top-level designs are created. The designs, named “loopback” and “passthrough”, are created under <project_dir>/sdi_eval/impl/<synplify/precision>/loopback and <project_dir>/sdi_eval/impl/<synplify/precision>/passthru respectively. Further information about these two designs is given in the following sections. The designs can be implemented directly on the LatticeECP3™ Video Protocol Board (VPB) if the IP was created using the default parameters in the IP GUI. The LatticeECP3 VPB has the LFE3-95E-7FN1156CES device on it. If one or more parameters are changed in the IP GUI, the sample designs can still be used, but may require some changes depending on the parameters used to configure the IP.

Loopback Design

The loopback design is meant to test the transmit (Tx) and receive (Rx) logic of the IP without the help of an external SDI source or sink. The design includes the Lattice video pattern generator module in FPGA logic, LatticeECP3 SERDES PCS and a character LCD display interface in addition to the IP. The loopback scheme is shown in Figure 1.

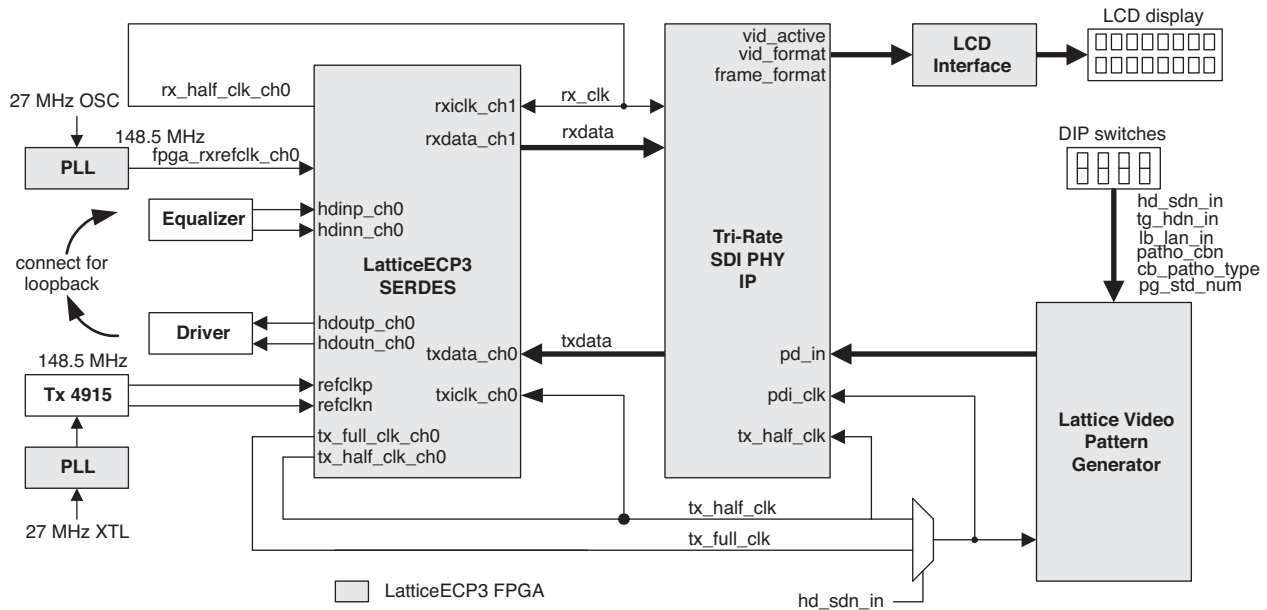
Figure 1. The Loopback Scheme



A waveform monitor and/or a waveform generator can be optionally used instead of the loopback cable to monitor and/or source the SDI video. All the transmit functions and most of the receive functions of the IP can be tested with the loopback setup. One major output that is not tested using a loopback cable connection is the actual parallel received data and its relative timing to other status outputs. The passthrough design can be used to test the received video data.

The loopback design is designed for and tested on the VPB that includes the LatticeECP3-95E-7, 1156-ball fpBGA package, commercial grade silicon. A detailed block diagram of the loopback design is shown in Figure 2.

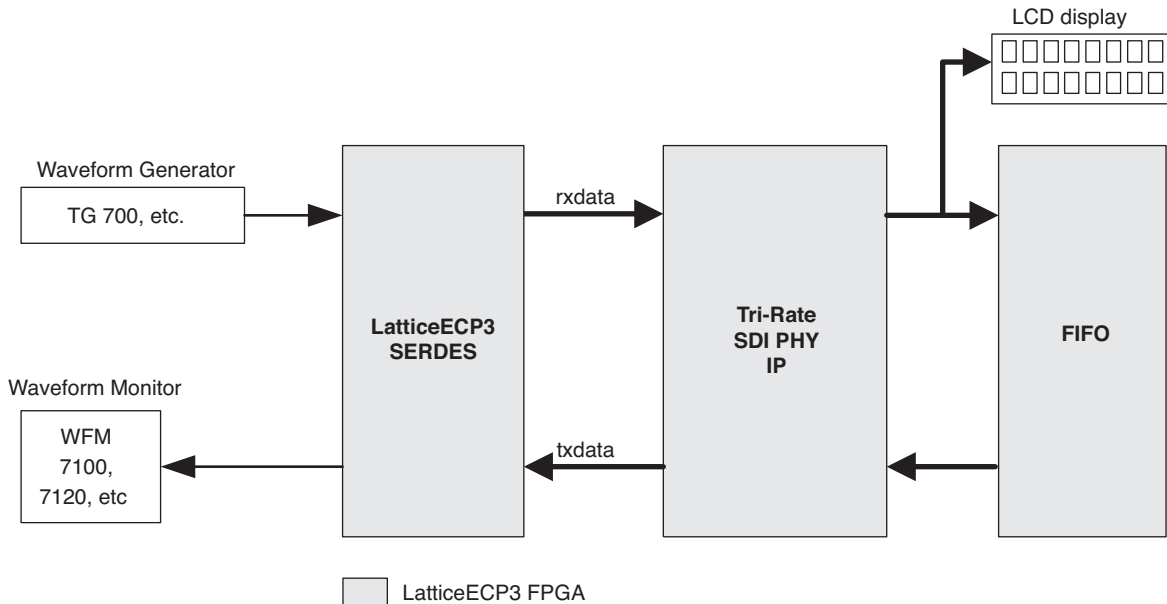
Figure 2. Block Diagram of the Loopback Design



Passthrough Design

The passthrough design is set up to receive video from a standard SDI source and re-transmit it through the IP to a SDI monitor. This design does not use a pattern generator in the FPGA. The passthrough scheme is shown in Figure 3.

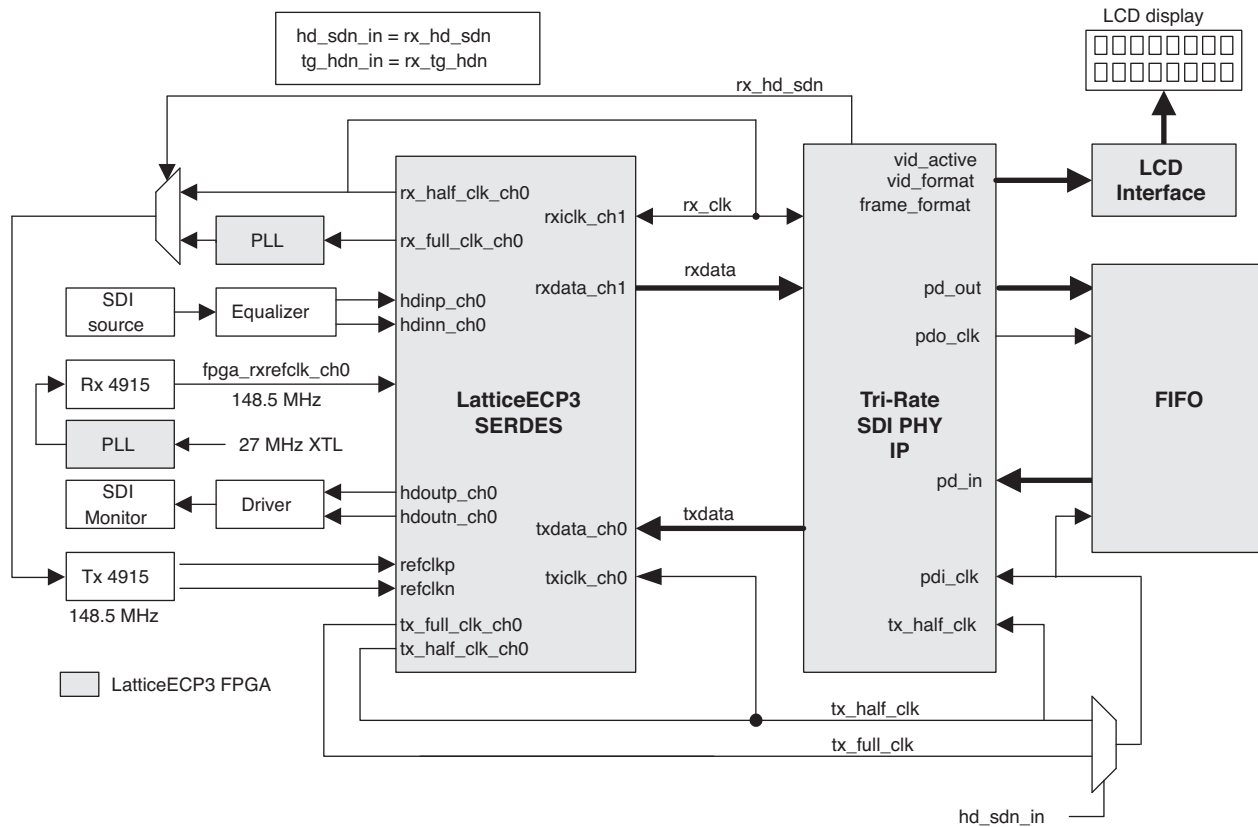
Figure 3. The Passthrough Scheme



As shown in Figure 3, the output data from the receiver is fed to the transmitter through a FIFO. Another major change in passthrough design from the loopback design is the Tx clocking scheme. Since the transmit rate must exactly match the receive rate, the passthrough design uses the recovered clock from the SERDES receiver to

clock the transmit logic. A detailed block diagram of the passthrough design is shown in Figure 4. As shown in the figure, the recovered clock is cleaned up using a GS 4915 clock cleaner and used as the transmit reference clock.

Figure 4. Block Diagram of the Passthrough Design



Simulating the Sample Design

The IP project directory contains the simulation environment to run loopback testing of the IP. The environment includes the testbench, test configuration file and simulation script file. The testbench instantiates the loopback sample design with an additional pattern checker that is enabled for simulation. To simulate the design using the Aldec® ActiveHDL® simulator:

1. Open Aldec ActiveHDL.
2. From the menu, select **Tools -> Execute Macro**.
3. Browse to `<project_dir>/sdi_eval/<module_name>/sim/aldec/scripts/<module_name>_rtl.do`.
4. This will start the compilation and simulation. After several minutes, the simulation will end with the test status.

A simulation script is also provided for the ModelSim® simulator.

Testbench and Configuration File

The testbench instantiates and tests the demo design that includes the SDI IP, Lattice video pattern generator and a data checker. The testbench applies a number of different video streams, each spanning a certain number of lines. The total number of video streams to be applied and the rate, standard and number of lines for each video stream are read from the configuration file `sdi_config.mem`. This configuration file can be edited to change the test patterns or their duration. A sample configuration file with comments is shown below.

Sample sdi_config.mem File

(All entries are in binary)

```

00000110      -> Number of video streams to be applied (=6)
101           -> Rate: 000-SD, 001-HD, 011-3Ga, 101-3Gb-DS, 111-3Gb-DL
00111        -> Video Pattern number (refer to Table 1)
000000000100 -> Number of lines of video to apply after lock
011          |
01111        |   Data for video stream 2
000000000100 |
001          |
01100        |
000000000100 |
111          |
01110        |   Data for video stream 4
000000000100 |
000          |
01010        |
000000000100 |
011          |
00010        |
000000000100 |

```

The Lattice video pattern generator module provided with the IP can generate different types of color bar and path-ological patterns. The pattern numbers for different video formats and rates are given in Table 1.

Table 1. Pattern Generator Standards

lb_lan_in	tg_hdn_in	hd_sdn_in	pg_std_num	pg_std_num (Decimal)	vid_format	frame_format	Content
SD							
0	0	0	xxxx0	0	1440 x 486	60i	4:2:2
0	0	0	xxxx1	1	1440 x 576	50i	4:2:2
HD							
0	0	1	xx000	0	1920 x 1035	60i	4:2:2
0	0	1	xx001	1	1920 x 1080	50i, 295M	4:2:2
0	0	1	xx010	2	1920 x 1080	30p	4:2:2
0	0	1	xx011	3	1920 x 1080	60i	4:2:2
0	0	1	xx100	4	1920 x 1080	25p	4:2:2
0	0	1	xx101	5	1920 x 1080	50i	4:2:2
0	0	1	xx110	6	1920 x 1080	24p	4:2:2
0	0	1	xx111	7	1280 x 720	60p	4:2:2
3G-A							
0	1	1	00000	0	1920 x 1080	60p	4:2:2
0	1	1	00001	1	1920 x 1080	50p	4:2:2
0	1	1	00010	2	1280 x 720	60p	4:4:4:4
0	1	1	00011	3	1280 x 720	50p	4:4:4:4
0	1	1	00100	4	1920 x 1080	30p	4:4:4:4
0	1	1	00101	5	1280 x 720	30p	4:4:4:4
0	1	1	00110	6	1920 x 1080	25p	4:4:4:4
0	1	1	00111	7	1280 x 720	25p	4:4:4:4
0	1	1	01000	8	1920 x 1080	24p	4:4:4:4

Table 1. Pattern Generator Standards (Continued)

lb_lan_in	tg_hdn_in	hd_sdn_in	pg_std_num	pg_std_num (Decimal)	vid_format	frame_format	Content
0	1	1	01001	9	1280 x 720	24p	4:4:4:4
0	1	1	01010	10	1920 x 1080	60i	4:4:4:4
0	1	1	01011	11	1920 x 1080	50i	4:4:4:4
0	1	1	01100	12	1920 x 1080	30p	4:4:4, 12 bits
0	1	1	01101	13	1920 x 1080	25p	4:4:4, 12 bits
0	1	1	01110	14	1920 x 1080	24p	4:4:4, 12 bits
0	1	1	01111	15	1920 x 1080	60i	4:4:4, 12 bits
0	1	1	10000	16	1920 x 1080	50i	4:4:4, 12 bits
0	1	1	10001	17	1920 x 1080	30p	4:2:2, 12 bits
0	1	1	10010	18	1920 x 1080	25p	4:2:2, 12 bits
0	1	1	10011	19	1920 x 1080	24p	4:2:2, 12 bits
0	1	1	10100	20	1920 x 1080	60i	4:2:2, 12 bits
0	1	1	10101	21	1920 x 1080	50i	4:2:2, 12 bits
3G-B-Dual Stream							
1	0	1	xx000	0	1920 x 1035	60i	4:2:2
1	0	1	xx001	1	1920 x 1080	50i (295)	4:2:2
1	0	1	xx010	2	1920 x 1080	30p	4:2:2
1	0	1	xx011	3	1920 x 1080	60i	4:2:2
1	0	1	xx100	4	1920 x 1080	25p	4:2:2
1	0	1	xx101	5	1920 x 1080	50i	4:2:2
1	0	1	xx110	6	1920 x 1080	24p	4:2:2
1	0	1	xx111	7	1280 x 720	60p	4:2:2
3G-B-Dual Link							
1	1	1	00000	0	1920 x 1080	60p	4:2:2
1	1	1	00001	1	1920 x 1080	50p	4:2:2
1	1	1	00100	4	1920 x 1080	30p	4:4:4:4
1	1	1	00110	6	1920 x 1080	25p	4:4:4:4
1	1	1	01000	8	1920 x 1080	24p	4:4:4:4
1	1	1	01010	10	1920 x 1080	60i	4:4:4:4
1	1	1	01011	11	1920 x 1080	50i	4:4:4:4
1	1	1	01100	12	1920 x 1080	30p	4:4:4, 12 bits
1	1	1	01101	13	1920 x 1080	25p	4:4:4, 12 bits
1	1	1	01110	14	1920 x 1080	24p	4:4:4, 12 bits
1	1	1	01111	15	1920 x 1080	60i	4:4:4, 12 bits
1	1	1	10000	16	1920 x 1080	50i	4:4:4, 12 bits
1	1	1	10001	17	1920 x 1080	30p	4:2:2:4, 12 bits
1	1	1	10010	18	1920 x 1080	25p	4:2:2:4, 12 bits
1	1	1	10011	19	1920 x 1080	24p	4:2:2:4, 12 bits
1	1	1	10100	20	1920 x 1080	60i	4:2:2:4, 12 bits
1	1	1	10101	21	1920 x 1080	50i	4:2:2:4, 12 bits

Only the integer frame rates (24p, 30p, 60i and 60p) are shown in Table 1, but the corresponding fractional frame rates (23.98p, 29.97p, 59.94i and 59.94p) can be generated by using the fractional clocks (74.175 MHz and 148.35 MHz).

Implementing and Testing the Sample Design

The sample designs can be implemented by simply opening the provided ispLEVER® project files and running the Generate Bitstream Data process in the Project Navigator.

The VPB requires that both the LatticeECP3 and MachXO™ devices on it be programmed for proper operation. The MachXO controls several peripheral devices on the board, including the clock generator and clock cleaner chip sets. The MachXO source, constraint and project files for the loopback and passthrough configurations are created under <project_dir>/sdi_eval/<module_name>/impl/<synplify/precision>/MachXO. Open the MachXO project by double-clicking on the project file and create the bitstream by following the usual process.

Board Switch Assignments for Sample Designs

Both the loopback and the passthrough sample designs use the following reset buttons:

- **Pushbutton switch SW10** – Master reset (both logic and SERDES reset). Depress the switch momentarily for reset.
- **Pushbutton switch SW9** – SERDES Rx reset. Depress the switch momentarily for reset.

The loopback design uses the DIP switches shown in Table 2. The switches have a “0” value when pushed toward the bottom of the board (toward the PCI Express fingers). They take on a “1” value when pushed toward the top of the board (toward the channel link connector).

Table 2. Switch Connections on the VPB

Switch	Name	Description	
SW1-1	hd_sdn_in	Pattern generator transmit rate {lb_lan_in, tg_hdn_in, hd_sdn_in} 000- SD, 001- HD, 011- 3Ga, 101- 3Gb-DS, 111- 3Gb-DL	
SW1-2	tg_hdn_in		
SW1-3	lb_lan_in		
SW1-4	txd_ldr_en	Selects the LDR path for the SERDES output when the transmitted rate is SD. The switch has no effect when transmitting 3G or HD rates. 0 - Selects SERDES path, 1 - Selects LDR path.	
SW3-1	Video Standard	Standard number = {SW4-1,SW3-4,SW3-3,SW3-2,SW3-1}. See Table 1 for the format.	
SW3-2			
SW3-3			
SW3-4			
SW4-1			
SW4-2	patho_cb_type	Color bar or pathological pattern type {SW4-3,SW4-2}.	
		When “patho_cbn”=0	When “patho_cbn”=1
00 – 100% color bar		00 – SDI checkfield	
SW4-3		01 – 75% color bar	01 – Equalizer pattern
		1x – SMPTE color bar	10 – PLL pattern
			11 – Undefined
SW4-4	patho_cbn	Pathological or color bar. 0 – Color bar, 1 – Pathological.	

Note that the pattern generator interprets the lb_lan_in, tg_hdn_in and hd_sdn_in values differently from the IP. The values shown in Tables 1 and 2 are for the pattern generator. For example, the pattern generator differentiates 3G Level-B-DS and 3G Level-B-DL using the values 101 and 111 for {lb_lan_in, tg_hdn_in, hd_sdn_in} whereas the IP identifies all 3G Level-B streams with the value 111.

Transmitter Testing

Connect the transmitter output BNC connector labeled “SDI Tx #0” to an SDI monitor. Set the DIP switches according to the rate and pattern to be transmitted. The selected pattern is displayed in the monitor.

Receiver Testing

Connect an SDI source to the receiver input-BNC connector, labeled “SDI Rx #1”. The received rate and standard are displayed on the character LCD display. If the LCD display unit is not connected, the status can also be read from the LEDs. The LEDs also display the SERDES and CRC error status. Note that the 3G Level-B identified by the IP and displayed in the LCD is based on the format for stream 1 of the 3G video.

The LED status (0 is off, 1 is lit) is shown in Table 3.

Table 3. LED Status Display

LED	Color	Name	Description
D10	Blue	rx_los_ch1	Rx loss of signal (LOS): 0 – No LOS error, 1 – LOS error
D11	Green	rx_lol_ch1	Rx loss of lock: 0 – Rx CDR is locked, 1 – Rx CDR loss of lock error
D12	Orange	crc_error	CRC error detected. 0 – No CRC error, 1 – CRC error
D13	Red	pll_lol	SERDES transmit PLL loss of lock: 0 – PLL locked, 1 – PLL unlocked.
D14	Blue	rx_hd_sdn	Receiver's HD/SD rate status: 0 – SD, 1 – HD.
D15	Green	rx_tg_hdn	Receiver's 3G/HD rate status: 0 – Not 3G, 1 – 3G.
D16	Orange	vid_format	Detected video format output: {D17,D16} 00 – 1440x486/576 01 – 1280x720 10 – 1920x1035 11 – 1920x1080
D17	Red		
D22	Blue	frame_format	Detected frame format output: {D24,D23,D22} 000 – Reserved 001 – 24p or 23.98p or 23.98 psF 010 – 25p 011 – 30p or 29.97p 100 – 50i 101 – 60i or 59.94i 110 – 50p 111 – 60p or 59.94p
D23	Green		
D24	Orange		
D26	Red	vid_active	Video active output: 0 – Receiver not locked to any video, 1 – Locked to video.

LCD Display

There are four display pages in the LCD display as shown below.

Table 4. Display Pages

	Page 0	Page 1	Page 2	Page 3
Line 1	Tx Rate/Format	TX VPID	Rx VPID	Rx PCT
Line 2	Rx Rate/Format			

The display for each of the pages is formatted as given below.

Tx or Rx Rate/Format

T → 3Ga 1080 60i

R → 3Gb 1080 59.9p

TX or RX VPID

T → VP <byte1> <byte2> <byte3> <byte4>

R → VP <byte1> <byte2> <byte3> <byte4>

Rx PCT (Rx Placer error, Crc error, Time)

PCT → <placer error> < crc_error> <time>

Placer error is either a SAV error or an EAV error.

Time is the time elapsed since reset (pushbutton SW8).

Use pushbutton switch SW7 to cycle the LCD display through pages.

Use pushbutton switch SW8 to reset the errors and time.

Loopback Testing

Connect the transmitter output labeled “SDI Tx #0” to the receiver input labeled “SDI Rx #1”. Change the switches to generate different rates and formats and verify the reception at the LCD display. You can also remove the loopback cable and connect the output to a SDI monitor and feed the input from a SDI generator. Note that the Tx and Rx rates and formats are not related to each other and can be selected independently.

Passthrough Testing

Connect a SDI Generator to the input labeled “SDI Rx #1” and a SDI Monitor to the output labeled “SDI Tx #0”. Set the desired rate and pattern in the signal generator and see the same video passed through to the output. The DIP switches are not read in the passthrough mode.

References

- IPUG82 – [Lattice Tri-Rate Serial Digital Interface Physical Layer IP Core User's Guide](#)
- EB39 – [LatticeECP3 Video Protocol Board User's Guide](#)

Technical Support Assistance

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Revision History

Date	Version	Change Summary
April 2009	01.0	Initial release.
October 2009	01.1	Added support for 3G Level-B and VPID insertion/extraction.
		Included fractional frame rate detection logic.
		Added multi-page LCD display including display of CRC/placer errors and time elapsed since reset.
		Used PLL for both Tx and Rx reference clocks.
		Created a common MachXO design for both passthrough and loopback sample designs.