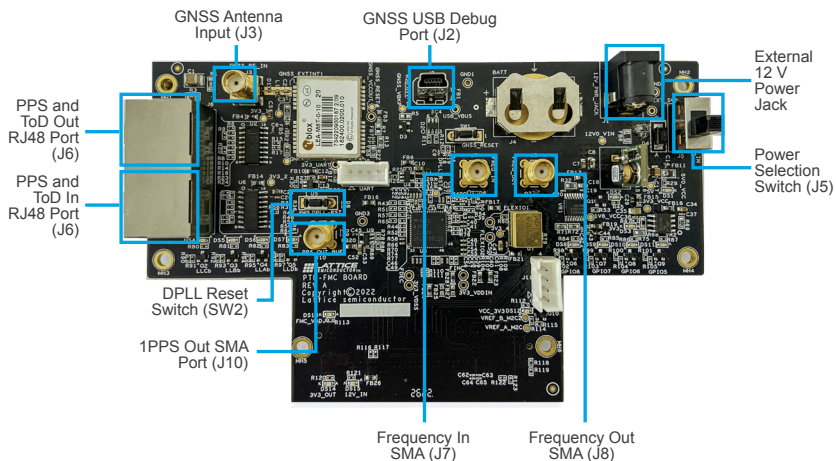
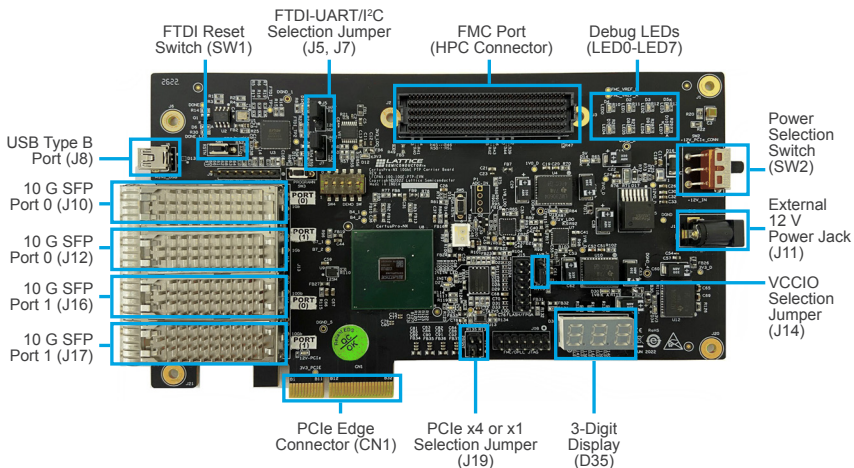


This document provides a brief introduction to the Lattice ORAN Timing and Synchronization Kit.



## 1 Check Kit Contents

The Lattice ORAN Timing and Synchronization Kit contains the following items:

- 1x EVK Mother board
- 1x EVK Daughter board
- 1x Mini-USB to USB-A cable (to flash the firmware and connect the EVK to GUI application on Linux)
- 2x SFP module for the 10G Ethernet
- 2x Fiber Optic cables with 3m length (to connect the EVK over 10G Ethernet)
- GNSS Antenna
- 1x PCIe cable (to connect the EVK PCIe edge connector to a PCIe slot on Linux PC)
- 1x 230 V/120 V to 12 V Adaptor Power adaptor (Optional)

## 2 Computer Requirements

- Linux Ubuntu 20.04 (LTS) (recommended)
- CPU: Core-i3 5th generation or higher with Virtualization ON (if supported)
- RAM: 4GB or higher
- ROM: 120GB or higher
- Secure boot: Disabled (if available)

## 3 FPGA Requirements

- Bit file for the EVK Mother Board (PTP\_1\_8\_44\_hw\_1\_0\_14\_licensed.bit)

## 4 Software Requirements

- Linux software package for the Lattice ORAN V1.1 solution stack (ltpTPEmbeddedSW-x.x-xx.deb).
- Lattice Radiant Software 3.2 or later to flash the firmware.
- Lattice Propel Builder v2022.1

## 5 Powering the Boards and Observing the Demo Program

- Connect a shunt on jumper pins as shown below. The jumpers should be in the indicated configuration.
- Insert two SFP modules for 10G interface into the 10G ports (J16 and J17). And connect the fiber optics cables to the SFP modules.
- Make sure the power switch (SW2) on the mother board is switched to the 12V\_PClE.
- Make sure the power switch (J5) on daughter board is switched to the 12V\_PClE.
- Connect the daughter board to the mother board through the FMC port. Make sure they are firmly connected.
- Connect the mother board PCIe edge connector, through PCIe cable, to the Linux PC PCIe card slot.
- Power on the Linux PC and the EVK shall be powered on.

Part	Description	Settings
J5 (Motherboard)	FTDI- UART or I <sup>2</sup> C selection	Default 1–2 UART, Short 2-3 for I <sup>2</sup> C
J7 (Motherboard)	FTDI- UART or I <sup>2</sup> C selection	Default 1–2 UART, Short 2-3 for I <sup>2</sup> C
J14 (Motherboard)	VCCIO selection for Bank 0	Default short 1-2 for VCCIO=3.3 V, short 2-3 for VCCIO=1.8 V
J19 (Motherboard)	PCIe link selection	Default Short 2-4 for PCIe X4, Short 1-2 for PCIe X1
J13 (Daughterboard)	Clock selection for IN0 input of DPLL	Default 1–2

## 6 Doing More with the Lattice ORAN Timing and Synchronization Kit

Check the Lattice website at [www.latticesemi.com/oran-timing-synchronization-kit](http://www.latticesemi.com/oran-timing-synchronization-kit) to download the full User's Guide, the full source code of the default demo, and other resources. You can use the Lattice Radiant software to develop and program your own demos.

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[www.latticesemi.com/support](http://www.latticesemi.com/support)

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