Lattice Propel 2022.1 Builder

User Guide

FPGA-UG-02177-1.0

November 2022
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Glossary

A list of words or terms specialized in this document.

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<th>Glossary</th>
<th>Definition</th>
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<tr>
<td>BSP</td>
<td>Board Support Package, the layer of software containing hardware-specific drivers and libraries to function in a particular hardware environment.</td>
</tr>
<tr>
<td>CPU</td>
<td>Central Processing Unit.</td>
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<tr>
<td>CSV</td>
<td>Comma Separated Values file.</td>
</tr>
<tr>
<td>DRC</td>
<td>Design Rule Check.</td>
</tr>
<tr>
<td>DUT</td>
<td>Design Under Test.</td>
</tr>
<tr>
<td>ESI</td>
<td>Previous name of Propel.</td>
</tr>
<tr>
<td>FPGA</td>
<td>Field Programmable Gate Array.</td>
</tr>
<tr>
<td>GUI</td>
<td>Graphic User Interface.</td>
</tr>
<tr>
<td>HDL</td>
<td>Hardware Description Language.</td>
</tr>
<tr>
<td>HSM</td>
<td>Hardware Security Module.</td>
</tr>
<tr>
<td>IDE</td>
<td>Integrated Development Environment.</td>
</tr>
<tr>
<td>IP-XACT</td>
<td>An XML format that defines and describes electronic components and their designs.</td>
</tr>
<tr>
<td>LHS</td>
<td>Left Hand Side.</td>
</tr>
<tr>
<td>LSB</td>
<td>Least Significant Bit.</td>
</tr>
<tr>
<td>MSB</td>
<td>Most Significant Bit.</td>
</tr>
<tr>
<td>Perspective</td>
<td>A group of views and editors in the Workbench window.</td>
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<tr>
<td>PGE</td>
<td>Package Generate Engine</td>
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<tr>
<td>Programmer</td>
<td>A tool can program Lattice FPGA SRAM and external SPI Flash through various interfaces, such as JTAG, SPI, and I²C.</td>
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<tr>
<td>RHS</td>
<td>Right Hand Side.</td>
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<tr>
<td>RISC-V</td>
<td>A free and open instruction set architecture (ISA) enabling a new era of processor innovation through open standard collaboration.</td>
</tr>
<tr>
<td>SBX</td>
<td>The files that store the spatial index of the features</td>
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<td>SDK</td>
<td>Embedded System Design and Develop Kit. A set of software development tools that allows the creation of applications for software package on the Lattice embedded platform.</td>
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<tr>
<td>SoC</td>
<td>System on Chip. An integrated circuit that integrates all components of a computer or other electronic systems.</td>
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<tr>
<td>SRAM</td>
<td>Static Random Access Memory.</td>
</tr>
<tr>
<td>TCL</td>
<td>Tool Command Language.</td>
</tr>
<tr>
<td>UFM</td>
<td>User Flash Memory.</td>
</tr>
<tr>
<td>VIP</td>
<td>Verification IP.</td>
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<tr>
<td>Workspace</td>
<td>The directory where stores your work, it is used as the default content area for your projects as well as for holding any required metadata.</td>
</tr>
<tr>
<td>Workbench</td>
<td>Refers to the desktop development environment in Eclipse IDE platform.</td>
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1. Introduction

Lattice Propel™ 2022.1 Builder is a graphical tool used to assemble complex System-on-Chip (SoC) modules which can be used in the supported Lattice FPGA devices. These modules and/or IP can be assembled and connected easily by simply dragging and dropping the modules and/or IP into the Schematic Window.

1.1. Purpose

Embedded system solutions play an important role in FPGA system design allowing you to develop the software for a processor in an FPGA device. It provides flexibility for you to control various peripherals from a system bus.

To develop an embedded system on an FPGA, you need to design the System on Chip (SoC) with an embedded processor. Lattice Propel Builder helps you develop your system with a RISC-V processor, peripheral IP, and a set of tools by a simple drag-and-drop.

The purpose of this document is to introduce Lattice Propel 2022.1 Builder tool and design flow to help you quickly get started to build a small demo system. You can also find the recommended flows of using Lattice Propel Builder in this document.

1.2. Audience

The intended audience for this document includes embedded system designers and embedded software developers using Lattice MachXO3D, MachXO3L, MachXO3LF, MachXO2, LIFCL, LFD2NX, LFMNX, LFCPNX, LFMXO5, and LAV-AT devices. The technical guidelines assume readers have expertise in the embedded system area and FPGA technologies.
2. **Lattice Propel Builder Design Flows**

The Propel Builder design flow includes creating a SoC project design flow, and verification design flow, which are discussed in detail in the following sections.

2.1. **Builder Environment**

After Propel 2022.1 is installed, you can launch the stand-alone Propel Builder by double-clicking the Builder icon to launch Builder. Refer to the [Lattice Propel 2022.1 Installation for Windows User Guide (FPGA-AN-02056)](https://www.latticesemi.com/legal) for details on the installation. After the Propel Builder is launched, a single workbench window is displayed. The workbench contains Menu, Toolbar, Design View, IP catalog, Schematic view, address mapping, Start Page, and TCL console. Figure 2.1 shows the workbench with opening a project.

1. Menu bar
2. Toolbar
3. IP Catalog and Design View
4. Schematic View, Address Mapping, and Start Page
5. TCL Console

![Propel Builder Workbench Window](image)
2.2. Project Design Flow

2.2.1. Creating a New SoC Project

1. Choose File > New Design from the Lattice Propel Builder Menu bar. The Create System Design – Design Information wizard opens (Figure 2.2).

![Figure 2.2. Create System Design – Design Information Wizard]

2. The default Project Type is displayed in the Type field.
   - You can select SoC Project from the drop-down menu, if you need to create a SoC project.
   - You can select SoC Verification from the drop-down menu, if you need to create a verification project. Refer to the Verification Project Design Flow section for more details.

3. Enter the desired project name in the Name field.

4. (Optional) The default location is shown in the Location field. Use the Browse... option to change the project workspace location.

5. Click Next. The Create System Design - Configure Propel Project wizard opens (Figure 2.3).
6. (Optional) The default Verilog is displayed in the **Language** field. Use the drop-down menu to change the default language.

7. Specify a device or a board.
   - To specify a device for your new SoC project, use the drop-down menu to select desired device information (Family, Device, Package and Speed), and select Empty Project in the **Templates** field (Figure 2.4).
Figure 2.4. Specify a Device for a New SoC Project

- Or, to specify a board for a new SoC project, check the Board option (Figure 2.6).

Figure 2.5. Specify a Board for a New SoC Project
• The Configure Propel Project wizard is shown (Figure 2.7). From the Board Select area, select the desired board, such as CertusPro-NX Evaluation.

![Configure Propel Project wizard](image)

Figure 2.6. Specify a Board for a New SoC Project

8. Click Next. The Project Information wizard opens (Figure 2.7).

![Create System Design – Project Information Wizard](image)

Figure 2.7. Create System Design – Project Information Wizard

9. Check and confirm the project information.

10. Click Finish. Propel Builder GUI opens (Figure 2.8).
2.2.2. Creating Template SoC Project

Templates are customized with common-used programs as well as pre-defined family, device, package, speed and operating condition. This HelloWorld template is programmed to run HelloWorld demo. You can make changes based on this template.

1. Choose File > New Design from the Lattice Propel Builder Menu bar. The Create System Design wizard (Figure 2.9).opens
2. The default Project Type is displayed in the **Type** field. Select **SoC Project** from the drop-down menu.

3. Enter a project name in the **Name** field, such as **HelloWorld**.

4. (Optional) The default location is shown in the **Location** field. Use the **Browse...** option to change the project workspace location.

5. Click **Next**.

6. From the Configure Propel Project wizard, you can specify a device or a board for a Template SoC project (**Figure 2.10**).
• To specify a device for your new Template SoC project, use the drop-down menu to select desired device information (Family, Device, Package and Speed), and select Hello World Project from the Templates field (Figure 2.11).

Note:
Different device families are supported and available in Radiant or Diamond software accordingly.
• Available in Radiant software only: LFCPNX (CertusPro-NX)/LFD2NX (Certus-NX)/LMXO5 (MachXO5-NX)/
LIFCL (CrossLink-NX).
• Available in Diamond software only: LFMNX/MachXO2/MachXO3D/MachXO3L/MachXO3LF.

Figure 2.11. Specify a Device for Template SoC Project (2)

• Or, to specify a board for a new Template SoC project, check the Board option (Figure 2.12).
7. The Configure Propel Project wizard is shown (Figure 2.13). From the Board Select area, select the desired board, such as CertusPro-NX Evaluation.

8. Select a desired template from the Templates area, such as Hello World Project (Figure 2.13).
9. Click **Next**. The Project Information wizard opens (Figure 2.14).

![Figure 2.14. Project Information Wizard](image)

10. Check and confirm the project information.

11. Click **Finish**. Propel Builder GUI opens (Figure 2.16).
2.2.3. Opening a SoC Existing Project

1. Choose File > **Open Design** from Propel Builder GUI Menu, or Click **Open Design** icon from Propel Builder Toolbar. The Open sbx dialog opens (Figure 2.16).

![Figure 2.15. Propel Builder GUI showing HelloWorld Template SoC Project](image)

![Figure 2.16. Open Sbx Dialog](image)

2. Browse to find the default project workspace folder or your own project workspace folder. Choose the sbx file, such as HelloWorld.sbx (Figure 2.17).
3. Click **Open**. The Builder GUI shows the SoC design.

Note: Choose **File > Recent Designs** from Propel Builder GUI Menu. You can quickly open a most recently closed project.

### 2.2.4. Adding Modules

After starting a Propel Builder project, you can add modules by dragging them from the IP Catalog view to the Schematic view. The IP Catalog view comes with a large variety of modules for common use and some glue logic modules as well, which can be found from the **IP on Local** tab (Figure 2.18). Click the **IP on Server** tab to find and download more modules for specialized use.

1. (Optional) From the Propel Builder GUI **IP Catalog** area (Figure 2.18), choose the **IP on Server** tab. Select a desired IP. Click the **Install** button. After the IP is installed successfully, the new IP can be shown in the **IP on Local** tab.
From the IP on Local tab, select a desired IP, such as GPIO. Double-click the IP module or drag and drop the IP module to the Schematic view. A Module/IP Block wizard pops up (Figure 2.19).
3. Enter a component name in the Component name area, such as gpio0. Click Next. Module/IP Block Wizard shows the Configure Component from IP gpio Version 1.6.0 page (Figure 2.20).

4. (Optional) Click the Value field. You can enter a desired value for a property, check the checkbox to select a property, or select a desired value from the dropdown menu for a property in the Value area. By changing the value, the properties are thus configured. The property in gray is not configurable.

5. Click Generate. Module/IP Block wizard shows the Check Generated Result page (Figure 2.21).
Figure 2.21. Module/IP Block Wizard - Check Generated Result

6. Select **Insert to project** (Figure 2.21) at the bottom of the Check Generate Result wizard.
7. Click **Finish**. The **Define Instance** dialog box opens (Figure 2.22).

Figure 2.22. Design Instance Dialog Box

8. (Optional) Change the instance name, if desired. Space and special characters are not allowed.
9. Click **OK**. The schematic block for the module appears in the **Schematic** view (Figure 2.23).
2.2.5. Adding Glue Logic

Propel 2022.1 builder supports glue logic modules as well as IP modules. You can add glue logic modules by dragging them from the IP Catalog view (Figure 2.24) to the Schematic view.
Figure 2.24. IP Catalog
• Concat
  a. From the IP Catalog, select the **concat** module. Double-click the concat module or drag and drop concat module to the Schematic view. A Glue Logic wizard (**Figure 2.25**) pops up.

![Figure 2.25. Glue Logic for Concat Module](image)

b. Click the **RHS** field to change the default right-hand side bus width to a desired one. Click the **LHS** field to change the default left-hand side bus width to a desired one. Click the **Add** button to add LHS (Left-hand Side). Click the **Remove** button to remove LHS (Left-hand Side). You can only add or remove LHS but not RHS. LHS and RHS are thus configured.

c. Click **OK**. The schematic block for the concat module in red appears in the Schematic view (**Figure 2.26**).

![Figure 2.26. Schematic View Shows a Concat Module](image)

• Equation
  a. From the IP Catalog, select the **equation** module. Double-click the equation module, or drag and drop the equation module to the Schematic view. A Glue Logic wizard (**Figure 2.27**) pops up.
Figure 2.27. Glue Logic Wizard for Equation Module

b. Click the **Module Name** field to change the default value to a desired name. Click the **Expression** field to change the default expression to a desired one. The expression supports and (&), or (|), negation (!). The module name and expression are thus configured.

c. Click **OK**. The schematic block for the equation module in red appears in the Schematic view (Figure 2.28).

Figure 2.28. Schematic View Shows an Equation Module

- Invert
  
a. From the IP Catalog, select the **invert** module. Double-click the invert module or drag and drop invert module to the Schematic view. The schematic block for the invert module in red appears in the Schematic view (Figure 2.29).
Figure 2.29. Schematic View Shows the Invert Module

- **Rtl**
  
  a. From the IP Catalog, select the rtl module. Double-click the rtl module or drag and drop the rtl module to the Schematic view. A Glue Logic wizard (Figure 2.30) pops up.

  ![Glue Logic Wizard for Rtl Module](image)

  Figure 2.30. Glue Logic Wizard for Rtl Module

  b. You can edit your own rtl module in the **Rtl** area by entering the rtl module function.
c. Or you can use an existing rtl module by checking the **Use Existing File** checkbox. After checking the **Use Existing File** checkbox (Figure 2.31), browse to find the existing RTL module file path from the **Path** filed. And, check the **CopyToDesign** checkbox, if you want to copy the rtl module to the design.

![Figure 2.31. Existing Rtl Module Configuration](image)

Figure 2.31. Existing Rtl Module Configuration

d. Click **OK**. The schematic block for the rtl module in red appears in the Schematic view (Figure 2.32).

![Figure 2.32. Schematic View Shows the Custom Rtl Module](image)

Figure 2.32. Schematic View Shows the Custom Rtl Module

**Note**: Currently, Rtl Module only supports Verilog HDL.
- Split
  a. From the IP Catalog, select the split module. Double-click the split module, or drag and drop the split module to the Schematic view. A Glue Logic wizard (Figure 2.33) pops up.

![Figure 2.33. Glue Logic Wizard for Split Module](image)

b. Click LHS field to change the default left-hand side bus widths to a desired one. Click RHS field to change the default right-hand side bit width to a desired one. Click the [Add] button to add an RHS. Click the [Remove] button to remove an RHS. You can only add or remove RHS but not LHS. LHS and RHS are thus configured.

c. Click OK. The schematic block for the split module in red appears in the Schematic view (Figure 2.34).

![Figure 2.34. Schematic View Shows Split Module](image)
2.2.6. Undo/Redo

Propel 2022.1 Builder supports one-level undo/redo. You can click the Undo icon from Propel Builder Toolbar to go back to last action. Click the Redo icon from Propel Builder Toolbar to recover last undo action.

- **Undo**: Choose **Edit > Undo** from the Lattice Propel Builder Menu bar. Or, click the **Undo** icon from Propel Builder GUI Toolbar.

- **Redo**: Choose **Edit > Redo** from the Lattice Propel Builder Menu bar. Or, click the **Redo** icon from Propel Builder Toolbar.

**Note**: Currently, Propel 2022.1 Builder only supports single undo/redo.

2.2.7. Modifying the Project Settings

Propel 2022.1 Builder supports changing the projects settings. You can modify the device, package, speed and operating conditions by double clicking the device part number from the Design View.

1. Double click the device part number from the Design View (**Figure 2.35**), the Modify Device Info wizard pops up (**Figure 2.36**).
2. Use the drop-down menu to choose the desired device in **Device** filed in the Modify Device Info wizard (Figure 2.36). Use the drop-down menu to change the package, speed and operating condition in **Package, Speed, Operating Condition** filed.

![Figure 2.36 Modify Device Info](image)

3. Click **OK**. The System Builder dialog (Figure 2.37) pops up to show the warning message about configuring all IP.

![Figure 2.37 System Builder Dialog](image)

4. Click **Yes** to configure all IP in current project. The new device part number shows in Design View (Figure 2.38).
2.2.8. Working with the Schematic View

You can make changes in the Schematic view including automatic layout to clean up the display, moving, resizing, renaming blocks manually, highlighting objects and zooming the display in and out.

- To view signal list of block:

  Click the plus sign $+$ of the desired block to see what signals it contains. The plus sign changes to a negative sign $-$ and shows the signal list as shown in Figure 2.39. Click the negative sign $-$ to close the expanded bus. The schematic returns to the previous form.
• To select one or more objects:
  Select one object or more objects in one of the following ways:
  • Click on the object in the Schematic view. The selected object turns to red (Figure 2.40).

![Figure 2.39. Signal List of Modules](image)
Figure 2.40. Select Object

- Ctrl-click or Shift-click in the Schematic view to select more than one objects.
- Click the Area_select icon from the Propel Builder Toolbar. Click and drag to draw a selection rectangle around the modules and ports in the Schematic view. Click the icon again to turn off the Area_select mode.
- From the Schematic view, right-click and choose Select All or press Ctrl-A to select all the objects.
  Note: Ctrl-click or Shift-click on the object in the Schematic view can also de-select the object while leaving the others selected.
- To re-arrange the schematic:
  Propel Builder allows re-arranging the objects in the schematic view. You can re-arrange modules and the ports. Drag objects to re-arrange the schematic. Propel Builder has rules for placing objects to adjust the schematic in an organized arrangement:
  a. Select the desired modules (one or more modules can be dragged at the same time) or ports (one or more ports can be dragged at the same time).
  b. Click on the selected items and drag it to the desired location.
  c. Release the mouse button.
  Note: The selected objects can be moved to the specified location, or as near as the rules allow. Other objects in the schematic can also be moved to accommodate the selected objects’ new location.
- To bring selected objects to the center of the Schematic view using the Locate Object mode:
  a. Click the Locate Object icon from the Propel Builder Toolbar. The background turns to dark gray.
  b. Select the object in the List view of the Design View. The selected object is in the center of the Schematic View (Figure 2.41).
• To automatically simplify the layout:
  Right-click anywhere in the Schematic view and choose **Relayout**.

• To duplicate a module:

  Select the desired module and click **Clone**. Or right-click on the module and choose **Clone**. A copy of the schematic block appears with a new instance name (Figure 2.42).
To restore a deleted module:

a. In the List view of the Design View (Figure 2.43), go to the Components folder. The deleted module can still be found in the List view in plain text. Those not deleted are shown in bold-faced text.

![Design View](image)

**Figure 2.43. Design View**

b. Right-click on the desired component and choose **Instantiate**. The Define Instance dialog box (Figure 2.44) open.

![Define Instance Dialog Box](image)

**Figure 2.44. Define Instance Dialog Box**
c. Enter a name for the new instance.

d. Click OK. The module appears in the Schematic view and the List view of Design Info, and the component name is bold-faced.

- To reconfigure a module:
  a. Double-click the module, or right-click the module. Choose Reconfig. The Module/IP Block wizard (Figure 2.45) opens.

![Module/IP Block Wizard](image)

**Figure 2.45. Module/IP Block Wizard – Configure Component**

b. Configure component (including General property, Main Settings and Mater Priority Settings) at Configure IP table in the Module/IP Block Wizard. Click Generate to generate the module as usual. The schematic block for the module changes to match the new configuration.

**Note:** For a SoC design, if the init file (mem file) of System Memory module instance is updated in a C project, the initialization section of the system memory module instance should be re-configured. Or, use the ECO flow to update the information. Refer to the Diamond online help for more on how to use an ECO flow.

- To resize module blocks:
  a. Select the desired module block. The block is highlighted in red with black corners (Figure 2.46).
b. Click and drag one of the corners to change the size and shape of the block.
c. Release the mouse button. All the other objects move to make room for this block.

*Note:* Right-click the module block and choose Unresize Instance to restore the size of the module block.

There are a variety of methods to zoom within the Schematic view, including toolbar commands and dragging in the Schematic view.

The following commands are available from the Propel Builder Toolbar.

- **Zoom In** (Ctrl++) — enlarges the view of the entire layout.
- **Zoom Out** (Ctrl+-) — reduces the view of the entire layout.
- **Zoom Fit** — reduces or enlarges the entire layout so that it fits inside the window.
- **Zoom To** — enlarges the size of one or more selected objects on the layout and fills the window with selection.

*Note:* The mouse wheel provides a finer zoom control by rolling the mouse wheel forward to zoom in and backward to zoom out while pressing the Ctrl key.

- To zoom by holding the mouse button and dragging.
  - To zoom to fit the window, drag up and to the left. The image adjusts to fill the window.
  - To zoom out, drag up and to the right. The dragging distance determines the amount of zoom. The image is reduced and centered in the window.
  - To zoom in, drag down and to the left. The dragging distance determines the amount of zoom. The image is enlarged and centered in the window.
  - To zoom in in a specific area, start at the upper-left corner of the area and drag to the lower-right corner of the area. The area that dragging across is adjusted to fill the window.

*Note:* Make sure that the Area select icon is not selected in the Toolbar. If you need to use Area select and zoom by dragging frequently, choose Design > Options from Propel Builder menu bar. The Options Dialog opens (Figure 2.47). Select Use right mouse button for zooming actions and click OK. Then you can select an instance using the left mouse button, zoom in or zoom out using the right mouse button, and the Area select icon disappears from the Propel Builder Toolbar.
To move the schematic image within the Schematic view by panning and scrolling:

- To pan the image: Hold down the Ctrl key and the left mouse button while dragging the image.
- To scroll vertically: Rotate the mouse wheel. Or, click in the vertical scroll bar.
- To scroll horizontally: Hold down the Shift key and rotate the mouse wheel. Or, click in the horizontal scroll bar.

To show the connectivity of a module: right-click the module and choose Show connectivity. All nets connected to the module, all pins and ports connected to the nets are highlighted (Figure 2.48).
To highlight an object: select an object and click **Highlight** or, right-click the object and choose **Highlight**. The object is highlighted in blue (**Figure 2.49**). Click **Highlight** again. You can remove highlighting.

To change the name of an object:

a. Select the object from the List view of Design View. Information of the selected object is shown in the Properties area (**Figure 2.50**).
b. Change the name and click Enter. The name changes in the Schematic view and List view of Design Info.

- To print a schematic:
  a. Choose File > Print Preview. The Print Preview window (Figure 2.51) opens.

b. Expand the Print Preview window to the desired size.

c. Click the Page Setup button and adjust the paper size and margins, if necessary.

d. Click the Print button.

e. Adjust the printer settings, if necessary. Click Print.
2.2.9. Connecting Modules

You can connect the pins of modules to other modules or to top-level ports by dragging a line between them or by selecting connection points, or by assigning a constant value to an input pin or bus. Propel Builder does not allow obvious inappropriate connections, such as a connection between two output pins or mismatched buses.

- To connect modules by drawing:
  - Move the cursor to a pin or port. The cursor changes to a pencil icon. Click and hold while dragging to another pin, port, or net. An allowed pin or port shows a green checkmark when you hover over it (Figure 2.52). An allowed net becomes bold when you hover over it (Figure 2.53).

![Figure 2.52. Draw a Pin or a Port](image)

- Click on the pin, port, or net that you want to connect to. If the connection is allowed, a line appears connecting the two objects. Propel Builder creates a path around other objects.

- You can connect multiple ports once. When more than one port are selected (Figure 2.54), click connect from the right-click menu to implement it.
Figure 2.54. Select More than One Ports

- When the net is complete, right-click to leave the drawing mode.

- To connect modules by selecting points:
  - Select the pins, ports, and nets that you want to connect.
  - Right-click one of the selected objects. Choose Connect.

- To connect pins by auto connecting:
  - Right-click a bank and choose Auto Connect (Figure 2.55). The Connect Ports dialog appears (Figure 2.56).
b. By default, **Auto connect** selects all ports. You can also deselect the interface/clock/rest pins that you do not want to auto-connect (**Figure 2.56**).
Auto connect Rules

Auto connect can initialize three types of connections: Clock/Reset connection, Interface connection, and other connection.

- Clock/Reset Connection

For clock/reset connection, you can choose only one clock port and one reset port in the Driver selection area. In the example below, you can choose only one clock port from osc0_inst.hf_clk_out_o, pll0_inst.clkop_o, or pll0_inst.clkos_o, and one reset port from cpu0_inst.system_reset_n_0 or rstn_i (Figure 2.57).
Following are rules of how clock/reset driver port auto connects to the destination.

- Whether or not the SoC project contains a CPU instance.

If the SoC project contains a CPU instance, and the CPU instance has an output clock/reset port, such as cpu0_inst.system_resetn_o (Figure 2.58), the clock/reset of other instances are thus connected to the clock/reset port of the CPU Instance (Figure 2.58).

If the SoC project does not contain a CPU instance, clock/reset on all instances connect to the top clock/reset port. Top clock/reset port is the port such as rstn_i in Figure 2.58.
The output clock/reset port on one instance should not be connected to its own clock/reset input port, for example, `cpu0_inst.system.resetn_o` should not connect to `cpu0_inst.rst_n_i` in Figure 2.58.

- Interface Connection

Bus interfaces can only connect from one interface to another interface. It is a one-to-one relation, not a one-to-multiple relation, and the interfaces must have the same interface type.

In the example below (see Figure 2.59), `cpu0_inst.AHBL_M1_DATA` is a bus interface, and it can only connect to one destination, `ahbl0_inst.AHBL_S00`. Because they have the same interface type: AHBLite. For interface type, you can check the **Bus Type** in Design View (Figure 2.59).

![Figure 2.59. Interface Type of cpu0_inst.AHBL_M1_DATA](image)

Following rules are how interface connect.

If project contains a CPU instance, the interface connection starts from the CPU instance, then to one bus/bridge instance, and then to another bus/bridge instance. After connecting all bus/bridge instances one by one (`cpu0 > ahbl0 > ahbl2apb0 > apb0`), finally connects to other instances (gpio0, uart0). See Figure 2.60 and Figure 2.61.

![Figure 2.60. Interface Connection on from CPU to Bus/Bridge instances in Schematic View](image)
If the last instance connected has the same bus interface type as CPU instance, then it connects back to CPU instance (see Figure 2.62 and Figure 2.63). In Figure 2.64 and Figure 2.65, you can see gpio0_inst.INTR and cpu0_inst.IRQ_S0 have the bus type: Interrupt.
If the project does not contain CPU instance, the interface connection starts from the bus/bridge instance, and then to each bus/bridge instance one by one, and finally connects to the other instances.

**Note:** If the bus interface is an instruction set, such as CPU0_inst.AHBL_M0_INSTR, it does not perform auto-connect.

- Other connection
  - If ports have the same port name, for example, rxd_i and uart0_ins.rdx_i, they are connected.
- To assign a constant value to an input pin:
  - Select the desired pin and right-click the pin. Choose Assign Constant Value (Figure 2.66).
b. A small dialog box appears (Figure 2.67). Enter the desired value. To erase the value and start over, click X. For all buses (more than one pin), the format is hexadecimal. Make sure the value fits the number of pins in the bus. For example, a 3-pin bus can accept 0-7, but not 8.

- Usually, disconnecting modules just means deleting a net. If the net has multiple branches, just delete one branch, leaving the rest of the nets intact.

  - To disconnect one branch of a net, right-click the pin of that branch and choose Disconnect. The branch going to that pin disappears.
  - To disconnect a whole net, right-click the net and choose Delete. The whole net is deleted.
2.2.10. Creating Top-Level Ports

With multiple modules in a Propel Builder project, top-level ports need to be created for a complete Propel Builder module. You can create a top-level port either manually or automatically.

For input ports that connect to more than one pin, such as for clock and reset signals, the manual way is more convenient than the automatic way. If the port names automatically-generated need to be changed, the manual way is better.

For other pins, the automatic way is usually preferred. The automatic way enables you to create the appropriate port type and connect net simultaneously. The automatic way can also create multiple ports at the same time.

The automatic way of creating ports is the most effective. If all the modules are selected, Propel Builder can automatically create ports for all the remaining unconnected pins for selected modules in one step.

- To create a port for a pin or bus manually:
  a. Right-click in the Schematic view, and choose Create Port. The Create Port dialog box pops up (Figure 2.68).

  ![Create Port Dialog Box](image)

  Figure 2.68. Create Port Dialog Box

  b. Enter a name for the port in the Name field.
  c. Choose a direction for the port, such as Input in the Direction field.
  d. Choose the port type from the Type field. The default type is General.
  e. (Optional) Select the Bus Options. Enter the number for the most significant bit (MSB) and the least significant bit (LSB). These two options define the bus width.
  f. Click OK. The port appears. Figure 2.69 shows an input port, port name of which is on the left. Figure 2.70 shows an output port and an inout port, port names of which are on the right.

  ![Input Port](image)

  Figure 2.69. Input Port

  ![Output Port and Inout Port](image)

  Figure 2.70. Output Port and Inout Port

  g. Connect the port to the module pins. Refer to the Connecting Modules section for more details.
To create ports automatically:

a. Select the pins that are to be connected to the top-level ports. All the pins in a module can be selected by clicking its block. Any pins that are already connected to a net or a constant value are skipped.

b. Right-click on one of the selected pins, interfaces or modules, and choose **Export**. The selected pins are extended by lines to new top-level port symbols. The names of the ports and nets are added to the List view. Zoom out or scroll the image in the Schematic view to see the new ports.

c. Port or net names can be changed, if needed.

To modify port:

a. Click on port, **Properties** window open (**Figure 2.71**)

![Figure 2.71. Properties of Port](image)

b. Port direction can be modified. You can use the drop-down menu to choose the desired port direction. TCL command is shown in **Design View**. (**Figure 2.72**).

**Note:** Port width can only be modified if it is already multi-bit. An error message is prompted out or shown in TCL console, if the input value does not meet rules (**Figure 2.72**).
c. PortBus MSB, LSB and direction can be modified. Click on PortBus and then use the drop-down menu to choose the desired direction.

Note: An error message is prompted out or shown in TCL console, if the input value does not meet rules (Figure 2.73).
2.2.11. Adjusting Address Spaces

The Address view shows the base address, size of the address segment, and the end address for each leaf memory-mapped slave connection in the Propel Builder project. Propel Builder can automatically assign address values, while the base address value can be changed manually. The addresses are automatically assigned when master and slave components were connected. The ranges are set when the modules are configured. The end addresses are calculated.

The Lock option on each address space prevents Auto Assign from changing the base address value. The Lock option is selected automatically when you manually change the address value. To reset the address space, clear the Lock option before clicking the Auto Assign icon.

**Note:** There is no Lock option on LocalMemory. The value of the base address can always be changed, while Auto Assign does not reset it to its original value.

1. In the Propel Builder main window, click the Address tab. The Address view (Figure 2.74) shows.

![Figure 2.74. Address View](image)

2. (Optional) Set or clear the Lock options as desired in Address view.

3. (Optional) Double-click the base address in Address view (Figure 2.75). Type the new value and press Enter. Values must align with 1K boundaries, such as 0x00000400, 0x00000800, or 0x00000C00. The end address value changes based on the new value. The Lock option is selected automatically at this time.

![Figure 2.75. Edit Base Address](image)
Note: If there is a conflict of a related address space, it is shown in red in the graphic.

2.2.12. Validating the Design
The design rule check (DRC) can be run at any time. This checks whether or not there is any illegal connection or overlapping address space.
To perform the design rule check:

1. From the toolbar of the Propel Builder main window, click the Validate Design icon. The DRC results appear in the Tcl Console.

2.2.13. Generating the RTL file
The final step for creating a Propel Builder module is to generate a .sbx file, which defines a Propel Builder project, an RTL file, and the instantiation templates. The RTL file includes the Verilog code for the module. The instantiation templates have Verilog and VHDL code to help instantiate the Propel Builder module in a design.

- From the toolbar of the Propel Builder main window, click the Generate icon. This step also saves the Propel Builder design and runs the design rules check (DRC).
- From the toolbar of the Propel Builder main window, click the Generate Memory Report icon. The SoC design memory information is generated. The memory report folder (mem_report) is generated. All design memory information is shown in detail in the memory report files. The Memory Report files are in HTML format (Figure 2.76).

2.2.14. Opening Project in Diamond or Radiant
In a complete SoC project, a Diamond or Radiant project can be created including a Propel Builder design, and after that the SoC project can be opened in Diamond or Radiant software. According to device in the SoC project, Propel Builder can launch Diamond or Radiant software accordingly. If the device is LCMXO3D, MachXO3L, MachXO3LF, MachXO2, LFMNX, the Diamond icon is shown in the Builder GUI Toolbar. If the device is LIFCL, LFD2NX, LFCPNX, and LFMX05, the Radiant icon is shown in the Builder GUI Toolbar. For a template SoC project, you can launch Diamond or Radiant software directly after template SoC project is created.
- To launch Diamond software:
  a. Click the Diamond icon from the Propel Builder toolbar.
  b. Lattice Diamond is launched with a Diamond project generated for SoC at background (Figure 2.77).
c. (Optional) From the File List view of Diamond:
   - modify the top-level RTL file (<proj_name>_Top.v) to match the SoC design, presupposition of which is that there is a top-level RTL file in your SoC design.
   - create a top-level RTL file (<proj_name>_Top.v) to match the SoC design, if the SoC design is created from an Empty Project template and there is no top-level RTL file in your SoC design.

d. (Optional) Modify LPF constraint file (<proj_name>.lpf) to match the SoC design, if you have modified the SoC design. This step is a must to the SoC design that is created from Empty Project template.

e. Switch to Process view of the Diamond project (Figure 2.78). Make sure at least one programming file (IBIS Model, Verilog Simulation File, VHDL Simulation File, Bitstream File, or JEDEC file) is selected in the Export Files section. Available programming files can be different upon specific device included.
Right-click Export Files, and choose Run. The programming file is generated. The programming file can be used in the Diamond Programmer.

**Note:** Refer to the Diamond online help for more details of the Diamond project. Re-launch the Diamond project, if the project settings are modified in Propel 2022.1 Builder.

- To launch Radiant software:
  - Click the Radiant icon from the Propel Builder toolbar.
  - Lattice Radiant is launched with a Radiant project generated for SoC at background.
c. (Optional) From the File List view of Radiant:
   - modify the top-level RTL file (<proj_name>_Top.v) to match the SoC design, presupposition of which is that there is a top-level RTL file in your SoC design; or
   - create a top-level RTL file (<proj_name>_Top.v) to match the SoC design, if the SoC design is created from an Empty Project template and there is no top-level RTL file in your SoC design.

d. (Optional) Modify pdc constraint file (<proj_name>.pdc) to match the SoC design, if you have modified the SoC design. This step is a must to the SoC design that is created from Empty Project template.

e. Click Run all. The Programming file is generated. It can be used in the Radiant Programmer.

Notes:
- Refer to the Radiant online help for more details of the Radiant project.
- About ipx based Radiant implementation flow in Propel Builder:
  - To enable Radiant constraint propagation flow, the design source files need to be switched from original HDL files to ipx file when generating the Radiant project.
  - Ipx based Radiant implementation flow is for project created in later than Propel Builder 2022.1. For project created before Propel Builder 2022.1, use a different method for exporting files. If you want to use ipx flow in these old projects, open them in P2022.1 and regenerate, then export to Radiant to change how it is exported to Radiant. (Figure 2.80).
2.2.15. Launching SDK

After a SoC design is completed, Propel SDK can be launched in Propel Builder for software development. For template SoC project, you can launch SDK directly by clicking **Run Propel** icon from Propel Builder toolbar after template SoC project created.

1. Click the **Run Propel** icon from the Propel Builder GUI Toolbar. Lattice Propel Launcher (Figure 2.81) opens.
2. Click **Launch**. Propel SDK GUI opens and the C Project wizard (Figure 2.82) pops up for loading the system and the board support package (BSP) to create a C/C++ project. Enter a project name in the **Project Name** field, such as `HelloWorld_C`. Click **Next**.

![C/C++ Project](image)

**Figure 2.82. Propel SDK GUI and C/C++ Project Wizard**

3. Click **Next**. The C/C++ project dialog (Figure 2.83) opens.
Figure 2.83. Create C/C++ Project

4. Click **Finish**. The C/C++ project is created and is displayed using the C/C++ perspective. A perspective is a collection of tool views for a particular purpose. The C/C++ perspective is for creating C/C++ programs. 

**Note:** Refer to Lattice Propel 2022.1 SDK User Guide (FPGA-UG-02176) for more details on how to create a C/C++ project and develop the C/C++ project in Propel SDK.
2.3. Verification Project Design Flow

2.3.1. Creating a Verification Project

1. Choose File > **New Design** from the Lattice Propel Builder Menu Bar. The Create System Design wizard opens (Figure 2.84).

![Figure 2.84. Create System Design – Design Information Wizard](image)

2. Choose SoC Verification from the **Type** field.
3. Enter a project name in the **Name** field, such as Verification_Project.
4. (Optional) Use the “**Browse...**” option to change the project location in the **Location** field, if needed.
5. Click **Next**. The Propel Project Configure wizard is shown as **Figure 2.85**.
6. (Optional) The default Hardware Description Language (HDL) is displayed in the Language area. Use the drop-down menu to change the default language.

7. Select an existing SBX design by using Browse... to choose an SBX file, such as HelloWorld.

8. Click Next. The Project Information wizard opens.

9. Click Finish. A dut_inst of SoC project can be seen in the Schematic view (Figure 2.86).
Figure 2.86. Verification Project

**Note:** The default instance name of an imported Design Under Test (DUT) is dut_inst. By default, its boundary is shown with dotted line, and the filled-in color is gray. If there is any change in the SOC design, the dut_inst DUT block can be updated accordingly by double-clicking this dut_inst DUT block, or by right-clicking this dut_inst DUT block and choosing Reconfig.

10. Click the plus sign of this dut_inst DUT block. You can see the whole SoC Design (Figure 2.87). Click the negative sign to close the expanded bus.

Figure 2.87. Whole SoC Design

### 2.3.2. Switching SoC Project to Verification Project

Propel Builder supports switching SoC project to verification project manually after creating a SoC project.

1. Create a SoC Project, such as HelloWorld project. Refer to the [Creating Template SoC Project](#) section for more details.
**Note:** Corresponding Verification project is created automatically when creating a new empty SOC project. Hello World Templates can have pre-developed Verification projects.

2. Click **Switch Verification and Soc Design** icon from Propel Builder GUI Toolbar. Propel Builder dialog box opens (Figure 2.88), if a project is not saved.

![Figure 2.88. Propel Builder Dialog Box](image)

3. Click **Yes** in the Propel Builder dialog box. The Propel Builder GUI switches to verify the project (Figure 2.89).

![Figure 2.89. Switching to Project Verification](image)

**Note:** If the SoC project needs to be re-configured, click **Switch Verification and Soc Design** again to switch the verification project to the SoC project.

### 2.3.3. Opening a Verification Project

Refer to the **Opening a SoC Existing Project** section for procedure in detail.
2.3.4. Adding Modules, IP and VIPs
Refer to the Adding Modules section for procedure in detail.

2.3.5. Working with the Schematic View
Refer to the previous Working with the Schematic View section for procedure in detail.

2.3.6. Connecting Modules
Refer to the previous Connecting Modules section for procedure in detail.

2.3.7. Monitoring DUT
This feature is available to a SOC Verification project only. In Propel Builder, the pin inside DUT can be connected to the input pin of a VIP. The connected pins can be found at both ends of the orange line, as shown in Figure 2.90. Only pin and pin bus are supported in the current release of Propel Builder.

![Figure 2.90. Monitoring DUT](image)

The testbench generated for this Verification project is shown in Figure 2.91. This testbench file can be used for simulation.

![Figure 2.91. Testbench of the Verification Project](image)
2.3.8. Generating Simulation Environment

1. Click the Generate icon from the Propel Builder Toolbar to generate a testbench file including the scripts for the chosen simulator, file list for HDLs, and some other files. The testbench file structure is shown in Figure 2.92.

```
[sim]  -- generated simulation environment
   [hdl_header]
   soc_regs.v  -- register definitions of all the components in DUT/SOC
   sys_platform.v  -- base address, user settings of all the components in DUT/SOC
   [misc]
   *.*  -- all the mem, hex, txt files will be copied here
   flist.f  -- file list for HDLs
   msim.do  -- do script for simulator, it can be qsim for Questasim
   wave.do  -- do script for adding signals in waveform window
   <project_name>.sv  -- top testbench, SystemVerilog based
```

**Figure 2.92. Testbench File Structure**

Unlike those HDLs generated in the SOC design, the testbench generation in the Verification project is just a start point for you to work with. Make sure that you generate a new testbench, if there is an existing simulation environment. A dialog box pops up prompting you to make a choice of Yes or No (Figure 2.93).

```
Propel Builder

? Current simulator has been changed. This operation will overwrite the most recent simulation result. Do you want to continue?

Yes  No
```

**Figure 2.93. Propel Builder – A Reminding Dialog Box**

2.3.9. Launching Simulation

1. Click Launch Simulation icon from the Propel Builder Toolbar to launch simulation.
2. The default simulation tool, ModelSim, OEM version, opens (Figure 2.94).
Figure 2.94. Simulation GUI

Note: Before launching simulation, you can change Simulator to Questasim by clicking **Design > Options** from the Builder Menu bar. Builder Options Wizard opens (Figure 2.95). Click **Directories** to set a desired Questasim Location.
Figure 2.95. Builder Options Wizard
2.4. Advanced Usage

2.4.1. Supported Interface
Lattice Propel Builder and IP Packager share the same usage of interfaces. These interfaces are listed below.

- Interrupt
- AMBA3 AHB Lite
- AMBA3 APB
- AMBA4 AXI4
- AMBA4 AXI4 Lite
- AMBA4 AXI4 Stream
- Localbus

Refer to the IP Packager section for detailed usage of these interfaces in the IP Packager.

2.4.2. Supported Language
Propel 2022.1 Builder supports the following languages:

- Verilog HDL
- SystemVerilog
- VHDL
- Mixed Verilog/VHDL

Currently, verification projects only support Verilog HDL.

2.4.3. Supported Hierarchical IP
Hierarchical IP instantiates a hierarchical component that contains a reference to a design along with a description of the top-level interface of the component.

Click Expand IP sign on the left corner of the hierarchical IP (Figure 2.96) to show the detailed design scope of this IP (Figure 2.97).

![Figure 2.96. Hierarchical IP]
2.4.4. Export Interface

AHB Lite or APB interface ports can be connected to external IP outside of Propel Builder. You must use AHB-Lite or APB feedthrough modules to hold the address space (when feedthrough module is configured as master) or memory map (when feedthrough module is configured as slave) information. The interface to be exported should be connected first to feedthrough, then the other end of the feedthrough can be exported. An example is shown in Figure 2.98.

In the example above, to export interface ahbl_int_inst.AHB_M02:

1. Instantiate an AHB-Lite feedthrough module from IP catalog, and configure it as slave. The instance name here is ahbl_s0_inst.
2. Set the address width and data width for the memory map.
3. Connect ahbl_int_inst.AHB_M02 to ahbl_s0_inst.AHBL_S0.
4. Export ahbl_s0_inst.AHBL_M0 for external IP.

You can see the memory map for ahbl_s0_inst is shown in the Address Editor (Figure 2.99).
2.4.5. Define Custom Template

Saving design as template is an enhancement feature of Propel Builder, which allows you to create your own new project template based on existing design. You can deploy this template into Propel Builder later or share it with others by saving template into a .ptmp file. See below on how to make a .ptmp file.

This function takes effect from Propel Builder 2022.1, so the design created in earlier Propel Builder versions cannot define its custom template.

- Export current template configuration:
  
  Choose **Tools > Create Template** from Propel Builder Menu Bar. Template Configuration (Figure 2.100) opens.

---

Figure 2.99. Memory Map for ahbl_s0_inst in Address Editor
a. Fill in general information such as Template name, Description, Vendor.

b. Select Processor, Device Family, and Supported Boards:
   - The device used in the current design is listed by default. You must make sure the design can work on all the devices in the list.
   - How:
   - Click on IP instance in Schematic view, the Design View shows the corresponding information of this IP.
   - Check VLNV for this IP name (Figure 2.101). Go to IP Catalog, click on before this IP to show the IP Information. In Device Supported area, all the devices this IP supports are listed (Figure 2.102). Make
sure all the IP instances in the design have the device support which are listed in the Board Family list in Template Configuration (Figure 2.100).

![Figure 2.101. Check IP Name in Design View](image)

![Figure 2.102. Check Device Supported in IP Information](image)

- You can add the board information manually in **Supported Boards** (refer to Figure 2.4 for board information) and you must ensure the correctness of the board information and the design can work on this board.

c. **Template Resources:**
   - Optional resources include the newly created project such as C application project, user RTLs.
Output:

- By default, after you click the **Generate** button, the new template can be installed to your custom template folder, which is a folder named **PropelTemplateLocal** under $HOME (Figure 2.103).

![Figure 2.103. Export Template to PropelTemplateLocal Folder](image)

- If you want to share this template, you can click **Share Template** and output this template to a .ptmp file which can be later installed to Propel Builder by other people.

- Template manager page for custom templates:

You can import/delete/export a selected template in **Template Manager** when creating a new system design (Figure 2.104 and Figure 2.105).

![Figure 2.104. Template Manager Entry](image)
Figure 2.105. Templates Manager Page

- To import a template, click Import (Figure 2.105), and then choose the desired .ptmp file (Figure 2.106).

Figure 2.106. Import ptmp File

- Custom template installation path:
  Custom templates are installed in $HOME/PropelTemplateLocal directory by default (Figure 2.107).
You can move it to another location in Options page (Figure 2.108).
Figure 2.108. Template Manager Page – Change to New Location
2.4.6. Include Sub Sbx File

Right Click on Schematic View and choose Add Sbx Instance (Figure 2.109), and then chose the sbx file you want to input (Figure 2.110).

![Figure 2.109. Right Click on Schematic View](image)

![Figure 2.110. Input sbx File and Instance Name](image)
3. IP Packager

IP Packager is a tool for you to create an IP package easily. You can edit port, file, parameter, and memory in the IP Packager, and pack a customized IP directly.

IP Package is a collection of all required files related to an IP. All the related files are organized in different directories (Figure 3.1).

- [IP Package]
  - metadata.xml
  - [rtl]
  - [testbench]
    - [ldc]
    - constraint.ldc
  - [driver]
    - [ip_eval]
  - [plugin]
    - plugin.py
  - [doc]
    - introduction.html
    - EULA.txt

**Figure 3.1. Example Directories and Files of an IP Package**

- metadata.xml [mandatory]: XML metadata file which mainly describes legal usage and interface of an IP.
- rtl [mandatory]: Directory for parameterized HDL source files. HDL source files contain configurable parameters for you to configure.
- testbench [optional]: Directory for test bench files.
- ldc [optional]: Directory template constraint file. The file name should be constraint.ldc.
- driver [optional]: Directory for driver source code files.
- plugin [optional]: Directory for Python script to implement internal logic of the soft IP. The file name of Python script should be plugin.py.
- doc [mandatory]: Directory for documentation files. It should contain one mandatory introduction file, one mandatory license agreement file, and other optional documents.

The custom IP package can be used in Propel Builder for SoC design. IP instance package (Figure 3.2) is generated when user configures IP in Propel Builder.

- <instance_name>
  - <instance_name>.cfg
  - <instance_name>.ipx
  - component.xml
  - design.xml
  - [rtl]
    - <instance_name>.v
    - <instance_name>_bb.v
  - [constraints]
    - <instance_name>.ldc
  - [driver]
  - [ip_eval]
  - [misc]
    - <instance_name>_tmpl.v
    - <instance_name>_tmpl.vhd

**Figure 3.2. Example Directories and Files of an IP Instance Package**
3.1. Launching IP Packager

1. Choose **Tools > IP Packager** from the Lattice Propel Builder Menu Bar.
   
   **Note:** You can also launch IP Packager from Radiant 3.2 or later version if you have already installed Radiant. To launch IP Packager, you can go to the Windows Start menu and choose **Programs > Lattice Radiant Software > Accessories > IP Packager.**

2. IP Packager is launched (**Figure 3.3**).

![Figure 3.3. IP Packager GUI](image)

3.2. Packing Custom IP Flow

3.2.1. Opening an IP Directory

1. Choose **File > Open IP Directory** from the Propel Builder Menu or Click the **Open Design** icon from Propel Builder Toolbar. The Select Folder dialog opens (**Figure 3.4**).

![Figure 3.4. Select Folder dialog](image)
2. Choose a desired IP directory.

3. Click **Select Folder**. The IP Packager GUI shows the IP Package project (Figure 3.5). IP package project includes three mandatory parts (Meta Data, Design File, and Doc) and two optional parts (Test Bench and Misc) that need to be edited. Refer to the **Editing IP** section for more details.
Figure 3.5. IP Packager with IP Project Details

Note: If you prepared all directories and files of an IP module in advance, the IP Packager can load the information. If you do not want to update the IP module information, you can skip the Editing IP section below.
3.2.2. Editing IP

1. From the IP Packager Project area, click **Meta Data**. The IP Packager GUI shows Meta Data information in detail (Figure 3.6).

   ![IP Packager with Meta Data Details](image)

   **Figure 3.6. IP Packager with Meta Data Details**

   a. To configure basic information:
      - Click **Basic Info** from Meta Data view (Figure 3.7).
You can see the Basic Info properties in detail as shown in Figure 3.8.

Configure the basic information by entering desired value for a property or checking the checkbox for the property in the property field. For example, click the Vendor filed to enter a desired vendor value.

**Note:** IP Packager supports both Radiant and Propel software. IP Packager currently is based on Radiant 2022.1 but does not support Radiant version of which is lower than 2022.1. “Minimal Radiant version” should be set to 2022.1 or 2022.1+. For Propel, IP Packager currently is based on Propel 2022.1, not support Propel version of which is lower than 2022.1. “Minimal Propel version” should be set to 2022.1 or 2022.1+. If the version of Radiant or Propel is invalid, a warning message is shown (Figure 3.9).
b. To configure parameters:
   - Parameters are settings that can be used in Ports/Interfaces/Memory map configuration. You can think of them as macros. For example, click on Port `gpio_i`, you can see its configuration. In `gpio_i`, there is a value using `EXTERNAL_BUF` that is defined in Parameters (Figure 3.10).
Figure 3.10. Preview on Parameters

- Two-level hierarchy (Tab/Group) is used to categorize the parameters. Click on the IP Preview icon from the toolbar (Figure 3.11), you can see the hierarchy relations (Figure 3.12).
Figure 3.11. Two-Level Hierarchy to Categorize Parameters
Figure 3.12. IP Preview Showing Two-level Hierarchy in Parameters

- Naming rules for parameters:
  - Parameters in all groups should not have the same name, which is similar that macro redefinition is not allowed.
  - Characters support in naming are letters with mixed case, numbers and underscore (_).
- To add a parameter, right-click Parameters from Meta Data view and choose Add Parameter Tab (Figure 3.13). Tab1 is created under Parameters.
Right-click Tab1 under Parameters from Meta Data view, and choose Add Parameter Group. Group1 is newly added under Tab1 (Figure 3.14).

Right-click Group1 under Tab1 from the Meta Data view, and choose Add Parameter. NewParam1 is newly added under Group1 (Figure 3.15).
Figure 3.15. NewParam1 Added to Group1

- Double-click **NewParam1** to rename the parameter (Figure 3.16). The parameter name is also used as the unique ID of the parameter setting.

![Diagram](image)

Figure 3.16. Rename a Parameter

- Double-click the property value field to enter the desired parameter value, or select the desired value from drop-down menu (Figure 3.17). The properties are thus configured. Property listed in bold must be configured. The details of each property is shown in Table 3.1.
Figure 3.17. Configure a Parameter

Table 3.1. Details of Parameter Property

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
<th>Mandatory</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>title</td>
<td>String</td>
<td>No</td>
<td>Short title of the setting. If “title” is not specified, value of “setting” is used. Example: title=&quot;Device Architecture&quot;</td>
</tr>
<tr>
<td>type</td>
<td>param, input, command</td>
<td>Yes</td>
<td>A setting can be a Verilog parameter, Verilog macro definition or user input. Param, 94olean_macro and input settings can be used to compute values of other param and input settings. They only differ in generated files. Param is written out as a Verilog parameter value of the IP module. 9solean_macro is translated to a Verilog macro definition by the define compiler directives, but input is not. Command shows as a button. Example: type=&quot;param&quot;</td>
</tr>
<tr>
<td>value_type</td>
<td>bool, string, int, float, path</td>
<td>Yes</td>
<td>Type of the value. Supported types are bool, int, float, string, and path. The int type supports unlimited precision. The float type supports the precision of float type of C programming language. Refer to the Characteristics of Floating Types section of the 1999 ISO/IEC C Standard for details. The path type indicates a string which represents a path. “/” is used as separator. Example: value_type=&quot;string&quot;</td>
</tr>
<tr>
<td>default</td>
<td>Python expression</td>
<td>No</td>
<td>Default value of the setting. If the setting has no “default” attribute but has “options” attribute, the first option is picked as default value. If the setting has neither “default” attribute nor “options” attribute, the initial value of setting is set to 0 for int, 0.0 for float, &quot;&quot; for string and False for bool. By default, it is not allowed to reference to other setting values. Use value_expr as reference values. Example: default=&quot;LIFCL&quot;</td>
</tr>
<tr>
<td>value_expr</td>
<td>Python expression</td>
<td>No</td>
<td>Python expression to compute the value of the setting. The result is used as the parameter value if the setting is not editable. For example, divider is calculated by frequencies.</td>
</tr>
<tr>
<td>Property</td>
<td>Value</td>
<td>Mandatory</td>
<td>Description</td>
</tr>
<tr>
<td>-------------------</td>
<td>-------------------------------------------------</td>
<td>-----------</td>
<td>------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>options</td>
<td>Python list or list of tuples</td>
<td>No</td>
<td>Candidate options for the setting, which is used by GUI to display a dropdown selector. It can be set to a simple list or a list of tuples. If it is a simple list, elements are displayed and written. If it is a list of tuples, the first item in tuple is displayed and the second item in tuple is written. Example: options=&quot;[0.1, 0.2, 0.5, 1.0]&quot;</td>
</tr>
<tr>
<td>output_formatter</td>
<td>str</td>
<td>No</td>
<td>Control how parameter values are written in output RTL files. Following formatters are supported. Str: parameter values are written as strings nostr: quotation marks of strings are removed Example: output_formatter=&quot;str&quot;</td>
</tr>
<tr>
<td>bool_value_mapping</td>
<td>Python tuple or list with 2 string elements</td>
<td>No</td>
<td>The map-to-map bool values to dedicated strings. By default, bool values are written as 1, 0. Example: bool_value_mapping=&quot;('True', 'False')&quot;</td>
</tr>
<tr>
<td>editable</td>
<td>Python expression</td>
<td>No</td>
<td>Python expression to determine if the setting is editable. When a setting is not editable, it is grayed out in GUI display and its value is computed by value_expr. Otherwise, user input is used. Example: editable=&quot;(FEEDBACK_PATH == 'PHASE_AND_DELAY')&quot; (FEEDBACK_PATH is a setting ID in metadata.xml)</td>
</tr>
<tr>
<td>hidden</td>
<td>True</td>
<td>No</td>
<td>Python expression to determine whether or not the setting is hidden in GUI. If hidden is set to True (default is False), the item is hidden in GUI. The expression is resolved to 96oolean value after the user setting is changed. Example: hidden=&quot;True&quot;</td>
</tr>
<tr>
<td>drc</td>
<td>Python expression</td>
<td>No</td>
<td>Python expression to do DRC on the setting. True means DRC pass. Example: drc=&quot;check_valid_addr_pre(I2C_LEFT_ADDRESSING_PRE,i2c_left_addressing_width)&quot; (check_valid_addr_pre is defined in plugin.py setting ID: I2C_LEFT_ADDRESSING_PRE i2c_left_addressing_width )</td>
</tr>
<tr>
<td>regex</td>
<td>Regular expression</td>
<td>No</td>
<td>Regular expression to do DRC on the value. For example, the value should be prefixed by &quot;0b&quot;. Example: regex=&quot;0b[01]+&quot;</td>
</tr>
<tr>
<td>value_range</td>
<td>Python tuple or list with 2 comparable elements</td>
<td>No</td>
<td>Valid range of setting value, which is used to do DRC on the setting. The maximum value can be infinity “float(‘inf’)”. Example: value_range=&quot;(0, 1023) if(i2c_right_enable) else (-9999, 9999)&quot;</td>
</tr>
<tr>
<td>config_groups</td>
<td>Python expression</td>
<td>No</td>
<td>A name or names to group settings together. It is copied from IP-XACT configGroups attribute, and only supports “SystemBuilder” value. If it is defined, related RTL parameter is brought out to IP instance top module, so that System Builder can re-define its value.</td>
</tr>
<tr>
<td>Description</td>
<td>String</td>
<td>No</td>
<td>Detailed description of the setting.</td>
</tr>
<tr>
<td>Macro_name</td>
<td>id, value</td>
<td>No</td>
<td>Specify how to name the Verilog macro in ‘verilog_macro’ type setting item, the ID or value of this setting item. The default value is ‘setting’, which means the setting’s ID will be defined as a Verilog macro. If it is set as ‘value’, the evaluated</td>
</tr>
<tr>
<td>Property</td>
<td>Value</td>
<td>Mandatory</td>
<td>Description</td>
</tr>
<tr>
<td>----------</td>
<td>-------</td>
<td>-----------</td>
<td>-------------</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>setting value is the Verilog macro. Example: maro_name=&quot;value&quot; Result: `define &lt;setting value&gt; Note: This is only be considered in the setting item whose ‘value_type’ attribute is set to ‘string’.</td>
</tr>
</tbody>
</table>

- Repeat steps above to configure all parameters as desired.

c. To configure Ports:
   - Click Ports from the Meta Data Tree, three port types (IN, OUT, INOUT) (Figure 3.18) are listed.

   ![Figure 3.18. Three Port Types](image)

   - Right-click IN from the Ports area, and choose Add Port (Figure 3.19).

   ![Figure 3.19. Right-click Menu of the IN Port](image)

   **Note:** You can add all ports by using Infer Ports from HDL, if you prepare valid RTL files and add RTL files in Design Files section. Click Infer Ports from HDL, the Add inferred ports to meta data wizard pops up (Figure 3.20). If you have added some ports and then choose Infer Ports from HDL, all the previously-added ports are removed and only ports from the HDL file can be added.
**NewPort1** is created. Double click NewPort1 to rename the port (Figure 3.21).

- **Figure 3.20. Add inferred ports to meta data Wizard**

- Configure all properties of the IN port as desired (Figure 3.22). Property listed in bold must be configured. The details of each property is shown in Table 3.2.
Table 3.2. Details of Port Property

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
<th>Mandatory</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>range</td>
<td>Python tuple or list with two-integer elements</td>
<td>No</td>
<td>Range of this port. It should be a Python expression whose evaluation result is a tuple or array with two elements. Example: range=&quot;(A_WDT-1, 0)&quot; (A_WDT is a setting ID)</td>
</tr>
<tr>
<td>conn_port</td>
<td>Valid Verilog module name</td>
<td>No</td>
<td>Name of port of IP core module to which this port connects. Value of “name” is used if “conn_port” is not specified. Example: conn_port=&quot;clk&quot;</td>
</tr>
<tr>
<td>conn_range</td>
<td>Python tuple or list with two-integer elements</td>
<td>No</td>
<td>Range of conn_port. It should be a Python expression whose evaluation result is a tuple or array with two elements. Example: conn_range=&quot;(A_WDT-1, 0)&quot; (A_WDT is a setting ID)</td>
</tr>
<tr>
<td>stick_high</td>
<td>Python expression</td>
<td>No</td>
<td>Python script. True: tie this port to 1. Example: stick_high=&quot;True&quot;</td>
</tr>
<tr>
<td>stick_low</td>
<td>Python expression</td>
<td>No</td>
<td>Python script. True: tie this port to 0. Example: stick_low=&quot;no_seq_pins()&quot; (no_seq_pins is defined in plugin.py)</td>
</tr>
<tr>
<td>stick_value</td>
<td>Python expression</td>
<td>No</td>
<td>Python script. Tie port to the evaluation result of this attribute.</td>
</tr>
<tr>
<td>dangling</td>
<td>Python expression</td>
<td>No</td>
<td>Python script. True: keep this port unconnected. Example: dangling=&quot;not USE_COUT&quot; (USE_COUT is a setting ID)</td>
</tr>
<tr>
<td>attribute</td>
<td>Python expression</td>
<td>No</td>
<td>Python script. The value can be written to the .v file as the attribute of the port. Example:</td>
</tr>
<tr>
<td>Property</td>
<td>Value</td>
<td>Mandatory</td>
<td>Description</td>
</tr>
<tr>
<td>--------------</td>
<td>----------------</td>
<td>-----------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>port_type</td>
<td>String</td>
<td>No</td>
<td>‘data’, ‘reset’ and ‘clock’ are valid values. The default value is ‘data’.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Port_type can be passed to the IPXact component.xml as a lssccip:isClk or lssccip:isRst node in vendorExtensions in component/model/ports/port.</td>
</tr>
</tbody>
</table>

- Repeat steps above to configure all ports as desired.

d. To configure Interfaces:
   - Right-click **Interfaces** from the Meta Data view, and choose **Add Interface** (Figure 3.23). A new interface **NewInterface1** is created.

   ![Figure 3.23. Right-click Menu of an Interface](image)

   - Double click **NewInterface1** to rename interface (Figure 3.24).

   ![Figure 3.24. Rename Interface](image)

   - Configure the interface as desired (Figure 3.25).
Figure 3.25. Configure an Interface

- Repeat steps above to configure all interfaces as desired.
e. To configure Memory Map:
   • Right-click Memory Map from the Meta Data Tree, and choose Import Memory Map from CSV (Figure 3.26). New memory map is created (Figure 3.27).
   • **Note:** Propel 2022.1 Builder only supports using Import Memory Map from CSV to create memory map. There are some issues if you use Add Memory Map.

![Memory Map Menu](image)

Figure 3.26. Right-click Menu of a Memory Map
Figure 3.27. Generate New Memory Map
2. From the IP Packager Project area, click **Design Files**. IP Packager GUI shows the Design Files information (Figure 3.28).

![IP Packager with Design File Details](image)

**Figure 3.28.** IP Packager with Design File Details

- Click the **Add** button to select a desired rtl file in the Design Files field. Click the **Remove** button to remove an RTL file. Use the “...” option to add a desired timing constraint file and synplify Pro Constraint file.

  **Note:** Design file configuration is mandatory. Specify at least one RTL file. If the RTL file needs to be encrypted, check the **Encryption** option for it.
3. From the IP Packager Project area, click **Test Bench**. The Test Bench information is shown in detail (Figure 3.29).

![IP Packager with Test Bench Details](image)

**Figure 3.29. IP Packager with Test Bench Details**

Follow the steps as those for configuring the Design Files to configure the Test Bench. The Test Bench files configuration is not mandatory.
4. From the IP Packager Project area, click Misc. The Misc related information is shown in detail (Figure 3.30). Configure Misc information as desired.
5. From the IP Packager Project area, click **Doc Assistant**. The Doc Assistant information is shown in detail (Figure 3.31).

![Figure 3.31. IP Packager with Doc Assistant Details](image)

- Enter the desired title, description, and device in the **Title**, **Description**, and **Device support** fields accordingly.
- Double-click and enter a revision in **Revision** field. Double-click and enter revision contents in **Content** field. Refer to Figure 3.32 as an example. Click the **Add** button. A new blank row is added to the Revision History area. You can add desired revision and contents accordingly. Select the revision you want to delete, and click the **Remove** button to remove a Revision.
- Click the **Save and Add to IP Package** button to create an introduction html page and save this file to the IP package.
Figure 3.32. Configure Doc Assistant
3.2.3. Previewing IP

1. Choose **Edit > IP Preview** from Propel Builder menu. Or, click the **IP Preview** icon from Propel Builder Toolbar.

2. IP Preview pops up showing the configuration component for the IP module (Figure 3.33), if the IP project configuration is correct. Otherwise, the IP Packager pops up an error message (Figure 3.34).

![Figure 3.33. IP Preview Shows Configuration for IP Module](image)

![Figure 3.34. IP Packager Pops up Error Message](image)
3.2.4. Packaging IP

1. Choose Edit > Package IP from Propel Builder menu. Or, click the Package IP icon from Propel Builder Toolbar.
2. IP Packager pops up a message showing the packaging is completed successfully (Figure 3.35).

![Figure 3.35. IP Packager Pops up Successful Packaging Message](image)

**Note:** When the setting value is changed, the packaging operation is disabled. You must perform a preview operation before packaging. If the preview is successful, the packet operation is enabled. Otherwise, error messages are displayed in the output widget.

3.3. Editing IP Package Files

3.3.1. Metadata File

Metadata.xml can be generated after editing IP. You also can manually edit the file. IP Platform uses XML file to describe metadata of a soft IP. Namespace “lsccip” is used in XML file. The content of the XML file consists of three mandatory nodes including <general>, <settings> and <ports>, five optional nodes including <busInterfaces>, <addressSpaces>, <memoryMaps>, <componentGenerators> and <estimatedResources>. One optional new child node <outFileConfigs> is added to support the customized IP generation flow in Propel (Figure 3.36).

```
<lsccip:ip
 xmlns:lsccip="http://www.latticesemi.com/XMLSchema/Radiant/ip"
xmns:xsi="http://www.w3.org/2001/XMLSchema-instance"
version="1.0">
  <lsccip:general>
    .......
  </lsccip:general>
  <lsccip:settings>
    .......
  </lsccip:settings>
  <lsccip:ports>
    .......
  </lsccip:ports>
</lsccip:ip>
```

![Figure 3.36. Example XML of Metadata Layout](image)

1. `<general>` node: describes general information about a soft IP, for example, name, version, and category. Table 3.3 shows the child nodes of `<general>` node.
Table 3.3. Child Nodes of General Node

<table>
<thead>
<tr>
<th>Child Node</th>
<th>Mandatory</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>vendor</td>
<td>Yes</td>
<td>Soft IP vendor. Official soft IP should have vendor name. Example: “latticesemi.com”</td>
</tr>
<tr>
<td>library</td>
<td>Yes</td>
<td>Library of the soft IP. If “library” is not set, the default value “ip” is used. Example: “ip”, “interface”</td>
</tr>
<tr>
<td>name</td>
<td>Yes</td>
<td>Name of the soft IP. The name must be unique among soft IP of the same vendor and library. Example: “adder”</td>
</tr>
<tr>
<td>display_name</td>
<td>No</td>
<td>Name to be displayed in the software. If “display_name” is not set, software displays “name” directly. Example: “Adder”</td>
</tr>
<tr>
<td>version</td>
<td>Yes</td>
<td>Version of the soft IP. Example: 1.0.0</td>
</tr>
<tr>
<td>category</td>
<td>Yes</td>
<td>Category of the soft IP. Category can be hierarchical. Levels are separated by “,”. Example: Memory_Modules,Distributed_RAM</td>
</tr>
<tr>
<td>keywords</td>
<td>No</td>
<td>Keywords of the soft IP. Multiple keywords are separated by “,”. Example: BusType_AHB,BusType_APB</td>
</tr>
<tr>
<td>min_radiant_version</td>
<td>Yes</td>
<td>The minimal Radiant version, which supports the soft IP. Example: 1.0 (no service pack), 1.0.1 (with service pack)</td>
</tr>
<tr>
<td>max_radiant_version</td>
<td>No</td>
<td>The maximal Radiant version, which supports the soft IP. Example: 2.0.</td>
</tr>
<tr>
<td>supported_products</td>
<td>No</td>
<td>FPGA products supported by the soft IP.</td>
</tr>
<tr>
<td>Type</td>
<td>No</td>
<td>Enhancement for cpu IP.</td>
</tr>
<tr>
<td>Min esi_version</td>
<td>No</td>
<td>The minimal ESI version, which supports the soft IP. Enhancement for esi.</td>
</tr>
<tr>
<td>Max esi_version</td>
<td>No</td>
<td>The maximal ESI version, which supports the soft IP. Enhancement for esi.</td>
</tr>
<tr>
<td>Supported_platforms</td>
<td>No</td>
<td>Default is Radiant, specific for esi.</td>
</tr>
</tbody>
</table>
2. `<settings>` node: describes parameters information that should contain one or more `<setting>` nodes. In an IP instance package, Verilog parameters are used to configure the soft IP. All user configurable parameters should be added to the `<settings>` section as `<setting>` nodes. Beside parameters, you can add `<setting>` nodes for user-input only. Table 3.4 shows attributes of `<setting>` nodes.

### Table 3.4. Attributes of Setting Nodes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Value</th>
<th>Mandatory</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>id</td>
<td>String</td>
<td>Yes</td>
<td>The unique ID of the setting, which is also be referred as: Parameter name in RTL codes Python variable name Tcl variable name To make value of the “id” valid in Verilog HDL, Python and Tcl, it should consist of only letters, digits, and underscore. The first character should be letter. Example: id=&quot;num_outputs&quot;</td>
</tr>
<tr>
<td>title</td>
<td>String</td>
<td>No</td>
<td>Short title of the setting. If “title” is not specified, value of “setting” is used. Example: title=&quot;Number of Output&quot;</td>
</tr>
<tr>
<td>type</td>
<td>param, input, command</td>
<td>Yes</td>
<td>A setting can be a Verilog parameter, Verilog macro definition or user input. Param, 112oolean_macro and input settings can be used to compute values of other param and input settings. They only differ in generated files. Param is written out as a Verilog parameter value pf the IP module, 112oolean_macro is translated to a Verilog macro definition by the define compiler directives, but input is not. Command shows as a button. Example: type=&quot;param&quot;</td>
</tr>
<tr>
<td>value_type</td>
<td>bool, string, int, float, path</td>
<td>Yes</td>
<td>Type of the value. Supported types are bool, int, float, string, and path. The int type supports unlimited precision. The float type supports the precision of float type of C programming language. Refer to the Characteristics of Floating Types section of the 1999 ISO/IEC C Standard for details. The path type indicates a string which represents a path. “/” is used as separator. Example: value_type=&quot;int&quot;</td>
</tr>
<tr>
<td>default</td>
<td>Python expression</td>
<td>No</td>
<td>Default value of the setting. If the setting has no “default” attribute but has “options” attribute, the first option is picked as default value. If the setting has neither “default” attribute nor “options” attribute, the initial value of setting is set to 0 for int, 0.0 for float, “” for string and False for bool. Example: default=&quot;1.0&quot;</td>
</tr>
<tr>
<td>value_expr</td>
<td>Python expression</td>
<td>No</td>
<td>Python expression to compute the value of the setting. The result is used as parameter value if the setting is not editable. For example, divider is calculated by frequencies. Example: value_expr=&quot;int(round((sys_clock_freq * 250.0) / i2c_left_desired_frequency))-1&quot;</td>
</tr>
<tr>
<td>options</td>
<td>Python list or list of tuples</td>
<td>No</td>
<td>Candidate options for the setting, which is used by GUI to display a dropdown selector. It can be set to a simple list or a list of tuples. If it is a simple list, elements are displayed and written. If it is a list of tuples, the first item in tuple is displayed and the second item in tuple is written. Example: options=&quot;[0.1, 0.2, 0.5, 1.0]&quot;</td>
</tr>
<tr>
<td>Attribute</td>
<td>Value</td>
<td>Mandatory</td>
<td>Description</td>
</tr>
<tr>
<td>-------------------</td>
<td>----------------------------</td>
<td>-----------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>output_formatter</td>
<td>str</td>
<td>No</td>
<td>Control how parameter values are written in output RTL files. Following formatters are supported. Str: parameter values are written as strings nostr: quotation marks of strings are removed Example: output_formatter=&quot;str&quot;</td>
</tr>
<tr>
<td>bool_value_mapping</td>
<td>Python tuple or list with 2 string elements</td>
<td>No</td>
<td>The map-to-map bool values to dedicated strings. By default, bool values are written as 1, 0. Example: bool_value_mapping=&quot;('True', 'False')&quot;</td>
</tr>
<tr>
<td>editable</td>
<td>Python expression</td>
<td>No</td>
<td>Python expression to determine if the setting is editable. When a setting is not editable, it is grayed out in GUI display and its value is computed by value_expr. Otherwise, user input is used. Example: editable=&quot;(FEEDBACK_PATH == 'PHASE_AND_DELAY') (FEEDBACK_PATH is a setting ID in metadata.xml)</td>
</tr>
<tr>
<td>hidden</td>
<td>True</td>
<td>No</td>
<td>Python expression to determine whether the setting is hidden in GUI. If hidden is set to True (default is False), the item is hidden in GUI. The expression is resolved to Boolean value after the user setting is changed. Example: hidden=&quot;True&quot;</td>
</tr>
<tr>
<td>drc</td>
<td>Python expression</td>
<td>No</td>
<td>Python expression to do DRC on the setting. True means DRC pass. Example: drc=&quot;check_valid_addr_pre(I2C_LEFT_ADDRESSING_PRE,i2c_left_addressing_width) (check_valid_addr_pre is defined in plugin.py setting ID: I2C_LEFT_ADDRESSING_PRE i2c_left_addressing_width )</td>
</tr>
<tr>
<td>regex</td>
<td>Regular expression</td>
<td>No</td>
<td>Regular expression to do DRC on the value. For example, the value should be prefixed by “0b”. Example: regex=&quot;0b[01]+&quot;</td>
</tr>
<tr>
<td>value_range</td>
<td>Python tuple or list with 2 comparable elements</td>
<td>No</td>
<td>Valid range of setting value, which is used to do DRC on the setting. The maximum value can be infinity “float('inf')”. Example: value_range=&quot;(0, 1023) if(i2c_right_enable) else (-9999, 9999)&quot;</td>
</tr>
<tr>
<td>config_groups</td>
<td>Python expression</td>
<td>No</td>
<td>A name or names to group settings together. It is copied from IP-XACT configGroups attribute, and only supports “SystemBuilder” value. If it is defined, related RTL parameter is brought out to IP instance top module, so that System Builder can re-define its value.</td>
</tr>
<tr>
<td>Description</td>
<td>String</td>
<td>No</td>
<td>Detailed description of the setting.</td>
</tr>
<tr>
<td>Group1</td>
<td>String</td>
<td>No</td>
<td>Group the settings. Settings of the same “group1” is displayed as sub-items under a group item on GUI. The settings with the same “group1” should be written continuously if you want GUI to group them under one group item. Otherwise, you can see multiple groups with the same name in GUI. Example: group1=&quot;Output Setting&quot;</td>
</tr>
</tbody>
</table>
| group2            | String                     | No        | Group the “group1” groups. “group1” groups of the same “group2” is displayed in a separate page on GUI. So, two-level hierarchy is supported in GUI display. Unlike ‘group1’, you need not write setting nodes with the same ‘group2’ continuously. You must follow the rule for ‘group1’ that all the settings with the same ‘group1’ must be in the same ‘group2’.
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3. `<ports>` node: IP module package has some ports in its implementation. These ports should be described in `<ports>` section as `<port>` child nodes. If an input port is stuck to fixed value, or an output port is dangling, the port is not used and is invisible after generation. Table 3.5 shows the attributes of `<port>` nodes.

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Value</th>
<th>Mandatory</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>Valid Verilog port name</td>
<td>Yes</td>
<td>Name of a port. Name: “Clk”</td>
</tr>
<tr>
<td>dir</td>
<td>in, out, inout</td>
<td>Yes</td>
<td>Direction of a port. Name: “in”</td>
</tr>
<tr>
<td>range</td>
<td>Python tuple or list with 2 int elements</td>
<td>No</td>
<td>Range of this port. Name: “(A_WDT-1, 0)”</td>
</tr>
<tr>
<td>conn_mod</td>
<td>Valid Verilog module name</td>
<td>Yes</td>
<td>Name of an IP core module to which this port connects.</td>
</tr>
<tr>
<td>conn_port</td>
<td>Valid Verilog module name</td>
<td>No</td>
<td>Name of port of an IP core module to which this port connects.</td>
</tr>
<tr>
<td>conn_range</td>
<td>Python tuple or list with 2 int elements</td>
<td>No</td>
<td>Range of conn_port. Name: “(A_WDT-1, 0)”</td>
</tr>
<tr>
<td>stick_high</td>
<td>Python expression</td>
<td>No</td>
<td>Python script. True: tie this port to 1.</td>
</tr>
<tr>
<td>stick_low</td>
<td>Python expression</td>
<td>No</td>
<td>Python script. True: tie this port to 0.</td>
</tr>
<tr>
<td>stick_value</td>
<td>Python expression</td>
<td>No</td>
<td>Python script. Tie port to the evaluation result of this attribute.</td>
</tr>
<tr>
<td>Dangling</td>
<td>Python expression</td>
<td>No</td>
<td>Python script. True: keep this port unconnected.</td>
</tr>
<tr>
<td>bus_interface</td>
<td>Valid bus interface name</td>
<td>No</td>
<td>Bus interface name defined in <code>&lt;busInterfaces&gt;</code> node.</td>
</tr>
<tr>
<td>Attribute</td>
<td>Value</td>
<td>Mandatory</td>
<td>Description</td>
</tr>
<tr>
<td>------------</td>
<td>---------------------------</td>
<td>-----------</td>
<td>---------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>attribute</td>
<td>Python expression</td>
<td>No</td>
<td>Python script. The value is written to the .v file as the attribute of the port. Example: attribute=&quot;&quot;(<em>) AAB, BBB=1 <em>)&quot;&quot; =&gt; (</em> AAB, BBB=1</em>) input PORT;</td>
</tr>
<tr>
<td>port_type</td>
<td>String</td>
<td>No</td>
<td>‘data’, ‘reset’ and ‘clock’ are valid values. The default value is ‘data’ port_type will be passed to the IPXact component.xml as a lscip:isClk or lscicp:isRst node in vendorExtensions in component/model/ports/port</td>
</tr>
</tbody>
</table>

4. `<busInterfaces> node: contains a list of all interface ports of the soft IP (Figure 3.37). The description follows IP-XACT format. Refer to IEEE 1685-2014: IEEE Standard for IP-XACT, Standard Structure for Packaging, Integrating, and Reusing IP within Tool Flows for more details. The busInterface has a list of portMap, which defines logicalPort name and physicalPort name. In `<ports>` nodes, one port can have optional “bus_interface” attribute, which binds the port with a busInterface. If one port is bound to the busInterface, its name should match physicalPort name of one portMap of the busInterface, so that port and busInterface/portMap is bound together. Whether or not a port can be used is based on user configuration. If the port is used, the corresponding portMap in busInterface is written to the output IP-XACT file. Otherwise, the corresponding portMap in busInterface is not written to the output IP-XACT file.
Figure 3.37. Example of busInterface Node
5. `<addressSpaces>` node: specifies the addressable area seen by bus interfaces of type master (Figure 3.38). The description follows IP-XACT format. Refer to IEEE 1685-2014: IEEE Standard for IP-XACT, Standard Structure for Packaging, Integrating, and Reusing IP within Tool Flows for more details.

```
<lsccip:addressSpaces>
  <lsccip:addressSpace>
    <lsccip:name>ahbm_addr_space</lsccip:name>
    <lsccip:range>4k</lsccip:range>
    <lsccip:width>32</lsccip:width>
  </lsccip:addressSpace>
</lsccip:addressSpaces>
```

Figure 3.38. Example of addressSpaces Node

6. `<memoryMaps>` node: specifies the information about the range of registers, memory, or other address blocks accessible through slave interface (Figure 3.39). The description follows IP-XACT format. Refer to IEEE 1685-2014: IEEE Standard for IP-XACT, Standard Structure for Packaging, Integrating, and Reusing IP within Tool Flows for more details and examples.

To represent dynamic availability of some elements, `<register>` and `<field>` node are extended with an optional `isPresent` element (introduced in IEEE Std 1685-2014), which defines whether the enclosing element is present or not. The value of `isPresent` element is a Python expression. Parameters defined in `<settings>` node can be used in the expression.

If a register is used based on user configuration, the register is written to output IP-XACT file. Otherwise, the register is not written to output IP-XACT file.
<lsccip:memoryMaps>
  <lsccip:memoryMap>
    <lsccip:name>ahbs_mem_map</lsccip:name>
    <lsccip:description>AHB-Lite Slave 0 memory map</lsccip:description>
    <lsccip:addressBlock>
      <lsccip:name>registers</lsccip:name>
      <lsccip:displayName>registers</lsccip:displayName>
      <lsccip:description>Register Block</lsccip:description>
      <lsccip:baseAddress>0</lsccip:baseAddress>
      <lsccip:range>4096</lsccip:range>
      <lsccip:width>32</lsccip:width>
      <lsccip:usage>register</lsccip:usage>
      <lsccip:access>read-write</lsccip:access>
      <lsccip:register>
        <lsccip:name>Status</lsccip:name>
        <lsccip:displayName>Status Register</lsccip:displayName>
        <lsccip:description>Status Register</lsccip:description>
        <lsccip:addressOffset>0x10</lsccip:addressOffset>
        <lsccip:size>4</lsccip:size>
        <lsccip:volatile>true</lsccip:volatile>
        <lsccip:access>read-only</lsccip:access>
        <lsccip:field>
          <lsccip:name>FIFO_Empty</lsccip:name>
          <lsccip:displayName>FIFO_Empty</lsccip:displayName>
          <lsccip:description>Indicates current status of the interface in the receive direction: 0 - There is data available. 1 - The FIFO is empty.</lsccip:description>
          <lsccip:isPresent>1 != int_setting</lsccip:isPresent>
          <lsccip:bitOffset>0</lsccip:bitOffset>
          <lsccip:bitWidth>1</lsccip:bitWidth>
          <lsccip:volatile>true</lsccip:volatile>
          <lsccip:access>read-only</lsccip:access>
          <lsccip:writeValueConstraint>
            <lsccip:minimum>0</lsccip:minimum>
            <lsccip:maximum>0</lsccip:maximum>
          </lsccip:writeValueConstraint>
          <lsccip:testable testConstraint="unConstrained">false</lsccip:testable>
        </lsccip:field>
      </lsccip:register>
    </lsccip:addressBlock>
  </lsccip:memoryMap>
</lsccip:memoryMaps>

Figure 3.39. Example of memoryMaps Node
7. `<componentGenerators>` node: contains a list of componentGenerator elements. Each componentGenerator element defines a generator that is run on generated IP instance package. Each generator is called after other IP instance package files are generated. For example, a component generator can generate memory initialization file for a memory IP (Figure 3.40).

```xml
<lsccip:componentGenerators>
  <lsccip:componentGenerator>
    <lsccip:name>memGenerator</lsccip:name>
    <lsccip:generatorExe>script/mem_gen.py</lsccip:generatorExe>
  </lsccip:Generator>
</lsccip:Generators>
```

Figure 3.40. Example of componentGenerators Node

8. `<estimatedResources>` node: contains a list of estimatedResource element. Each estimatedResource element defines the formula to calculate one type of resource used in the IP instance package. Table 3.6 shows the element in `<estimatedResource>` node.

<table>
<thead>
<tr>
<th>Element</th>
<th>Value</th>
<th>Mandatory</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>String</td>
<td>Yes</td>
<td>Name of the resource.</td>
</tr>
<tr>
<td>Number</td>
<td>Python expression</td>
<td>Yes</td>
<td>Python script to calculate the number of the resource.</td>
</tr>
</tbody>
</table>

9. `<outFileConfigs>` node: specifies all customized output file configuration nodes `<fileConfig>` for whole customized flow. FileConfig node contains a group of attributes to specify a specific file or directory generation.
A full description of a soft IP might be large. Metadata.xml supports to build a large XML file from small manageable chunks. The approach is implemented by Xinclude (Figure 3.41).

```
metadata.xml
<lsccip:ip version="1.0"
xmlns:lsccip="http://www.latticesemi.com/XMLSchema/Radiant/ip"
xmlns:xi="http://www.w3.org/2001/XInclude">
  <lsccip:general> ... </lsccip:general>
  <xi:include href="setting.xml" parse="xml" />
  <xi:include href="memory_map.xml" parse="xml" />
  <xi:include href="address_space.xml" parse="xml" />
  <xi:include href="bus_interface.xml" parse="xml" />
  <lsccip:ports> ... </lsccip:ports>
</lsccip:ip>

setting.xml
<lsccip:settings
xmlns:lsccip="http://www.latticesemi.com/XMLSchema/Radiant/ip">
  <lsccip:setting id="int_setting" type="input" value_type="int"
    conn_mod="example" default="1" title="Integer Setting" />
  <lsccip:setting id="bool_with_value_mapping" type="param"
    value_type="bool" conn_mod="example"
    default="False" bool_value_mapping="('Enabled', 'Disabled')" />
</lsccip:settings>
```

Figure 3.41. Example of Xinclude Usage

You can use metadata.xsd in Appendix A to check the metadata file. For those elements borrowed from IPXact, refer to the related xsd files of IPXact.

3.3.2. Implementation RTL Files

You should put all IP implementation RTL files in ‘rtl’ sub directory of whole IP package. Lattice Builder platform does not support hierarchical rtl directories. All RTL sources can be put in one directory level. Three file suffix names (‘.v’, ‘.sv’ and ‘.vhd’) are supported for RTL files to represent ‘Verilog’, ‘System Verilog’ and ‘Vhdl’ language types accordingly.

IP Platform always generates a wrapper module by default for the whole IP generation. This wrapper is in Verilog HDL no matter what the language type of the IP implementation RTLs is. Providing a Verilog-HDL top to handle the interface translation among different language types is strongly recommended.

If the IP is implemented in Verilog HDL (including System Verilog) only, all the contents are copied in one .v/.sv RTL file and modules are defined in the wrapper top module. All module names have unified naming rule to avoid name collision such as Top module name, PMI module name, Primitive module name, Blackbox module name.

If some portions of an IP module in the RTL file are encrypted, the corresponding portions generated in Verilog file are also encrypted.

All the RTLs are kept and copied to an IP instance directory, if there is VHDL in IP implementation RTLS. Therefore, the module-naming rule does not need to be unified. You can specify different lib (default is work) for VHDL source that is specified in “wrapper” file generator (Figure 3.42).

```
<lsccip:outFileConfigs>
  <lsccip:fileConfig name="wrapper" lib='test2.vhd=libA;test3.vhd=libB' />
</lsccip:outFileConfigs>
```

Figure 3.42. Example of Specifying Lib for VHDL
3.3.3. Python Script Plugin File

Python expressions can be used in metadata file to implement complex logic. To support complex logic, you can add any python functions in plugin.py file (Figure 3.43) of an IP package, and then call the functions in Python expressions in metadata file.

Each setting item value can be referred to in a Python expression in metadata.xml by its ID as a Python variable. An expression is evaluated by demand. The plugin has its individual namespace and all the setting items values are exported to plugin as a global map variable IP_SETTINGS. You can use IP_SETTINGS [item ID] to refer to an item or set its value in plugin code.

A global variable '__PLUGIN_VER' is defined with value ‘2.0’. You can check this variable if you want to provide a plugin that can work on both current and legacy IP platforms.

```python
def cntr_opt():
    #return ("Down" : 0, 
    #    "Up" : 1, 
    #    "UpDown":2)
    return [("Down", 0), 
            ("Up", 1),
            ("UpDown", 2)]

def cntr_ldir():
    return (CNTR_DIR == 0) | (CNTR_DIR == 1)

def cntr_lwd():
    if (CNTR_WIDTH < 2):
        return 2
    else:
        return CNTR_WIDTH

def cntr_hval_check():
    if (CNTR_HVALUE <= CNTR_LVALUE):
        ret = 0
        PluginUtil.post_error("Higher count value should be greater than the Lower count value.")
    else:
        ret = 1
    return ret

def get_device_name{value}:
    x = runtime_info.device_info.architecture(value)
    return x
```

Figure 3.43. Template of Plugin File
3.3.4. Memory Map CSV File

Propel 2022.1 Builder supports importing memory map from a CSV file to create memory map. You can edit a CSV file. Figure 3.44 shows the CSV file template. Each row to be imported is with one of the keywords among MEMORYMAP, REGISTER, and FIELD. Row with no keyword is ignored, such as the header row (orange squared part in Figure 3.44). The header row is to help identify the column.

![Figure 3.44. Example of Memory Map CSV File](image-url)

<table>
<thead>
<tr>
<th></th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
<th>G</th>
<th>H</th>
<th>I</th>
<th>J</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>name</td>
<td>description</td>
<td>baseAddress</td>
<td>range</td>
<td>width</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>MEMORYMAP</td>
<td>ABC</td>
<td>desc1</td>
<td>0x0</td>
<td>32</td>
<td>64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>name</td>
<td>displayName</td>
<td>description</td>
<td>addressOffset</td>
<td>size</td>
<td>volatile</td>
<td>access</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>REGISTER</td>
<td>QSPI_CTRL</td>
<td>QSPI_CTRL</td>
<td>QSPI Control Register</td>
<td>0x00</td>
<td>32</td>
<td>TRUE</td>
<td>read-write</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>field</td>
<td>displayName</td>
<td>description</td>
<td>bitOffset</td>
<td>bitWidth</td>
<td>volatile</td>
<td>access</td>
<td>default</td>
<td>testable</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>FIELD</td>
<td>spi_mode</td>
<td>spi_mode</td>
<td>Sets the SPI mode</td>
<td>0</td>
<td>2</td>
<td>TRUE</td>
<td>read-write</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>FIELD</td>
<td>sck_div</td>
<td>sck_div</td>
<td>Sets the SPI clock divider</td>
<td>2</td>
<td>3</td>
<td>TRUE</td>
<td>read-write</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>FIELD</td>
<td>reserved</td>
<td>reserved</td>
<td>Reserved bits</td>
<td>5</td>
<td>26</td>
<td>TRUE</td>
<td>read-write</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>FIELD</td>
<td>soft_reset</td>
<td>soft_reset</td>
<td>Resets internal soft logic</td>
<td>31</td>
<td>1</td>
<td>TRUE</td>
<td>read-write</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>name</td>
<td>displayName</td>
<td>description</td>
<td>addressOffset</td>
<td>size</td>
<td>volatile</td>
<td>access</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>REGISTER</td>
<td>CMD_DATA</td>
<td>CMD_DATA</td>
<td>Command Data Register</td>
<td>0x04</td>
<td>32</td>
<td>TRUE</td>
<td>read-write</td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>field</td>
<td>displayName</td>
<td>description</td>
<td>bitOffset</td>
<td>bitWidth</td>
<td>volatile</td>
<td>access</td>
<td>default</td>
<td>testable</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>FIELD</td>
<td>cmd_data</td>
<td>cmd_data</td>
<td>Command data to transmit in transaction phase 1 (always big endian)</td>
<td>0</td>
<td>32</td>
<td>TRUE</td>
<td>read-write</td>
<td></td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>FIELD</td>
<td>name</td>
<td>displayName</td>
<td>description</td>
<td>addressOffset</td>
<td>size</td>
<td>volatile</td>
<td>access</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>REGISTER</td>
<td>TX_FIFO_DATA</td>
<td>TX_FIFO_DATA</td>
<td>TX FIFO Data Register</td>
<td>0x08</td>
<td>32</td>
<td>TRUE</td>
<td>write-only</td>
<td></td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>FIELD</td>
<td>tx_fifo_data</td>
<td>tx_fifo_data</td>
<td>Data to transmit in transaction phase 2.</td>
<td>0</td>
<td>32</td>
<td>TRUE</td>
<td>write-only</td>
<td>NA</td>
<td>FALSE</td>
</tr>
</tbody>
</table>
4. **TCL Commands**

Propel Builder provides TCL commands to execute actions. You can manually enter TCL commands in Tcl Console (Figure 4.1), if you prefer using command lines rather than using the GUI.

![Tcl Console]

Figure 4.1. Tcl Console

4.1. **sbp_design**

The sbp_design command is used as one of the high-level management commands such as opening, closing, of the design files created by the Propel Builder.

4.1.1. **Open**

Opens an existing Propel Builder design for modification.

<table>
<thead>
<tr>
<th>Usage</th>
<th>sbp_design open -name &lt;design name&gt; -path &lt;design path&gt; [-device &lt;device name&gt;]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Example</td>
<td>sbp_design open -name project1 -path project1.sbx</td>
</tr>
</tbody>
</table>

4.1.2. **Close**

Closes a Propel Builder design currently opened.

<table>
<thead>
<tr>
<th>Usage</th>
<th>sbp_design close</th>
</tr>
</thead>
</table>

4.1.3. **New**

Creates a new Propel Builder design.

<table>
<thead>
<tr>
<th>Usage</th>
<th>sbp_design new -name &lt;new design name&gt; -path &lt;new design path&gt; -device &lt;device name&gt; -language &lt;language type&gt; -board &lt;board name&gt;</th>
</tr>
</thead>
</table>

4.1.4. **Save**

Saves the current Propel Builder design to file on disk or save it as a new file. You can choose to save the design to the project location (Example 1) or to a specific path (Example 2).

<table>
<thead>
<tr>
<th>Usage</th>
<th>sbp_design save [-path &lt;new design path&gt;]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Example 1</td>
<td>sbp_design save</td>
</tr>
<tr>
<td>Example 2</td>
<td>sbp_design save -path new_design.sbx</td>
</tr>
</tbody>
</table>
4.1.5. Drc
Runs the design rule check for the Propel Builder design file.

<table>
<thead>
<tr>
<th>Usage</th>
<th>sbp_design drc</th>
</tr>
</thead>
</table>

4.1.6. Generate
Generates RTL code to instantiate and connect the IP cores specified in the Propel Builder design file.

<table>
<thead>
<tr>
<th>Usage</th>
<th>sbp_design generate</th>
</tr>
</thead>
</table>

4.1.7. Auto Assign Addresses
Automatically assigns memory mapped addresses to all the slaves in the system. These addresses should be chosen to avoid slaves with multiple non-contiguous address ranges.

<table>
<thead>
<tr>
<th>Usage</th>
<th>sbp_design auto_assign_addresses</th>
</tr>
</thead>
</table>

4.1.8. Verify
Launches the SOC verification engine to verify design.

<table>
<thead>
<tr>
<th>Usage</th>
</tr>
</thead>
<tbody>
<tr>
<td>sbp_design verify [-h] [-workfolder &lt;workfolder_path&gt;] [-sbx_file &lt;sbx_file_path&gt;]</td>
</tr>
<tr>
<td>{sim_gen,pfr_pack,regmap_gen,auto_run}</td>
</tr>
<tr>
<td>positional arguments: {sim_gen,pfr_pack,regmap_gen,auto_run} specify the application</td>
</tr>
<tr>
<td>sim_gen Simulation Generation Flow</td>
</tr>
<tr>
<td>pfr_pack PFR Security Engine Packager Flow</td>
</tr>
<tr>
<td>regmap_gen Memory Map Generation Flow</td>
</tr>
<tr>
<td>auto_run Automation Flow</td>
</tr>
<tr>
<td>optional arguments:</td>
</tr>
<tr>
<td>-h, --help show this help message and exit</td>
</tr>
<tr>
<td>--workfolder WORKFOLDER, -wf WORKFOLDER assign the working folder. Otherwise, the default one (current working folder) will be used</td>
</tr>
<tr>
<td>--sbx_file SBX_FILE, -sf SBX_FILE specify the sbx_file</td>
</tr>
<tr>
<td>Example</td>
</tr>
</tbody>
</table>

4.1.9. PGE
Runs command with different parameters to call SGE function, DGE function, and Signature inside of PGE (Package Generate Engine).

- Runs command to call SGE to generate files for SDK.

<table>
<thead>
<tr>
<th>Usage</th>
</tr>
</thead>
<tbody>
<tr>
<td>sbp_design pge sge -i &lt;input path&gt; [-o &lt;output path&gt;]</td>
</tr>
<tr>
<td>-i [Required] the top-level SoC project sbx file full path.</td>
</tr>
<tr>
<td>-o [Optional] output full path, if the parameter is not specified, output path is the same as SoC project path. sge folder is generated at output path, at present sge folder under the SoC project root directory.</td>
</tr>
</tbody>
</table>
• Runs command to call DGE to generate TCL script that can be used to generate a Diamond or Radiant project.

Usage

```
sbp_design pge dge -i <input path> [-o <output path>] [-diamond] [-radiant]
```

- `i` [Required] the top level SoC project sbx file full path.
- `-o` [Optional] output full path, if the parameter is not specified, output path is the same as SoC project path. For DGE, tcl script and related files are generated at output path. At present, Diamond or Radiant project share the same workspace with SoC project.
- `-diamond` [Optional] flag to execute DGE for diamond project.
- `-radiant` [Optional] flag to execute DGE for Radiant project.

• Run command to generate signature.

• PGE gets partial UFM3 contents including version packet(I), Sentry PFR configure data (D), and call Flash Address Tool to sign with private key from Factory HSM.

Usage

```
sbp_design pge gen_signature -cfile <c binary file> -dfile <d binary file> -output <output binary file>
```

### 4.1.10. Undo
Undo operation. Currently, software only supports single undo.

**Usage**

```
sbp_design undo
```

### 4.1.11. Redo
Redo operation. Currently, software only supports single redo.

**Usage**

```
sbp_design redo
```

### 4.1.12. Set Device
Modify the device information including device, package, speed, operating condition.

**Usage**

```
sbp_design set_device -device <device name> -speed <speed value> -package <package value> -operating <operating condition>
```

### 4.2. Other TCL Commands
The following commands are used for specifying connectivity and IP instantiation to the Propel Builder backend.

#### 4.2.1. sbp_add_component
Instantiates an IP component into the system. Must specify the component VLNV identifier. This corresponds to a component instance in the IP-XACT design. For example, the command below can instantiate an AHB-Lite interconnect component.

**Usage**

```
sbp_add_component -vlnv <VLNV> -name <instance_name>
```

**Example**

```
sbp_add_component -vlnv lattice:ip:ahbl_interconnect:1.0 -name ahblite_interconnect
```
4.2.2. sbp_add_sbxcomp
Instantiates a hierarchical component from sbx file into the system.

Usage
sbp_add_sbxcomp -name <hname> -path <sbx_file_absolute_path_name>

Example
sbp_add_sbxcomp -name sim_comp -path "C:/test/test.sbx"

4.2.3. sbp_add_gluelogic
Instantiates a gluelogic component into the system.

Usage
sbp_add_gluelogic -name <instance_name> -logicinfo <logic json info from sbp_create_glue_logic>

Example
sbp_add_gluelogic -name equation_module_inst -logicinfo [sbp_create_glue_logic equation_module {}]

Note: This is an internal command. Modify existing usage is not recommended.

4.2.4. sbp_create_glue_logic
Create gluelogic information when adding gluelogic component. rtl_path must be a file path if gluelogic comes from a file. Else be empty.

Usage
sbp_create_glue_logic <type> <module_name> <rtl_path> <json cfg data>

Example
sbp_add_gluelogic -name equation_module_inst -logicinfo [sbp_create_glue_logic equation_module {}]

Note: This is an internal command. Modify existing usage is not recommended.

4.2.5. sbp_add_port
Creates a top-level I/O port. Must specify the direction.

Usage
sbp_add_port [-from <bit number>] [-to <bit number>] -direction <in/out/inout> <port_name>

4.2.6. sbp_modify_port
Modify existing top-level ports to change the width and the direction.

Usage
sbp_modify_port -name <port_name> [-from <bit number> ] [-to <bit number>] -direction <dir>

4.2.7. sbp_connect_net
Connects all of the specified pins and/or ports to the same net. The arguments can be pins or ports in the system design. Only one of the arguments can be the driver (output pin/port), driving all other input pin/ports. Example below connects the clk port to all components, assuming component pins are all named clk.

Usage
sbp_connect_net [-name <net name>] <pin/port> <pin/port>

Example
sbp_connect_net [sbp_get_pins clk] {CLOCK_IN}

4.2.8. sbp_connect_interface_net
Connects a bus interface pin/port to another interface pin/port. This corresponds to the interconnection element in the IP-XACT design.

Usage
sbp_connect_interface_net <pin/port> <pin/port>

4.2.9. sbp_connect_constant
Connects a constant integer to a pin/pinbus/port/portbus. To assign to a pin/pinbus, the object must be an input pin/pinbus. To assign to a port/portbus, the object must be an output port/portbus. If the integer requires multiple
bits, not 0 or 1, then the object must be a bus. The tcl command can be used to assign the same constant to multiple pin/pinbus/port/portbus at the same time.

<table>
<thead>
<tr>
<th>Usage</th>
<th>sbp_connect_constant -constant &lt;integer&gt; &lt;pin/pin bus/ port/portbus&gt; &lt;pin/pin bus/ port/portbus&gt;…</th>
</tr>
</thead>
<tbody>
<tr>
<td>Example</td>
<td>sbp_connect_constant -constant 1 {test/i2c_mst_apb/rst_n_i} {test/riscv/clk_i}</td>
</tr>
</tbody>
</table>

### 4.2.10. sbp_connect_whitebox

User can do connection cross the hierarchy boundary for verification purpose.

<table>
<thead>
<tr>
<th>Usage</th>
<th>sbp_connect_whitebox &lt;design_name/vip_inst_name/pin_name&gt; &lt;design_name/uit_inst_name/port_name&gt;</th>
</tr>
</thead>
</table>

### 4.2.11. sbp_disconnect_whitebox

Removes the connection cross the hierarchy boundary.

<table>
<thead>
<tr>
<th>Usage</th>
<th>sbp_disconnect_whitebox &lt;design_name/vip_inst_name/pin_name&gt; &lt;design_name/uit_inst_name/port_name&gt;</th>
</tr>
</thead>
</table>

### 4.2.12. sbp_disconnect_interface_net

Disconnects an interface pin/port from the interface nets they attached to. Note that any interface pin or interface port can attach to one interface net at the most.

<table>
<thead>
<tr>
<th>Usage</th>
<th>sbp_disconnect_interface_net &lt;pin/port&gt; &lt;pin/port&gt;</th>
</tr>
</thead>
</table>

### 4.2.13. sbp_disconnect_net

Disconnects all of the specified input pins and/or ports from the nets they attached to. Note that any pin or port can attach to one net at the most. Can also be used to disconnect a constant that is connected to a pin/port with connect_constant.

<table>
<thead>
<tr>
<th>Usage</th>
<th>sbp_disconnect_net &lt;pin0&gt; &lt;pin1&gt; &lt;port2&gt;</th>
</tr>
</thead>
</table>

### 4.2.14. sbp_assign_addr_seg

Assigns a memory map between a pair of master and slave interfaces. Range specifies the range of the segment, for example, 32'h0000400, 32'h0001000. Offset specifies the base offset of the range, for example, 32'h0000400

<table>
<thead>
<tr>
<th>Usage</th>
<th>sbp_assign_addr_seg -offset &lt;offset&gt; &lt;slave connection name&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>Example</td>
<td>sbp_assign_addr_seg -offset 32'h00001000 simple/riscv/AHBL_S00</td>
</tr>
</tbody>
</table>

### 4.2.15. sbp_unassign_addr_seg

The Tcl command unsets the fixed offset flag for a memory map allowing the auto_assign Tcl command to assign the memory map offset.

<table>
<thead>
<tr>
<th>Usage</th>
<th>sbp_unassign_addr_seg &lt;slave interface name&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>Example</td>
<td>sbp_unassign_addr_seg simple/spi/AHB_S00</td>
</tr>
</tbody>
</table>

### 4.2.16. sbp_assign_local_memory

Assigns a base address to a local memory map of a master address space.

<table>
<thead>
<tr>
<th>Usage</th>
<th>sbp_assign_local_memory -offset &lt;offset&gt; &lt;master_addr_space&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>Example</td>
<td>sbp_assign_local_memory -offset 'h0050000 Foundation_SoC/riscv/ahbl_m_data_Address_Space</td>
</tr>
</tbody>
</table>

---
4.2.17. sbp_export_pins
Exports a list of pins or interface pins, or all not-yet-connected pins of the components to the top-level port list in the design. The function detects whether or not the argument is pin(s) or component(s). In the two examples below, Example 1 demonstrates a Tcl command to export the pin init_done, while Example 2 demonstrates a Tcl command to export all pins and interfaces of the ddr3 component.

<table>
<thead>
<tr>
<th>Usage</th>
<th>sbp_export_pins &lt;pin/component&gt;</th>
<th>sbp_export_pins (ddr3/init_done)</th>
</tr>
</thead>
</table>

4.2.18. sbp_export_interface
Exports bus interfaces that are passed as arguments to the Tcl command from the component to the top-level component. Example below exports the AHBL_MASTER bus interface of the RISC-V component to the top-level component.

<table>
<thead>
<tr>
<th>Usage</th>
<th>sbp_export_interfaces &lt;interface&gt; &lt;interface&gt; &lt;interface&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>Example</td>
<td>sbp_export_interfaces simple/riscv/AHBL_MASTER</td>
</tr>
</tbody>
</table>

4.2.19. sbp_rename
The rename Tcl command renames objects within the design. The new name of the object and the current hierarchical name of the given object are used as the parameter value. The object can be an interface connection, connection, port, interface, or component. The example below demonstrates the changing of the name of a port in milestone project from CLK to CLOCK.

<table>
<thead>
<tr>
<th>Usage</th>
<th>sbp_rename -name &lt;new name&gt; &lt;object name&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>Example</td>
<td>sbp_rename -name CLOCK milestone/CLK</td>
</tr>
</tbody>
</table>

4.2.20. sbp_replace
The Replace (Re-Config) Tcl command replaces a component with a new configuration for itself. VLNV refers to the newly-generated IP, component name refers to the existing component that is to be replaced, and instance refers to the instance name of the component with new configuration.

<table>
<thead>
<tr>
<th>Usage</th>
<th>sbp_replace -vlnv &lt;VLNV&gt; -name &lt;instance&gt; -component &lt;component name&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>Example</td>
<td>sbp_replace -vlnv lattice:ip:ahblite_bus_0:1.1 -name ahbl_bus_0 -component simple/ahblite</td>
</tr>
</tbody>
</table>

4.2.21. sbp_copy
Copies objects, IP instances and nets, from the current or other open sbp designs to the current sbp design. All objects are post-fixed with a postfix string. For example, you can write TCL code below to duplicate the components and connections with new instance names post fixed with X, by calling copy on all the components, ports and nets. Pins are automatically duplicated while the components are duplicated.

<table>
<thead>
<tr>
<th>Usage</th>
<th>sbp_copy -postfix &lt;postfixString&gt; objects</th>
</tr>
</thead>
<tbody>
<tr>
<td>Example</td>
<td>sbp_copy –postfix X $selected_objs</td>
</tr>
</tbody>
</table>
4.2.22. sbp_delete

Deletes objects, IP instances and nets, from the current sbp design. In the examples below, Example 1 demonstrates a Tcl command to delete a port, while Example 2 demonstrates a Tcl command to delete ddr3 component.

<table>
<thead>
<tr>
<th>Usage</th>
<th>Sbp_delete objects -type &lt;type name&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>Example 1</td>
<td>sbp_delete [sbp_get_ports &lt;clock&gt;] -type port</td>
</tr>
<tr>
<td>Example 2</td>
<td>sbp_delete (ddr3) -type component</td>
</tr>
</tbody>
</table>

4.2.23. sbp_get_pins

Gets a list of pin names that match a pattern string, and/or the pins that are associated with an object. The object in the [-from <objectName>] option can be a net or a component. The example below gets the clk pin from the interconnect IP.

<table>
<thead>
<tr>
<th>Usage</th>
<th>sbp_get_pins [-from &lt;object Name&gt;] [pattern]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Example</td>
<td>sbp_get_pins -from ahblite_interconnect clk</td>
</tr>
</tbody>
</table>

4.2.24. sbp_get_interface_pins

Gets a list of interface names that match a pattern string, and/or the interfaces that are associated with an object. The object in the [-from <objectName>] option can be an interface net or a component. The example below can get all AHB-Lite slave interface pins from the interconnect IP.

<table>
<thead>
<tr>
<th>Usage:</th>
<th>sbp_get_interface_pins [-from &lt;objectName&gt;] [pattern]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Example:</td>
<td>sbp_get_interface_pins -from ahblite_interconnect S*_AHB</td>
</tr>
</tbody>
</table>

4.2.25. sbp_get_ports

Get a list of the names of ports that match a pattern string, and/or the ports that are associated with an object. The object in the [-from <objectName>] option can be a net.

<table>
<thead>
<tr>
<th>Usage</th>
<th>sbp_get_ports [-from &lt;objectName&gt;] [pattern]</th>
</tr>
</thead>
</table>

4.2.26. sbp_get_interface_ports

Gets a list of interface names that match a pattern string, and/or the interface ports that are associated with an object. The object in the [-from <objectName>] option can be an interface net.

<table>
<thead>
<tr>
<th>Usage</th>
<th>sbp_get_interface_ports [-from &lt;objectName&gt;] [pattern]</th>
</tr>
</thead>
</table>

4.2.27. sbp_get_nets

Gets a list of net names that match a pattern string, and/or the nets that are associated with an object. The object in the [-from <objectName>] option can be a pin or a port.

<table>
<thead>
<tr>
<th>Usage</th>
<th>sbp_get_nets [-from &lt;objectName&gt;] [pattern]</th>
</tr>
</thead>
</table>

4.2.28. sbp_get_interface_nets

Gets a list of interface net names that match a pattern string, and/or the interface nets that are associated with an object. The object in the [-from <objectName>] option can be an interface pin or an interface port.

| Usage          | sbp_get_interface_nets [-from <objectName>] [pattern] |
4.2.29. sbp_set_property

Sets the properties of an input object. The first argument is a list of name value pairs. We have a list of parameters because the GUI IP configuration dialog submits changes to many parameters of an IP component at the same time when the dialog is closed. In the examples below, Example 1 changes the data width of the RAM block named "ebr_0", while Example 2 changes the number of master interfaces to two and number of slave interface to three on AHB-Lite interconnect block named "ahbl_interconnect".

<table>
<thead>
<tr>
<th>Usage</th>
<th>sbp_set_property &lt;name0 value0 name1 value1 ...&gt; object</th>
</tr>
</thead>
<tbody>
<tr>
<td>Example 1</td>
<td>sbp_set_property {datawidth 32} {test/ebr_0}</td>
</tr>
<tr>
<td>Example 2</td>
<td>sbp_set_property {NUM_MI 2 NUM_SI 3} test/ahbl_interconnect</td>
</tr>
</tbody>
</table>

4.2.30. sbp_get_property

Gets the property of the object. The example below is to get the number of slave interfaces of AHB-Lite interconnect block named “ahbl_interconnect_0”.

<table>
<thead>
<tr>
<th>Usage</th>
<th>sbp_get_property &lt;parameter name&gt; &lt;object&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>Example</td>
<td>sbp_get_property NUM_SI ahbl_interconnect_0</td>
</tr>
</tbody>
</table>

4.2.31. sbp_report_properties

Prints all the properties and values associated to the type of the object.

<table>
<thead>
<tr>
<th>Usage</th>
<th>sbp_report_properties object</th>
</tr>
</thead>
<tbody>
<tr>
<td>Example</td>
<td>sbp_report_properties ahbl_interconnect</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Outputs</th>
<th>Name: ahbl_interconnect</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>NUM_SI: 1</td>
</tr>
<tr>
<td></td>
<td>NUM_MI: 2</td>
</tr>
<tr>
<td></td>
<td>DATA_WIDTH: 32</td>
</tr>
<tr>
<td></td>
<td>ADDRESS_WIDTH: 32</td>
</tr>
</tbody>
</table>

4.2.32. sbp_get_components

Gets a list of component names that match a pattern string, and/or the components that are associated with an object. The default pattern string is a wildcard "*" that matches all components. The pattern string may consist of string segments and wildcards. The example below returns all the component names that contain “interconnect”. The command returns an empty string if no match is found.

<table>
<thead>
<tr>
<th>Usage</th>
<th>sbp_get_components &lt;component name&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>Example</td>
<td>sbp_get_components {<em>interconnect</em>}</td>
</tr>
</tbody>
</table>

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Appendix A. metadata.xsd

<?xml version="1.0" encoding="gb2312"?>
<!-- IP Metadata Schema 0.0.5 -->
<!--
Change Log:
  0.0.0  21-Jul-2016 initial revision.
  0.0.1  22-Jul-2016 1. removed enum_value from <setting> 2. change value_mapping to scriptType
  0.0.2  29-Jul-2016 1. removed GUI out of metadata scope
  0.0.3  30-Jul-2016 1. add value list support
  0.0.4  07-Jan-2021 1. new features in Radiant 3.0
  0.0.5  06-Apr-2021 1. fully support Verilog macro
-->
<x:schema xmlns:xs="http://www.w3.org/2001/XMLSchema"
  targetNamespace="http://www.latticesemi.com/XMLSchema/Radiant/ip"
  xmlns:lsccip="http://www.latticesemi.com/XMLSchema/Radiant/ip"
  elementFormDefault="qualified"
  attributeFormDefault="unqualified">
  <xs:import schemaLocation="xml.xsd"
  <xs:include schemaLocation="busInterface.xsd"/>
  <xs:include schemaLocation="memoryMap.xsd"/>
  <xs:include schemaLocation="file.xsd"/>
  <xs:include schemaLocation="generator.xsd"/>
  <xs:include schemaLocation="design.xsd"/>

  <xs:attributeGroup name="ipany.att">
    <xs:anyAttribute processContents="lax"/>
  </xs:attributeGroup>
<!-- version string type definition-->
  <xs:simpleType name="threeFigureVersionType">
    <xs:annotation>
      <xs:documentation>The syntax for version string.</xs:documentation>
    </xs:annotation>
    <xs:restriction base="xs:string">
    </xs:restriction>
  </xs:simpleType>

  <xs:simpleType name="twoFigureVersionType">
    <xs:annotation>
      <xs:documentation>The syntax for Radiant version string.</xs:documentation>
    </xs:annotation>
    <xs:restriction base="xs:string">
      <xs:pattern value="[0-9]+\.[0-9]+"/>
    </xs:restriction>
  </xs:simpleType>

  <xs:simpleType name="scriptType"
Any python expressions. Could be a simple const variable like

```
&quote;1&quote;, or a tuple &quote;(0, 10)&quote;, or a function call
&quote;user_func1()&quote;, or a complex expression &quote;a==12&quote;
```

Is this setting variable for parameter of IP core module, verilog macro, or just for user input?

Valid values are &quote;input&quote;, &quote;verilog_macro&quote;, &quote;param&quote;, and &quote;command&quote.;

Specify what is used to name the Verilog macro, ID or Value?

Valid values are &quote;id&quote; and &quote;value&quote;.

Value type of setting variable. Valid types are &quote;bool&quote;, &quote;string&quote; and &quote;int&quote;,
<xs:complexType name="settingsType">
    <xs:sequence>
        <xs:element minOccurs="0" maxOccurs="unbounded" name="setting" type="lsccip:settingElementType" />
    </xs:sequence>
    <xs:attribute ref="xml:base" use="optional" />
</xs:complexType>

<!-- ip.ports.port -->
<xs:complexType name="portElementType">
    <xs:annotation>
        <xs:documentation>IP port definition.</xs:documentation>
    </xs:annotation>
    <xs:attribute name="name" type="xs:string" use="required" />
    <xs:attribute name="dir" type="xs:string" use="required" />
    <xs:attribute name="conn_mod" type="xs:string" use="required" />
    <xs:attribute name="conn_port" type="xs:string" use="optional" />
    <xs:attribute name="conn_range" type="xs:string" use="optional" />
    <xs:attribute name="range" type="lsccip:scriptType" use="optional" />
    <xs:attribute name="stick_high" type="lsccip:scriptType" use="optional" />
    <xs:attribute name="stick_low" type="lsccip:scriptType" use="optional" />
    <xs:attribute name="stick_value" type="lsccip:scriptType" use="optional" />
    <xs:attribute name="dangling" type="lsccip:scriptType" use="optional" />
    <xs:attribute name="bus_interface" type="xs:string" use="optional" />
    <xs:attribute name="attribute" type="lsccip:scriptType" use="optional" />
    <xs:attribute name="port_type" use="optional" default="data">false</xs:attribute>
</xs:complexType>
<xs:restriction base="xs:string">
  <xs:enumeration value="data"></xs:enumeration>
  <xs:enumeration value="reset"></xs:enumeration>
  <xs:enumeration value="clock"></xs:enumeration>
</xs:restriction>
</xs:simpleType>
</xs:attribute>
<xs:attribute ref="xml:base" use="optional"/>
</xs:complexType>
<!-- ip.outFileConfigs -->
<xs:complexType name="outFileConfigsType">
  <xs:sequence>
    <xs:element maxOccurs="unbounded" name="fileConfig" type="lsccip:fileConfigType" />
  </xs:sequence>
</xs:complexType>
<!-- ip.outFileConfigs.fileConfig -->
<xs:complexType name="fileConfigType">
  <xs:annotation>
    <xs:documentation>Configure output file</xs:documentation>
  </xs:annotation>
  <xs:attribute name="name" type="xs:string" use="required" />
  <xs:attribute name="use" use="optional" default="merge">
    <xs:annotation>
      <xs:documentation>
        Merge the new attributes to existing configuration or replace all
      </xs:documentation>
    </xs:annotation>
    <xs:simpleType>
      <xs:restriction base="xs:string">
        <xs:enumeration value="merge"></xs:enumeration>
        <xs:enumeration value="replace"></xs:enumeration>
      </xs:restriction>
    </xs:simpleType>
  </xs:attribute>
  <xs:attribute name="type" use="optional" default="file">
    <xs:annotation>
      <xs:documentation>
        Indicate the item is generate a file or directory
      </xs:documentation>
    </xs:annotation>
    <xs:simpleType>
      <xs:restriction base="xs:string">
        <xs:enumeration value="file"></xs:enumeration>
        <xs:enumeration value="directory"></xs:enumeration>
      </xs:restriction>
    </xs:simpleType>
  </xs:attribute>
  <xs:attribute name="description" type="xs:string" use="optional">
  </xs:attribute>
  <xs:attribute name="enable_output" type="xs:string" use="optional" default="True">
  </xs:attribute>
<xs:annotation>
  <xs:documentation>
  Python expression represent a boolean value to indicate the output is enabled or disabled
  </xs:documentation>
</xs:annotation>

<xs:attribute name="phase" type="xs:int" use="optional">
  default="0">
</xs:attribute>

<xs:attribute name="file_base_name" type="xs:string" use="optional">
</xs:attribute>

<xs:attribute name="file_suffix" type="xs:string" use="optional">
</xs:attribute>

<xs:attribute name="sub_dir" type="xs:string" use="optional">
</xs:attribute>

<xs:attribute name="file_generator" type="xs:string" use="optional">
</xs:attribute>

<xs:attribute name="src_dir" type="xs:string" use="optional">
</xs:attribute>

<xs:attribute name="dest_dir" type="xs:string" use="optional">
</xs:attribute>

<xs:attribute name="src_file" type="xs:string" use="optional">
</xs:attribute>

<xs:attribute name="export" use="optional" default="input_only">
  <xs:annotation>
    <xs:documentation>
    Indicate export all setting items or input only
    </xs:documentation>
  </xs:annotation>
  <xs:simpleType>
    <xs:restriction base="xs:string">
      <xs:enumeration value="all"></xs:enumeration>
      <xs:enumeration value="input_only"></xs:enumeration>
    </xs:restriction>
  </xs:simpleType>
</xs:attribute>

<xs:attributeGroup ref="lsccip:ipany.att"/>

<!-- ip.interface -->
<xs:complexType name="portsType">
  <xs:sequence>
    <xs:element maxOccurs="unbounded" minOccurs="1" name="port" type="lsccip:portElementType" />
  </xs:sequence>
</xs:complexType>
<xs:complexType name="generalType">
  <xs:sequence>
    <xs:element maxOccurs="1" minOccurs="0" name="vendor" type="xs:string" />
    <xs:element maxOccurs="1" minOccurs="0" name="library" type="xs:string" />
    <xs:element maxOccurs="1" minOccurs="1" name="name" type="xs:string" />
    <xs:element maxOccurs="1" minOccurs="0" name="display_name" type="xs:string" />
    <xs:element maxOccurs="1" minOccurs="1" name="version" type="xs:string" />
    <xs:element maxOccurs="1" minOccurs="1" name="category" type="xs:string" />
    <xs:element maxOccurs="1" minOccurs="0" name="keywords" type="xs:string" />
    <xs:element maxOccurs="1" minOccurs="0" name="type" type="xs:string" />
    <xs:element maxOccurs="1" minOccurs="0" name="instantiatedOnce" type="xs:boolean" />
    <xs:element maxOccurs="1" minOccurs="1" name="min_radiant_version" type="lsccip:twoFigureVersionType" />
    <xs:element maxOccurs="1" minOccurs="0" name="max_radiant_version" type="lsccip:twoFigureVersionType" />
    <xs:element maxOccurs="1" minOccurs="0" name="min_esi_version" type="lsccip:twoFigureVersionType" />
    <xs:element maxOccurs="1" minOccurs="0" name="max_esi_version" type="lsccip:twoFigureVersionType" />
    <xs:element maxOccurs="1" minOccurs="0" name="supported_products" type="lsccip:supportedProductsType" />
    <xs:element maxOccurs="1" minOccurs="0" name="supported_platforms" type="lsccip:supportedPlatformsType" />
  </xs:sequence>
</xs:complexType>

<xos:complexType name="supportedPlatformsType">
  <xs:sequence>
    <xs:element maxOccurs="unbounded" minOccurs="1" name="supported_platform" type="lsccip:supportedPlatformType" />
  </xs:sequence>
</xs:complexType>

<xos:complexType name="supportedPlatformType">
  <xs:sequence>
    <xs:element maxOccurs="unbounded" minOccurs="0" name="supported_templates" type="lsccip:supportedTemplatesType" />
    <xs:attribute name="name" type="xs:string" />
  </xs:sequence>
</xs:complexType>

<xos:complexType name="supportedTemplatesType">
  <xs:sequence>
  </xs:sequence>
</xs:complexType>
<xs:element maxOccurs="unbounded" minOccurs="0" name="supported_template" type="lsccip:supportedTemplateType" />
</xs:sequence>
</xs:complexType>

<xs:complexType name="supportedTemplateType">
  <xs:attribute name="processor" type="xs:string" />
  <xs:attribute name="family" type="xs:string" />
  <xs:attribute name="name" type="xs:string" />
  <xs:attribute name="version" type="xs:string" use="optional" />
</xs:complexType>

<xs:complexType name="supportedProductsType">
  <xs:sequence>
    <xs:element maxOccurs="unbounded" minOccurs="1" name="supported_family" type="lsccip:supportedFamilyType" />
  </xs:sequence>
</xs:complexType>

<xs:complexType name="supportedFamilyType">
  <xs:sequence>
    <xs:element maxOccurs="unbounded" minOccurs="0" name="supported_device" type="lsccip:supportedDeviceType" />
  </xs:sequence>
  <xs:attribute name="name" type="xs:string" />
</xs:complexType>

<xs:complexType name="supportedDeviceType">
  <xs:sequence>
    <xs:element maxOccurs="unbounded" minOccurs="0" name="supported_speed_grade" type="lsccip:supportedSpeedType" />
  </xs:sequence>
  <xs:attribute name="name" type="xs:string" />
</xs:complexType>

<xs:complexType name="supportedSpeedType">
  <xs:sequence>
    <xs:element maxOccurs="unbounded" minOccurs="0" name="supported_package" type="lsccip:supportedPackageType" />
  </xs:sequence>
  <xs:attribute name="name" type="xs:string" />
</xs:complexType>

<xs:complexType name="supportedPackageType">
  <xs:attribute name="name" type="xs:string" />
</xs:complexType>

<!-- ip.estimatedResources -->
<xs:complexType name="estimatedResourcesType">
  <xs:annotation>
    <xs:documentation>
      IP estimated resources definition.
    </xs:documentation>
  </xs:annotation>
</xs:complexType>
<xs:sequence>
  <xs:element name="estimatedResource" type="lsccip:estimatedResourceType"
  minOccurs="1" maxOccurs="unbounded"/>
</xs:sequence>
</xs:complexType>

<xs:complexType name="estimatedResourceType">
  <xs:sequence>
    <xs:element name="name" type="xs:string"/>
    <xs:element name="number" type="xs:string"/>
  </xs:sequence>
</xs:complexType>

<!-- ip -->
<xs:element name="ip">
  <xs:complexType>
    <xs:sequence>
      <xs:element name="general" type="lsccip:generalType"/>
      <xs:element name="settings" type="lsccip:settingsType"/>
      <xs:element name="ports" type="lsccip:portsType"/>
      <xs:element name="outFileConfigs" type="lsccip:outFileConfigsType"
      maxOccurs="1" minOccurs="0">
        <xs:unique name="fileCfgKey">
          <xs:selector xpath="lsccip:fileConfig"/>
          <xs:field xpath="@name"/>
        </xs:unique>
      </xs:element>
      <xs:element ref="lsccip:busInterfaces" minOccurs="0"/>
      <xs:element ref="lsccip:addressSpaces" minOccurs="0"/>
      <xs:element ref="lsccip:memoryMaps" minOccurs="0"/>
      <xs:element ref="lsccip:componentGenerators" minOccurs="0"/>
      <xs:element ref="lsccip:choices" minOccurs="0"/>
      <xs:element ref="lsccip:fileSets" minOccurs="0"/>
      <xs:element ref="lsccip:design" minOccurs="0"/>
    </xs:sequence>
  </xs:complexType>
</xs:element>
</xs:schema>
References

- Lattice Propel 2022.1 SDK User Guide (FPGA-UG-02176)
- Lattice Propel 2022.1 Installation for Windows Usage Guide (FPGA-AN-02056)
- Lattice Propel 2022.1 Installation for Linux User Guide (FPGA-AN-02057)
- Lattice Diamond Online Help
- Lattice Radiant Online Help
Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.
# Revision History

## Revision 1.0, November 2022

<table>
<thead>
<tr>
<th>Section</th>
<th>Change Summary</th>
</tr>
</thead>
<tbody>
<tr>
<td>All</td>
<td>Production release.</td>
</tr>
</tbody>
</table>