MIPI D-PHY Module - Lattice Radiant Software

User Guide

FPGA-IPUG-02061-1.2

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
CIL	Control Interface Logic
CSI	Camera Serial Interface
DSI	Display Serial Interface
FPGA	Field-Programmable Gate Array
IP	Intellectual Property
LMMI	Lattice Memory Mapped Interface
PLL	Phase-locked Loop

1. Introduction

1.1. Overview

MIPI D-PHY bus is a physical serial data communication layer on which the protocols like CSI-2 (Camera Serial Interface 2), DSI (Display Serial Interface) runs. It physically connects the camera sensor to the application processor (for CSI-2) and application processor to the display device (for DSI) as shown in the Figure 1.1.

The Lattice Semiconductor MIPI D-PHY IP incorporates one clock lane and configurable number of data transmission lanes. The MIPI D-PHY IP supports 1, 2, 3, 4 data lanes.

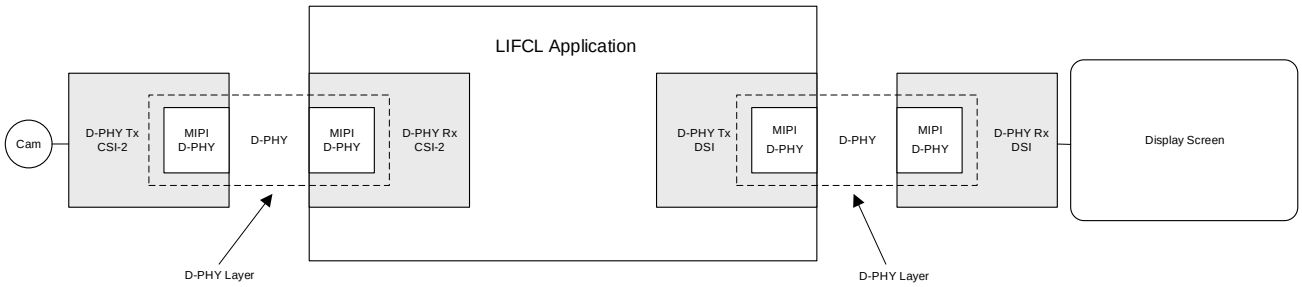

Figure 1.1. MIPI D-PHY Module

Every data lane of the transmitter/receiver consists of two wires (differential pair or two single-ended): d_p_io and d_n_io. The clock lane consists of clk_p_io and clk_n_io (differential pair or two single-ended). Data transmission occurs on these paired wires connecting receiver and transmitter communicating modules.

The Lattice Radiant® Software Place and Route tool integrated with the Synplify Pro® or LSE synthesis tools is used for implementation of the design. The design can be used with CrossLink™-NX and Certus™-NX FPGA devices.

1.2. Features

Features General for both Hard and Soft MIPI D-PHY IP:

- Interfaces to MIPI CSI-2/DSI, Rx and Tx Devices
- Supports Unidirectional HS (High-Speed) operation mode
- Supports Bidirectional LP (Low Power) operation modes
- Deserializes and Serializes HS data into byte data packets
- Provides methods for contention detection and termination switching
- Supports 1, 2, 3, 4 data lanes and one clock lane
- Configurable Rx/Tx
- External reference clock source

Hard MIPI D-PHY IP:

- Maximum rate is up to 2500 Mbps per lane
- Supported gearing – 8x, 16x
- Configurable via LMMI PLL settings
- Bypass CIL Mode
- Continues/Non-continuous DPHY Clock Mode
- Reference Clock Frequency to MIPI PLL 24 MHz to 200 MHz
- Interface Clock Frequency 40 MHz to 1250 MHz

Soft MIPI D-PHY IP:

- Supported rate is up to 1500 Mbps per lane
- Supported gearing 8x
- *MIPI_DPHY* I/O type
- Interface Clock Frequency 40 MHz to 750 MHz

1.3. Conventions

1.3.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.3.2. Signal Names

Signal names that end with:

- *_n* are active low
- *_i* are input signals
- *_o* are output signals
- *_io* are bi-directional input/output signals

2. Functional Description

2.1. Overview

Depending on the configuration set from Attribute Table (see Table 2.2), the internal resources of MIPI D-PHY Module allow you to configure it either as a hard MIPI D-PHY Tx, a hard MIPI D-PHY Rx, a soft MIPI D-PHY Tx, or a soft MIPI D-PHY Rx (see Figure 2.1).

Regardless of the implementation, the MIPI D-PHY Module provides the same external interface.

The generated MIPI D-PHY Tx/Rx Module wrapper is used to make a connection between the hard D-PHY Module and higher protocol layers.

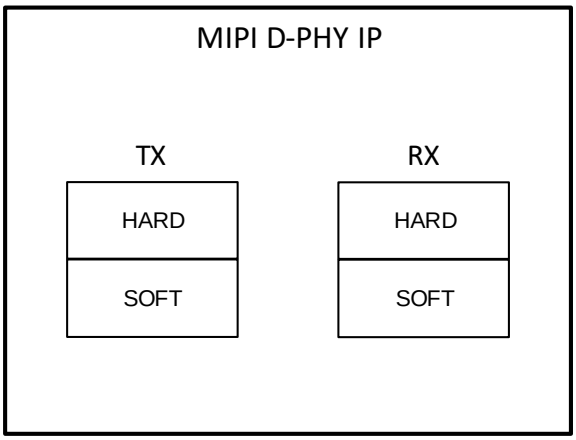

Figure 2.1. MIPI D-PHY

Each Lane of MIPI D-PHY Module includes both the HS and LP modes.

The HS Modules operate in a differential manner. They utilize the low voltage swing of the payload data signals to transfer the information. It contains an on-die termination between Dp and Dn. The Low power module, an unterminated module, operate in single ended manner.

For transmitting the payload data (image data), the all type of MIPI D-PHY Module-s use the high-speed modules, whereas for transmitting the control and status information the all type of MIPI D-PHY IP-s use the low power modules utilizing low frequency signals.

The bandwidth can be increased by increasing the number of data lanes. By increasing the number of lanes, the same quantity of data can be transmitted on multiple lanes in lesser time. MIPI D-PHY Module uses forward source synchronous clock, which is used by all the data lanes of MIPI D-PHY receiver for capturing the high-speed data signals.

The Hard MIPI D-PHY represents Universal Lane Module, which incorporates D-PHY Lane I/O Buffers Module on the Lane Side and Control Interface Logic (CIL) as shown in Figure 2.2.

D-PHY Lane I/O Buffers Module includes high-speed differential transmitter (HS-Tx), high-speed differential receiver (HS-Rx), low power single-ended transmitter (LP-Tx), low power single-ended receiver (LP-Rx) and low power contention detector (LP-CD).

Control Interface Logic controls the operation of D-PHY Lane I/O Buffers Module and provides the PHY-Protocol Interface (PPI) logic, which includes set of signals to cover the functionality of the Lane and interface to the protocol level side. The CIL functions depend on the Lane type and Lane side.

The HS-TX and the HS-RX within a single Lane Module are never enabled simultaneously during normal operation.

The LP-CD function is required for bi-directional operation. The LP-CD function is enabled to detect contention situations while the LP-TX is driving Low-Power states. The LP-CD checks for contention before driving a new state on the line.

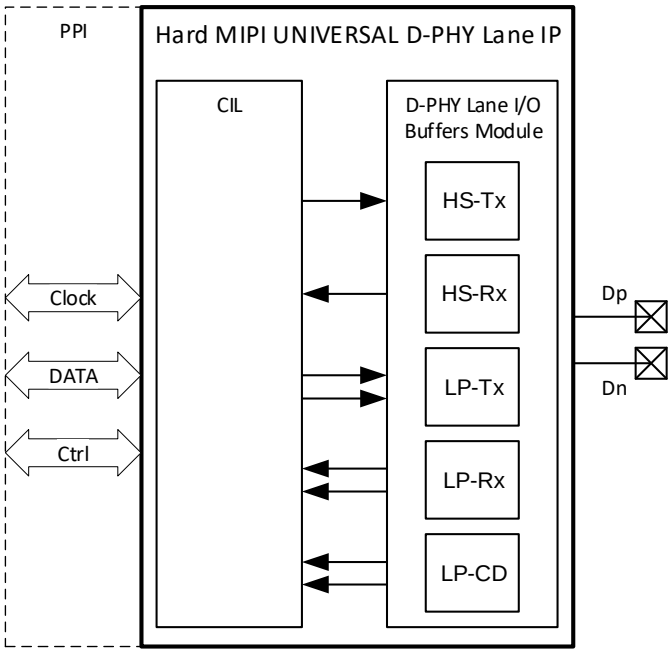

Figure 2.2. Hard MIPI D-PHY IP Universal Lane

2.1.1. Operation Mode

The Global Operation Module controls HS request path and timing using attributes in Table 2.2.

This module controls the timing entering HS and coming from HS entering to LP. Figure 2.3 shows the LP-to-HS transition flow diagram for data lanes.

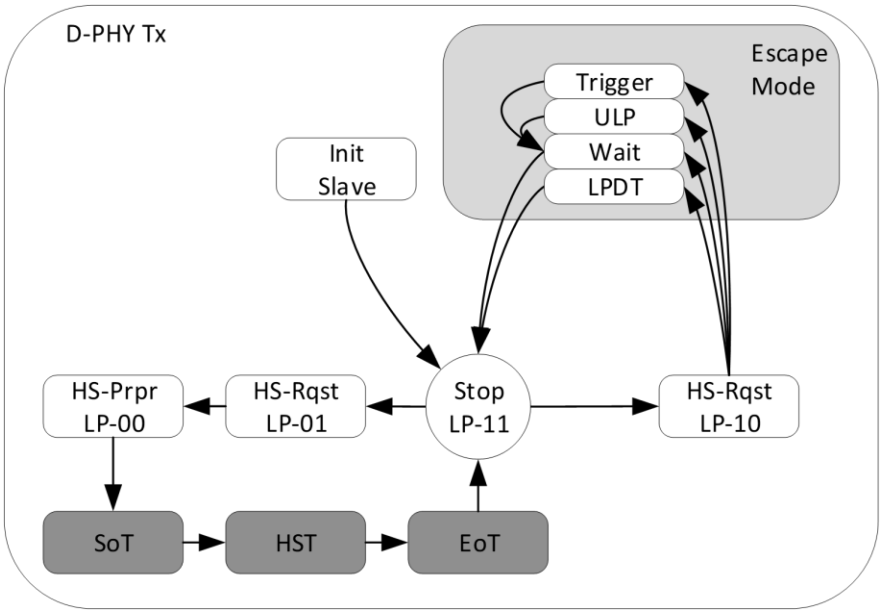

Figure 2.3. MIPI D-PHY Tx LP to HS Transition Flow Diagram on Data Lanes

During normal operation, a Data Lane is either in control mode or in high-speed mode.

For sending payload data (the image data), the transmitter drives a particular sequence on data lanes to enter the receiver from the low power mode to high-speed mode.

As part of the initialization of D-PHY, initially all the lanes are held at LP11 state for a specified time. This LP11 state is also known as stop state. After this, for sending the image data, the transmitter drives a particular sequence on the receiver to enter the receiver lanes from the low power mode to high-speed mode. The high-speed entry sequence, see Figure 2.4, consists of driving LP11->LP01->LP00 (LP->HS transition) on the differential lane. On successful reception of this sequence, the high-speed receiver module enables its termination to receive the high-speed differential data.

After LP-to-HS transition, the transmitter sends HS Zeros (V(Dn)>V(Dp)) for a specified amount of time to make sure that the receiver is enabled properly before any payload data is transmitted.

Before the payload data of every HS burst on each lane, the transmitting D-PHY inserts a sync sequence (00011101). This sync sequence is used by the data lanes of the receiving D-PHY to establish synchronization with the high-speed payload data.

The LP11 state brings back the data lane from high-speed mode to low power mode.

After every HS burst, the data lanes go to LP11 state. A single HS burst represents the image data corresponding to one of the horizontal lines of an image and the LP11 state in-between the HS bursts represents the blanking periods.

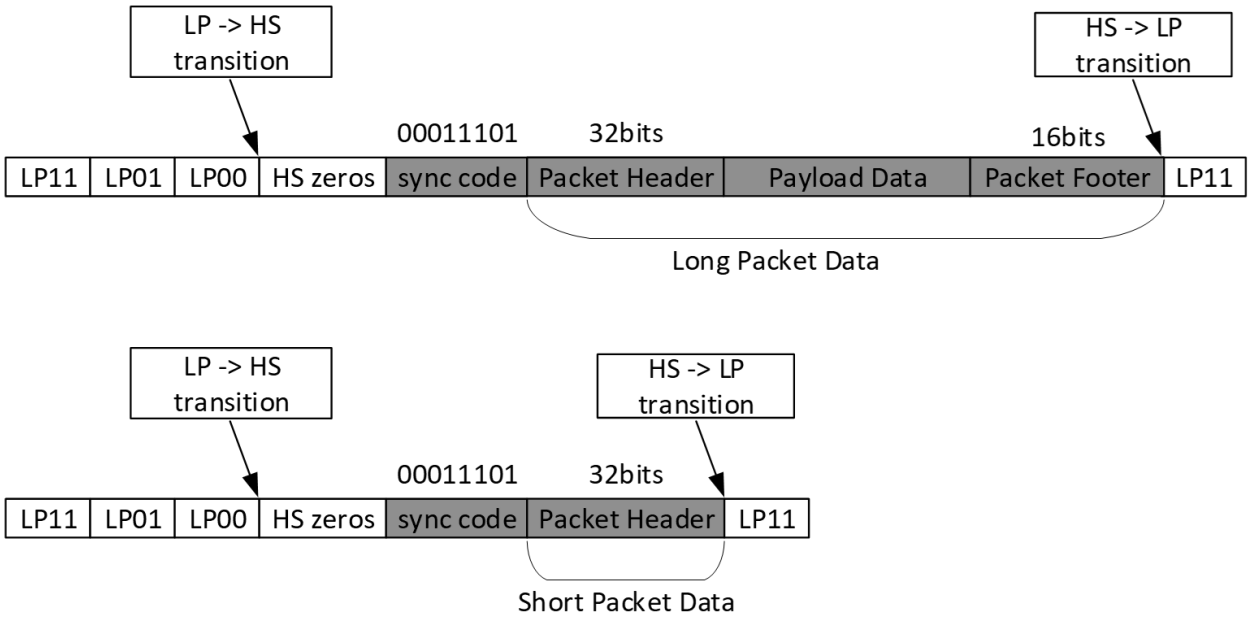

Figure 2.4. High-Speed Entry Sequence and Payload Data Transmission Cycle on Data Lanes.

2.1.2. LMMI Interface

The LMMI (Lattice Memory Mapped Interface) Slave Module is used for configuring the control registers of the Hard MIPI D-PHY Module. For pin connections, see Table 2.2.

For more information on LMMI, see Lattice Memory Mapped Interface and Lattice Interrupt Interface User Guide (FPGA-UG-02039).

2.2. Signal Description

A list of Input and Output signals along with their descriptions is shown in Table 2.1.

Table 2.1. MIPI D-PHY Module Port Descriptions

Port Name	Direction	Mode/Configuration	Description
Clock and Reset			
clk_byte_o	Out	—	Byte clock
sync_clk	In	—	GDDR SYNC reference clock
clk_p_io, clk_n_io	In/Out	—	MIPI D-PHY clock lane.
lp_tx_clk_p_i	In	Available when Interface Type is *Transmitter*.	Low power transmit positive lane data
lp_tx_clk_n_i	In	Available when Interface Type is *Transmitter*.	Low power transmit negative lane data
lmmi_clk_i	In	—	LMMI Interface clock.
lmmi_resetn_i	In	—	Active low signal to reset the configuration registers.
sync_rst_i	In	—	GDDR SYNC reset
LMMI Interface			
lmmi_request_i	In	—	Start transaction.
lmmi_wr_rdn_i	In	—	Write = HIGH, Read = LOW
lmmi_offset_i[4:0]	In	—	Register offset, starting at offset 0.
lmmi_wdata_i[3:0]	In	—	Write data
lmmi_rdata_o[3:0]	Out	—	Read data
lmmi_rdata_valid_o	Out	—	Read transaction is complete and lmmi_rdata_o[] contains valid data.
lmmi_ready_o	Out	—	Slave is ready to start a new transaction. Slave can insert wait states by holding this signal low.
MIPI D-PHY High-Speed Tx			
hs_tx_en_i	In	Available when Interface Type is *Transmitter*.	High-speed transmit mode enable
hs_tx_data_i[DW[1]-1:0]	In	Available when Interface Type is *Transmitter*.	High-speed transmit data
hs_tx_data_en_i	In	Available when Interface Type is *Transmitter*.	High-speed transmit data enable
MIPI D-PHY High-Speed Rx			
hs_rx_en_i	In	Available when Interface Type is in *Receiver*.	High-speed receive mode enable
hs_rx_data_o[DW[1]-1:0]	Out	Available when Interface Type is in *Receiver*.	High-speed receive data. The data is gated by *clk_byte_o* clock.
hs_rx_data_sync_o[BUS_WIDTH – 1:0]	Out	Available when Interface Type is *Receiver*.	Produces a pulse when de-serializer detects sync char(B8). On negedge of the pulse the bus *hs_rx_data_o* contains a valid data.
hs_tx_cil_ready_o[NUM_of_LANES – 1:0]	Out	Available when Interface Type is *Transmitter* and *DPHY Mode = CIL Bypassed*	This active high signal indicates that TxDataHS is accepted by the corresponding lane to be serially transmitted.
data_lane_ss_o[NUM_of_LANES – 1:0]	Out	Available when Interface Type is *Receiver* and *DPHY Mode = CIL Bypassed*	This active high signal indicates that the corresponding lane is currently in Stop state.

Port Name	Direction	Mode/Configuration	Description
MIPI D-PHY Low Power Tx			
lp_tx_data_p_i[BUS_WIDTH – 1:0]	In	Available when Interface Type is *Transmitter*.	Low power transmit data
lp_tx_data_n_i[BUS_WIDTH – 1:0]	In	Available when Interface Type is *Transmitter*.	Low power transmit data
lp_tx_data_en_i	In	Available when Interface Type is *Transmitter*.	Low power transmit data enable
MIPI D-PHY Low Power Rx			
lp_rx_en_i	In	Available when Interface Type is *Receiver*.	Low power receive mode enable
lp_rx_clk_p_o	Out	Available when Interface Type is *Receiver*.	Low power receive positive lane data
lp_rx_clk_n_o	Out	Available when Interface Type is *Receiver*.	Low power receive positive lane data
lp_rx_data_p_o[BUS_WIDTH – 1:0]	Out	Available when Interface Type is *Receiver*.	Low power receive data positive
lp_rx_data_n_o[BUS_WIDTH – 1:0]	Out	Available when Interface Type is *Receiver*.	Low power receive data negative
MIPI DPHY			
data_p_io[NUM_of_LANES – 1:0], data_n_io[NUM_of_LANES – 1:0]	In/Out	—	MIPI D-PHY data lanes
Misc			
pll_clockop_i	In	Available when Interface Type is *Transmitter* and DPHY PLL Mode is *External*.	Input clock from external PLL
pll_clockos_i	In	Available when Interface Type is *Transmitter* and DPHY PLL Mode is *External*.	90 degree shifted input clock from external PLL
pd_dphy_i	In	—	Power down
ready_o	Out	—	Ready from DPHY or from PLL

Notes:

1. DW = BUS_WIDTH* GEAR
2. *BUS_WIDTH* – Number of D-PHY Lanes, 1, 2, 4 (available on GUI)
3. *GEAR* – Number of bits to be transferred

2.3. Attribute Summary

MIPI D-PHY Module Configuration Attributes summary is shown in Table 2.2. All attributes can be configured from the General tab of the Lattice Radiant Software user interface.

Table 2.2. Attributes Summary

Attribute	Selectable Values	Value Entry Format	Defaults	Dependency On Other Attributes	Additional Requirements
Interface Type	Transmitter, Receiver	Pull-down Menu	Receiver	—	—
MIPI Interface Mode	CSI2, DSI	Pull-down Menu	CSI2	—	—
DPHY Module Type	Hard MIPI DPHY, Soft MIPI DPHY	Pull-down Menu	Hard MIPI DPHY	Hard MIPI DPHY is only available on Crosslink-NX devices.	—
Hard DPHY Mode	CIL Bypassed, CIL Enabled	Pull-down Menu	CIL Bypassed	Configuration Type = Hard MIPI DPHY	—
DPHY PLL Mode	Internal, External	Pull-down Menu	External	Interface Type = Transmitter	—
DPHY Clock Mode	Continuous, Non-continuous	Pull-down Menu	Continuous	Configuration Type = Hard MIPI DPHY	—
Interface Clock Frequency (MHz)	40 – 750	Real Number Field	160 MHz	Configuration Type = Soft MIPI DPHY	—
	40 – 1250			Configuration Type = Hard MIPI DPHY	
Interface Data Rate (Mbps)	80 – 1500	Calculated	320 Mbps	Configuration Type = Soft MIPI DPHY	Display for information only
	80 – 2500			Configuration Type = Hard MIPI DPHY	
Gearing Ratio	For Soft – 8 For Hard - 8, 16	Pull-down Menu	8	Interface Type = Receiver	—
	For Soft 8 For Hard – 8, 16			Interface Type = Transmitter	
Bus Width	1, 2, 4	Integer Field	1	—	—
Reference Clock Frequency (MHz)	24 - 200	Integer Field	24	Interface Type = Transmitter	—

2.4. Register Description

All Configuration registers (MIPI programmable bits) in Table 2.3 are controlled through LMMI bus.

Table 2.3. Configuration Registers (MIPI Programmable Bits)

Offset	Bit[3]	Bit[2]	Bit[1]	Bit[0]
0x0	HSEL	AUTO_PD_EN	MASTER_SLAVE	DSI_CSI
0x1	RXCDRP[1]	RXCDRP[0]	RSEL[1]	RSEL[0]
0x2	EN_CIL	RXLPRP[2]	RXLPRP[1]	RXLPRP[0]
0x3	TST[0]	PLLCLKBYPASS	LOCK_BYP	DESKEW_EN
0x4	CN[0]	TST[3]	TST[2]	TST[1]
0x5	CN[4]	CN[3]	CN[2]	CN[1]
0x6	CM[3]	CM[2]	CM[1]	CM[0]
0x7	CM[7]	CM[6]	CM[5]	CM[4]
0x8	TxDataWidthHS[0]	CO[2]	CO[1]	CO[0]
0x9	Lane0_sel[0]	RxDataWidthHS[1]	RxDataWidthHS[0]	TxDataWidthHS[1]
0x10	uc_PRG_RXHS_SETTLE[0]	cfg_num_lanes[1]	cfg_num_lanes[0]	Lane0_sel[1]
0x11	uc_PRG_RXHS_SETTLE[4]	uc_PRG_RXHS_SETTLE[3]	uc_PRG_RXHS_SETTLE[2]	uc_PRG_RXHS_SETTLE[1]
0x12	uc_PRG_HS_ZERO[1]	uc_PRG_HS_ZERO[0]	uc_PRG_HS_PREPARE	uc_PRG_RXHS_SETTLE[5]
0x13	uc_PRG_HS_ZERO[5]	uc_PRG_HS_ZERO[4]	uc_PRG_HS_ZERO[3]	uc_PRG_HS_ZERO[2]
0x14	uc_PRG_HS_TRAIL[2]	uc_PRG_HS_TRAIL[1]	uc_PRG_HS_TRAIL[0]	uc_PRG_HS_ZERO[6]
0x15	u_PRG_RXHS_SETTLE[1]	u_PRG_RXHS_SETTLE[0]	uc_PRG_HS_TRAIL[4]	uc_PRG_HS_TRAIL[3]
0x16	u_PRG_RXHS_SETTLE[5]	u_PRG_RXHS_SETTLE[4]	u_PRG_RXHS_SETTLE[3]	u_PRG_RXHS_SETTLE[2]
0x17	u_PRG_HS_ZERO[1]	u_PRG_HS_ZERO[0]	u_PRG_HS_PREPARE[1]	u_PRG_HS_PREPARE[0]
0x18	u_PRG_HS_ZERO[5]	u_PRG_HS_ZERO[4]	u_PRG_HS_ZERO[3]	u_PRG_HS_ZERO[2]
0x19	u_PRG_HS_TRAIL[3]	u_PRG_HS_TRAIL[2]	u_PRG_HS_TRAIL[1]	u_PRG_HS_TRAIL[0]
0x20	TEST_ENBL[1]	TEST_ENBL[0]	u_PRG_HS_TRAIL[5]	u_PRG_HS_TRAIL[4]
0x21	TEST_ENBL[5]	TEST_ENBL[4]	TEST_ENBL[3]	TEST_ENBL[2]
0x22	TEST_PATTERN[3]	TEST_PATTERN[2]	TEST_PATTERN[1]	TEST_PATTERN[0]
0x23	TEST_PATTERN[7]	TEST_PATTERN[6]	TEST_PATTERN[5]	TEST_PATTERN[4]
0x24	TEST_PATTERN[11]	TEST_PATTERN[10]	TEST_PATTERN[9]	TEST_PATTERN[8]
0x25	TEST_PATTERN[15]	TEST_PATTERN[14]	TEST_PATTERN[13]	TEST_PATTERN[12]
0x26	TEST_PATTERN[19]	TEST_PATTERN[18]	TEST_PATTERN[17]	TEST_PATTERN[16]
0x27	TEST_PATTERN[23]	TEST_PATTERN[22]	TEST_PATTERN[21]	TEST_PATTERN[20]
0x28	TEST_PATTERN[27]	TEST_PATTERN[26]	TEST_PATTERN[25]	TEST_PATTERN[24]
0x29	TEST_PATTERN[31]	TEST_PATTERN[30]	TEST_PATTERN[29]	TEST_PATTERN[28]
0x30	—	—	0*	cont_clk_mode

***Note**: When writing to this register, keep bit to 0. Otherwise, the IP might malfunction.

3. IP Generation and Evaluation

This chapter provides information on how to generate and synthesize MIPI D-PHY module using Lattice Radiant Software, as well as on how to run simulation. For more on Lattice Radiant Software, please refer to the Lattice Radiant Software 2.1 User Guide and relevant Lattice tutorials.

3.1. Licensing the IP

No license is required for this module.

3.2. Generating and Synthesizing the IP

Lattice Radiant Software allows you to generate and customize modules and IPs and integrate them into the device architecture.

To generate MIPI D-PHY Module in Lattice Radiant Software:

1. In the Module/IP Block Wizard, create a new Lattice Radiant Software project for MIPI D-PHY module.
2. In the dialog box of the Module/IP Block Wizard window, configure MIPI D-PHY module according to custom specifications, using drop-down menus and check boxes. As a sample configuration, see Figure 3.1. For configuration options, see Table 2.2.

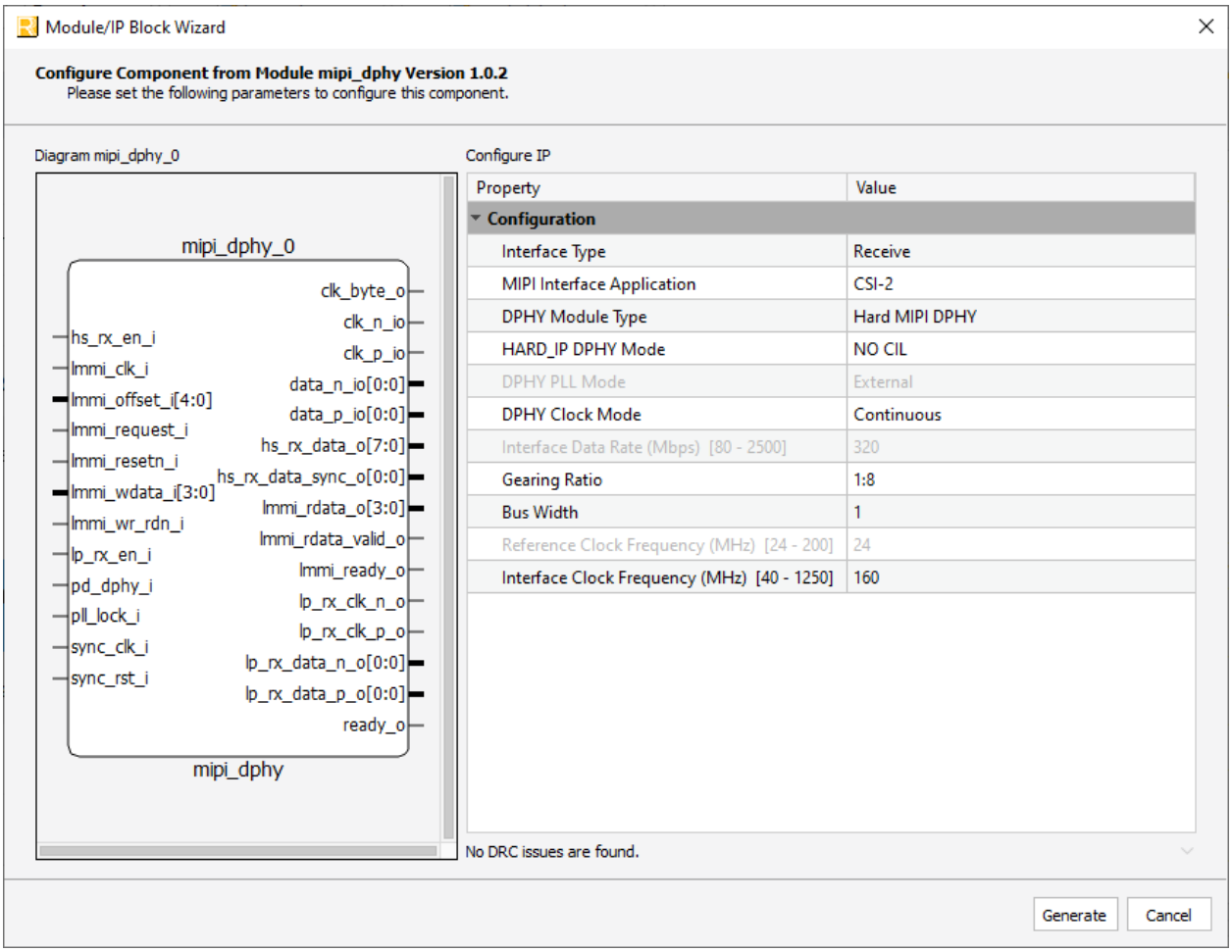

Figure 3.1. Configure Block of MIPI D-PHY

3. Click **Generate**. The Check Generating Result dialog box opens, showing design block messages, and results as shown in Figure 3.2.

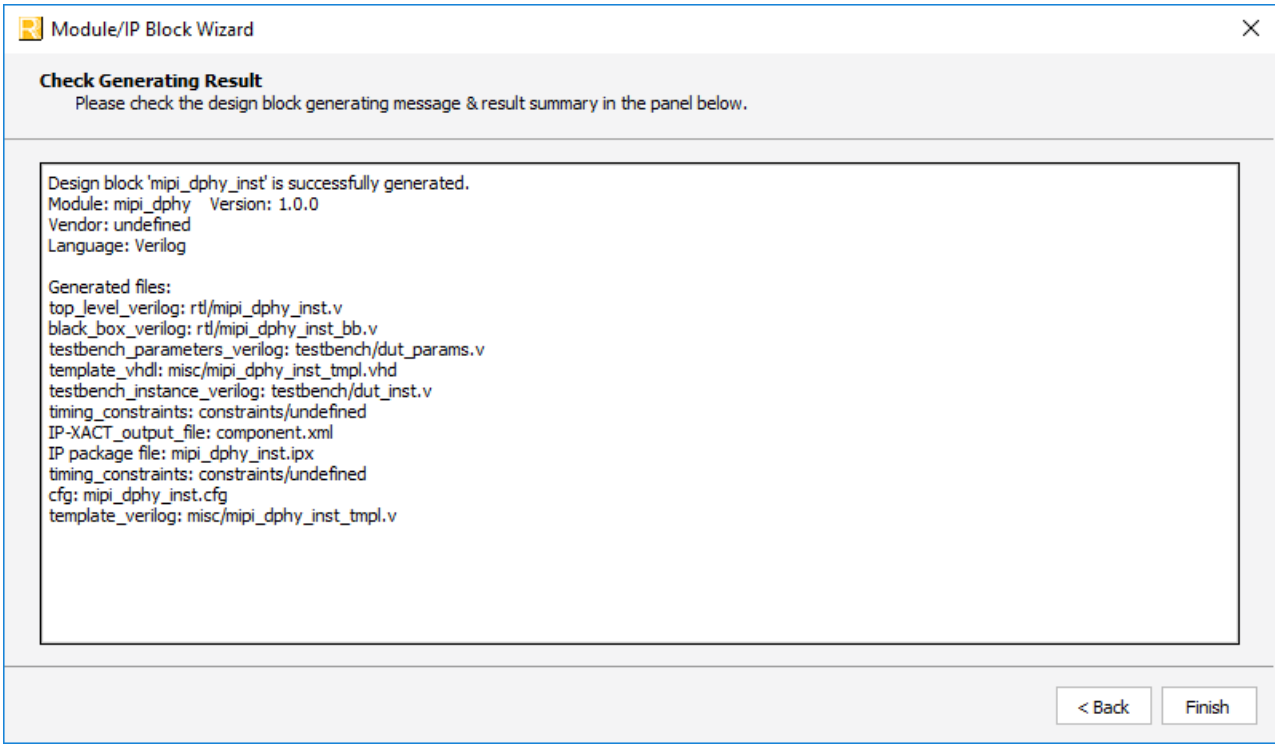

Figure 3.2. Check Generating Result

4. Click **Finish** to generate the Verilog file.
5. Upon generating desired design, you can synthesize it by clicking **Synthesize Design** located on the top left corner of the screen, as shown in Figure 3.3.

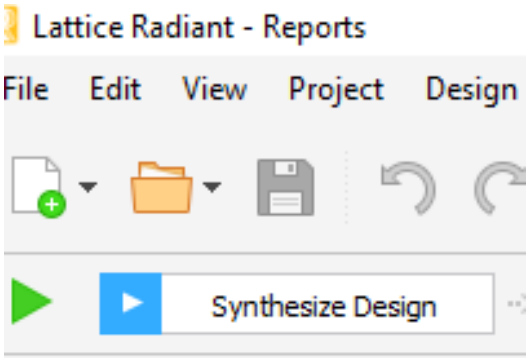

Figure 3.3. Synthesizing Design

3.3. Running Functional Simulation

To run Verilog simulation:

1. Right-click the implementation name and select **Add > Existing Simulation File**.
2. Search for the *<IP_name>/testbench/tb_top.v* file from the dialog box and click **Add**.
3. Click the  button located on the **Toolbar** to initiate the **Simulation Wizard** shown in Figure 3.4

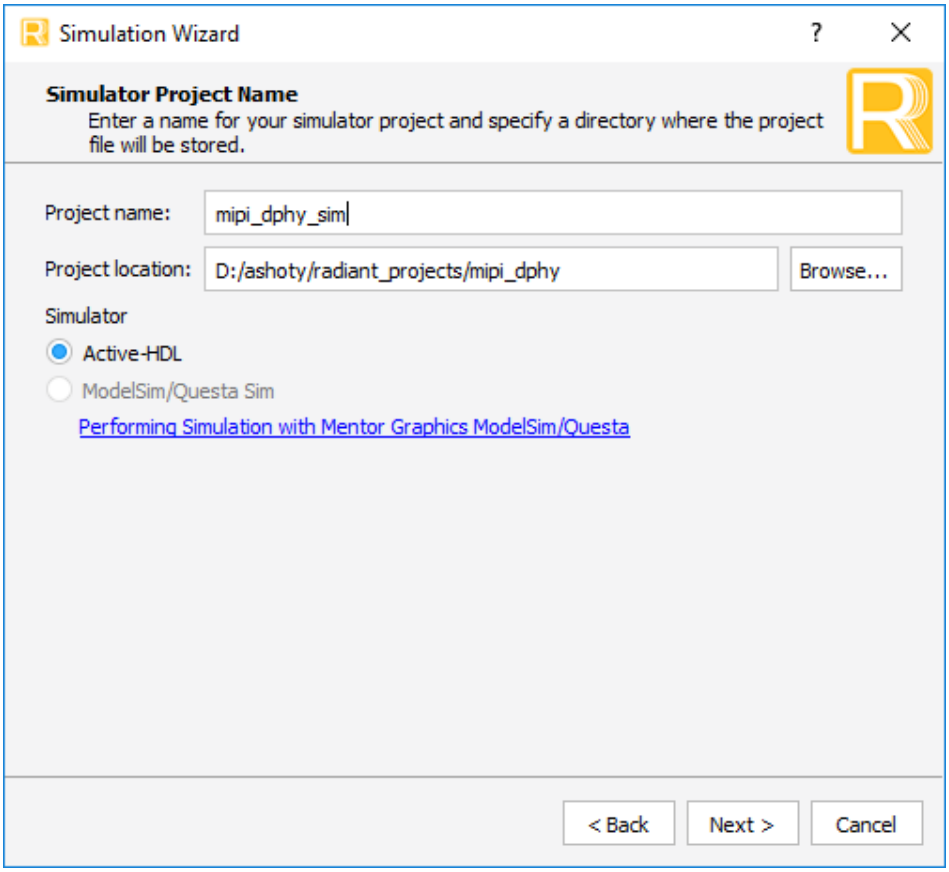

Figure 3.4. Simulation Wizard

4. Double-click **Next** to open the **Add and Reorder Source** window as shown in Figure 3.5.

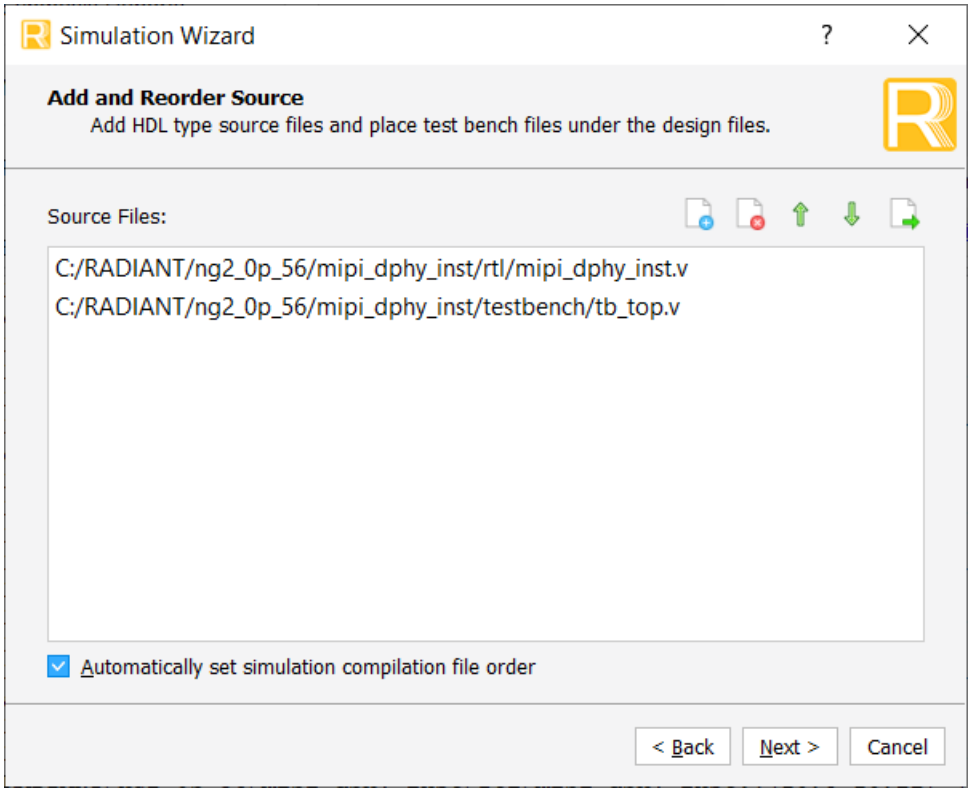

Figure 3.5. Adding and Reordering Source

5. Click **Next** to run simulation.

3.4. Hardware Evaluation

There is no restriction on the hardware evaluation of this module.

Appendix A. Limitations

The following is a known limitation:

- When MIPI_DPHY soft IP is configured with the following selections in the user interface, simulation might fail when Reference Clock Frequency is set to higher than 60 MHz:

  Interface Type = Receive
  DPHY Module Type = Hard MIPI DPHY
  Hard_IP DPHY Mode = CIL

References

For complete information on Lattice Radiant Project-Based Environment, Design Flow, Implementation Flow and Tasks, as well as on the Simulation Flow, see the Lattice Radiant Software 2.1 User Guide.

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Document Revision 1.2, Lattice Radiant SW version 2.1, June 2020

Section	Change Summary
All	• Added Certus-NX support. • Added Lattice Radiant Software 2.1 support.

Functional Description	• Added pll_clockop_i and pll_clockos_i ports in Table 2.1. MIPI D-PHY Module Port Descriptions.
	• Updated Table 2.2. Attributes Summary:
	  • Added DPHY Module Type dependency.
	  • Removed attributes.

IP Generation and Evaluation	• Updated Figure 3.1. Configure Block of MIPI D-PHY. • Updated procedure steps in Running Functional Simulation.
Appendix A. Limitations	Removed limitation.

Document Revision 1.1, Lattice Radiant SW version 2.0, February 2020

Section	Change Summary
Functional Description	• Added pll_clockop_i and pll_clockos_i ports in Table 2.1. MIPI D-PHY Module Port Description. • Added DPHY PLL Mode attribute in Table 2.2. Attributes Summary.
IP Generation and Evaluation	Updated Figure 3.1. Configure Block if MIPI D-PHY.
Appendix A. Limitations	Changed MIXEL to Hard_IP.

Document Revision 1.0, Lattice Radiant SW version 2.0, December 2019

Section	Change Summary
All	Changed document status from Preliminary to final.
Acronyms in This Document	Added this section.
Functional Description	• Revised port names to lp_rx_data_p_o[BUS_WIDTH – 1:0] and lp_rx_data_n_o[BUS_WIDTH – 1:0] in Table 2.1. MIPI D-PHY Module Port Descriptions. • Revised 0x30 offset information and added footnote in Table 2.3. Configuration Registers (MIPI Programmable Bits).
IP Generation and Evaluation	• Updated source file in Running Functional Simulation procedure to tb_top.v. • Updated Figure 3.5. Adding and Reordering Source.
Appendix A. Limitations	Added this section.
References	Removed reference to JEDEC website.
All	Minor editorial changes

Document Revision 0.80, Lattice Radiant SW version 2.0, October 2019

Section	Change Summary
All	Preliminary release

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