AHB-Lite to AXI4 Bridge IP Core

User Guide

FPGA-IPUG-02242-1.0

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
AMBA	Advanced Micro-controller Bus Architecture
AXI	Advanced Extensible Interface Bus
AHB	Advanced High-performance Bus
FPGA	Field Programmable Gate Array
RTL	Register Transfer Level

1. Introduction

1.1. Overview of the IP

The Lattice Semiconductor AHB-Lite to AXI4 Bridge provides an interface between a single high speed AHB-Lite manager (compliant to AMBA 3 AHB-Lite Protocol Specification) and a AXI4 subordinate (compliant to AMBA AXI and ACE Protocol Specification Version H.c).

1.2. Quick Facts

The design is implemented in Verilog HDL. The IP can be configured and generated using the Lattice Propel Builder and implemented within the Lattice Radiant software.

Table 1.1 Summary

IP Requirements	Supported FPGA Family	CertusPro-NX™, Lattice Avant™
	IP Version	1.0.0
Resource Utilization	Targeted Devices	Refer to Appendix A. Resources Utilization
	Supported User Interface	AHB-Lite and AXI4
Design Tool Support	IP Configuration and Generation	Lattice Propel Builder™ software
	IP Implementation (Synthesis, Map, Place and Route)	Lattice Radiant™ software

1.3. Features

The key features of the AHB-Lite to AXI4 Bridge includes:

- Supports configurable data bus width: 8, 16, 32, 64, 128, 256, 512, and 1024 bits.
- Supports configurable address width: 11 to 32 bits.
- Supports configurable AXI4 ID bus width (1 to 11 bits) so that the width can be matched with subordinate's ID bus width, but the ID value for this bridge will be always tied to 0 since AHB does not have the concept of ID.
- Supports basic and burst transfer. Single and indefinite length increment transfer on AHB are converted to INCR burst with length=0 on AXI.
- Supports narrow transfer where the requested transfer size can be less than data bus width.
- Supports Secure Access at AXI interface.
- Supports optional timeout indicator if there is no response from AXI subordinate within certain timeframe.
- Supports write/read data bus pipeline for relaxing timing critical path.

Some limitations of AHB-Lite to AXI4 Bridge are listed below:

- Burst transfer only supports 4, 8 and 16 beats as these are bounded by AHB's specification.
- Fixed burst transfer, out of order transaction, and exclusive accesses on AXI interface bus are not supported.
- Does not support AXI QOS (Quality of Service), Region identifier, and Uer Defined signals on AXI interface bus.
- AXI and AHB interface are expected to have the same address and data bus width, as well as operating at the same clock domain.
- AHB locked transfer request will be ignored as this feature is not supported on AXI4.

1.4. Licensing and Ordering Information

The AHB-Lite to AXI4 Bridge IP is provided at no additional cost with Lattice Propel Builder.

1.5. IP Validation Summary

The IP is validated using the following synthesis tool:

- **Simulation** – Questa Simulator, Modelsim Lattice-Edition
- **Timing and Hardware** – Lattice Radiant software

The table below shows the validation status for this IP core. The ✓ mark indicates whether the IP has been validated for Simulation, Timing, or with Hardware.

Table 1.2 IP Validation Level

Device Family	IP Version	Validation Level		
		Simulation	Timing	Hardware
CertusPro-NX, Lattice Avant	1.0.0	✓	✓	✓

1.6. Minimum Device Requirements

There is no minimum device requirements for this IP and can be used on any CertusPro-NX or Avant device family.

1.7. Naming Conventions

1.7.1. Signal Names

- _*n* are active low (asserted when value is logic 0)
- _*i* are input signals
- _*o* are output signals

2. Functional Description

2.1. Overview

The AHB-Lite to AXI4 Bridge is used for interfacing one AHB-Lite Manager and one AXI4 Subordinate. The read and write transfers on AHB side are translated into equivalent AXI transaction to be compatible with the subordinate. Some additional wait states are expected on the AHB bus due to the translation operation and pipeline in the bridge.

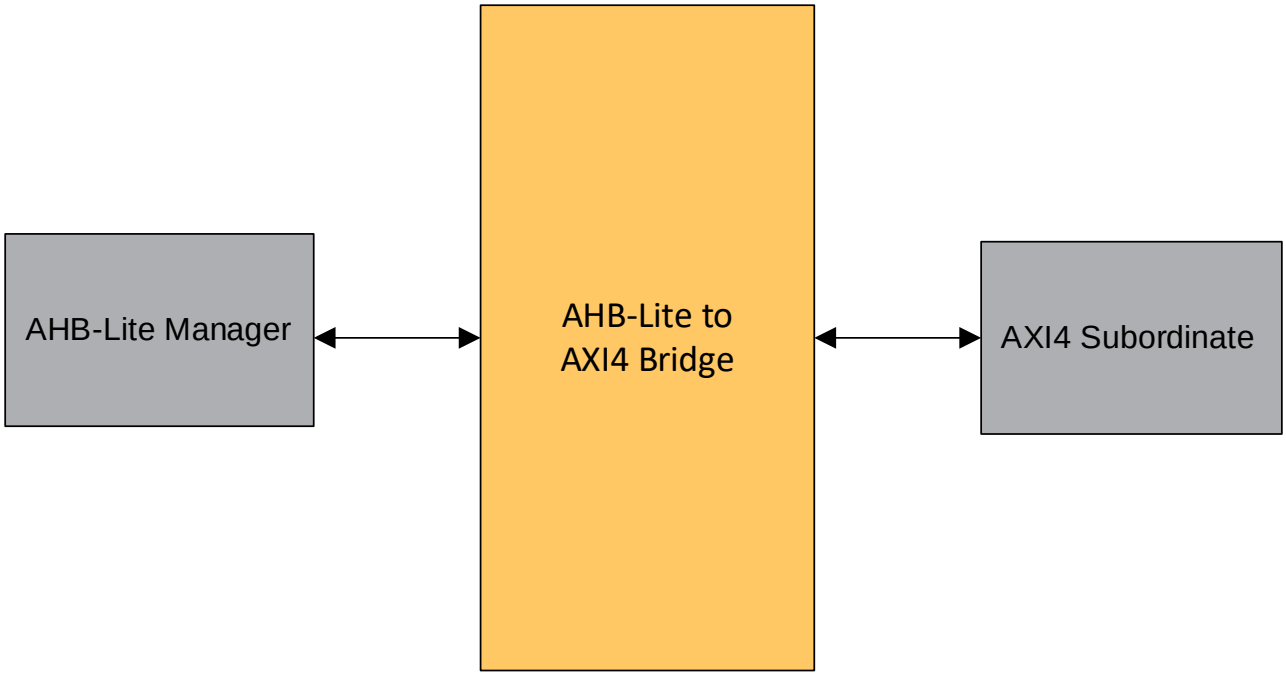

Figure 2.1 AHB-Lite to AXI4 Bridge

2.2. Interface Description

Figure 2.2 below shows the interface diagram of the AHB-Lite to AXI4 Bridge IP. The diagram shows all the available ports on the IP core.

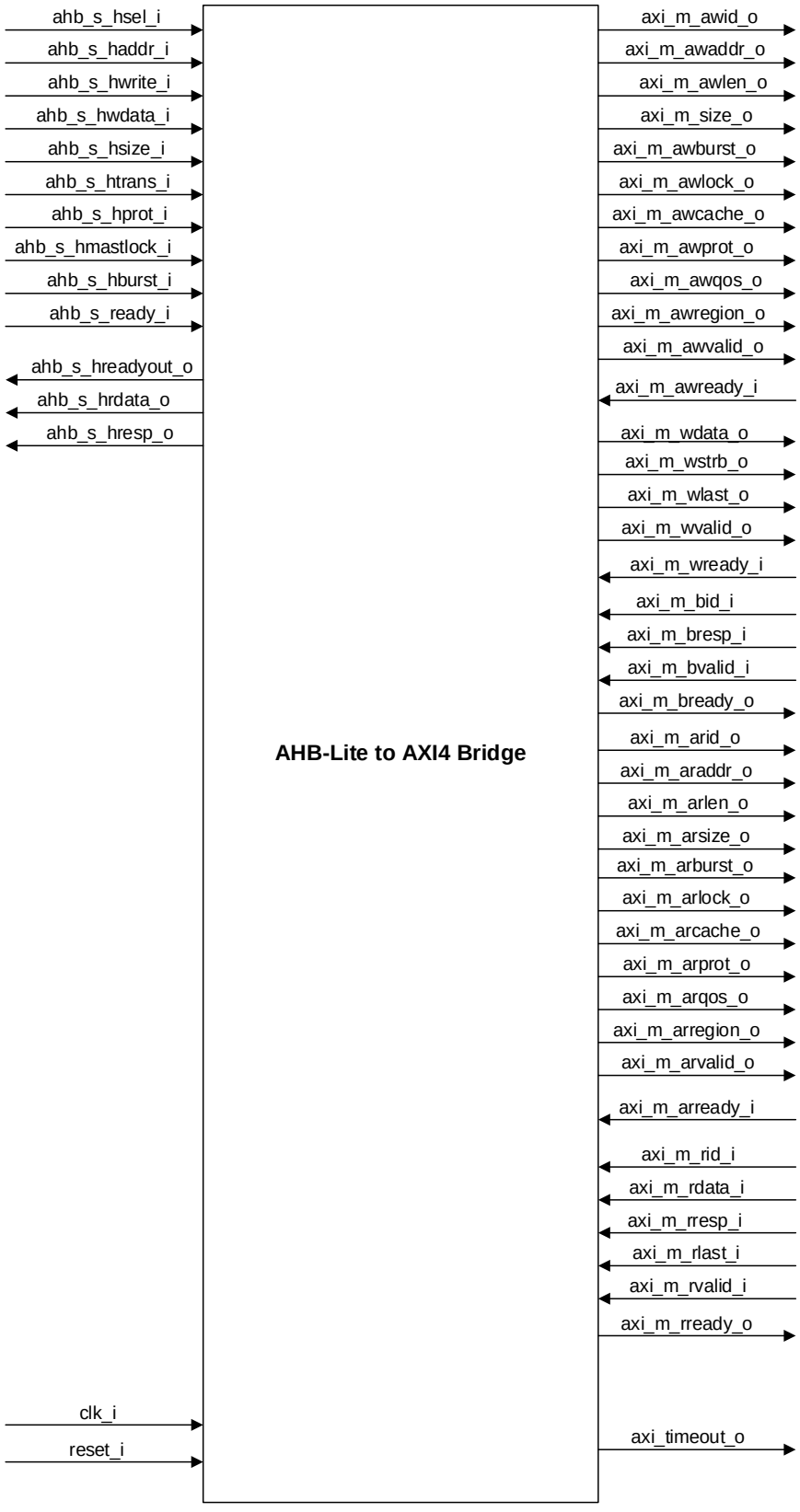

Figure 2.2 IP Core Block Diagram

Table 2.1 Signal Description

Pin Name	Direction	Width (Bits)	Description
Clock and Reset			
clk_i	In	1	AHB-Lite to AXI4 bridge clock.
resetn_i	In	1	Active low reset. It is recommended to share the same reset source as the AHB manager so that HREADY signals are sync correctly.
AHB-Lite Interface (AHBL_S)			
ahb_s_hsel_i	In	1	AHB-lite subordinate select.
ahb_s_haddr_i	In	M_ADDR_WIDTH	AHB 32-bit system address bus
ahb_s_hwrite_i	In	1	Indicates the transfer direction. This signal indicates an AHB write access when High and an AHB read access when Low.
ahb_s_hwdata_i	In	DATA_WIDTH	Write data. The write data bus transfers data from the manager to the subordinates during write operations. The width of the port is configurable. Refer to Table 2.2.
ahb_s_hsize_i	In	3	Indicates AHB size of transfer.
ahb_s_htrans_i	In	2	AHB Transfer Type, which can be NONSEQ, SEQ, IDLE, or BUSY.
ahb_s_hprot_i	In	4	Protection type. Indicates if it is a data access or instruction access transaction. It also indicates if this is a privileged mode or user mode.
ahb_s_hmastlock_i	In	1	Indicates that it is a locked sequence of transfers. This signal is unused internally.
ahb_s_hburst_i	In	3	AHB Burst type. The burst type indicates if the transfer is a single transfer or forms part of a burst. The burst can be incrementing or wrapping.
ahb_s_hready_i	In	1	Ready signal from AHB manager to indicate that the previous transfer is completed. This signal can be connected to *ahb_s_hreadyout_o* if the AHB manager does not have a HREADY output port.
ahb_s_hreadyout_o	Out	1	Ready signal to AHB manager to indicate that the previous transfer is completed.
ahb_s_hrdata_o	Out	DATA_WIDTH	AHB read data to the manager. Width of the port is configurable.
ahb_s_hresp_o	Out	1	Transfer Response. When Low, it indicates that the transfer status is OKAY. When High, it indicates that the transfer status is an ERROR. SLVERR and DECERR on AXI bus will be translated to error response on AHB-Lite bus. If the returning AXI ID does not match with the outgoing AXI ID (which is always 0), an error response will be triggered as well.
AXI4 Interface (AXI4_M)			
axi_ m_awid_o	Out	AXI_ID_WIDTH	AXI write ID. This output signal will always be tied to 0.
axi_m_awaddr_o	Out	M_ADDR_WIDTH	Write address. In a write burst transaction, this signal holds the address of the first transfer.
axi_m_awlen_o	Out	8	Burst length. This indicates the number of beats per AXI burst.
axi_m_awsize_o	Out	3	Burst size. Indicates the size of each transfer in the burst.
axi_m_awburst_o	Out	2	Burst type. The burst type and the size information. Determines how the address of each transfer within the burst is calculated.

Pin Name	Direction	Width (Bits)	Description
axi_m_awlock_o	Out	1	Lock Type. Only normal access type is supported as exclusive access is not supported on AHBL manager.
axi_m_awcache_o	Out	4	Memory type. Only 4 types of encoding are supported which are: device non-bufferable, device bufferable, normal non-cacheable non-bufferable, normal non-cacheable bufferable are supported. The rest are not supported as they are not included in AHB-lite.
axi_m_awprot_o	Out	3	Access permission signals to protect against illegal transaction. Two protection encoding are supported which are Privileged/Unprivileged access, Data/Instruction access. Secure and non-secure access is not supported as this is not supported on AHB-lite.
axi_m_awqos_o	Out	4	QoS identifier sent for each transaction. Not supported and will always be tied to 0.
axi_m_awregion_o	Out	4	Region identifier sent for each transaction. Not supported and will always be tied to 0.
axi_m_awvalid_o	Out	1	Write address valid. Indicates that the address and control bits on the channel are valid.
axi_m_awready_i	In	1	Write address ready. Indicates the readiness of the subordinate. When asserted, the subordinate is ready for a new address.
axi_m_wdata_o	Out	DATA_WIDTH	Write data.
axi_m_wstrb_o	Out	DATA_WIDTH	Write strobes. This signal indicates which eight bits of the write data bus are valid. This signal will be tied to all 1's as the Write Strobe feature is not supported in AHB-lite.
axi_m_wlast_o	Out	1	Write last. This signal indicates if the current transfer is the last data transfer in a write transaction.
axi_m_wvalid_o	Out	1	Write valid. This signal indicates data and strobes on the bus are valid.
axi_m_wready_i	In	1	Write data ready. Indicates the readiness of the subordinate. When asserted, the subordinate is ready for new data.
axi_m_bid_i	In	AXI_ID_WIDTH	Write response ID from subordinate.
axi_m_bresp_i	In	2	Write response which indicates the status of a write transaction.
axi_m_bvalid_i	In	1	Write response valid. When asserted, the subordinate is signaling a valid write response.
axi_m_bready_o	Out	1	Response ready. Indicates that the manager is now ready to accept a write response.
axi_m_arid_o	Out	AXI_ID_WIDTH	AXI read address ID. This output signal will always be tied to 0.
axi_m_araddr_o	In	M_ADDR_WIDTH	Read address. In a read burst transaction, this signal holds the address of the first transfer.
axi_m_arlen_o	Out	8	AXI read burst length. This indicates the number of beats per AXI burst.
axi_m_arsize_o	Out	3	Burst size. This signal indicates the size of each transfer in the burst.
axi_m_arburst_o	Out	2	Burst type. The burst type and the size information. Determines how the address of each transfer within the burst is calculated.
axi_m_arlock_o	Out	1	Lock Type. Only normal access type is supported as exclusive access is not supported on AHB manager.

Pin Name	Direction	Width (Bits)	Description
axi_m_arcache_o	Out	4	Memory type. Only 4 types of encoding are supported which are: device non-bufferable, device bufferable, normal non-cacheable non-bufferable, normal non-cacheable bufferable are supported. The rest are not supported as they are not included in AHB-lite.
axi_m_arprot_o	Out	3	Access permission signals to protect against illegal transaction. Two protection encoding are supported which are Privileged/Unprivileged access, Data/Instruction access. Secure and non-secure access is not supported as this is not supported on AHB-lite.
axi_m_arqos_o	Out	4	QoS identifier sent for each transaction. Not supported and will always be tied to 0.
axi_m_arregion_o	Out	4	Region identifier sent for each transaction. Not supported and will always be tied to 0.
axi_m_arvalid_o	Out	1	Read address valid. Indicates that the address and control information is valid.
axi_m_arready_i	In	1	Read address ready. Indicates the readiness of the subordinate. When asserted, the subordinate is ready for a new address.
axi_m_rid_i	In	AXI_ID_WIDTH	Identification tag for read data and response.
axi_m_rdata_i	In	DATA_WIDTH	Read data.
axi_m_rresp_i	In	2	Read response. Indicates the read transaction status.
axi_m_rlast_i	In	1	Read last. This signal indicates if the current transfer is the last data transfer in a read transaction.
axi_m_rvalid_i	In	1	Read valid. Indicates that the read data channel signals are valid.
axi_m_rready_o	Out	1	Read ready. Indicates the readiness of the manager. When asserted, the manager is ready to receive data.
Optional interface (enabled when AXI Timeout counter > 0)			
axi_timeout_o	Out	1	AXI timeout signal. Asserted when AXI subordinate does not response within the threshold set for that option. When this signal is asserted, it is recommended to reset the entire AXI4 and AHB-Lite bus to recover the bus as the AXI subordinate is probably hung.

2.3. Attributes

Table 2.2 below provides the list of user-configurable attributes for AHB-Lite to AXI4 Bridge. The attribute values are configured using the IP Core Block Wizard in the Propel Builder software.

Table 2.2 IP Parameters

Attribute Name	Attribute ID	Selectable Values	Default	Dependency on Other Attributes	Description
General Settings tab					
Address Width	M_ADDR_WIDTH	11-32	32	-	Specifies the bit width of AHB and AXI address bus signals.
Data Bus width	DATA_WIDTH	8, 16, 32, 64, 128, 256, 512, 1024	32	-	Specifies the bit width of AHB and AXI data bus signals.

Attribute Name	Attribute ID	Selectable Values	Default	Dependency on Other Attributes	Description
General Settings tab					
AXI Transaction ID width	AXI_ID_WIDTH	1-11	4	-	Specifies the bit width of AXI Transaction ID signals. The ID value will always be set to 0.
AXI Secure access	AXI_SECURE_ACCESS	0,1	0	-	Specifies the support for secure access at AXI side. Enabling this parameter will enable secure access for all AXI transactions.
AXI Timeout counter	AXI_TIMEOUT	0,16,32, 64,128	0	-	Specifies the number of clock cycles to wait for AXI subordinate to response and assert timeout signal if it is not responding. e.g: • 0 – no timeout counter will be implemented. • 16 – Timeout if there is no response from bridge within 16 clock cycles
Read Data bus Pipeline Enable	RDDATA_PIPELINE	0,1	0	-	Enable this parameter to add a pipeline stage to Read Data bus. Useful for relaxing the timing critical path if there is any violated path detected on this bus.
Write Data bus Pipeline Enable	WRDATA_PIPELINE	0,1	0	-	Enable this parameter to add a pipeline stage to Write Data bus. Useful for relaxing the timing critical path if there is any violated path detected on this bus.
Narrow transfers support	NARROW_TRANSFER	0,1	0	DATA_WIDTH > 8	Enable this parameter to support narrow transfer feature where the requested transfer size can be less than the DATA_WIDTH selected.

3. Timing Diagram

3.1. Write Operation

3.1.1. Write Data Bus Pipeline Disabled

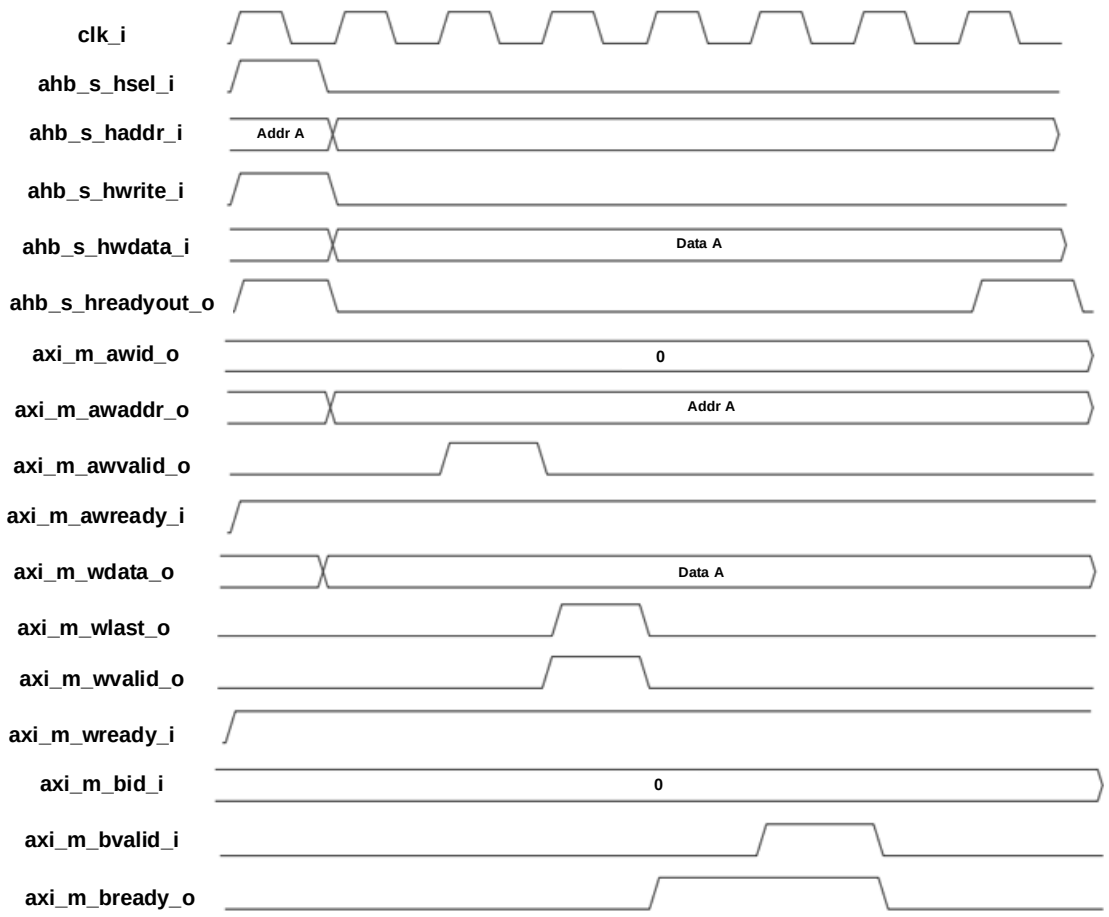

Figure 3.1 Timing Diagram of Write Transfer with Data Bus Pipeline Disabled

Figure 3.1 shows a basic write transfer with write data bus pipeline disabled.

1. At the first clock cycle, the AHB-Lite manager initiates a write transfer by driving the address and control signals. This is the address phase of the AHB write transfer.
2. At the 2nd clock cycle, the data phase of AHB starts and the AHB manager drives the HWDATA bus with a valid data.
3. At the 3rd clock cycle, the bridge is driving the AXI's write address channels to start the write transfer at the AXI4 bus. The transaction is acknowledged immediately since AWREADY signal is asserted from the beginning. If it is not asserted, the AWVALID signal will be held high until the bridge sees the ready signal turns high.
4. At the 4th clock cycle, the write data channel on AXI are being asserted to transfer the data. The transaction is immediately being acknowledged, since WREADY signal is asserted from the beginning.
5. At the 5th clock cycle, the Bready signal at AXI Write response channel is asserted and waiting for the Bvalid signal to be asserted.

6. At the 6th clock cycle, the bridge sees a Bvalid signal asserted, indicating that the write transfer is complete. The Bready signal is de-asserted at this point.
7. At the 8th clock cycle, the bridge asserts the HREADYOUT signal on the AHB-Lite bus, indicating to the AHB manager that the write transfer is complete and ready for the next transfer.

3.1.2. Write Data Bus Pipeline Enabled

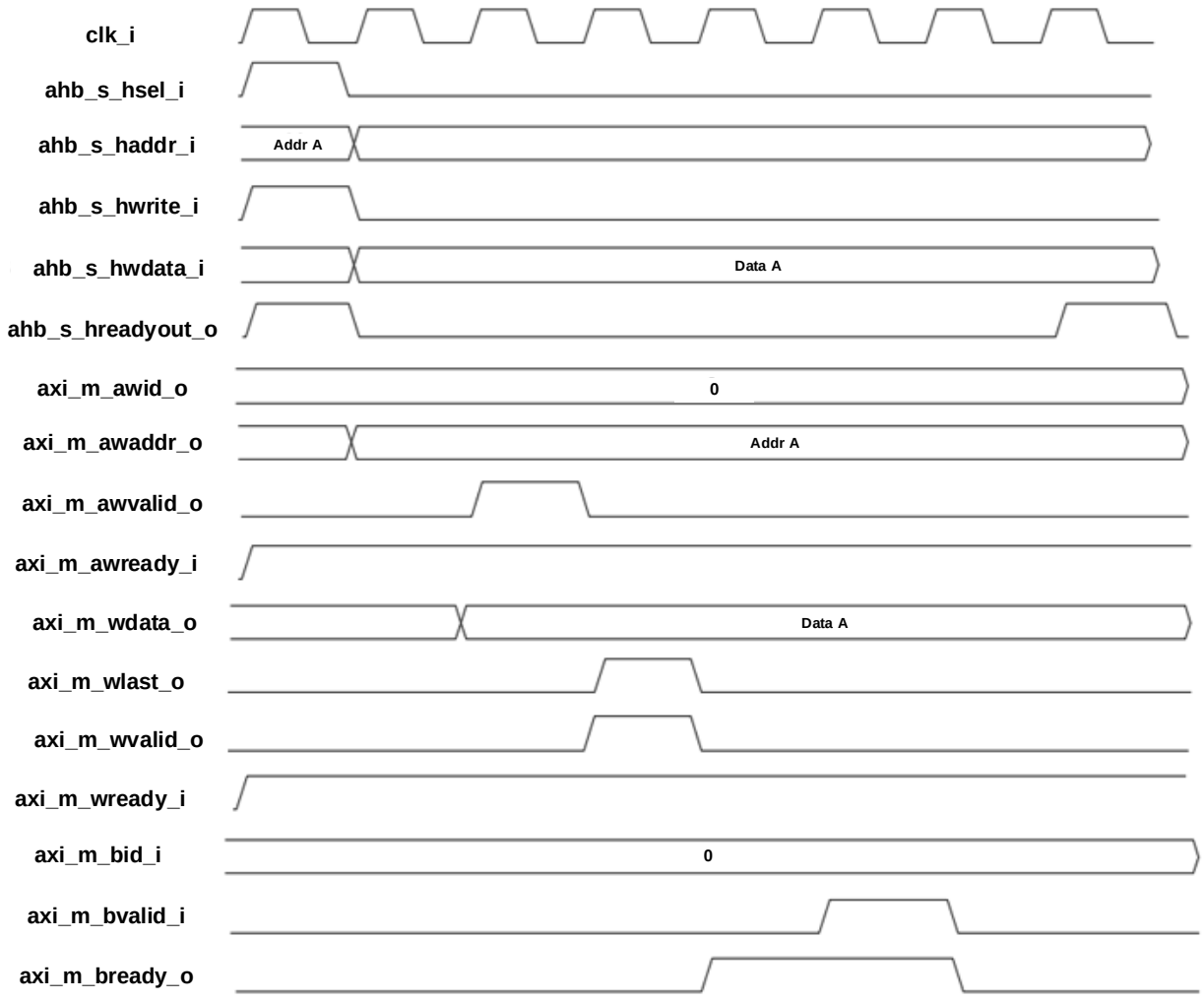

Figure 3.2 Timing Diagram of Write Transfer with Write Data Bus Pipeline Enabled

Figure 3.2 shows a basic write transfer with a write data bus pipeline enabled. Generally, the write operation works similar as the write transfer with a write data bus pipeline disabled. The only exception is at the 2nd clock cycle, the AXI's WDATA signal is still not driven by valid data. The data reaches the output at 1 clock cycle later, which is at the 3rd clock cycle.

3.2. Read Operation

3.2.1. Read Data Bus Pipeline Disabled

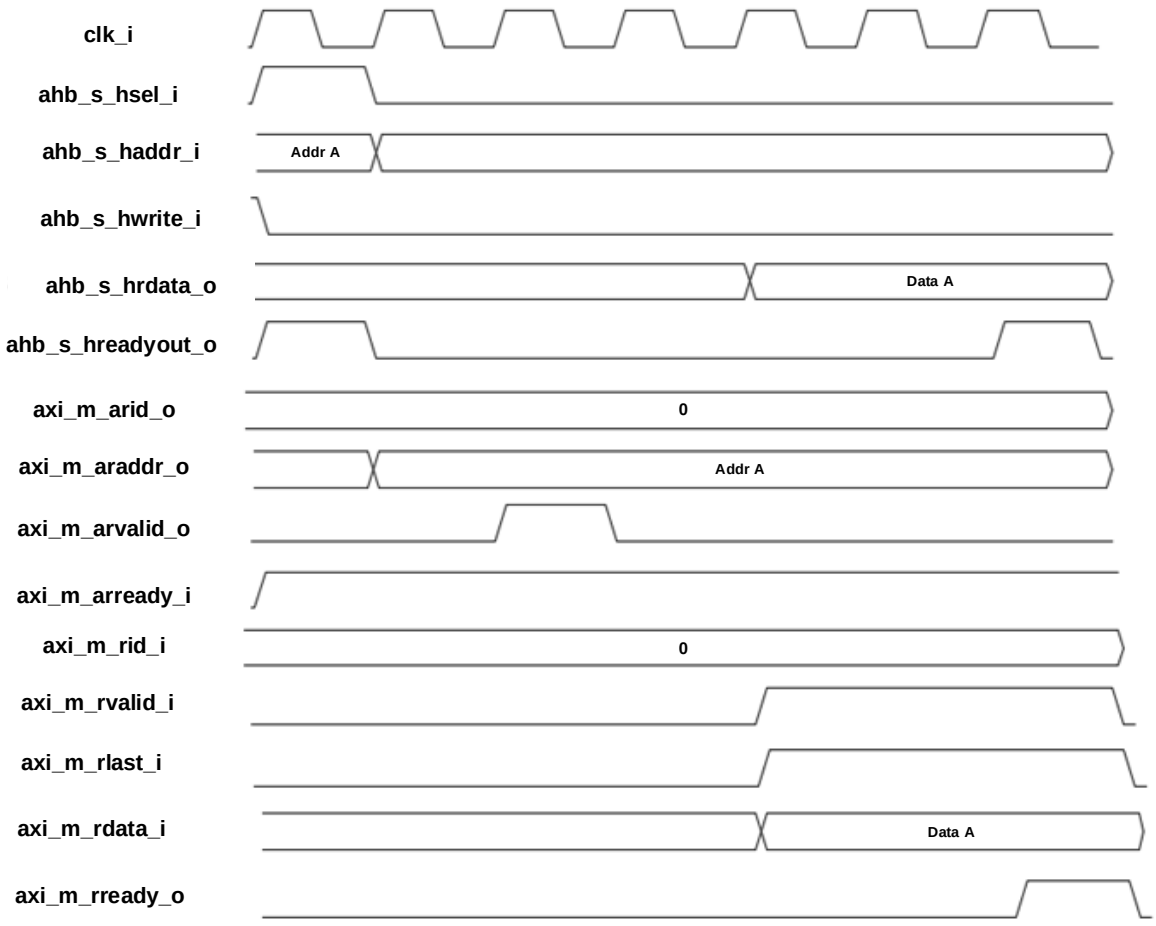

Figure 3.3 Timing Diagram of Read Transfer with Read Data Bus Pipeline Disabled

Figure 3.3 shows a basic read transfer with read data bus pipeline disabled.

1. At the first clock cycle, the AHB-Lite manager initiates a read transfer by driving the address and control signals. This is the address phase of the AHB read transfer.
2. At the 2nd clock cycle, the data phase of the AHB transfer starts, and the AHB manager is waiting for the valid read data.
3. At the 3rd clock cycle, the bridge starts to initiate a read transfer to the AXI subordinate by driving the read address channels.
4. The bridge waits for the valid read data after initiating the transfer. The read data channel returns the read data at the 5th clock cycle.
5. The Read data channel holds the valid data until the bridge indicates that the transfer is complete by asserting the Rready at the 7th clock cycle. At the same clock cycle, the HREADYOUT to the AHB-Lite manager is also asserted.

3.2.2. Read Data Bus Pipeline Enabled

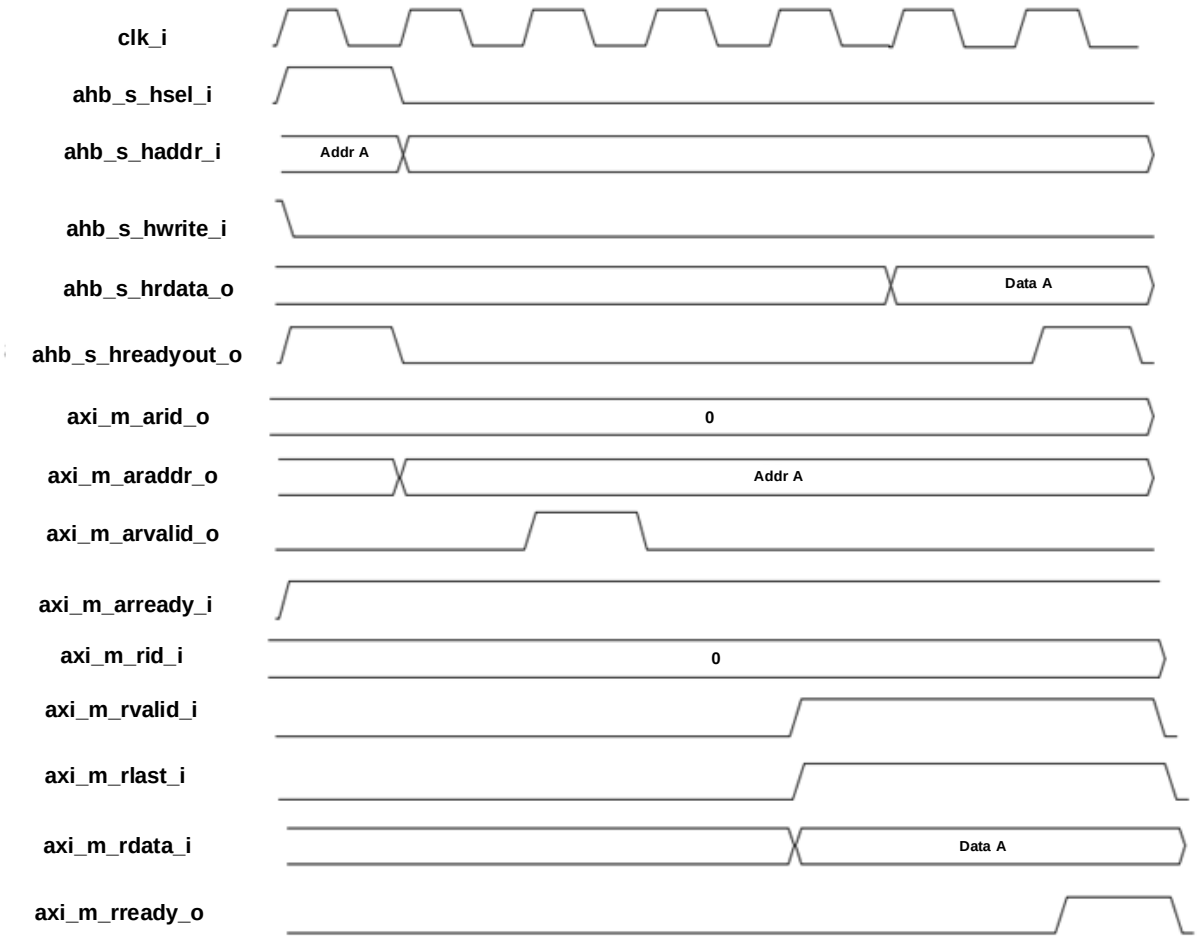

Figure 3.4 Timing Diagram of Read Transfer with Read Data Bus Pipeline Enabled

Figure 3.4 shows the basic read transfer with the read data bus pipeline enabled. Generally, the read operation works similar as the read transfer with the pipeline disabled. The only exception is the HRDATA on the AHB-Lite interface is outputting the read data at the 6th clock cycle instead of the 5th clock cycle.

4. Designing with the IP

This section provides information on how to generate the IP Core using the Lattice Propel Builder software. For more details on the Lattice Propel software, refer to the Lattice Propel User Guide.

4.1. Generating and Instantiating the IP

You can use the Lattice Propel software to generate this IP module along with other components required in your System-on-Chip (SoC) design. The steps below describes the procedure for generating the AHB-Lite to AXI4 Bridge IP in the Lattice Propel software.

1. Create a new Lattice Propel software project or open an existing project.
2. In the **IP Catalog** tab, double click **AHB-Lite to AXI4 Bridge** under **IP > Processors_Controllers_and_Peripherals** category. The Module/IP Block Wizard window opens as shown in Figure 4.1. Enter your desired component name in the **Component Name** field then click **Next**.

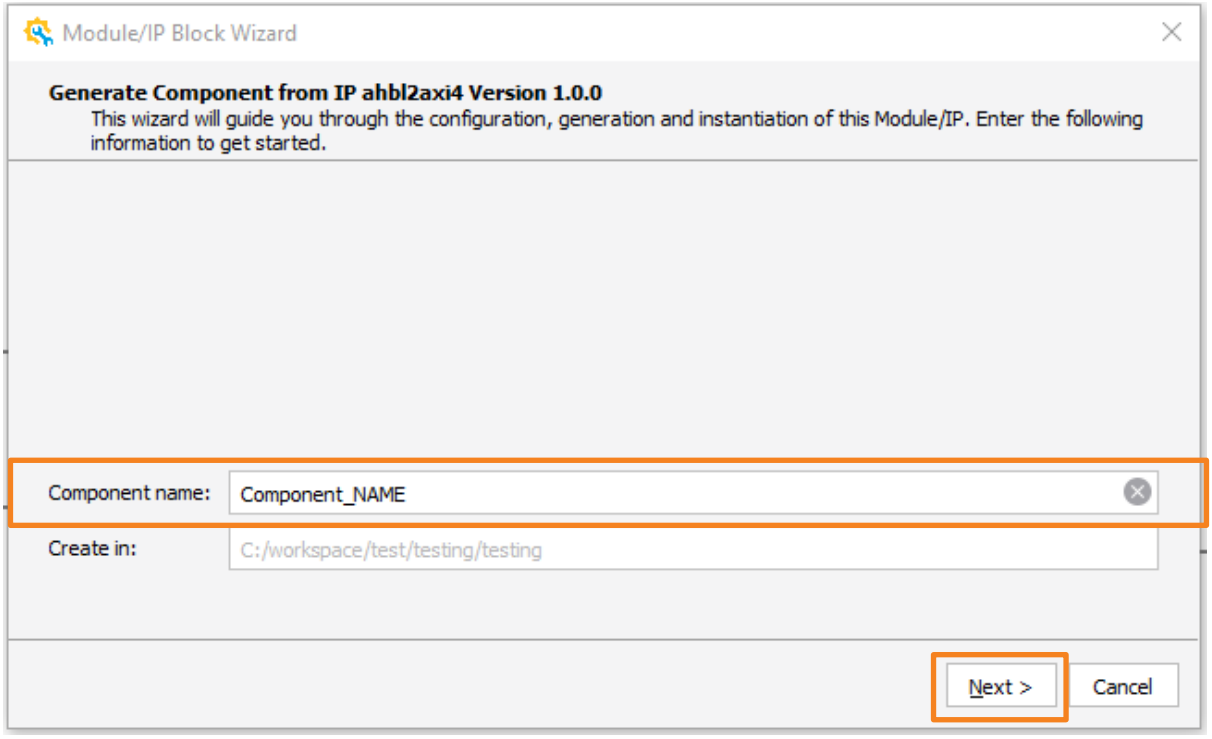

Figure 4.1 Enter Component Name

3. In the next Module/IP Block Wizard window, customize the IP according to your required configuration. Figure 4.2 shows an example configuration. For more details on the configuration options, please refer to Section 2.3.

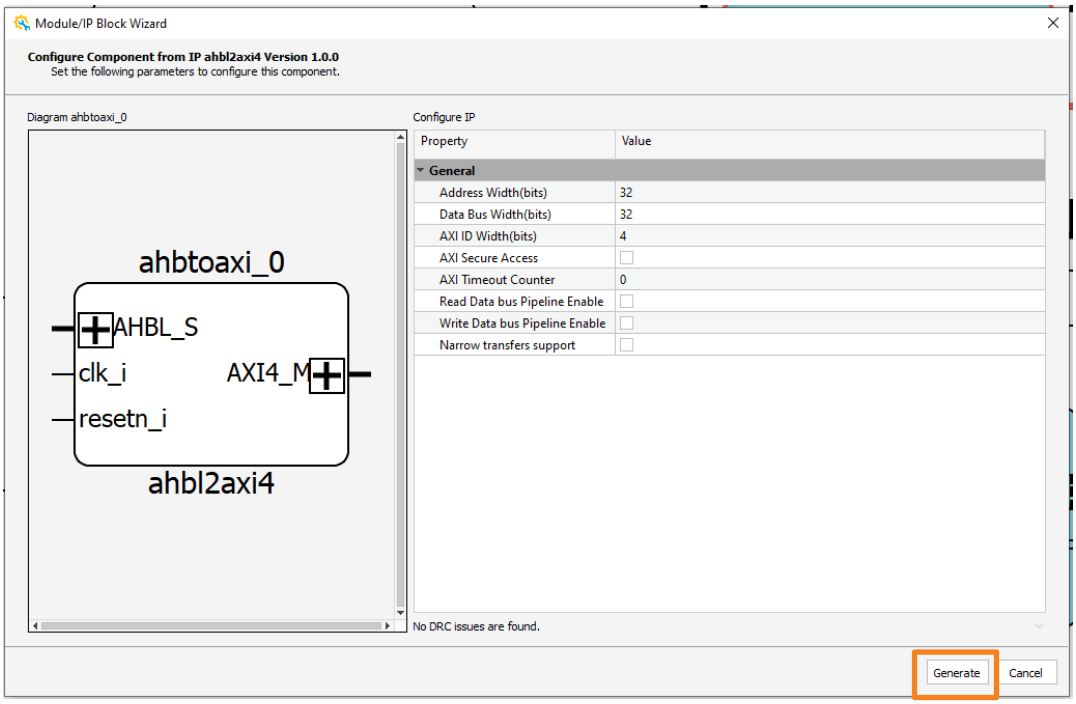

Figure 4.2 IP Configuration

4. Click the **Generate** button. The **Check Generated Result** dialog box opens as shown in Figure 4.3. This dialog box shows the design block messages and results.

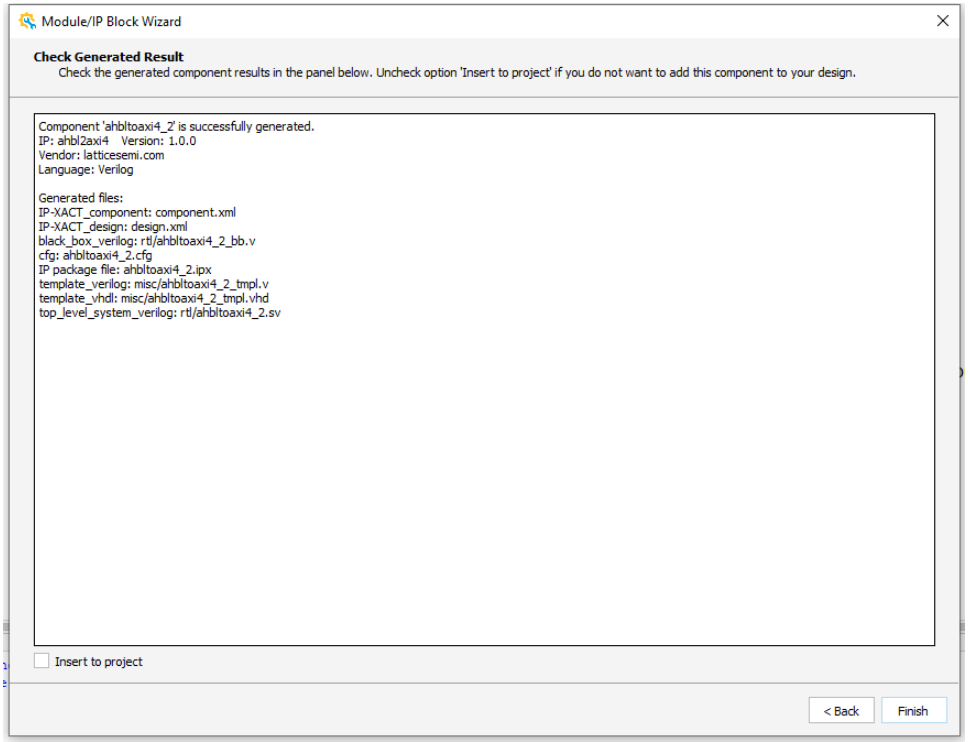

Figure 4.3 Check Generated Result

5. The generated IP will appear as a block diagram in the Schematic window. Connect it to the rest of the components in your system as shown in Figure 4.4.

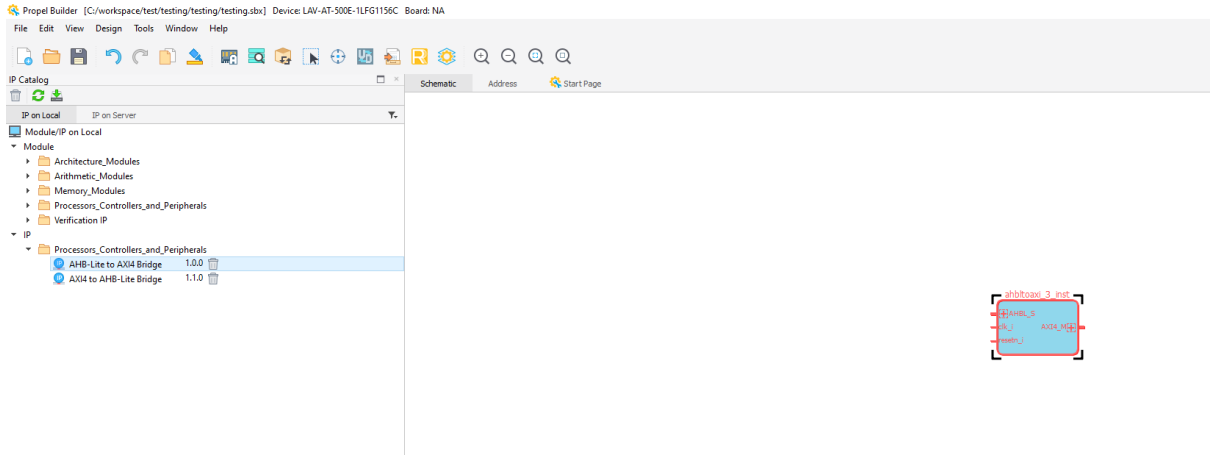

Figure 4.4 Schematic Window

6. Once all the components are connected, click **Design -> Validate Design** to validate your design. If everything is okay, click **Design -> Generate** to generate the RTL files for your created system. All the generated files are placed under <directory paths in the **Create in** field as shown in **Step 2>** / lib/ latticesemi.com/ folder.

4.1.1. Generated Files and Structure

The generated AHB-Lite to AXI4 Bridge IP package includes the black box (<Component name>_bb.v) and the instance templates (<Component name>_tmpl.v/vhd) that's use to instantiate the core in a top-level design. An example RTL top-level reference source file (Component name>.v) is given that can be used as an instantiation template for the module. The generated files are listed in Table 4.1.

Table 4.1 Generated Files

Attribute	Description
<Component name>.ipx	This file contains the information on the files associated to the generated IP.
<Component name>.cfg	This file contains the parameter values used in the IP configuration.
component.xml	Contains the ipxact:component information of the IP.
design.xml	Documents the configuration parameters of the IP in IP-XACT 2014 format.
rtl/<Component name>.v	This file provides an example RTL top file that instantiates the module.
rtl/<Component name>_bb.v	This file provides the synthesis black box.
misc/<Component name>_tmpl.v misc /<Component name>_tmpl.vhd	These files provide instance templates for the module.

Appendix A. Resource Utilization

Table A.1 shows a sample of the resource utilization of the AHB-Lite to AXI4 Bridge IP on the Lattice Avant devices.

Table A.1 Estimated Device Resource Utilization on the Lattice Avant

Attribute Values					Clock Fmax (MHz)	LUTs	Register	EBRs
Data Width	AXI Timeout counter	Read Data bus Pipeline Enable	Write Data bus Pipeline Enable	Narrow Transfer Support				
32	0	0	0	0	350	95	82	0
32	0	1	1	0	350	89	144	0
32	128	0	0	0	350	118	108	0
32	128	1	1	0	350	115	170	0
256	0	0	0	0	350	95	82	0
256	0	1	1	0	350	97	604	0
256	128	0	0	0	350	118	108	0
256	128	1	1	0	350	122	620	0
32	0	0	0	1	350	105	96	0
32	0	1	1	1	350	106	161	0
32	128	0	0	1	350	128	115	0
32	128	1	1	1	350	125	170	0
256	0	0	0	1	350	125	116	1
256	0	1	1	1	350	128	634	1
256	128	0	0	1	350	150	139	1
256	128	1	1	1	350	156	652	1

Notes:

1. Address width is always set to 32 bits in all configurations listed.
2. The resource values are populated using LAV-AT-E70-1LFG676C device compiled in the Lattice Radiant 2023.1 design software with Synplify Pro. When the IP is combined with other blocks in the FPGA, the value can be expected to vary from the value in the table.

Table A.2 shows a sample of the resource utilization of AHB-Lite to AXI4 Bridge IP on CertusPro-NX devices.

Table A.2 Estimated Device Resource Utilization on the CertusPro-NX

Attributes Values					Clock Fmax (MHz)		LUTs	Register	EBRs
Data Width	AXI Timeout counter	Read Data bus Pipeline Enable	Write Data bus Pipeline Enable	Narrow Transfer Support	Performance Grade = 7 & 8_Low-Power	Performance Grade = 9_Low-Power and all High-Performance grade			
32	0	0	0	0	160	200	83	87	0
32	0	1	1	0	160	200	83	151	0
32	128	0	0	0	160	200	109	105	0
32	128	1	1	0	160	200	104	169	0
256	0	0	0	0	160	200	83	87	0
256	0	1	1	0	160	200	86	599	0
256	128	0	0	0	160	200	109	105	0
256	128	1	1	0	160	200	104	617	0
32	0	0	0	1	160	200	94	94	0
32	0	1	1	1	160	200	94	158	0
32	128	0	0	1	160	200	115	112	0

Attributes Values					Clock Fmax (MHz)		LUTs	Register	EBRs
Data Width	AXI Timeout counter	Read Data bus Pipeline Enable	Write Data bus Pipeline Enable	Narrow Transfer Support	Performance Grade = 7 & 8_Low-Power	Performance Grade = 9_Low-Power and all High-Performance grade			
32	128	1	1	1	160	200	115	176	0
256	0	0	0	1	160	200	116	118	2
256	0	1	1	1	160	200	116	630	2
256	128	0	0	1	160	200	137	136	2
256	128	1	1	1	160	200	137	648	2

Notes:

1. Address width is always set to 32 bits in all configurations listed.
2. The resource values are populated using LFCPNX-50-7ASG256C & LFCPNX-50-9ASG256C device compiled in Lattice Radiant 2023.1 design software with Synplify Pro. When the IP is combined with other blocks in FPGA, the value can be expected to vary from the value in the table.

References

For more information refer to:

- Lattice Sales Office
- Lattice Insights for Lattice Semiconductor training courses and learning plans
- AMBA AXI and ACE Protocol Specification Version H.c
- AMBA 3 AHB-Lite Protocol Specification
- CertusPro-NX Webpage
- Lattice Avant-E Webpage
- Lattice Propel FPGA design software
- Lattice Proper User Guide
- Lattice Propel Builder User Guide

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.0, December 2023

Section	Change Summary
All	Initial release.

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