I3C Target IP Core - Lattice Radiant Software

User Guide

FPGA-IPUG-02227-1.1

July 2023

Disclaimers

Lattice makes no warranty, representation, or guarantee regarding the accuracy of information contained in this document or the suitability of its products for any particular purpose. All information herein is provided AS IS, with all faults and associated risk the responsibility entirely of the Buyer. Buyer shall not rely on any data and performance specifications or parameters provided herein. Products sold by Lattice have been subject to limited testing and it is the Buyer's responsibility to independently determine the suitability of any products and to test and verify the same. No Lattice products should be used in conjunction with mission- or safety-critical or any other application in which the failure of Lattice's product could create a situation where personal injury, death, severe property or environmental damage may occur. The information provided in this document is proprietary to Lattice Semiconductor, and Lattice reserves the right to make any changes to the information in this document or to any products at any time without notice.

Inclusive Language

This document was created consistent with Lattice Semiconductor's inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice's inclusive language FAQ# 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

Contents

Figures

Tables

Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
ACK	Acknowledgement
AHB	Advanced High-Performance Bus
APB	Advanced Peripheral Bus
CCC	Common Command Code
D2D	Device to Device
DA	Dynamic Address
DAA	Dynamic Address Assignment
DDR	Double Data Rate
EBR	Embedded Block RAM
FIFO	First In First Out
FPGA	Field Programmable Gate Array
GUI	Graphical User Interface
HDL	Hardware Description Language
HDR	High Data Rate
HJ	Hot Join
I2C	Inter-Integrated Circuit
I3C	Improved Inter Integrated Circuit
IBI	In Band Interrupt
IP	Intellectual Property
LMMI	Lattice Memory Mapped Interface
LSE	Lattice Synthesis Engine
MDB	Mandatory Data Byte
SA	Static Address
SCL	Serial Clock
SDA	Serial Data

1. Introduction

The Lattice I3C IP Core is designed to comply with the MIPI I3C specification.

The MIPI I3C interface eases sensor system design architectures in mobile wireless products by providing a fast, low-cost, low-power, two-wire digital interface for sensors. I3C is a single scalable, cost effective, power efficient protocol to solve issues with the high protocol overhead, power consumption, nonstandard protocol, separate lines for interrupt and the rest requirement. Implementing the I3C Specification greatly increases the implementation flexibility for an ever-expanding sensor subsystem as efficiently and at as low cost as possible.

I3C is backward compatible with many Legacy I2C Devices, but I3C offers greater than 10x speed improvements, more efficient bus power management, new communication Modes, and new Device roles, including an ability to change Device Roles over time (i.e., the initial Controller can cooperatively pass the Controller Role to another I3C Device on the Bus, if the requesting I3C Device supports Secondary Controller feature).

1.1. Quick Facts

Table 1.1 presents a summary of the I3C Target IP Core.

Table 1.1. Quick Facts

IP Requirements	Supported FPGA Family	CrossLink™-NX, Certus™-NX, CertusPro™-NX, iCE40 UltraPlus™, MachXO5™-NX, Lattice Avant™
Resource Utilization	Supported User Interfaces	LMMI (Lattice Memory Mapped Interface), APB, AHB-Lite
	Resources	See Table A.1 and Table A.2.
Design Tool Support	Lattice Implementation	IP Core v3.x.x – Lattice Radiant software 2.2 or later
	Synthesis	Lattice Synthesis Engine (LSE)
		Synopsys® Synplify Pro for Lattice
	Simulation	For the list of supported simulators, see the Lattice Radiant Software User Guide.

1.2. Features

The maximum number of devices that an I3C Bus supports depends on trace length, capacitive load per Device, and the types of Devices (I2C versus I3C) present on the bus, because these factors affect clock frequency requirements. The Lattice I3C Target IP supports the following features:

- Two-wire serial interface up to 12.5 MHz using Push-Pull
- Legacy I2C Device co-existence on the same Bus (with some limitations)
- Dynamic Addressing
- I2C-like Single Data Rate messaging (SDR)
- Optional High Data Rate Modes (HDR)
  - HDR-DDR for Double Data Rate
- In-Band Interrupt and Hot-Join support
- Asynchronous Time Stamping (Mode 0)
- MIPI I3C Spec v1.1.1
- Target Reset without additional wires
- Monitoring Device Early Termination

The Lattice I3C Target IP does not support the following features:

- Optional High Data Rate Modes (HDR)
  - HDR-TSL for Ternary Symbol Legacy-inclusive-Bus (I^2C Devices allowed)
  - HDR-TSP for ternary Symbol for Pure Bus (no I^2C Devices allowed)
  - HDR-BT for Bulk Transport
- Virtual target
- Synchronous Timing and Asynchronous Time Stamping (Except Mode 0)
- Grouped Addressing

- Monitoring Device Early Termination
- D2D Tunneling
- Multi-Late Data Transfer

1.3. Conventions

1.3.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.3.2. Signal Names

Signal names that end with:

- _n are active low (asserted when value is logic 0)
- _i are input signals
- _o are output signals
- _io are bidirectional signals

1.3.3. Attribute

The names of attributes in this document are formatted in title case and italicized.

2. Functional Description

2.1. Overview

I3C Target IP supports several communication formats, all sharing a two-wire interface: SDA bidirectional data line and SCL input.

The Lattice I3C Target supports the following mode:

- SDR mode
- HDR-DDR mode

The I3C Target listens to I3C bus for relevant I3C commands sent by the I3C Controller and responds accordingly. This includes all Broadcast Commands (CCC), and any Directed Commands (CCC) addressed specifically to that I3C Target Device and supported by that I3C Target Device.

The I3C Target can also optionally:

- Request In-Band Interrupts
- Generate Hot-Join events

The I3C Target IP accepts commands from LMMI or from the optional APB/AHB-Lite interface. These commands are decoded into (1) configurations for the I3C Target that may be requested by the Controller and (2) I3C signals that the Target may transmit to the I3C bus.

Furthermore, the I3C Target can operate in interrupt or polling mode. This means that the user can choose to poll the I3C Target for a change in status at periodic intervals or wait to be interrupted by the I3C Target when data needs to be read or written.

I3C Target IP functional diagram is shown in Figure 2.1.

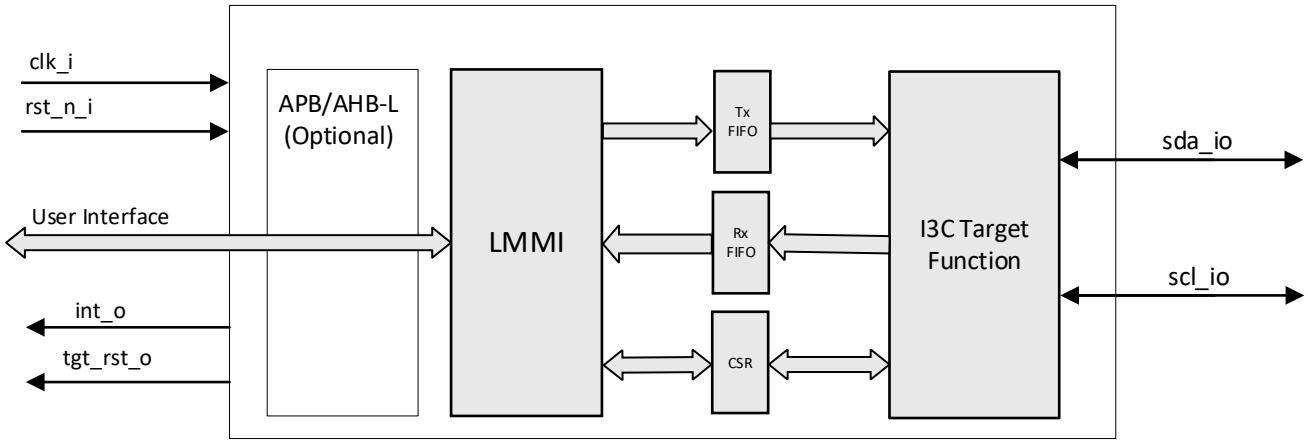

Figure 2.1. I3C Target IP Core Functional Diagram

2.2. Reset Propagation

To ensure that reset has been properly propagated inside the IP, wait for at least 20 system clock cycles after system reset de-assertion before doing any IP operation.

2.3. I3C Transfers in SDR Mode

The following section describes the I3C Target response for different I3C transactions from the Controller in SDR mode.

2.3.1. Broadcast CCC

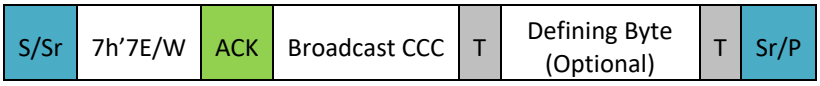

Figure 2.2. Broadcast CCC

When I3C Controller sends a broadcast CCC using the above format, the Target will ACK the I3C Broadcast Address 7'h7E/W. Depending on the received CCC and optional defining byte, the Target will process the command and respond accordingly.

2.3.2. Direct CCC

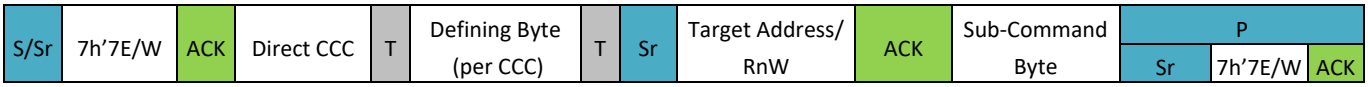

Figure 2.3. Direct CCC

When I3C Controller sends a direct CCC to the Target using the above format, the Target will ACK the I3C Broadcast Address 7'h7E/W. When the Target Address is transmitted in the bus at the address header, it will either:

1. ACK if the CCC and the optional defining byte are both supported and the CCC T-bit is correct.
2. NACK if CCC is not supported or CCC T-bit is incorrect.

Depending on the received CCC, the Target will process the command and respond accordingly.

2.3.3. Private Write

Figure 2.4. I3C Private Write Initiated with START Condition

Figure 2.5. I3C Private Write Initiated with Repeated START Condition

When I3C Controller initiates a Private Write to Target, the Target will ACK if it receives the I3C Broadcast Address 7'h7E/W or its own Address followed by a Write bit.

Data written by the Controller will be stored in the Rx FIFO of Target. If enabled in Target, interrupt *rxfifo_not_empty* will be asserted to notify User that Rx FIFO has data for reading.

2.3.4. Private Read

User shall typically write data to the Tx FIFO of Target first before the I3C Controller initiates a Private Read.

Figure 2.6. I3C Private Read Initiated with START Condition

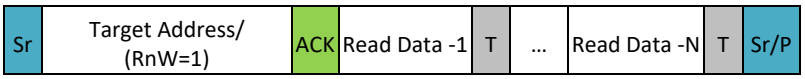

Figure 2.7. I3C Private Read Initiated with Repeated START Condition

When I3C Controller initiates a Private Read from Target, the Target will ACK if it receives the I3C Broadcast Address 7'h7E/W then its own Address followed by a Read bit. It will then proceed to transmit data that is stored in the Tx FIFO. Target will continue sending the Read data until Read is aborted by one of the following scenarios:

1. Controller stops the Read by pulling SDA Low in the T-bit of data.
2. All content of Tx FIFO has been transmitted. Target will signal end of Message by pulling SDA Low while SCL is Low in the T-bit of the last data then releasing SDA when it sees SCL positive edge. The Controller shall then take over SDA and generate a STOP or a Repeated START.

If Tx FIFO is empty when Controller initiates Private Read, Target will respond depending on *txfifo_empty_rd_nak* register.

1. If *txfifo_empty_rd_nak* is set to 0 (Default), Target will ACK its Address and return 0xFF Read Data then pull SDA Low at T-bit to signal end-of-message by default. If enabled, *read_txfifo_empty* interrupt will be set to notify User of the Private Read attempt by the Controller.
2. If *txfifo_empty_rd_nak* is set to 1, Target will NACK its Address.

2.4. I2C Mode

When Target is not yet assigned a Dynamic Address, it may act as an I2C Target given that it is assigned a Static Address. To assign a Static Address to the I3C Target IP, check the *Static Address Enable* attribute and input a valid Static Address (must not use reserved I3C addresses).

If Target is already assigned a Dynamic Address, it will no longer ACK when its Static Address is transmitted in the I3C bus.

2.4.1. I2C Write

In I2C Write, Target will ACK when its Static Address is transmitted in the I3C bus. The Controller then proceeds to send the 8-bit write data, then Target will pull down ACK at 9th bit to accept data.

Figure 2.8. I2C Write

2.4.2. I2C Read

In I2C Read, Target will ACK when its Static Address is transmitted in the I3C bus. It will then proceed to transmit read data in Open Drain mode then Controller will either: (1) ACK and continue reading the data or (2) NACK to end reading of data.

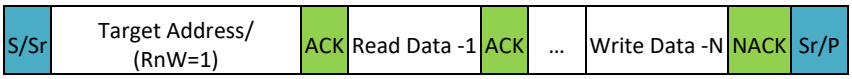

Figure 2.9. I2C Read

If Tx FIFO is empty when Controller initiates I2C Read, Target will respond depending on *txfifo_empty_rd_nak* register.

1. If *txfifo_empty_rd_nak* is set to 0 (Default), Target will ACK its Address and return 0xFF Read Data then wait for Controller to end I2C read by sending NACK. If enabled, *read_txfifo_empty* interrupt will be set to notify User of the Private Read attempt by the Controller.
2. If *txfifo_empty_rd_nak* is set to 1, Target will NACK its Address.

2.5. Common Command Codes

Table 2.1 lists the supported CCCs of this IP:

Table 2.1. Supported Common Command Codes

CCC	Type	Required[1]	Command
0x00	Broadcast	R	ENEC
0x01	Broadcast	R	DISEC
0x06	Broadcast	R	RSTDAA
0x07	Broadcast	R	ENTDAA
0x09	Broadcast	R	SETMWL
0x0A	Broadcast	R	SETMRL
0x2A	Broadcast	R	RSTACT
0x80	Direct	R	ENEC
0x81	Direct	R	DISEC
0x89	Direct	R	SETMWL
0x8A	Direct	R	SETMRL
0x8B	Direct	R	GETMWL
0x8C	Direct	R	GETMRL
0x90	Direct	R	GETSTATUS
0x9A	Direct	R	RSTACT
0x02	Broadcast	C	ENTAS0
0x03	Broadcast	O	ENTAS1
0x04	Broadcast	O	ENTAS2
0x05	Broadcast	O	ENTAS3
0x28	Broadcast	C	SETXTIME [2]
0x29	Broadcast	O	SETAASA
0x82	Direct	C	ENTAS0
0x83	Direct	O	ENTAS1
0x84	Direct	O	ENTAS2
0x85	Direct	O	ENTAS3
0x87	Direct	O	SETDASA
0x88	Direct	C	SETNEWDA
0x8D	Direct	C	GETPID
0x8E	Direct	C	GETBCR
0x8F	Direct	C	GETDCR
0x94	Direct	C	GETMXDS
0x95	Direct	C	GETCAPS
0x98	Direct	C	SETXTIME [2]
0x99	Direct	C	GETXTIME

Notes:

1. R – Required, O – Optional, C – Conditional
2. Supported Defining Bytes for SETXTIME CCC: 0xDF and 0xFF

2.6. I3C Transfers in HDR-DDR Mode

An HDR Mode period in the I3C Bus involves five steps:

1. The Controller sends a Broadcast Enter HDR Mode CCC indicating which HDR Mode to enter.
2. The I3C Bus switches from SDR Mode to the requested HDR Mode.
3. The Controller issues the first structured protocol per the HDR Mode framing, typically a Command or Header followed by optional Data sent by the Controller or the Target.
4. The Controller sends an HDR Restart Pattern or Exit Pattern.
5. If an HDR Restart Pattern is sent, then the Controller issues another structured protocol element for the New HDR Mode transfer. The Controller can repeat this process to remain in HDR Mode or send an HDR Exit Pattern to exit the HDR Mode.
6. If the Controller sends an HDR Exit Pattern, then it is always followed by an I3C STOP, which ends in the Bus Free Condition.

2.6.1. Typical HDR-DDR Mode Frame

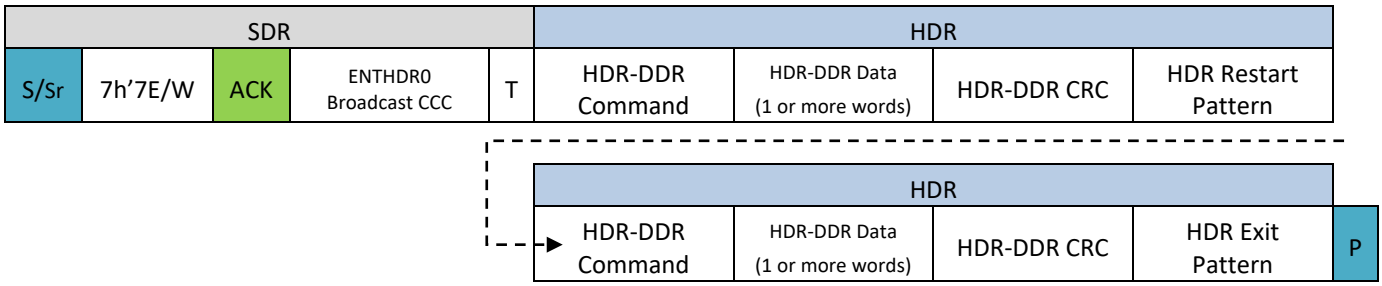

Figure 2.10. Typical HDR-DDR Mode Frame

2.6.2. HDR-DDR Write

	HDR-DDR Command			HDR-DDR Write Data (N)		HDR-DDR CRC	
Enter HDR or HDR Restart	[15] **1'b0** (Write) [14:8] Reserved	[7:1] Target Address [0] Parity Adj. (P0 = 1'b1)	ACK	[15:8] 1st Data Byte	[7:0] 2nd Data Byte	CRC5 for all Data	HDR Restart or Exit Pattern

Figure 2.11. HDR-DDR Write

2.6.3. HDR-DDR Read

	HDR-DDR Command			HDR-DDR Read Data (N)		HDR-DDR CRC	
Enter HDR or HDR Restart	[15] **1'b1** (Read) [14:8] Reserved	[7:1] Target Address [0] Parity Adj. (P0 = 1'b1)	ACK	[15:8] 1st Data Byte	[7:0] 2nd Data Byte	CRC5 for all Data	HDR Restart or Exit Pattern

Figure 2.12. HDR-DDR Read

2.6.4. HDR-DDR Broadcast CCCC

	HDR-DDR CCC Indicator			HDR-DDR CCC Command	
Enter HDR or HDR Restart	[15] **1'b0** (Write) [14:8] Reserved	[7:1] Broadcast Address [0] Parity Adj. (P0 = 1'b1)	ACK	[15:8] Broadcast CCC	[7:0] Defining Byte, 0x0 if unused

HDR-DDR CCC Data (Optional)		HDR-DDR CCC CRC	HDR-DDR CCC End Procedure
[15:8] 1st Data Byte	[7:0] 2nd Data Byte	CRC for all Data	

Figure 2.13. HDR-DDR Broadcast CCCC

2.6.5. HDR-DDR Direct Set CCC

	HDR-DDR CCC Indicator			HDR-DDR CCC Command		HDR-DDR CCC CRC
Enter HDR or HDR Restart	[15] **1'b0** (Write) [14:8] Reserved	[7:1] Broadcast Address [0] Parity Adj. (P0 = 1'b1)	ACK	[15:8] Direct CCC	[7:0] Defining Byte, 0x0 if unused	CRC for CCC Command

	HDR-DDR CCC Selector			HDR-DDR CCC Set Data (N times)		HDR-DDR CCC CRC
HDR Restart	[15] **1'b0** (Write) [14:8] Reserved	[7:1] Target Address [0] Parity Adj. (P0 = 1'b1)	ACK	[15:8] 1st Data Byte	[7:0] 2nd Data Byte	CRC for all Data

HDR-DDR CCC End Procedure

Figure 2.14. HDR-DDR Direct Set CCC

2.6.6. HDR-DDR Direct Get CCC

	HDR-DDR CCC Indicator			HDR-DDR CCC Command		HDR-DDR CCC CRC
Enter HDR or HDR Restart	[15] **1'b0** (Write) [14:8] Reserved	[7:1] Broadcast Address [0] Parity Adj. (P0 = 1'b1)	ACK	[15:8] Direct CCC	[7:0] Defining Byte, 0x0 if unused	CRC for CCC Command

	HDR-DDR CCC Selector			HDR-DDR CCC Get Data (N times)		HDR-DDR CCC CRC
HDR Restart	[15] **1'b1** (Read) [14:8] Reserved	[7:1] Target Address [0] Parity Adj. (P0 = 1'b1)	ACK	[15:8] 1st Data Byte	[7:0] 2nd Data Byte	CRC for all Data

Target to Controller Handoff	HDR-DDR CCC End Procedure

Figure 2.15. HDR-DDR Direct Get CCC

2.7. Hot-Join Mechanism

The I3C Target Device may issue a Hot-Join request to join the I3C bus after the bus is already configured. Target initiates Hot-Join Request by sending an IBI using the reserved address 7'h02 with Write bit after a START condition.

The Target may initiate Hot-Join by one of the following methods:

1. Passive – I3C Target may wait for a START condition transmitted in the I3C bus. It may then proceed to transmit the reserved address 7’h02 in the arbitrable address header.

   Note: I3C Target needs to know first if it is in an I3C bus before initiating Hot-Join passively. An I3C Bus is determined by an SDR Frame with START followed by the Broadcast Address. (See Errata 01 for MIPI I3C Specification, Specification Version 1.1.1).
2. Active – If the I3C Target detects Bus Idle condition, it may generate a START by pulling the SDA line Low and waiting for the I3C Controller to complete the start condition by pulling SCL low.

The Target will then proceed to send the reserved address 7’h02 in the arbitrable address header after the START condition.

2.7.1. Generating a Hot-Join Request

The I3C Target IP supports Hot-Join when the attribute *Hot-Join Capable* is checked.

To initiate a Hot Join request, confirm that Hot-Join is allowed by the Controller by reading the hj_en_ec register. If allowed (hj_en_ec is set to 1’b1), set the hj_req register to 1’b1. I3C Target will attempt to transmit the Hot-Join request in the I3C bus by either active or passive method as described above. If the Target loses address arbitration, it will stop transmitting the Hot-Join address and wait for the next valid opportunity to retransmit the Hot-Join request depending on retry settings. When the Hot-Join request has been generated, hj_req_gen interrupt will be asserted.

If I3C Controller ACKs the request, I3C Target has successfully joined the I3C bus and hj_done interrupt will be asserted to inform User that Hot-Join was successful. The Target will then wait for Dynamic Address Assignment.

If the Hot-Join request is NACKed by I3C Controller, hj_acnack interrupt will be asserted and I3C Target will then wait for the next valid condition to retry transmitting the Hot-Join request until the I3C Controller ACKs the request. If the Hot-Join request has been generated and NACKed by the Controller for hj_ibi_retry times, hj_done and hj_acknack interrupts will be asserted to inform User that Hot-Join was not successful.

2.8. In-Band Interrupt

In-Band Interrupts may be issued by I3C Targets to signal pending action from the I3C Controller.

The I3C Target issues IBI by sending its own address in the Arbitrated Address Header with a Read bit after a START condition.

The Target may initiate IBI by one of the following methods:

1. Passive – I3C Target may wait for a START condition transmitted in the I3C bus. It may then proceed to transmit its own dynamic address in the arbitrable address header.
2. Active – If I3C Bus Available condition is detected, I3C Target may generate a START by pulling the SDA line Low and waiting for the I3C Controller to complete the start condition by pulling SCL low.

The Target will then proceed to transmit its address in the arbitrable address header after the START condition.

2.8.1. Generating an In-band Interrupt

The I3C Target IP supports IBI when the attribute *IBI Capable* is checked.

To initiate an In-Band Interrupt, confirm that IBI is allowed by the Controller by reading the ibi_en_ec register. If allowed (ibi_en_ec is set to 1’b1), set the ibi_req register to 1’b1. I3C Target will attempt to transmit its own Dynamic Address in the arbitrable Address Header after a START condition. If the Target loses address arbitration, it will stop sending the IBI and wait for the next valid opportunity to retry sending the IBI. If IBI has been successfully generated, ibi_req_gen interrupt will be asserted.

If IBI is ACKed by the Controller, I3C Controller shall read the payload following IBI depending on BCR[2] of I3C Target.

- If BCR[2] is set to 0: there is no data byte following the IBI. *ibi_done* interrupt will be asserted.

- If BCR[2] is set to 1: the IBI has the following Mandatory Data Byte that shall be read by the Controller. The Target may also optionally send additional IBI data bytes (up to IBI Payload Size Limit by the Controller via the SETMRL CCC command). *ibi_done* interrupt will be asserted when reading of the IBI payload is stopped either by the Target or the Controller.

If IBI is NACKed by the I3C Controller, ibi_acknack interrupt will be asserted and I3C Target will then wait for the next valid condition to send the IBI until the I3C Controller ACKs the request. If IBI has been generated and NACKed by the Controller for hj_ibi_retry times, ibi_done and ibi_acknack interrupts will also be set to 1 to inform User that IBI was not successful.

2.8.2. Sending the IBI Payload

To send an IBI with mandatory data byte and optional additional payload (up to maximum IBI payload size), User shall write the data bytes to Tx FIFO with MDB as the first data and the additional IBI payload as the succeeding data. When the IBI is generated by Target and ACKed by the Controller, the Target will proceed to send the MDB and the additional data bytes until the maximum IBI payload size.

When all IBI payload is transmitted, i.e., maximum IBI payload size has been reached or Tx FIFO is empty, Target will end the transfer by pulling SDA Low at T-bit. ibi_done interrupt will be asserted to notify User that IBI is done, and all payload has been transmitted.

If the Controller chooses to end reading the additional IBI payload by pulling SDA Low during T-bit, ibi_done and ibi_payld_terminated interrupts will be set to 1 to notify User that IBI transfer is done but payload transfer is incomplete. When this interrupt is received, User may choose to reset the Tx FIFO by setting the txfifo_rst register.

2.8.3. Pending Read Notification

Pending Read Notification (MDB[7:5] = 3'b101) is supported by this IP.

If the I3C Controller accepts an IBI and reads the Pending Read Notification MDB from the Target, the Target considers Pending Read Notification as Active. Read Data associated with the MDB shall be available at the next Private Read.

For pending read notification, User shall write the data bytes to the Tx FIFO in this order:

1. Pending Read Notification MDB
2. IBI Payload (equal to maximum IBI payload size)
3. Associated read data

Only one Pending Read Notification may be active at a time while the Target is waiting for the Controller to read data. This means that when a Pending Read Notification is active, the Target cannot send another IBI with MDB for Pending Read Notification.

2.8.4. Limitation for IBI and Private Read

IBI Payload and read data from User are both stored in the Tx FIFO. If IBI Payload or Data for Private Read are written continuously to the Tx FIFO without being transmitted to the Controller (via IBI or Private Read), the intended data may not be sent correctly by the Target.

User shall ensure that all data corresponding to an intended IBI or Private Read has been transferred before initiating another IBI or Private Read. User may read the status registers ibi_payld_terminated (for IBI) and read_aborted (for Private Read) to confirm if all contents of Tx FIFO has been transmitted. If the status registers are set, transfer of Tx FIFO contents is not completed. When this occurs, User has the option to reset the Tx FIFO before writing new data for the next IBI or Private Read to ensure correctness of data.

2.9. Target Reset

Target Reset Action is configured by the Controller via RSTACT CCC. This will be the action of Target when it receives the Target Reset Pattern following an RSTACT CCC in a single frame. Following are the supported Defining Bytes of this IP:

Table 2.2. Target Reset

Defining Byte	Action	Description
0x0	No Action	No action.
0x1	Reset I3C Peripheral only	Reset I3C states and FIFO. Equivalent to *ip_core_rst* soft reset.
0x2	Reset Whole Target	Reset whole Target including DAA and previously configured settings via CCCs and register access. Equivalent to *ip_main_rst* soft reset.

When the IP receives RSTACT CCC, it informs the User by asserting rstact_ccc_rcvd interrupt. The configured reset action is stored in tgt_rst_act_set register. User shall read this register to determine what action to do when the Target Reset Pattern is received. When Target detects the following Target Reset Pattern, it then asserts tgt_rst_ptrn_rcvd interrupt. When User sees this interruption, User may then perform the configured reset action or inaction. User can use the soft reset registers, or the system reset (for whole Target reset) to perform the configured reset action.

The behavior is different when Target receives Target Reset Pattern without RSTACT. When Target receives Target Reset Pattern without RSTACT for the first time, it automatically resets the I3C Peripheral. If this occurs a second time, tgt_rst_o output is asserted. This informs the User to reset Whole Chip (Target Reset Escalation).

2.10. Secondary Controller Support

The I3C Target IP is instantiated by the I3C Controller IP when Secondary Controller support is enabled. All the capabilities of the I3C Target will then be available to the Secondary-Controller capable device.

2.10.1. Generating the Controller Role Request

To initiate a Controller Role request, confirm that Controller Role request is allowed by the Controller by reading the cr_en_ec register. If allowed (cr_en_ec is set to 1'b1), set the cr_req register to 1'b1. I3C Target will attempt to transmit its own Dynamic Address in the arbitrable Address Header after a START condition. If Target loses address arbitration, it will stop sending the Controller Role request and wait for the next valid opportunity to retry sending the request. If the Controller Role request has been successfully generated, cr_req_gen interrupt will be asserted.

If the request is ACKed by the Controller, cr_req_done interrupt will be asserted.

If the request is NACKed by the I3C Controller, I3C Target will then wait for the next valid condition to send the request until the I3C Controller ACKs. If the Controller Role request has been generated and NACKed by the Controller for hj_ibi_retry times, cr_req_done and cr_req_acknack interrupts will also be set to 1 to inform User that Controller Role request was not successful.

2.10.2. CCC for Secondary Controller Support

Table 2.3 lists the CCCs supported when Secondary Controller feature is enabled.

Table 2.3 CCCs for Secondary Controller Support

CCC	Type	Command Name
0x08	Broadcast	DEFTGTS
0x91	Direct	GETACCCR

2.11. HDR Support

This IP supports the following HDR mode:

- HDR-DDR mode

2.11.1. CCCs Permitted in HDR Mode

Table 2.4 lists CCCs supported by this IP in SDR mode and permitted in HDR mode, with notes and limitations.

Table 2.4 CCCs Supported in HDR Mode

CCC	Type	Command Name	Notes and Limitations	Supported in this IP?
0x00	Broadcast	ENEC	May not generally be useful in HDR Modes, as the Controller would need to exit HDR and return to SDR Mode for the Target to be able to raise any of the request types that are affected by these CCCs; see Section 5.2.1.2.4 of I3C MIPI specification.	Yes
0x01	Broadcast	DISEC		Yes
0x02	Broadcast	ENTAS0	See Section 5.2.1.2.4 of I3C MIPI Specification.	Yes
0x03	Broadcast	ENTAS1	See Section 5.2.1.2.4 of I3C MIPI Specification.	Yes
0x04	Broadcast	ENTAS2	See Section 5.2.1.2.4 of I3C MIPI Specification.	Yes
0x05	Broadcast	ENTAS3	See Section 5.2.1.2.4 of I3C MIPI Specification.	Yes
0x08	Broadcast	DEFTGTS	Not recommended for use in HDR Modes; generally only used for Secondary Controllers, to announce lists of known Targets, following changes to Target Dynamic Addresses or Hot-Join events, neither of which are permitted within HDR Modes.	No
0x09	Broadcast	SETMWL	See Section 5.2.1.2.4 of I3C MIPI Specification.	Yes
0x0A	Broadcast	SETMRL	See Section 5.2.1.2.4 of I3C MIPI Specification.	Yes
0x12	Broadcast	ENDXFER	Not recommended for use in HDR Modes.	Yes
0x28	Broadcast	SETXTIME	No limitations.	Yes
0x2A	Broadcast	RSTACT	Not recommended for use in HDR Modes.	No
0x80	Direct	ENEC	May not generally be useful in HDR Modes, as the Controller would need to exit HDR and return to SDR Mode for the Target to be able to raise any of the request types that are affected by these CCCs; see Section 5.2.1.2.4 of I3C MIPI specification.	Yes
0x81	Direct	DISEC		Yes
0x82	Direct	ENTAS0	See Section 5.2.1.2.4 of I3C MIPI Specification.	Yes
0x83	Direct	ENTAS1	See Section 5.2.1.2.4 of I3C MIPI Specification.	Yes
0x84	Direct	ENTAS2	See Section 5.2.1.2.4 of I3C MIPI Specification.	Yes
0x85	Direct	ENTAS3	See Section 5.2.1.2.4 of I3C MIPI Specification.	Yes
0x89	Direct	SETMWL	See Section 5.2.1.2.4 of I3C MIPI Specification.	Yes
0x8A	Direct	SETMRL	See Section 5.2.1.2.4 of I3C MIPI Specification.	Yes
0x8B	Direct	GETMWL	No limitations.	Yes
0x8C	Direct	GETMRL	No limitations.	Yes
0x8E	Direct	GETBCR	Not recommended for use in HDR Modes.	Yes
0x8F	Direct	GETDCR	Not recommended for use in HDR Modes.	Yes
0x90	Direct	GETSTATUS	No limitations.	Yes
0x92	Direct	ENDXFER	Not recommended for use in HDR Modes.	Yes
0x94	Direct	GETMXDS	No limitations.	Yes

0x95	Direct	GETCAPS	No limitations.	Yes
0x98	Direct	SETXTIME	No limitations.	Yes
0x99	Direct	GETXTIME	No limitations.	Yes
0x9A	Direct	RSTACT	Not recommended for use in HDR Modes.	No

2.12. Signal Description

Table 2.5 lists the input and output signals for I3C Target IP Core along with their descriptions.

Table 2.5 Ports Description

Signal Name	Direction	Description
System Clock and Reset		
rst_n_i	Input	Asynchronous Active Low System Reset from User.
clk_i	Input	System Clock (Fmax = 125 MHz).
tgt_rst_o	Output	Active High flag for Full Chip Reset by Target Reset escalation.[1]
I3C Interface (Internal IO Primitive)[2]		
scl_io	Inout	Bidirectional I3C Serial Clock.
sda_io	Inout	Bidirectional I3C Serial Data.
I3C Interface (External IO Primitive)[3]		
ext_scl_i	Input	I3C Serial Clock Input.
ext_sda_i	Input	I3C Serial Data Input.
ext_sda_o	Output	I3C Serial Data Output.
ext_sda_oe	Output	Active High I3C Serial Data Output Enable.
LMMI[4]		
lmmi_request_i	Input	Start transaction.
lmmi_wr_rdn_i	Input	Write = HIGH, Read = LOW.
lmmi_offset_i[7:0]	Input	Register offset within Target, starting at offset 0.
lmmi_wdata_i[7:0]	Input	Write data
lmmi_rdata_o[7:0]	Output	Read data.
lmmi_rdata_valid_o	Output	Read transaction is complete and lmmi_rdata_o contains valid data.
lmmi_ready_o	Output	Target is ready to start a new transaction.
LINTR Interface		
int_o	Output	Interrupt to the user. Stays high while an enabled interrupt is active.
AHB-Lite Interface[5]		
ahbl_hsel_i	Input	AHB-Lite Select signal.
ahbl_hready_i	Input	AHB-Lite Ready Input signal.
ahbl_haddr_i[9:0]	Input	AHB-Lite Address signal. [4]
ahbl_hburst_i[2:0]	Input	AHB-Lite Burst Type signal. Only single burst type is supported.
ahbl_hsize_i[2:0]	Input	AHB-Lite Transfer Size signal. Only Byte is supported.
ahbl_hmastlock_i	Input	AHB-Lite Locked Sequence signal. (Not supported in this IP)
ahbl_hprot_i[3:0]	Input	AHB-Lite Protection Control signal. (Not supported in this IP)
ahbl_htrans_i[1:0]	Input	AHB-Lite Transfer Type signal.
ahbl_hwrite_i	Input	AHB-Lite Direction signal. Write = High, Read = Low.
ahbl_hwdata_i[7:0]	Input	AHB-Lite Write Data signal.
ahbl_hreadyout_o	Output	AHB-Lite Ready Output signal.
ahbl_hrdata_o[7:0]	Output	AHB-Lite Read Data signal.
ahbl_hresp_o	Output	AHB-Lite Transfer Response signal.
APB Interface[6]		

apb_paddr_i[9:0]	Input	APB Address signal.[7]
apb_psel_i	Input	APB Select signal.
apb_penable_i	Input	APB Enable signal.
apb_pwrite_i	Input	APB Direction signal.
apb_pwdata_i[7:0]	Input	APB Write Data signal.
apb_pready_o	Output	APB Ready signal.
apb_prdata_o[7:0]	Output	APB Read Data signal.
apb_pslverr_o	Output	APB Completer Error signal.
Direct FIFO Interface[8]		
tx_valid_i	Input	Tx data valid signal. The user will set this to high when sending data (tx_data_i) to Tx FIFO.
tx_ready_o	Output	Tx FIFO ready signal. When high, it means Tx FIFO can accept incoming data. tx_data_i will be written to Tx FIFO when tx_valid_i and tx_ready_o == 1.
tx_data_i [7:0]	Input	Tx Data.
rx_valid_o	Output	Rx data valid signal. When high, it means Rx FIFO is not empty and rx_data_o contains valid data.
rx_ready_i	Input	Rx ready signal. The user will set this to high when it is ready to accept the Rx data. rx_data_o will take the next Rx FIFO entry when rx_valid_o and rx_ready_i == 1.
rx_data_o	Output	Rx data.

Notes:

1. For more details on target reset, see Section 5.1.11 of the MIPI Specification for I3C.
2. Bidirectional I3C interface is only available when internal IO primitives are enabled in IP generation GUI.
3. External IO I3C interface is only available when internal IO primitives are disabled in IP generation GUI.
4. LMMI Interface is only available when selected from the *User Interface*.
5. AHB-Lite Interface is only available when selected from the *User Interface*. Refer to AMBA 3 AHB-Lite Protocol Specification for details of the protocol.
6. APB Interface is only available when selected from the *User Interface*. Refer to AMBA 3 APB Protocol v1.0 Specification for details of the protocol.
7. For APB and AHB-Lite, Address port size will depend on *Address Offset* attribute.
   If *Address Offset* is in Bytes, address port is 8 bits: apb_paddr_i[7:0] and ahbl_haddr_i[7:0]
   If *Address Offset* is in DWORD, address port is 10 bits: apb_paddr_i[9:0] and ahbl_haddr_i[9:0]
8. Direct FIFO interface is only available when enabled in IP generation GUI.

2.13. Attributes Summary

Table 2.6 provides the list of user-selectable and compile time configurable parameters for the I3C Target IP Core. The parameter settings are specified using I3C Target IP Core Configuration user interface in Lattice Radiant.

Table 2.6 Attributes Summary

Attribute	Selectable Values	Default	Description
General			
User Interface	LMMI, APB, AHBL	APB	Selects memory-mapped interface from the list for register access by the host. Available values: LMMI (default), APB, AHBL.
Address Offset	*Address Offset* in Bytes, Address Offset in DWORD	*Address Offset* in DWORD	Selects addressing mode for registers. Applicable only when the *User Interface* is APB or AHBL. LMMI always uses byte addressing.
Optional Interface			
Enable Direct FIFO Interface	Checked, Unchecked	Unchecked	Select to provide a separate interface for (FIFO) data path.
Tx Data Width	-	8	Display Only.
Rx Data Width	-	8	Display Only.

IO Primitive Enable			
Enable internal IO primitive	Checked, Unchecked	Checked	Option to include or remove the IO primitive instance inside the IP. This means that SDA and SCL are seen as bidirectional IO ports at the top level. This option is enabled by default. Some FPGA devices might not have an IO that supports I3C. In that case, the user must disable this option and provide a custom IO. When this option is disabled, the SDA and SCL IO control signals (including pull up resistor controls) are exposed at the top level as ports.
Bus Characteristics			
Bus Type	SDR only, HDR-capable	SDR only	Indicates whether IP supports both SDR and HDR modes or SDR mode only.
HDR Mode	HDR-DDR	HDR-DDR	Indicates which HDR mode is supported. Applicable only when *Bus Type* = HDR-capable.
IBI Capable	Checked, not checked	Checked	Indicates whether IP supports IBI or not.
IBI Payload Size (including MDB)	0 – 255	1	Payload size (including MDB) following an IBI. If set to 0, no payload follows the IBI. Applicable only when *IBI Capable* = True.
Hot-Join Capable	Checked, not checked	Checked	Indicates whether IP supports Hot-Join or not.
Maximum Data Speed Limitation	Checked, not checked	Checked	Sets Bit 0 of BCR. When set to 1, Target device supports MXDS CCC to relay timing information to the Controller.
Device Characteristics			
DCR (HEX)	00 – FF	00	Device Characteristics register. It is recommended to assign a value to this register according to the list of the devices, which can be found at I3C Device Characteristics Register.
Manufacturer ID	0 – 32767	414	Defines Provisional ID[47:33] bits.
Part ID	0 – 65535	1	Defines Provisional ID[31:16] bits.
Instance ID	0 – 15	1	Defines Provisional ID[15:12] bits.
Additional ID	0 – 4095	0	Defines Provisional ID[11:0] bits.
Static Address Enable	Checked, not checked	Checked	Indicates that Target device may be assigned a Static Address.
Static Address (HEX) [1]	00 - 7F	08	Sets device static address. Applicable only when Static Address enable = True
Timing Characteristics			
System Clock Frequency (MHz)	Up to 50 MHz	25 MHz	Sets the system clock (clk_i) frequency.
Write Maximum Data Rate (MHz)	12.5 MHz	12.5 MHz	Display only. Applicable only when *Maximum Data Speed Limitation* = True. Indicates maximum sustained data rate for non-CCC Messages sent by Controller Device to Target Device.
Clock-to-data Turnaround Delay (t_{SCO})	–	0	Display only. Applicable only when *Maximum Data Speed Limitation* = True. Clock-to-Data Turnaround Time.
Read Maximum Data Rate (MHz)	–	12.5 MHz	Display only. Applicable only when *Maximum Data Speed Limitation* = True. Indicates maximum sustained data rate for non-CCC Messages sent by Target Device to Controller Device.
Maximum Read Turnaround Time (us)	–	0	Display only. Applicable only when *Maximum Data Speed Limitation* = True. Indicates how long the Controller needs to wait before reading

			the data it requested.

Note:
1. Static address must not use reserved I2C addresses.

2.14. Register Description

This section describes the configuration, control, and status registers of the IP. These are accessible via LMMI or the optional APB/AHB-Lite interface. By default, byte addressing is used for the registers.

If APB/AHB-Lite is selected, the user has the option to change addressing to DWORD. When DWORD addressing is selected, the register address is decoded from 8 leftmost bits of the address.

For example: LMMI offset 8'h01 -> APB/AHB-L DWORD address = {8'h01, 2'b00} or 10'h004

2.14.1. Bus Characteristics Register 0x00

Table 2.7 shows the Target Bus Characteristics Register.

Table 2.7. Bus Characteristics Register

Bits	Name	Access	Width	Reset
[7:6]	device_role	read-only	2	0x0 (Fixed)
[5]	advanced_caps	read-only	1	0x0
[4]	virtual_tgt_support	read-only	1	0x0 (Fixed)
[3]	offline_capable	read-only	1	0x0 (Fixed)
[2]	ibi_payload	read-only	1	0x1
[1]	ibi_capable	read-only	1	0x1
[0]	max_d_speed_limit	read-only	1	0x1

device_role

Fixed to 2'b00.

2'b00 – I3C Target.

2'b01 – I3C Controller-capable (Not implemented in this IP).

Others - Reserved for future definition by MIPI Alliance I3C WG (Not supported in this IP).

advanced_caps

0 – Does not support optional advanced capabilities.

1 – Supports optional advanced capabilities. When Target is configured with IBI capability and IBI payload, this is set to 1 for optional Pending Read MDB support.

virtual_tgt_support

Fixed to 0.

0 – Is not a Virtual Target and does not expose other downstream Device(s).

1 – Is a Virtual Target, or exposes other downstream Device(s) (Not supported in this IP).

offline_capable

Fixed to 0.

0 – Device will always respond to I3C Bus commands.

1 – Device will not always respond to I3C Bus Commands (Not supported in this IP).

ibi_payload

From *IBI Payload Size* attribute

0 – If *IBI Payload Size* attribute is set to 0. No data bytes follow the IBI.

1 – If *IBI Payload Size* attribute is set to greater than or equal to 1. One data byte (MDB) shall follow the accepted IBI, and additional data bytes may follow.

ibi_capable

From *IBI Capable* attribute

0 – Unchecked. Not capable.

1 – Checked. Capable.

max_d_speed_limit

From *Maximum Data Speed Limitation* attribute

0 – Unchecked. No limitation.

1 – Checked. With limitation. Controller shall use GETMXDS CCC to get specific limitation from Target.

2.14.2. Device Characteristics Register 0x01

Table 2.8 shows the Target Device Characteristics Register.

Table 2.8. Device Characteristics Register

Bits	Name	Access	Width	Reset
[7:0]	dcr	read-only	8	Takes the DCR parameter value

dcr

Device ID set by *User through DCR* attribute.

255 available codes for describing the type of sensor or Device (e.g., accelerometer, gyroscope, composite Devices). Default value is 8'b0 for generic Device.

2.14.3. Dynamic Address 0x02

Table 2.9 shows the assigned dynamic address and done flag.

Table 2.9. Dynamic Address

Bits	Name	Access	Width	Reset
[7]	daa_done	read-only	1	0x0
[6:0]	dyn_addr	read-only	7	0x0

daa_done

0 – dyn_addr is not yet assigned or is reset by RSTDAA CCC

1 – dyn_addr is assigned via ENTDAA, SETNEWDA, SETAASA or SETDASA CCC

dyn_addr

Dynamic Address Assigned to I3C Target

2.14.4. Events Command Enable 0x03

Table 2.10 shows the Hot-Join and IBI enable from Controller via ENEC/DISEC CCC.

Table 2.10. Events Command Enable

Bits	Name	Access	Width	Reset
[7:4]	*reserved*	read-only	4	0x0
[3]	hj_enec	read-only	1	0x1 – If Target is Hot-Join Capable 0x0 – If Target is not Hot-Join Capable
[2:1]	*reserved*	read-only	2	0x0
[0]	ibi_enec	read-only	1	0x1 – If Target is IBI Capable 0x0 – If Target is not IBI Capable

hj_enec
Hot-Join Enable by Controller
0 – Target-initiated Hot-Join is not allowed on the I3C bus.
1 – Target-initiated Hot-Join is allowed on the I3C bus.

ibi_enec

IBI Enable by Controller

0 – Target-initiated interrupts are not allowed on the I3C bus.

1 – Target-initiated interrupts are allowed on the I3C bus.

2.14.5. Events Command Device Configuration 0x04

Table 2.11 shows the Hot-Join and IBI capability configured by user using attributes.

Table 2.11. Events Command Device Configuration

Bits	Name	Access	Width	Reset
[7:4]	*reserved*	read-only	4	0x0
[3]	hj_cap	read-only	1	0x1 – If Target is Hot-Join Capable 0x0 – If Target is not Hot-Join Capable
[2:1]	*reserved*	read-only	2	0x0
[0]	ibi_cap	read-only	1	0x1 – If Target is IBI Capable 0x0 – If Target is not IBI Capable

hj_cap

0 – Target device is configured without Hot-Join Capability.

1 – Target device is configured with Hot-Join Capability.

ibi_cap

0 – Target device is configured without IBI Capability.

1 – Target device is configured with IBI Capability.

2.14.6. Events Command Request 0x05

Table 2.12 shows Hot-Join and IBI request from user.

Table 2.12. Events Command Request

Bits	Name	Access	Width	Reset
[7:4]	*reserved*	read-only	4	0x0
[3]	hj_req	read-write	1	0x0
[2:1]	*reserved*	read-only	2	0x0
[0]	ibi_req	read-write	1	0x0

hj_req

When set to High, Target will initiate Hot-Join request at the next valid opportunity. Reset to 0 when Hot-Join is done or disabled by the Controller.

ibi_req

When set to High, Target will initiate IBI at the next valid opportunity. Reset to 0 when IBI is done or disabled by the Controller.

2.14.7. Hot-Join/IBI Retry 0x06

Table 2.13 shows the number of retries for Hot-Join and IBI.

Table 2.13. Hot-Join/IBI Retry

Bits	Name	Access	Width	Reset
[7:0]	hj_ibi_retry	read-write	8	0x8

hj_ibi_retry

Indicates number of times the Target retries Hot-Join or IBI when it is NACKed by the Controller.
When set to 0, the number of tries is not limited.

2.14.8. Maximum Write Length (MSB) 0x07

Table 2.14 shows the most significant byte of Maximum Write Length set by the Controller.

Table 2.14. Maximum Write Length (MSB)

Bits	Name	Access	Width	Reset
[7:0]	mwl_msb	read-only	8	0x02

mwl_msb

Most Significant Byte of maximum write length set by I3C Controller via SETMWL CCC.

If SETMWL is greater than default value 512 (FIFO size), MWL will be set to 512.

2.14.9. Maximum Write Length (LSB) 0x08

Table 2.15 shows the least significant byte of Maximum Write Length set by the Controller.

Table 2.15. Maximum Write Length (LSB)

Bits	Name	Access	Width	Reset
[7:0]	mwl_lsb	read-only	8	0x00

mwl_lsb

Least Significant Byte of maximum write length set by I3C Controller via SETMWL CCC.

If SETMWL is greater than default value 512 (FIFO size), MWL will be set to 512.

2.14.10. Maximum Read Length (MSB) 0x09

Table 2.16 shows the most significant byte of Maximum Read Length set by the Controller.

Table 2.16. Maximum Read Length (MSB)

Bits	Name	Access	Width	Reset
[7:0]	mrl_msb	read-only	8	0x02

mrl_msb

Most Significant Byte of maximum write length set by I3C Controller via SETMRL CCC.

If SETMRL is greater than default value 512 (FIFO size), MRL will be set to 512.

2.14.11. Maximum Read Length (LSB) 0x0A

Table 2.17 shows the least significant byte of Maximum Read Length set by the Controller.

Table 2.17. Maximum Read Length (LSB)

Bits	Name	Access	Width	Reset
[7:0]	mrl_lsb	read-only	8	0x00

mrl_lsb

Least Significant Byte of maximum write length set by I3C Controller via SETMRL CCC.

If SETMRL is greater than default value 512 (FIFO size), MRL will be set to 512.

2.14.12. Maximum IBI Payload Size 0x0B

Maximum IBI Payload Size set by the Controller. Applicable only when Target is configured with IBI capability and IBI payload is set to greater than or equal to 1.

Table 2.18. Maximum IBI Payload Size

Bits	Name	Access	Width	Reset
[7:0]	max_ibi_payld	read-only	8	0x02

max_ibi_payld

Maximum IBI Payload set by I3C Controller via SETMRL CCC.

If the value is greater than FIFO size, the register will be set to FIFO size.

Unlimited payload size is not supported in this IP.

2.14.13. Maximum Write Data Speed (MaxWr) 0x0C

Applicable only when Target is configured with Maximum Data Speed Limitation.

Table 2.19. Maximum Write Data Speed (MaxWr)

Bits	Name	Access	Width	Reset
[7:4]	*reserved*	read-only	4	0x0
[3]	mxds2_w_defbyte	read-only	1	0x0 (Fixed)
[2:0]	mxds2_w_rate	read-write	3	0x0

mxds2_w_defbyte

0 – Target does not support defining byte for GETMXDS CCC.

1 – Target supports defining byte for GETMXDS CCC. (Not supported in this IP)

mxds2_w_rate

Maximum Sustained Data Rate for non-CCC Messages sent by Controller Device to Target Device

0 – f_{SCL} Max (default value)

1 – 8 MHz

2 – 6 MHz

3 – 4 MHz

4 – 2 MHz

Others –Reserved for future use by MIPI Alliance.

2.14.14. Maximum Read Data Speed (MaxRd) 0x0D

Applicable only when Target is configured with Maximum Data Speed Limitation.

Table 2.20. Maximum Read Data Speed (MaxRd)

Bits	Name	Access	Width	Reset
[7]	*reserved*	read-only	1	0x0
[6]	mxds2_r_wr2rd_stop	read-only	1	0x0 (Fixed)
[5:3]	mxds2_r_tsco	read-write	3	0x0
[2:0]	mxds2_r_rate	read-write	3	0x0

mxds2_r_wr2rd_stop

If maximum read turnaround time is not 0, then this field is used to tell the Controller whether the Target permits the Write-to-Read to be split by a STOP.

0 –STOP would cancel the Read

1 – The Target permits the Write-to-Read to be split by a STOP.. (Not supported in this IP)

mxds2_r_tsco

Clock to Data Turnaround Time (t_{SCO})

0 – ≤ 8 ns (default value)

1 – ≤ 9 ns

2 – ≤ 10 ns

3 – ≤ 11 ns

4 – ≤ 12 ns

5–6 – Reserved for future use by MIPI Alliance.

7 – t_{SCO} is > 12 ns, and is reported by private agreement.

mxds2_r_rate

Maximum Sustained Data Rate for non-CCC Messages sent by Target Device to Controller Device.

0 – f_{SCL} Max (default value)

1 – 8 MHz

2 – 6 MHz

3 – 4 MHz

4 – 2 MHz

Others – Reserved for future use by MIPI Alliance

2.14.15. Maximum Read Turnaround Time (MSB) 0x0E

Applicable only when Target is configured with Maximum Data Speed Limitation.

Table 2.21. Maximum Read Turnaround Time (MSB)

Bits	Name	Access	Width	Reset
[7:0]	max_rdturn_b2	read-write	8	0x0

max_rdturn_b2

Maximum Read Turnaround Time in µs.

Most significant byte of 24-bit field that can encode turnaround times from 0.0 seconds to 16 seconds.

2.14.16. Maximum Read Turnaround Time 0x0F

Applicable only when Target is configured with Maximum Data Speed Limitation.

Table 2.22. Maximum Read Turnaround Time

Bits	Name	Access	Width	Reset
[7:0]	max_rdturn_b1	read-write	8	0x0

max_rdturn_b1

Maximum Read Turnaround Time in µs.

Middle byte of 24-bit field that can encode turnaround times from 0.0 seconds to 16 seconds.

2.14.17. Maximum Read Turnaround Time (LSB) 0x10

Applicable only when Target is configured with Maximum Data Speed Limitation.

Table 2.23. Maximum Read Turnaround Time (LSB)

Bits	Name	Access	Width	Reset
[7:0]	max_rdturn_b0	read-write	8	0x0

max_rdturn_b0

Maximum Read Turnaround Time in µs.

Least significant byte of 24-bit field that can encode turnaround times from 0.0 seconds to 16 seconds.

2.14.18. Device Provisioned ID Byte6 0x11

Table 2.24 shows the Target Device PID.

Table 2.24. Device Provisioned ID Byte6

Bits	Name	Access	Width	Reset
[7:0]	pid_manuf[14:7]	read-write	8	0x03

pid_manuf[14:7]

Bits 14:7 of 15-bit MIPI Manufacturer ID. Reset value may be configured by user via *Manufacturer ID* attribute.

2.14.19. Device Provisioned ID Byte5 0x12

Table 2.25 shows the Target Device PID.

Table 2.25. Device Provisioned ID Byte5

Bits	Name	Access	Width	Reset
[7:1]	pid_manuf[6:0]	read-write	7	0x1E
[0]	pid_type_sel	read-only	1	0x0 (Fixed)

pid_manuf[6:0]

Bits 6:0 of 15-bit MIPI Manufacturer ID. Reset value may be configured by user via *Manufacturer ID* attribute.

pid_type_sel

Provisioned ID type selector

0 – Vendor Fixed Value

1 – Random value generated by device. (Not supported in this IP)

2.14.20. Device Provisioned ID Byte4 0x13

Table 2.26 shows the Target Device PID.

Table 2.26. Device Provisioned ID Byte4

Bits	Name	Access	Width	Reset
[7:0]	pid_part[15:8]	read-write	8	0x0

pid_part[15:8]

Bits 15:8 of 16-bit Part ID when pid_type_sel is 0. The meaning of this 16-bit field is left to the Device vendor to define. Reset value may be configured by user via *Part ID* attribute.

2.14.21. Device Provisioned ID Byte3 0x14

Table 2.27 shows the Target Device PID.

Table 2.27. Device Provisioned ID Byte3

Bits	Name	Access	Width	Reset
[7:0]	pid_part[7:0]	read-write	8	0x1

pid_part[7:0]

Bits 7:0 of 16-bit Part ID when pid_type_sel is 0. The meaning of this 16-bit field is left to the Device vendor to define. Reset value may be configured by user via *Part ID* attribute.

2.14.22. Device Provisioned ID Byte2 0x15

Table 2.28 shows the Target Device PID.

Table 2.28. Device Provisioned ID Byte2

Bits	Name	Access	Width	Reset
[7:4]	pid_inst	read-write	4	0x1
[3:0]	pid_add[11:8]	read-write	4	0x0

pid_inst

Instance ID field that should identify the individual Device, using a method selected by the system designer (e.g., straps, fuses, non-volatile memory, or another appropriate method). Reset value may be configured by user via *Instance ID* attribute.

pid_add[11:8]

Bits 11:8 of 12-bit Additional ID for definitions with additional meaning (e.g., Deeper device characteristics that may optionally include Device Characteristics Register values). Reset value may be configured by user via *Additional ID* attribute.

2.14.23. Device Provisioned ID Byte1 0x16

Table 2.29 shows the Target Device PID.

Table 2.29. Device Provisioned ID Byte1

Bits	Name	Access	Width	Reset
[7:0]	pid_add[7:0]	read-write	8	0x0

pid_add[7:0]

Bits 7:0 of 12-bit Additional ID for definitions with additional meaning (e.g., Deeper device characteristics that may optionally include Device Characteristics Register values). Reset value may be configured by user via *Additional ID* attribute.

2.14.24. Static Address 0x17

Applicable only when *Static Address Enabled* attribute is checked.

Table 2.30. Static Address

Bits	Name	Access	Width	Reset
[7]	*reserved*	read-only	1	0x0
[6:0]	stat_addr	read-write	7	0x8

stat_addr

Target Static Address assigned by user. Reset value may be configured by user via *Static Address* attribute. If static address is disabled, reset value is 0.

2.14.25. Device Capabilities Byte1 0x18

Device capabilities that Target returns when Controller sends GETCAPS CCC.

Table 2.31. Device Capabilities Byte1

Bits	Name	Access	Width	Reset
[7:4]	*reserved*	read-only	4	0x0
[3]	hdr_bt_mode	read-only	1	0x0 (Fixed)
[2]	hdr_tsl_mode	read-only	1	0x0 (Fixed)
[1]	hdr_tsp_mode	read-only	1	0x0 (Fixed)
[0]	hdr_ddr_mode	read-only	1	0x0 – SDR mode only. 0x1 – SDR and HDR-DDR mode is supported.

hdr_bt_mode

Fixed to 0. HDR-BT mode is not supported.

hdr_tsl_mode

Fixed to 0. HDR-BT mode is not supported.

hdr_tsp_mode

Fixed to 0. HDR-BT mode is not supported.

hdr_ddr_mode

Set to 1 when device is configured with HDR capability. Only HDR-DDR mode is supported.

2.14.26. Device Capabilities Byte2 0x19

Device capabilities that Target returns when Controller sends GETCAPS CCC.

Table 2.32. Device Capabilities Byte2

Bits	Name	Access	Width	Reset
[7]	hdr_ddr_abort_crc_caps	read-only	1	0x0 – If only SDR capable 0x1 – if HDR DDR capable
[6]	hdr_ddr_wr_abort_caps	read-only	1	0x0 – If only SDR capable 0x1 – if HDR DDR capable
[5:4]	grp_adr_caps	read-only	2	0x0 (Fixed)
[3:0]	i3c_spec_ver	read-only	4	0x1 (Fixed)

hdr_ddr_abort_crc_caps

I3C Target capability of emitting the CRC Word when a transaction in HDR-DDR Mode is aborted.

Set to 1 when device is configured with HDR capability.

0: No

1: Yes

hdr_ddr_wr_abort_caps

I3C Target capability of issuing the Write Abort in HDR-DDR Mode.

Set to 1 when device is configured with HDR capability.

0: No

1: Yes

grp_adr_caps

Indicates the Group Address function capabilities of this I3C Device. Fixed to 0.

0 – Does not support Group Address function.

1 – Can be assigned one Group Address (Not supported in this IP).

2 – Can be assigned two Group Addresses (Not supported in this IP).

3 – Can be assigned three or more Group Addresses (Not supported in this IP).

i3c_spec_ver

Indicates the minor version number of the MIPI I3C Specification with which this I3C v1.x Device complies (i.e., the 'x' in "I3C v1.x"). Setting to 0x0 is illegal.

2.14.27. Device Capabilities Byte3 0x1A

Device capabilities that Target returns when Controller sends GETCAPS CCC.

Table 2.33. Device Capabilities Byte3

Bits	Name	Access	Width	Reset
[7]	*reserved*	read-only	1	0x0
[6]	pend_rd_mdb	read-only	1	0x0
[5]	hdr_bt_crc32	read-only	1	0x0 (Fixed)
[4]	getstatus_defbyte	read-only	1	0x0 (Fixed)
[3]	getcaps_defbyte	read-only	1	0x0 (Fixed)
[2]	d2dxfer_ibi	read-only	1	0x0 (Fixed)
[1]	d2dxfer	read-only	1	0x0 (Fixed)
[0]	ml_data_xfer	read-only	1	0x0 (Fixed)

pend_rd_mdb

I3C Target support for IBI with Pending Read Notification MDB, which the Controller shall then follow with a Private Read request to fetch the data.

Set to 1 when device is configured with IBI with MDB capability.

0 – No

1 – Yes

hdr_bt_crc32

I3C Target support CRC-32 data integrity verification in HDR Bulk Transport Mode.

0 – No

1 – Yes (Not supported in this IP)

getstatus_defbyte

I3C Target support for defining byte in GETSTATUS CCC.

0 – No

1 – Yes (Not supported in this IP)

getcaps_defbyte

I3C Target support for defining byte in GETCAPS CCC.

0 – No

1 – Yes (Not supported in this IP)

d2dxfer_ibi

I3C Target capability to initiate Device to Device (D2D) Transfer using IBI with MDB 0x37.

0 – No

1 – Yes (Not supported in this IP)

d2dxfer

I3C Target support for D2D transfers either as a Source or a Subscriber/Receiver.

0 – No

1 – Yes (Not supported in this IP)

ml_data_xfer

I3C Target support for multi-Lane data transfer.

0 – No

1 – Yes (Not supported in this IP)

2.14.28. Oscillator Inaccuracy 0x1C

Table 2.34 shows the inaccuracy of Target's internal oscillator.

Table 2.34. Oscillator Inaccuracy

Bits	Name	Access	Width	Reset
[7:0]	osc_inaccuracy	read-write	8	0x0

osc_inaccuracy

Describes the maximum variation of the Target's internal oscillator in 1/10th percent (0.1%) increments, up to 25.5%.

Example: A value of 8'd25 represents a maximum frequency variation of 2.5%.

2.14.29. Receive FIFO 0x20

Table 2.35 shows the Receive FIFO.

Table 2.35. Receive FIFO

Bits	Name	Access	Width	Reset
[7:0]	rx_fifo	read-only	8	0x0

rx_fifo

Data bytes received from I3C bus are stored in this FIFO. User can get the received data by reading from this address multiple times depending on the number of data bytes to be read. User can read rxfifo_not_empty interrupt status register (Interrupt Status 2 Bit 6) first to determine if there is data to be read from rx_fifo.

2.14.30. Transmit FIFO 0x22

Table 2.36 shows the Transmit FIFO.

Table 2.36. Transmit FIFO

Bits	Name	Access	Width	Reset
[7:0]	tx_fifo	read-write	8	0x0

tx_fifo

Data to be sent to I3C bus is stored in this FIFO. User can do multiple writes to this address depending on the number of data bytes to be written. Reading from this address will indicate *txfifo_empty* status (0x1 – Empty, 0x0 – Not Empty).

2.14.31. Soft Reset 0x28

Table 2.37 shows the Soft Reset.

Table 2.37. Soft Reset

Bits	Name	Access	Width	Reset
[7:5]	*reserved*	read-only	3	0x0
[4]	ip_csr_rst	read-write	1	0x0
[3]	ip_core_rst	read-write	1	0x0
[2]	tx_fifo_rst	read-write	1	0x0
[1]	rx_fifo_rst	read-write	1	0x0
[0]	ip_main_rst	read-write	1	0x0

ip_csr_rst

When set to high, resets the IP read-write and write-only registers only. Auto clear.

ip_core_rst

When set to high, resets the internal state of I3C Core only (including Tx and Rx FIFO). Dynamic address and configurations via CCCs are not reset.
Auto clear.

tx_fifo_rst

When set to high, resets the Tx FIFO only. Auto clear.

rx_fifo_rst

When set to high, resets the Rx FIFO only. Auto clear.

ip_main_rst

When set to high, resets the whole IP including registers, FIFO, dynamic address, and CCC configurations. Auto clear.

2.14.32. Target Response 0x29

Table 2.38 shows the Target Response.

Table 2.38. Target Response

Bits	Name	Access	Width	Reset
[7:5]	*reserved*	read-only	3	0x0
[4]	fifo_loopback_en	read-write	1	0x0
[3:1]	*reserved*	read-only	3	0x0
[0]	txfifo_empty_rd_nak	read-write	1	0x0

fifo_loopback_en

0 – Data written through Private Write will be read from Rx FIFO. Data written to Tx FIFO will be read through Private Read.

1 – Data written through Private Write will be stored in Rx FIFO and transferred to Tx FIFO to be read through Private Read. Data written to the Tx FIFO by the user can still be read through Private Read.

txfifo_empty_rd_nak

Target response when Controller reads but Tx FIFO is empty.

0 – In SDR mode, Target will ACK its Address and return 0xFF read data then End-of-Message by pulling SDA Low at T-bit. If I3C bus is in HDR mode and Target is configured with HDR capability, Target will ACK its address and return 0x0 data then end Read.

1 – Target will NACK its Address

2.14.33. Get Status MSB 0x2A

Most significant byte that Target returns when Controller sends GETSTATUS CCC.

Table 2.39. Get Status MSB

Bits	Name	Access	Width	Reset
[7:0]	get_status_msb	read-write	8	0x0

get_status_msb

Reserved for vendor-specific meaning.

2.14.34. Get Status LSB 0x2B

Least significant byte that Target returns when Controller sends GETSTATUS CCC.

Table 2.40. Get Status LSB

Bits	Name	Access	Width	Reset
[7:6]	activity_mode	read-write	2	0x0
[5:4]	*reserved*	read-only	2	0x0
[3:0]	pending_interrupt	read-write	4	0x0

activity_mode

Contains the 2-bit ID of the Target Device's current activity mode. For Target devices without secondary controller capability, the meaning of this value will depend upon a private contract between the Target and the Controller.

pending_interrupt

Contains the interrupt number of any pending interrupt, or 0 if no interrupts are pending.

2.14.35. Bus Activity State 0x2C

Table 2.41 shows the Bus Activity State.

Table 2.41. Bus Activity State

Bits	Name	Access	Width	Reset
[7:2]	*reserved*	read-only	6	0x0
[1:0]	bus_act	read-only	2	0x0

bus_act

When bus_act_rcvd is set to 1, this register indicates the activity state received. Write 1 to clear.

0 –1 µs (Latency-free operation)

1 – 100 µs

2 – 2ms

3 – 50ms (Lowest-activity operation)

2.14.36. Target Reset Action 1 0x2D

Table 2.42 shows the Target Reset Action Information 1.

Table 2.42. Target Reset Action 1

Bits	Name	Access	Width	Reset
[7:0]	rst_act	read-only	8	0x0

rst_act

Target Reset Action configured by the Controller via Defining Byte of RSTACT CCC. When Target Reset Pattern is received after RSTACT CCC, user shall perform the configured reset action.

2.14.37. Target Reset Action 2 0x2E

Table 2.43 shows the Target Reset Action Information 2.

Table 2.43. Target Reset Action 2

Bits	Name	Access	Width	Reset
[7:2]	*reserved*	read-only	6	0x0
[1]	rst_act_set0_get1	read-only	1	0x0
[0]	rst_act_broad0_dir1	read-only	1	0x0

rst_act_set0_get1

Information on the Target Rese Action configured by Controller.

0 – Controller configured Target Reset Action by Direct SET RSTACT CCC

1 – Controller configured Target Reset Action by Direct GET RSTACT CCC

rst_act_broad0_dir1

Information on the Target Rese Action configured by Controller.

0 – Controller configured Target Reset Action by Broadcast RSTACT CCC

1 – Controller configured Target Reset Action by Direct Set/Get RSTACT CCC

2.14.38. Target Reset Action 3 0x2F

Table 2.44 shows the Target Reset Action Information 3

Table 2.44. Target Reset Action 3

Bits	Name	Access	Width	Reset
[7:0]	rst_act_set	read-only	8	0x80

rst_act_set

Target Reset Action configured by the Controller via Defining Byte of Direct SET RSTACT CCC. This is the value returned by Target when Controller sends Direct GET CCC.

2.14.39. Interrupt Status 1 0x30

Table 2.45 shows the Interrupt Status Information 1.

Table 2.45. Interrupt Status 1

Bits	Name	Access	Width	Reset
[7]	hj_req_gen	read-write	1	0x0
[6]	hj_done	read-write	1	0x0
[5]	hj_acknack	read-write	1	0x0
[4]	*reserved*	read-write	1	0x0
[3]	ibi_req_gen	read-write	1	0x0
[2]	ibi_done	read-write	1	0x0
[1]	ibi_acknack	read-write	1	0x0
[0]	ibi_payld_terminated	read-write	1	0x0

hj_req_gen

When set to 1, Hot-Join request is generated by Target. Write 1 to clear.

hj_done

When set to 1, Hot-Join address with Write bit is transmitted by Target and Controller has either ACKed or NACKed for HJ_IBI_RETRY times. Write 1 to clear.

hj_acknack

When set to 1, Hot-Join is NACKed by Controller after HJ_IBI_RETRY times. Write 1 to clear.

ibi_req_gen

When set to 1, IBI request is generated by Target. Write 1 to clear.

ibi_done

When set to 1, Target Address with Read bit has been transmitted by Target and Controller has either ACKED or NACKed the request for HJ_IBI_RETRY times. If with payload, IBI payload has been transmitted and finished either by End-of-Data (from Target) or STOP (from Controller). Write 1 to clear.

ibi_acknack

When set to 1, IBI is NACKed by Controller after HJ_IBI_RETRY times. Write 1 to clear.

ibi_payld_terminated

When set to 1, Controller aborted reading complete IBI payload. Write 1 to clear.

2.14.40. Interrupt Status 1 Enable 0x31

When set to 1, corresponding interrupt is enabled.

Table 2.46. Interrupt Status 1 Enable

Bits	Name	Access	Width	Reset
[7]	hj_req_gen_en	read-write	1	0x0
[6]	hj_done_en	read-write	1	0x0
[5]	hj_acknack_en	read-write	1	0x0
[4]	*reserved*	read-write	1	0x0
[3]	ibi_req_gen_en	read-write	1	0x0
[2]	ibi_done_en	read-write	1	0x0
[1]	ibi_acknack_en	read-write	1	0x0
[0]	ibi_payld_terminated_en	read-write	1	0x0

2.14.41. Interrupt Status 1 Set 0x32

Manually set corresponding interrupt to 1.

Table 2.47. Interrupt Status 1 Set

Bits	Name	Access	Width	Reset
[7]	hj_req_gen_set	write-only	1	0x0
[6]	hj_done_set	write-only	1	0x0
[5]	hj_acknack_set	write-only	1	0x0
[4]	*reserved*	read-only	1	0x0
[3]	ibi_req_gen_set	write-only	1	0x0
[2]	ibi_done_set	write-only	1	0x0
[1]	ibi_acknack_set	write-only	1	0x0
[0]	ibi_payld_terminated_set	write-only	1	0x0

2.14.42. Interrupt Status 2 0x33

Table 2.48 shows the Interrupt Status 2.

Table 2.48. Interrupt Status 2

Bits	Name	Access	Width	Reset
[7]	txfifo_full	read-write	1	0x0
[6]	rxfifo_not_empty	read-write	1	0x0
[5]	txfifo_full	read-write	1	0x0
[4]	*reserved*	read-only	1	0x0
[3]	read_txfifo_empty	read-write	1	0x0
[2]	read_aborted	read-write	1	0x0
[1]	da_par_err	read-write	1	0x0
[0]	tbit_err	read-write	1	0x0

txfifo_full

When set to 1, it indicates Tx FIFO is full. Write 1 to clear.

rxfifo_not_empty

When set to 1, it indicates that Rx FIFO is not empty. Write 1 to clear.

rxfifo_full

When set to 1, it indicates Rx FIFO is full. Write 1 to clear.

read_txfifo_empty

When set to 1, Controller initiated Read but Tx FIFO is empty. Write 1 to clear.

read_aborted

When set to 1, Read is aborted early by Controller. Write 1 to clear.

da_par_err

When set to 1, parity bit error in dynamic address assignment occurred. Write 1 to clear.

tbit_err

When set to 1, data T-bit Error occurred. Write 1 to clear.

2.14.43. Interrupt Status 2 Enable 0x34

When set to 1, corresponding interrupt is enabled.

Table 2.49. Interrupt Status 2 Enable

Bits	Name	Access	Width	Reset
[7]	txfifo_full_en	read-write	1	0x0
[6]	rxfifo_not_empty_en	read-write	1	0x0
[5]	rxfifo_full_en	read-write	1	0x0
[4]	*reserved*	read-only	1	0x0
[3]	read_txfifo_empty_en	read-write	1	0x0
[2]	read_aborted_en	read-write	1	0x0
[1]	da_par_err_en	read-write	1	0x0
[0]	tbit_err_en	read-write	1	0x0

2.14.44. Interrupt Status 2 Set 0x35

Manually set corresponding interrupt to 1.

Table 2.50. Interrupt Status 2 Set

Bits	Name	Access	Width	Reset
[7]	txfifo_full_set	write-only	1	0x0
[6]	rxfifo_not_empty_set	write-only	1	0x0
[5]	rxfifo_full_set	write-only	1	0x0
[4]	*reserved*	read-only	1	0x0
[3]	read_txfifo_empty_set	write-only	1	0x0
[2]	read_aborted_set	write-only	1	0x0
[1]	da_par_err_set	write-only	1	0x0
[0]	tbit_err_set	write-only	1	0x0

2.14.45. Interrupt Status 3 0x36

Table 2.51 shows the Interrupt Status 3.

Table 2.51. Interrupt Status 3

Bits	Name	Access	Width	Reset
[7]	enec_rcvd	read-write	1	0x0
[6]	tgt_rst_ptrn_rcvd	read-write	1	0x0
[5]	rstact_ccc_rcvd	read-write	1	0x0
[4]	bus_act_rcvd	read-write	1	0x0
[3]	setxtime_rcvd	read-write	1	0x0
[2]	*reserved*	read-only	1	0x0
[1]	bus_aval	read-write	1	0x0
[0]	bus_idle	read-write	1	0x0

enec_rcvd

When set to 1, Target received Broadcast/Direct ENEC/DISEC CCC from Controller. Write 1 to clear.

tgt_rst_ptrn_rcvd

When set to 1, Target received Target Reset Pattern from Controller. Write 1 to clear.

rstact_ccc_rcvd

When set to 1, Target received RSTACT CCC from Controller. Write 1 to clear.

bus_act_rcvd

When set to 1, Target received ENTASx CCC from Controller Write 1 to clear.

setxtime_rcvd

When set to 1, Target received SETXTIME with supported sub-command byte from Controller. Write 1 to clear.

bus_aval

When set to 1, I3C bus is in Bus Available condition. Write 1 to clear.

bus_idle

When set to 1, I3C bus is in Bus Idle condition. Write 1 to clear.

2.14.46. Interrupt Status 3 Enable 0x37

When set to 1, corresponding interrupt is enabled.

Table 2.52. Interrupt Status 3 Enable

Bits	Name	Access	Width	Reset
[7]	enec_rcvd_en	read-write	1	0x0
[6]	tgt_rst_ptrn_rcvd_en	read-write	1	0x0
[5]	rstact_ccc_rcvd_en	read-write	1	0x0
[4]	bus_act_rcvd_en	read-write	1	0x0
[3]	setxtime_rcvd_en	read-write	1	0x0
[2]	*reserved*	read-only	1	0x0
[1]	bus_aval_en	read-write	1	0x0
[0]	bus_idle_en	read-write	1	0x0

2.14.47. Interrupt Status 3 Set 0x38

Manually set corresponding interrupt to 1.

Table 2.53. Interrupt Status 3 Set

Bits	Name	Access	Width	Reset
[7]	enec_rcvd_set	write-only	1	0x0
[6]	tgt_rst_ptrn_rcvd_set	write-only	1	0x0
[5]	rstact_ccc_rcvd_set	write-only	1	0x0
[4]	bus_act_rcvd_set	write-only	1	0x0
[3]	setxtime_rcvd	write-only	1	0x0
[2]	*reserved*	read-only	1	0x0
[1]	bus_aval_set	write-only	1	0x0
[0]	bus_idle_set	write-only	1	0x0

2.14.48. Interrupt Status 5 0x3C

Table 2.54 shows Interrupt Status 5.

Table 2.54. Interrupt Status 5

Bits	Name	Access	Width	Reset
[7:4]	*reserved*	read-only	4	0x0
[3]	hdr_ddr_frm_err	read-write	1	0x0
[3]	hdr_ddr_par_err	read-write	1	0x0
[3]	hdr_ddr_crc_err	read-write	1	0x0
[3]	hdr_ddr_mon_err	read-write	1	0x0

hdr_ddr_frm_err

When set to 1, HDR-DDR framing error is detected. Write 1 to clear.

hdr_ddr_par_err

When set to 1, HDR-DDR parity error is detected. Write 1 to clear.

hdr_ddr_crc_err

When seet to 1, HDR-DDR CRC error is detected. Write 1 to clear.

hdr_ddr_mon_err

When set to 1, data transferred on the I3C bus is different from what Target intended to send. Write 1 to clear.

2.14.49. Interrupt Status 5 Enable 0x3D

When set to 1, corresponding interrupt is enabled.

Table 2.55. Interrupt Status 5 Enable

Bits	Name	Access	Width	Reset
[7:4]	*reserved*	read-only	4	0x0
[3]	hdr_ddr_frm_err_en	read-write	1	0x0
[3]	hdr_ddr_par_err_en	read-write	1	0x0
[3]	hdr_ddr_crc_err_en	read-write	1	0x0
[3]	hdr_ddr_mon_err_en	read-write	1	0x0

2.14.50. Interrupt Status 5 Set 0x3E

Manually set corresponding interrupt to 1.

Table 2.56. Interrupt Status 5 Set

Bits	Name	Access	Width	Reset
[7:4]	*reserved*	read-only	4	0x0
[3]	hdr_ddr_frm_err_set	write-only	1	0x0
[3]	hdr_ddr_par_err_set	write-only	1	0x0
[3]	hdr_ddr_crc_err_set	write-only	1	0x0
[3]	hdr_ddr_mon_err_set	write-only	1	0x0

2.14.51. Bus Mode 0x50

Table 2.57 shows the I3C Bus Mode.

Table 2.57. I3C Bus Mode

Bits	Name	Access	Width	Reset
[7:1]	*reserved*	read-only	7	0x0
[0]	bus_hdr_mode	read-only	1	0x0

bus_hdr_mode

When equal to High, I3C Bus is in HDR mode.

2.14.52. HDR-DDR Target Configuration 0x51

Table 2.58 shows the HDR-DDR Target Configuration for received HDR data.

Table 2.58. HDR-DDR Target Configuration

Bits	Name	Access	Width	Reset
[7:2]	*reserved*	read-only	4	0x0
[1]	hdr_ddr_wr_cmd_to_fifo	read-write	1	0x0
[0]	hdr_ddr_rd_cmd_to_fifo	read-write	1	0x0

hdr_ddr_wr_cmd_to_fifo

Applicable only when Target is configured with HDR capability.

When set to High, HDR-DDR Write Command is stored to Rx FIFO.

hdr_ddr_rd_cmd_to_fifo

Applicable only when Target is configured with HDR capability.

When set to High, HDR-DDR Read Command is stored to Rx FIFO.

2.14.53. HDR-DDR Abort Configuration 0x54

HDR-DDR Abort Configuration set by Controller via ENDXFER CCC.

Table 2.59. HDR-DDR Abort Configuration

Bits	Name	Access	Width	Reset
[7:6]	hdr_ddr_abort_crc	read-only	1	0x1
[5]	hdr_ddr_write_abort	read-only	1	0x0
[4]	hdr_ddr_write_nack	read-only	1	0x0
[3:0]	*reserved*	read-only	4	0x0

hdr_ddr_abort_crc

Applicable only when Target is configured with HDR capability.

2'b11 - No CRC Word follows Early Termination request

2'b01 - CRC Word follows Early Termination request

Other - reserved for future definition by MIPI alliance.

When set to High, Target can emit the CRC Word when a transaction in HDR-DDR Mode is aborted.

hdr_ddr_write_abort

Applicable only when Target is configured with HDR capability.

When set to Low, Target can issue the Write Abort in HDR-DDR Mode.

This IP will issue Write Abort in HDR-DDR Mode if the Rx FIFO is full.

hdr_ddr_write_nack

Applicable only when Target is configured with HDR capability.

When set to Low, Target can issue a NACK to an HDR-DDR Write Command.

This IP will issue NACK an HDR-DDR Write Command if the Rx FIFO is full.

2.14.54. Secondary Controller Registers

I3C Target registers are accessible when I3C Controller IP is configured with Secondary-Controller Capability. The address space of I3C Target is moved when Secondary Controller is supported. When the device is configured as Target-only, MSB of address space is 0. When the device is used for Secondary Controller support, MSB of address space is 1.

Example: 0x00 (Target-only) → 0x80 (Secondary-Controller support)

0x01 (Target-only) → 0x81 (Secondary Controller Support)

The following section describes I3C Target registers that have changes in reset value and/or definition when used for Secondary Controller. Registers not included in this section retain the definitions as when device is configured as I3C Target-only.

2.14.54.1. Dynamic Address 0x02

Table 2.60 shows the assigned dynamic address and done flag.

Table 2.60. Dynamic Address

Bits	Name	Access	Width	Reset
[7]	daa_done	read-only	1	0x1 – If Target is Secondary-Controller Capable 0x0 – If Target is not Secondary-Controller Capable
[6:0]	dyn_addr	read-only	7	Takes Dynamic Address parameter value

daa_done

0 – dyn_addr is not yet assigned or is reset by RSTDAA CCC.

1 – dyn_addr is assigned via ENTDAA, SETNEWDA, SETAASA or SETDASA CCC.

This is set to 1 if Target is configured with Secondary Controller capability.

dyn_addr

Dynamic Address Assigned to I3C Target.

If Target is configured with Secondary Controller capability and IP is set to be the Primary Controller, this register indicates the Dynamic Address that Controller will use when sending DEFTGTS CCC.

2.14.54.2. Bus Characteristics Register 0x00

Table 2.61 shows the Target Bus Characteristics Register.

Table 2.61. Bus Characteristics Register

Bits	Name	Access	Width	Reset
[7:6]	device_role	read-only	2	0x0 – Device is Target-only 0x1 – Device is Controller-Capable
[5]	advanced_caps	read-only	1	0x1 (Fixed)
[4]	virtual_tgt_support	read-only	1	0x0 (Fixed)
[3]	offline_capable	read-only	1	0x0 (Fixed)
[2]	ibi_payload	read-only	1	0x1
[1]	ibi_capable	read-only	1	0x1
[0]	max_d_speed_limit	read-only	1	0x0

device_role

2'b00 – I3C Target.

2'b01 – I3C Controller-capable.

Others - Reserved for future definition by MIPI Alliance I3C WG (Not supported in this IP).

advanced_caps

Fixed to 1 when device is configured with Secondary-Controller capability.

0 – Does not support optional advanced capabilities.

1 – Supports optional advanced capabilities. When Target is configured with IBI capability and IBI payload, this is set to 1 for optional Pending Read MDB support.

virtual_tgt_support

Fixed to 0.

0 – Is not a Virtual Target and does not expose other downstream Device(s).

1 – Is a Virtual Target or exposes other downstream Device(s) (Not supported in this IP).

offline_capable

Fixed to 0.

0 – Device will always respond to I3C Bus commands.

1 – Device will not always respond to I3C Bus Commands (Not supported in this IP).

ibi_payload

From *IBI Payload Size* attribute.

0 – If *IBI Payload Size* attribute is set to 0. No data bytes follow the IBI.

1 – If *IBI Payload Size* attribute is set to greater than or equal to 1. One data byte (MDB) shall follow the accepted IBI, and additional data bytes may follow.

ibi_capable

From *IBI Capable* attribute.

0 – Unchecked. Not capable.

1 – Checked. Capable.

max_d_speed_limit

From *Maximum Data Speed Limitation* attribute.

0 – Unchecked. No limitation.

1 – Checked. With limitation. Controller shall use GETMXDS CCC to get specific limitation from Target.

2.14.54.3. Events Command Enable 0x03

Hot-Join and IBI enable from Controller via ENEC/DISEC CCC.

Table 2.62. Events Command Enable

Bits	Name	Access	Width	Reset
[7:4]	*reserved*	read-only	4	0x0
[3]	hj_enec	read-only	1	0x1 – If Target is Hot-Join capable 0x0 – If Target is not Hot-Join capable
[2]	*reserved*	read-only	1	0x0
[1]	cr_enec	read-only	1	0x1
[0]	ibi_enec	read-only	1	0x1 – If Target is IBI capable 0x0 – If Target is not IBI capable

hj_enec

Hot-Join Enable by Controller.

0 – Target-initiated Hot-Join is not allowed on the I3C bus.

1 – Target-initiated Hot-Join is allowed on the I3C bus.

cr_enec

Controller Role Request Enable by Controller.

0 – Target-initiated Controller Role request is not allowed on the I3C bus.

1 – Target-initiated Controller Role request is allowed on the I3C bus.

ibi_enec

IBI Enable by Controller..

0 – Target-initiated interrupts are not allowed on the I3C bus.

1 – Target-initiated interrupts are allowed on the I3C bus.

*Reset value is 1 if Target is configured with IBI capability, 0 otherwise.

2.14.54.4. Events Command Device Configuration 0x04

Hot-Join and IBI capability configured by user using attributes.

Table 2.63. Events Command Device Configuration

Bits	Name	Access	Width	Reset
[7:4]	*reserved*	read-only	4	0x0
[3]	hj_cap	read-only	1	0x1 – If Target is Hot-Join capable 0x0 – If Target is not Hot-Join capable
[2]	*reserved*	read-only	1	0x0
[1]	cr_cap	read-only	1	0x1 – If Target is Secondary Controller capable 0x0 – If Target is not Secondary Controller capable

[0]	ibi_cap	read-only	1	0x1 – If Target is IBI capable 0x0 – If Target is not IBI capable

hj_cap

0 – Target device is configured without Hot-Join Capability

1 – Target device is configured with Hot-Join Capability

cr_cap

0 – Target device is configured without Secondary-Controller Capability

1 – Target device is configured with Secondary-Controller Capability

ibi_cap

0 – Target device is configured without IBI Capability

1 – Target device is configured with IBI Capability

2.14.54.5. Events Command Request 0x05

Hot-Join and IBI capability configured by user using attributes.

Table 2.64. Events Command Request

Bits	Name	Access	Width	Reset
[7:4]	*reserved*	read-only	4	0x0
[3]	hj_req	read-write	1	0x0
[2]	*reserved*	read-only	1	0x0
[1]	cr_req	read-write	1	0x0
[0]	ibi_req	read-write	1	0x0

hj_req

When set to High, Target will initiate Hot-Join request at the next valid opportunity. Reset to 0 when Hot-Join is done or disabled by the Controller.

cr_req

When set to High, Target will initiate Controller Role request at the next valid opportunity. Reset to 0 when Controller Role request is done or disabled by the Controller.

ibi_req

When set to High, Target will initiate IBI at the next valid opportunity. Reset to 0 when IBI is done or disabled by the Controller.

2.14.54.6. Maximum Write Data Speed (MaxWr) 0x0C

Applicable only when Target is configured with Maximum Data Speed Limitation.

Table 2.65. Maximum Write Data Speed (MaxWr)

Bits	Name	Access	Width	Reset
[7:4]	*reserved*	read-only	4	0x0
[3]	mxds2_w_defbyte	read-only	1	0x1 (Fixed)
[2:0]	mxds2_w_rate	read-write	3	0x0

mxds2_w_defbyte

Fixed to 1 when device is configured with Secondary-Controller capability.

0 – Target does not support defining byte for GETMXDS CCC.

1 – Target supports defining byte for GETMXDS CCC.

mxds2_w_rate

Maximum Sustained Data Rate for non-CCC Messages sent by Controller Device to Target Device.

0 – fSCL Max (default value)

1 – 8 MHz

2 – 6 MHz

3 – 4 MHz

4 – 2 MHz

Others –Reserved for future use by MIPI Alliance

2.14.54.7. Device Capabilities Byte 3 0x1A

Device capabilities that Target returns when Controller sends GETCAPS CCC.

Table 2.66. Device Capabilities Byte3

Bits	Name	Access	Width	Reset
[7]	*reserved*	read-only	1	0x0
[6]	pend_rd_mdb	read-only	1	0x0
[5]	hdr_bt_crc32	read-only	1	0x0 (Fixed)
[4]	getstatus_defbyte	read-only	1	0x1 (Fixed)
[3]	getcaps_defbyte	read-only	1	0x1 (Fixed)
[2]	d2dxfer_ibi	read-only	1	0x1 (Fixed)
[1]	d2dxfer	read-only	1	0x0 (Fixed)
[0]	ml_data_xfer	read-only	1	0x0 (Fixed)

pend_rd_mdb

I3C Target support for IBI with Pending Read Notification MDB, which the Controller shall then follow with a Private Read request to fetch the data.

Set to 1 when device is configured with IBI with MDB capability.

0 – No

1 – Yes

hdr_bt_crc32

I3C Target support CRC-32 data integrity verification in HDR Bulk Transport Mode.

0 – No

1 – Yes (Not supported in this IP)

getstatus_defbyte

I3C Target support for defining byte in GETSTATUS CCC. Set to 1 when Secondary-Controller Capable.

0 – No

1 – Yes

getcaps_defbyte

I3C Target support for defining byte in GETCAPS CCC. Set to 1 when Secondary-Controller Capable.

0 – No

1 – Yes

d2dxfer_ibi

I3C Target capability to initiate Device to Device (D2D) Transfer using IBI with MDB 0x37.

0 – No

1 – Yes (Not supported in this IP)

d2dxfer

I3C Target support for D2D transfers either as a Source or a Subscriber/Receiver.

0 – No

1 – Yes (Not supported in this IP)

ml_data_xfer

I3C Target support for Multi-Lane data transfer.

0 – No

1 – Yes (Not supported in this IP)

2.14.54.8. Interrupt Status 4 0x39

Table 2.67 shows the Interrupt Status 4.

Table 2.67. Interrupt Status 4

Bits	Name	Access	Width	Reset
[7]	get_acccr_rcvd	read-write	1	0x0
[6]	get_acccr_acknak	read-write	1	0x0
[5]	deftgts_rcvd	read-write	1	0x0
[4]	*reserved*	read-only	1	0x0
[3]	cr_req_gen	read-write	1	0x0
[2]	cr_req_done	read-write	1	0x0
[1]	cr_req_acknack	read-write	1	0x0
[0]	device_role_changed	read-write	1	0x0

get_acccr_rcvd

When set to 1, Target received GET_ACCCR CCC from Controller. Write 1 to clear.

get_acccr_acknak

When set to 1, Target NACKed GET_ACCCR CCC received from Controller. Write 1 to clear.

deftgts_rcvd

When set to 1, Target received DEFTGTS CCC from Controller (including data bytes describing each device in the bus). Write 1 to clear.

cr_req_gen

When set to 1, Controller Role request is generated by Target. Write 1 to clear.

cr_req_done

When set to 1, Target Address with Write bit has been transmitted by Target and Controller has either ACKed or NACKed the request for HJ_IBI_RETRY times. Write 1 to clear.

cr_req_acknak

When set to 1, Controller Role request is NACKed by Controller after HJ_IBI_RETRY times. Write 1 to clear.

device_role_changed

When set to 1, device role is changed either from Controller to Target or Target to Controller. Read the actual role from the device_role register. Write 1 to clear.

When device_role_changed interrupt is asserted and device_role is 1'b0, IP has successfully sent GETACCCR CCC and Controller Role will be transferred to the New Controller. IP will then monitor if the New Controller has asserted its role. If the New Controller did not assert its role, Controller Role Handoff will be cancelled and device_role will be set to 1'b1 again.

When device_role_changed interrupt is asserted and device_role is 1'b1, IP has successfully received GETACCCR CCC and Controller Role will be transferred to the IP. IP will then assert its role as Controller depending on the auto_assert_role register in I3C Controller IP.

2.14.54.9. Interrupt Status 4 Enable 0x3A

When set to 1, corresponding Interrupt is enabled.

Table 2.68. Interrupt Status 4 Enable

Bits	Name	Access	Width	Reset
[7]	get_acccr_rcvd_en	read-write	1	0x0
[6]	get_acccr_acknak_en	read-write	1	0x0
[5]	deftgts_rcvd_en	read-write	1	0x0
[4]	*reserved*	read-only	1	0x0
[3]	cr_req_gen_en	read-write	1	0x0
[2]	cr_req_done_en	read-write	1	0x0
[1]	cr_req_acknack_en	read-write	1	0x0
[0]	device_role_changed_en	read-write	1	0x0

2.14.54.10. Interrupt Status 4 Set 0x3B

Manually set corresponding interrupt to 1.

Table 2.69. Interrupt Status 4 Set

Bits	Name	Access	Width	Reset
[7]	get_acccr_rcvd_set	write-only	1	0x0
[6]	get_acccr_acknak_set	write-only	1	0x0
[5]	deftgts_rcvd_set	write-only	1	0x0
[4]	*reserved*	read-only	1	0x0
[3]	cr_req_gen_set	write-only	1	0x0
[2]	cr_req_done_set	write-only	1	0x0
[1]	cr_req_acknack_set	write-only	1	0x0
[0]	device_role_changed_set	write-only	1	0x0

2.14.54.11. DEFTGTS Count 0x40

Count information sent by the Active Controller via DEFTGTS CCC.

Table 2.70. DEFTGTS Count

Bits	Name	Access	Width	Reset
[7:0]	deftgts_count	read-only	8	0x0

deftgts_count

Describes the number of Targets and Groups present in the I3C bus.

2.14.54.12. DEFTGTS Rx FIFO Start 0x41

Pointer for start address of DEFTGTS data in Rx FIFO.

Table 2.71. DEFTGTS Rx FIFO Start

Bits	Name	Access	Width	Reset
[7:0]	rxfifo_deftgts_start	read-only	8	0x0

rxfifo_deftgts_start

Count N indicates the number of times user needs to read from Rx FIFO before DEFTGTS data is read. When equal to 0, next read data is start of DEFTGTS data.

2.14.54.13. DEFTGTS Rx FIFO Count 0x42

Number of DEFTGTS data bytes stored in Rx FIFO.

Table 2.72. DEFTGTS Rx FIFO Count

Bits	Name	Access	Width	Reset
[7:0]	rxfifo_deftgts_count	read-only	8	0x0

rxfifo_deftgts_count

Indicates number of DEFTGTS data bytes stored in Rx FIFO. When reading of DEFTGTS data is started (rxfifo_deftgts_start is equal to 8'h0), this count decreases by one every Rx FIFO read. When 0 count is reached, all DEFTGTS data has been read from Rx FIFO.

2.14.54.14. Controller Role Handoff 0x43

Target configuration for Controller Role Handoff.

Table 2.73. Controller Role Handoff

Bits	Name	Access	Width	Reset
[7]	get_acccr_auto_resp	read-write	1	0x1
[6:1]	*reserved*	read-only	6	0x0
[0]	device_role	read-write	1	0x0

get_acccr_auto_resp

Target auto-response when receiving GETACCCR CCC. Default response is NACK.

0 – Target will ACK the GETACCCR CCC

1 – Target will NACK the GETACCCR CCC

device_role

Current device role. User can write to this register to reset the device role (may be used when the system loses information on the device role).

0 – Device is acting as Target

1 – Device is acting as Controller

2.14.54.15. GETMXDS Controller-Capable Device 0x44

Return value for GETMXDS when defining byte is 0x91.

Table 2.74. GETMXDS Controller-Capable Device

Bits	Name	Access	Width	Reset
[7:3]	*reserved*	read-only	5	0x0
[2]	crh_set_act_state	read-write	1	0x0
[1:0]	crh_act_state	read-write	2	0x0

crh_set_act_state

Indicates whether the Active Controller should set the Bus to a certain Activity State before passing the Controller Role to this device.

0 – Active Controller should not set the bus to any Activity State before passing the Controller Role to this Device

1 – Active Controller should set the bus to the Activity State set in bits 1:0 before passing the Controller Role to this Device

crh_act_state

When crh_set_act_state is set to 1, this indicates whether the device initially acts with a given Activity State after becoming the Active Controller on the Bus. The indicated Activity State implies that the Device may have a delayed response to Bus

activity, and so the former Controller should wait the specified delay time for the indicated Activity State before testing this Device, to confirm that it is controlling the Bus before initiating the CE3 error recovery flow.

0 – Acts according to Activity State 0

1 – Acts according to Activity State 1

2 – Acts according to Activity State 2

3 – Acts according to Activity State 3

2.14.54.16. GETSTATUS Controller-Capable Device LSB 0x45

Return value for GETSTATUS when defining byte is 0x91. MSB of return value is from get_status_msb register at Addr 0x2A.

Table 2.75. GETSTATUS Controller-Capable Device

Bits	Name	Access	Width	Reset
[7:2]	*reserved*	read-only	6	0x0
[1]	handoff_delay_nack	read-write	1	0x0
[0]	deep_sleep_det	read-write	1	0x0

handoff_delay_nack

Indicates whether this Device is currently processing any DEFTGTS CCC Broadcasts that may have been sent by the Active Controller.

0 – The Device is not currently processing Broadcast data and can safely accept the Controller Role.

1 – The Device is currently processing DEFTGTS and may be updating its internal state. Active Controller may wait to send GETACCCR CCC to this Device or should at least be aware that any attempts to send GETACCCR CCC to this Device will be met with a NACK response until this bit is read again later with a value of 1'b0.

deep_sleep_det

Indicates whether the device has entered a deep sleep state in which it may have missed any DEFTGTS CCC sent by the Active controller. Consequently, this device's internal state of known Target devices should be considered outdated.

0 – The device has not entered a deep sleep state.

1 – The device has entered a deep sleep state. The Active Controller shall send another DEFTGTS CCC to update the device's internal state before sending GETACCCR CCC.

2.14.54.17. GETCAPS Controller-Capable Device 1 0x46

Return value for GETCAPS when defining byte is 0x91.

Table 2.76. GETCAPS Controller-Capable Device 1

Bits	Name	Access	Width	Reset
[7:3]	*reserved*	read-only	5	0x0
[2]	multi_lane_support	read-only	1	0x0 (Fixed)
[1]	grp_mgmt_support	read-only	1	0x0 (Fixed)
[0]	hot_join_support	read-only	1	0x1 (Fixed)

multi_lane_support

0 – The device shall not use MLANE CCC to change ML configuration of other I3C Targets.

1 – The device may use the MLANE CCC to change ML configuration of other I3C Targets. (Not supported in this IP)

grp_mgmt_support

0 – The device does not support Group Address capabilities.

1 – The device supports Group Address handoff or management capabilities. (Not supported in this IP)

hot_join_support

0 – The device does not support Hot-Join and will NACK any I3C Target Hot-Join requests. (This setting is not supported in this IP when device is configured with secondary controller capability).

1 – The device may support Hot-Join and will ACK an I3C Target Hot-Join request while it is the Active Controller on the Bus.

2.14.54.18. GETCAPS Controller-Capable Device 2 0x47

Table 2.77 shows the GETCAPS Controller-Capable Device 2.

Table 2.77. GETCAPS Controller-Capable Device 2

Bits	Name	Access	Width	Reset
[7:4]	*reserved*	read-only	6	0x0
[3]	dly_ctrl_handoff	read-only	1	0x1
[2]	deep_sleep_capable	read-write	1	0x0
[1]	ctrl_pass_back	read-write	1	0x0
[0]	ibi_support	read-only	1	0x1 (Fixed)

dly_ctrl_handoff

Tied to get_acccr_auto_resp register.

0 – The device does not need additional time to process Broadcast CCC data from the Active Controller. The Active Controller may expect it to ACK the GETACCCR CCC as part of the Controller Role Handoff procedure even if the device did not initially send a Controller Role Request.

1 – The device may need additional time processing data from the Controller. The Active Controller shall periodically check the value returned by GETSTATUS with 0x91 to determine if the device is ready to accept the Controller Role.

deep_sleep_capable

0 – The device shall remain active and continue to monitor the I3C bus to listen for Broadcast CCCs sent by the Active Controller and shall not enter a deep sleep state from which it must be resynchronized by the Active Controller before it can accept the Controller role.

1 – The device may enter a deep sleep state during which it may miss some Broadcast DEFTGTS sent by the Active Controller. This will require resynchronization upon re-entering a normal operating state before it can accept the Controller Role.

ctrl_pass_back

0 – The device shall not automatically pass the Controller Role back to the former Active Controller and shall support a Controller Role request from any Controller-capable device.

1 – The device shall automatically pass the Controller Role back to the former Active Controller from which it received its Controller Role. This is done via GETACCCR CCC once it has finished performing any tasks that require it to request and gain the Controller Role. This device shall support a Controller Role request from any Controller-capable device.

ibi_support

0 – The device does not support IBI and will NACK any I3C Target IBI. This setting is not supported in this IP when device is configured with Secondary Controller capability.

1 – The device may support IBI and will ACK an I3C Target IBI while it is the Active Controller on the Bus.

2.14.55. Data Format

- Data is in big endian format.
- SDR data consumes a byte in FIFO.

3. IP Core Generation, Simulation, and Validation

This section provides information on how to generate the I3C Target IP Core using the Lattice Radiant software and how to run simulation and synthesis. For more details on the Lattice Radiant software, refer to the Lattice Radiant software user guide.

3.1. Licensing the IP

An IP core-specific license string is required to enable full use of the I3C Target IP Core in a complete, top-level design. When the IP Core used in Lattice FPGA devices built on the Lattice Nexus™ platform, you can fully evaluate the IP core through functional simulation and implementation (synthesis, map, place, and route) without an IP license string. This IP core supports Lattice's IP hardware evaluation capability, which makes it possible to create versions of the IP core, which operate in hardware for a limited time (approximately four hours) without requiring an IP license string. See Hardware Validation section for further details. However, a license string is required to enable timing simulation and to generate bitstream file that does not include the hardware evaluation timeout limitation.

3.2. Generation and Synthesis

Lattice Radiant software allows you to generate and customize modules and IPs and integrate them into the device architecture.

To generate the I3C Target IP Core:

1. In the Module/IP Block Wizard, create a new Lattice Radiant software project for I3C Target module.
2. In the dialog box, configure the I3C Target module according to custom specifications, using drop-down menus and check boxes. As a sample configuration, see Figure 3.1 and Figure 3.2. For configuration options, see Table 2.6.

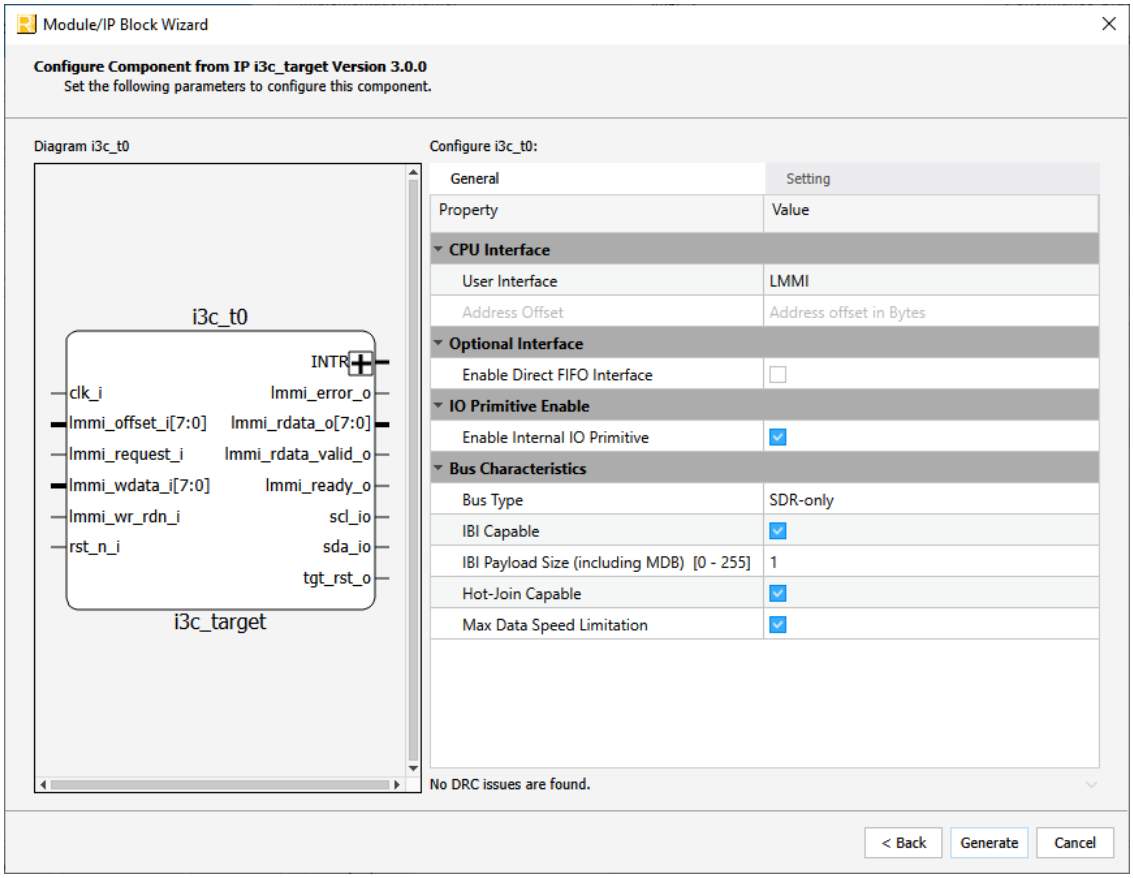

Figure 3.1. Configure Block of I3C Target Module – General Tab

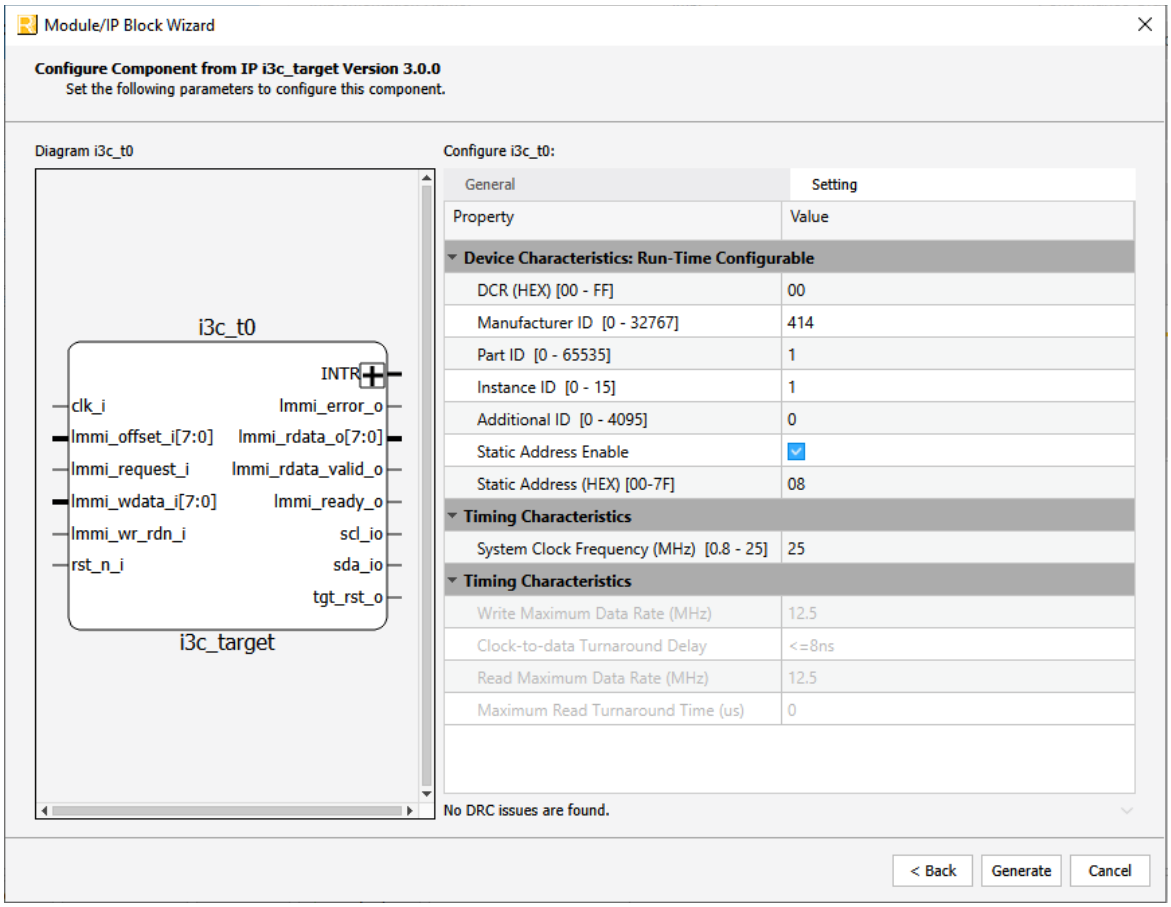

Figure 3.2. Configure Block of I3C Target Module – Settings Tab

3. Click **Generate**. The Check **Generating Result** dialog box opens, showing design block messages and results.
4. Click the **Finish** button to generate the Verilog file.

The generated I3C Target IP Core package includes the black box (<Instance Name>_bb.v) and instance templates (<Instance Name>_tmpl.v/vhd) that can be used to instantiate the core in a top-level design. An example RTL top-level reference source file (<Instance Name>.v) that can be used as an instantiation template for the IP core is also provided. You may also use this top-level reference as the starting template for the top-level for their complete design. The generated files are listed in Table 3.1.

Table 3.1 Generated File List

Attribute	Description
<Instance Name>.ipx	This file contains the information on the files associated to the generated IP.
<Instance Name>.cfg	This file contains the parameter values used in IP configuration.
component.xml	Contains the ipxact:component information of the IP.
design.xml	Documents the configuration parameters of the IP in IP-XACT 2014 format.
rtl/<Instance Name>.v	This file provides an example RTL top file that instantiates the IP core.
rtl/<Instance Name>_bb.v	This file provides the synthesis black box.
misc/<Instance Name>_tmpl.v misc /<Instance Name>_tmpl.vhd	These files provide instance templates for the IP core.

5. Upon generating desired design, you can synthesize it by clicking **Synthesize Design** located in the top left corner of the screen, as shown in Figure 3.3.

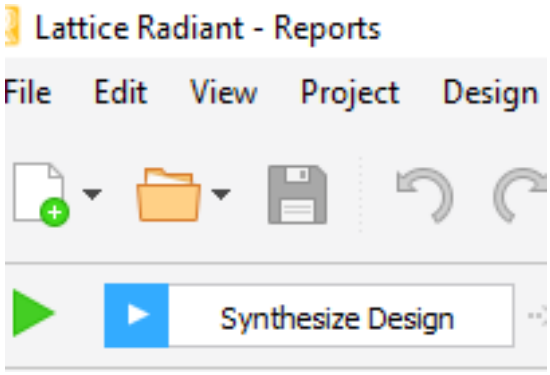

Figure 3.3. Synthesizing Design

3.3. Running Functional Simulation

To run Verilog simulation:

1. Click the button located on the **Toolbar** to initiate the **Simulation Wizard** shown in Figure 3.4.

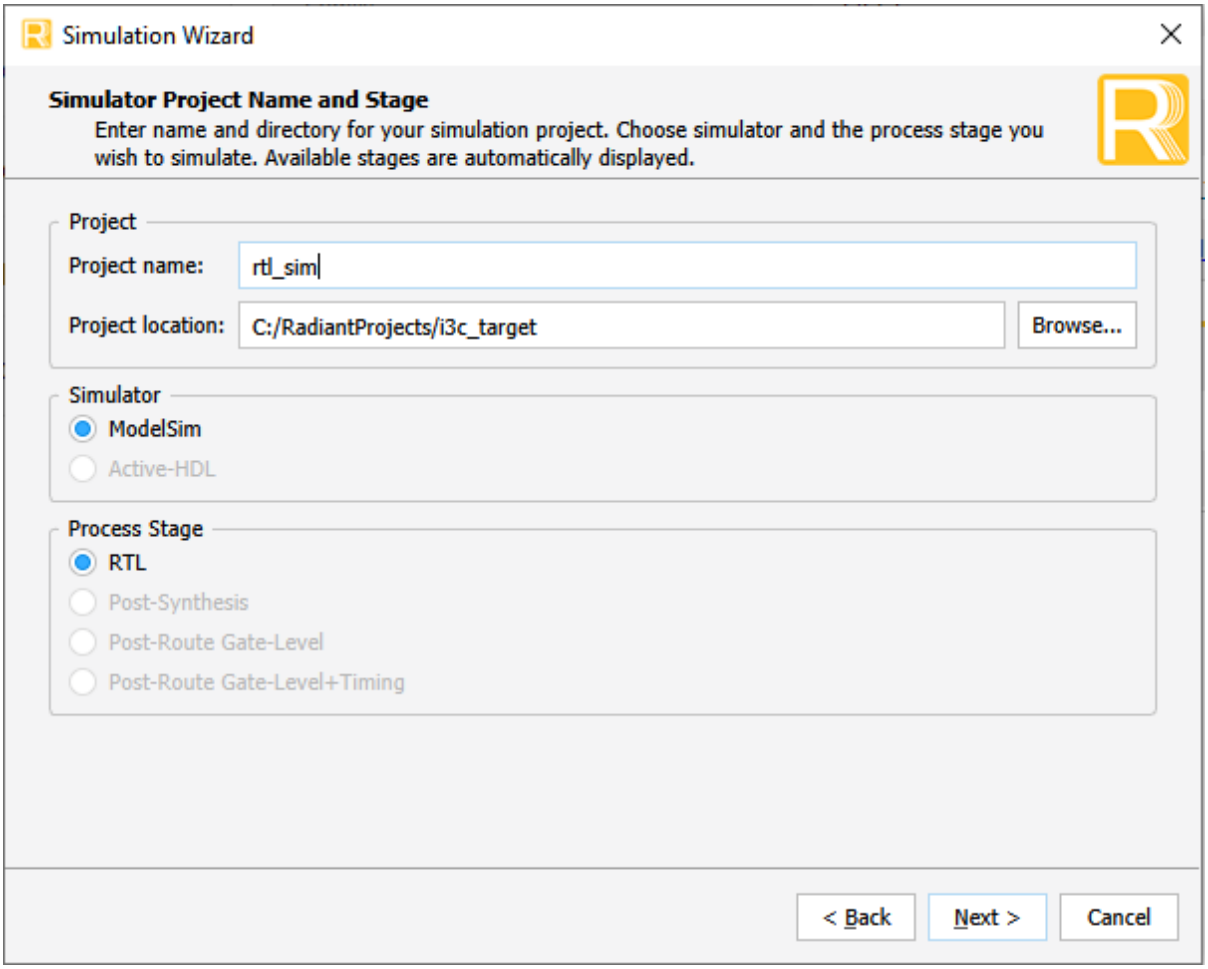

Figure 3.4. Simulation Wizard

2. Double-click **Next** to open the Add and Reorder Source window as shown in Figure 3.5.

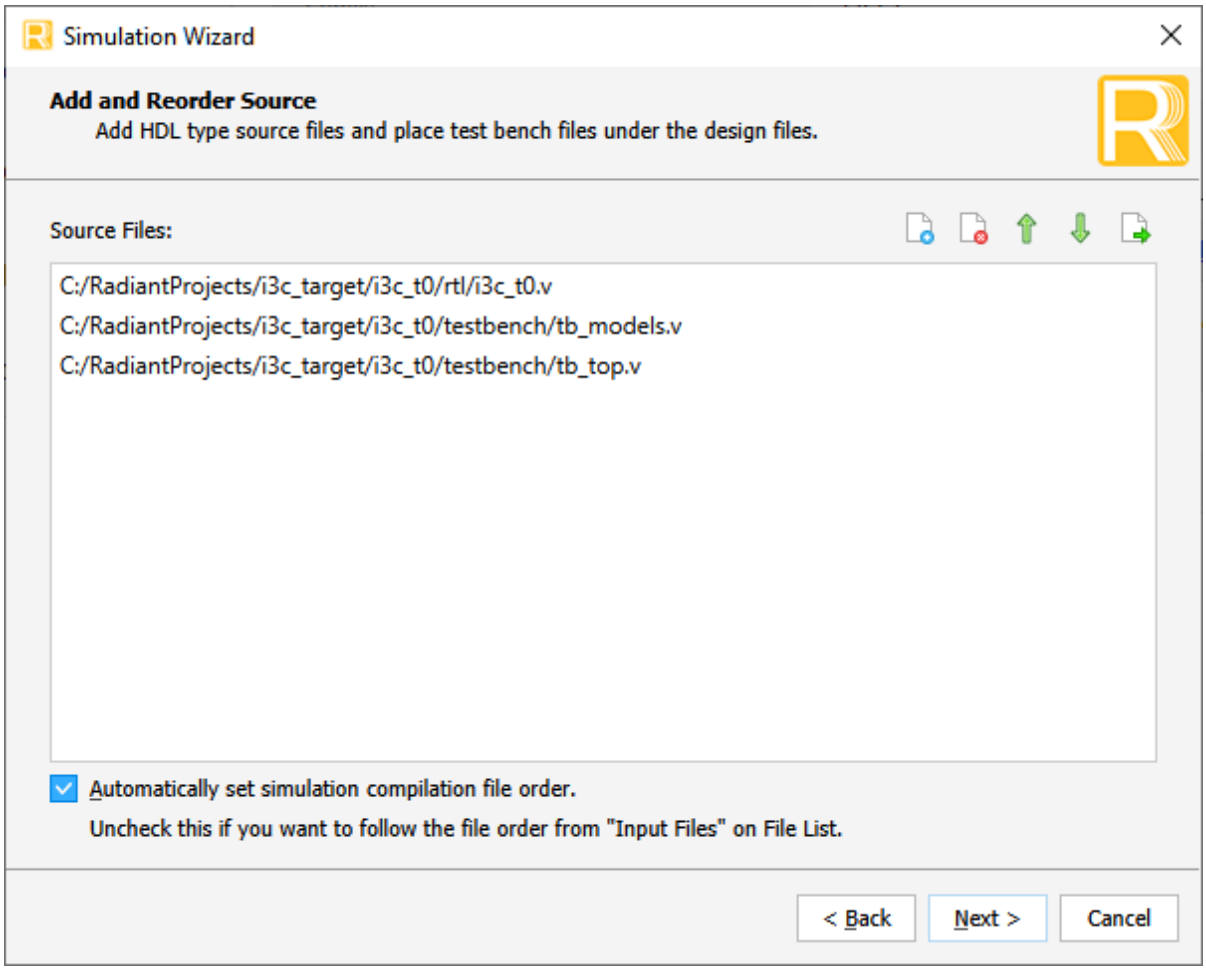

Figure 3.5. Adding and Reordering Source

3. Click **Next** and **Finish** to run simulation.

3.4. Constraining the IP

Refer to constraints/<instance_name>.ldc for the recommended constraints for this IP.

3.5. Hardware Validation

This IP has been validated using the following devices: Lattice CrossLink-NX and Lattice CertusPro-NX. This IP has not been validated yet using a Lattice Avant device.

3.6. IP Evaluation

The I3C Target IP Core supports Lattice's IP hardware evaluation capability when used with Lattice FPGA devices built on the Lattice Nexus platform. This makes it possible to create versions of the IP core that operate in hardware for a limited period of time (approximately four hours) without requiring the purchase of an IP license. It may also be used to evaluate the core in hardware in user-defined designs. The hardware evaluation capability may be enabled/disabled in the Strategy dialog box. By default, it is enabled. To change this setting, go to **Project > Active Strategy > LSE/Synplify Pro Settings**.

4. Ordering Part Number

The Ordering Part Number (OPN) for this IP Core are the following:

Table 4.1. Ordering Part Numbers

Part Number	Device	License Type
I3C-S-CNX-U	CrossLink-NX	Single Design License
I3C-S-CNX-UT	CrossLink-NX	Site License
I3C-S-CNX-US	CrossLink-NX	1 Year Subscription License
I3C-S-CTNX-U	Certus-NX	Single Design License
I3C-S-CTNX-UT	Certus-NX	Site License
I3C-S-CTNX-US	Certus-NX	1 Year Subscription License
I3C-S-CPNX-U	CertusPro-NX	Single Design License
I3C-S-CPNX-UT	CertusPro-NX	Site License
I3C-S-CPNX-US	CertusPro-NX	1 Year Subscription License
I3C-S-XO5-U	MachXO5-NX	Single Design License
I3C-S-XO5-UT	MachXO5-NX	Site License
I3C-S-XO5-US	MachXO5-NX	1 Year Subscription License
I3C-S-UP-U	iCE40 UltraPlus	Single Design License
I3C-S-UP-UT	iCE40 UltraPlus	Site License
I3C-S-UP-US	iCE40 UltraPlus	1 Year Subscription License
I3C-S-AVE-U	Avant-E	Single Design License
I3C-S-AVE-UT	Avant-E	Site License
I3C-S-AVE-US	Avant-E	1 Year Subscription License

Appendix A. Resource Utilization

The I3C Target module resource utilization is shown in Table A.1 using LFCPNX-100-7ASG256C device using Lattice Synthesis Engine of Lattice Radiant Software 2022.1. Default configuration is used, and some attributes are changed from default value to show the effect on the resource utilization.

Table A.1 Resource Utilization

Configuration	clk Fmax (MHz)	Registers	LUTs	EBRs	DSPs
Default	104.26	725	1887	2	0
IBI Capable = False	95.22	660	1637	2	0
Hot-Join Capable = False	99.25	707	1842	2	0
IBI Capable = False, Hot-Join Capable = False	100.17	627	1499	2	0

Notes:

1. Fmax is generated when the FPGA design only contains the SDR module, and the target frequency is 200 MHz. These values may be reduced when user logic is added to the FPGA design.
2. The distributed RAM utilization is accounted for in the total LUT4s utilization. The actual LUT4 utilization is distribution among logic, distributed RAM, and ripple logic.

The I3C Target module resource utilization is shown in Table A.2 using LIFCL-40-7BG256I device using Lattice Synthesis Engine of Lattice Radiant Software 2022.1. Default configuration is used, and some attributes are changed from default value to show the effect on the resource utilization.

Table A.2 Resource Utilization

Configuration	clk Fmax (MHz)	Registers	LUTs	EBRs	DSPs
Default	88.44	756	1832	2	0
IBI Capable = False	91.79	699	1555	2	0
Hot-Join Capable = False	98.16	707	1842	2	0
IBI Capable = False, Hot-Join Capable = False	91.56	627	1499	2	0

Notes:

1. Fmax is generated when the FPGA design only contains the SDR module, and the target frequency is 200 MHz. These values may be reduced when user logic is added to the FPGA design.
2. The distributed RAM utilization is accounted for in the total LUT4s utilization. The actual LUT4 utilization is distribution among logic, distributed RAM, and ripple logic.

References

For complete information on Lattice Radiant Project-Based Environment, Design Flow, Implementation Flow and Tasks, as well as on the Simulation Flow, see the Lattice Radiant Software user guide.

- CrossLink-NX FPGA web page
- Certus-NX FPGA web page
- CertusPro-NX FPGA web page
- iCE40 UltraPlus FPGA web page
- MachXO5-NX FPGA web page
- Lattice Avant-E FPGA web page
- Lattice Radiant Software FPGA webpage
- I3C MIPI specification

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/en/Support/AnswerDatabase

Revision History

Revision 1.1, July 2023

Section	Change Summary
Acronyms in This Document	Added *AHB*, *APB*, *GUI*, *HDL*, and *LSE* and their definitions.
Introduction	• Added sentence *The Lattice I3C IP Core is designed to comply with the MIPI I3C specification* in Introduction section. • Added *Resource* column in Table 1.1. Quick Facts. • Added bullet information *_io are bidirectional signals* in Signal Names section. • Added Attribute section.

Functional Description	• Updated Figure 2.1. I3C Target IP Core Functional Diagram.
	• Added Reset Propagation section and moved Common Command Codes section before I3C Transfers in SDR Mode section.
	• Replaced Broadcast with Target in Figure 2.14. HDR-DDR Direct Set CCC and Figure 2.15. HDR-DDR Direct Get CCC.
	• Updated Table 2.5 Ports Description for below:
	  • Added signal names *tgt_rst_o, ext_scl_i, ext_sda_i, ext_sda_o, ext_sda_oe, Direct FIFO Interface8, tx_valid_i, tx_ready_o, tx_data_i [7:0], rx_valid_o, rx_ready_i,* and *rx_data_o.*
	  • Deleted signal names *lmmi_error_o* and *tgt_rst_o*.
	  • Added table notes *For more details on target reset, see Section 5.1.11 of the MIPI Specification for I3C. Bidirectional I3C interface is only available when internal IO primitives are enabled in IP generation GUI. External IO I3C interface is only available when internal IO primitives are disabled in IP generation GUI. Direct FIFO interface is only available when enabled in IP generation GUI*.
	• Updated Table 2.6 Attributes Summary for below:
	  • Replaced default values of User Interface and Address Offset from *LMMI and Bytes* to *APB and DWORD*.
	  • Added attributes *Optional Interface, Enable Direct FIFO Interface, Tx Data Width, Rx Data Width, IO Primitive Enable,* and *Enable internal IO primitive*.
	  • Replaced Selectable values of System Clock Frequency (MHz) from *125* to *50* and deleted.
	  • Deleted Selectable values of *Write Maximum Data Rate (MHz), Clock-to-data Turnaround Delay (tSCO), Read Maximum Data Rate (MHz), Maximum Read Turnaround Time (us)*.
	• Replaced Reset information of [3] Bits from *0x1* to *0x1 – If Target is Hot-Join capable 0x0 – If Target is not Hot-Join capable* and Reset information of [0] Bits from *0x1* to *0x1 – If Target is IBI capable 0x0 – If Target is not IBI capable*, and deleted table note in Table 2.10. Events Command Enable.
	• Replaced Reset information of [3] Bits from *0x1* to *0x1 – If Target is Hot-Join capable 0x0 – If Target is not Hot-Join capable*, and Reset information of [0] from *0x1* to *0x1 – If Target is IBI capable 0x0 – If Target is not IBI capable* in Table 2.11. Events Command Device Configuration.
	• Added Reset information of [0] Bits as *– SDR mode only 0x1 – SDR and HDR-DDR mode is supported* in Table 2.31. Device Capabilities Byte1.
	• Replaced Names from *hdr_ddr_abort_crc*, *hdr_ddr_wr_abort* to *hdr_ddr_abort_crc_caps*, *hdr_ddr_wr_abort_caps* and replaced Reset information with *0x0 – If only SDR capable*, *0x1 – if HDR DDR capable* and *0x0 – If only SDR capable*, *0x1 – if HDR DDR capable*.
	• Added Interrupt Status 5 0x3C, Interrupt Status 5 Enable 0x3D, and Interrupt Status 5 Set 0x3E sections.
	• Updated the title of HDR-DDR Abort Configuration 0x54 section from *HDR-DDR Abort Configuration 0x54 set by Controller via ENDXFER CCC* and added sentence *HDR-DDR Abort Configuration set by Controller via ENDXFER CCC*.
	• Added sentences *I3C Target registers are accessible when I3C Controller IP is configured with Secondary-Controller Capability*, and *The following section describes I3C Target registers that have changes in reset value and/or definition when used for Secondary Controller. Registers not included in this section retain the definitions as when device is configured as I3C Target-only* in Secondary Controller Registers section.
	• Added Dynamic Address 0x02 and Maximum Write Data Speed (MaxWr) 0x0C section.

	• Replaced Reset information of device_role from *0x0* with *0x0 – Device is Target-only 0x1 – Device is Controller-Capable* and Reset information of advanced_caps from *0x0* to *0x1 (Fixed)* in Table 2.61. Bus Characteristics Register.
	• Added sentence *Fixed to 1 when device is configured with Secondary-Controller capability* in Bus Characteristics Register 0x00 section.
	• Replaced Reset information of hj_enec from *0x1* with *0x1 – If Target is Hot-Join capable 0x0 – If Target is not Hot-Join capable* and Reset information of advanced_caps from *0x1* to *0x1 – If Target is IBI capable 0x0 – If Target is not IBI capable* in Table 2.62. Events Command Enable.
	• Deleted sentences *Reset value is 1 if Target is configured with Hot-Join capability, 0 otherwise* and *Reset value is 1 if Target is configured with IBI capability, 0 otherwise* in Events Command Enable 0x03 section.
	• Deleted sentences *Reset value is 1 if Target is configured with Hot-Join capability, 0 otherwise. Reset value is 1 if Target is configured with Secondary-Controller Capability, 0 otherwise* and *Reset value is 1 if Target is configured with IBI capability, 0 otherwise* in Events Command Device Configuration 0x04 section.
	• Replaced Reset information of hj_cap, cr_cap, ibi_cap with *0x1 – If Target is Hot-Join capable 0x0 – If Target is not Hot-Join capable*, *0x1 – If Target is Secondary Controller capable 0x0 – If Target is not Secondary Controller capable*, *0x1 – If Target is IBI capable 0x0 – If Target is not IBI capable* in Table 2.63. Events Command Device Configuration.
	• Replaced name from *reserved* to *device_role_changed* and access from *read-only* to *read-write* in Table 2.67. Interrupt Status 4
	• Replaced name from *reserved* to *device_role_changed_en* and access from *read-only* to *read-write* in Table 2.68. Interrupt Status 4 Enable.
	• Added device_role_changed information in Interrupt Status 4 0x39 section.
	• Replaced Access from *read-write* to *write-only* in Table 2.69. Interrupt Status 4 Set.
	• Added *LSB* to title of GETSTATUS Controller-Capable Device LSB 0x45 section.
	• Added below information in HDR-DDR Abort Configuration 0x54 section:
	  • *2'b11 - No CRC Word follows Early Termination request.*
	  2'b01 - CRC Word follows Early Termination request.
	  Other - reserved for future definition by MIPI alliance.
	  • Replaced *High* with *Low* in hdr_ddr_write_abort and hdr_ddr_write_nack information.

IP Core Generation, Simulation, and Validation	• Added Constraining the IP and IP Evaluation sections.
Ordering Part Number	Added Avant-E part numbers in Table 4.1. Ordering Part Numbers.
Reference	Added links for CrossLink-NX, Certus-NX, CertusPro-NX, MachXO5-NX, iCE-40 UltraPlus, Avant-E web pages.

Revision 1.0, April 2023

Section	Change Summary
All	Initial release.

www.latticesemi.com