PLL Module - Lattice Radiant Software

User Guide

FPGA-IPUG-02220-1.0

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
FPGA	Field Programmable Gate Array
IP	Intellectual Property
LMMI	Lattice Memory Mapped Interface
APB	Advanced Peripheral Bus
PLL	Phase-Locked Loop

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1. Introduction

The Phase Locked Loop (PLL) Module is capable of frequency synthesis and clock phase management including clock injection delay cancellation. It has the flexibility of input and feedback source selections, multiple output selections, VCO phase rotation, and independent phase-shifting features. The multiple output clocks can be synchronized with the option to enable or be individually controlled dynamically by users.

1.1. Quick Facts

Table 1.1 presents a summary of the PLL Module.

Table 1.1. Quick Facts

IP Requirements	Supported FPGA Families	Lattice Avant
Resource Utilization	Targeted Devices	LAV-AT-500E
Design Tool Support	Lattice Implementation	Lattice Radiant® Software 2022.1
		Synopsys® Synplify Pro® for Lattice
	Simulation	For the list of supported simulators, see the Lattice Radiant Software User Guide.

1.2. Features

The key features of the PLL Module include:

- Multiple feedback inputs
- Multiple output clocks
- Lock detector – Phase and Frequency
- Reference clock divider values (NR) – 1 to 64
- Integer Feedback divider values (NF) – 2 to 4095
- Output divider values (NO) – 1 to 256
- Supports Fractional-N divider – up to 14 bits resolution
- Supports Spread Spectrum Clock Generation
  - Spreading rate adjustment range 15 kHz – 4 MHz
  - Spreading depth 0% – 10%
- VCO phase shift – 8 VCO phases
- Post Divider phase shift
- Dynamic VCO and divider phase shift
- Output clock bypass
- Programmable bandwidth

1.3. Conventions

1.3.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.3.2. Signal Names

Signal names that end with:

- *_n* are active low
- *_i* are input signals
- *_o* are output signals

1.3.3. Attribute Names

Attribute names in this document are formatted in title case and italicized (*Attribute Name*).

2. Functional Description

2.1. Overview

The PLL Module is capable of clock synthesis and clock phase management including clock tree delay cancellation.

The PLL Module performs frequency synthesis, multiplication, division, and clock injection delay removal. For clock synthesis applications where the removal of clock injection delay is not a requirement, the GPLL block has an internal feedback path that is used to complete the feedback loop. Applications that require the removal of the clock injection delay take the feedback clock from the output of the relevant clock tree.

A top-level block diagram of the Global Phase Locked Loop Module is shown in Figure 2.1.

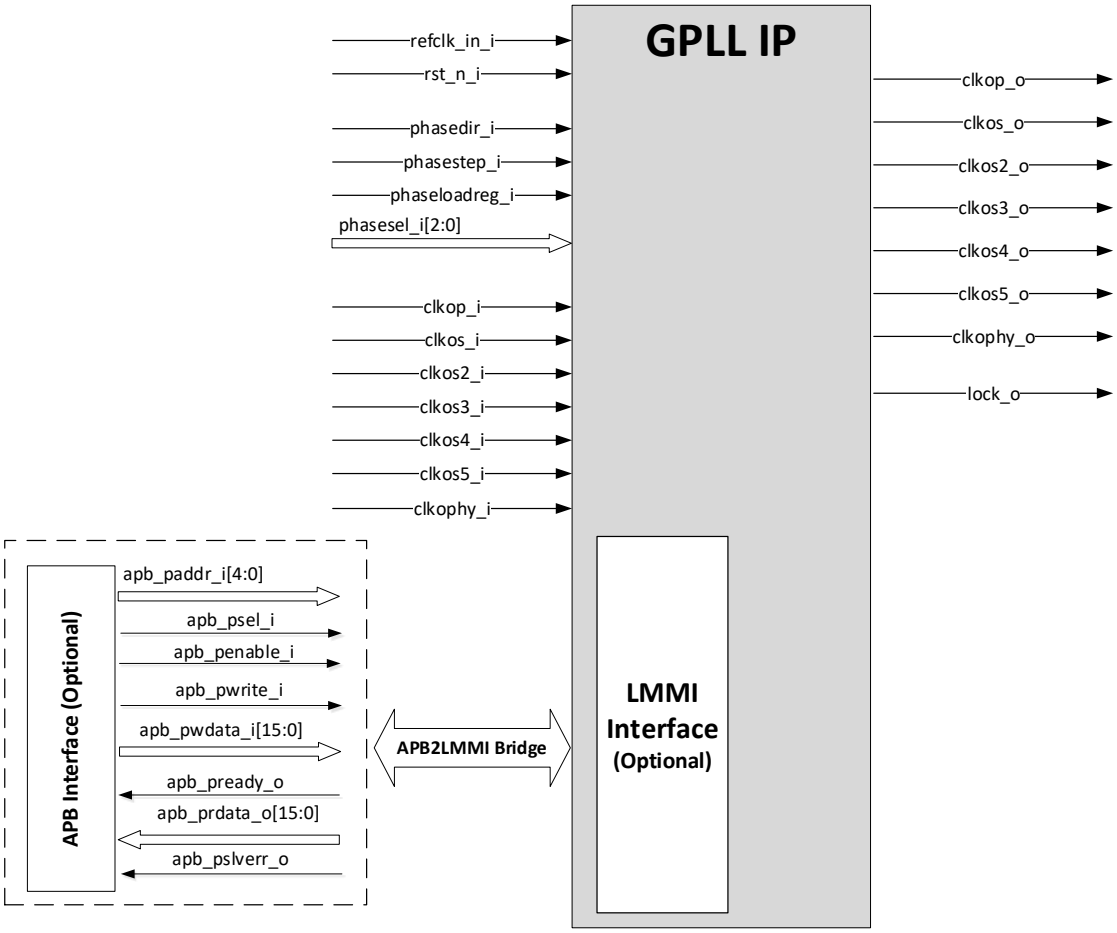

Figure 2.1. GPLL Top Level Block Diagram

This PLL Module has the flexibility of multiple feedback clock source selections. It has main logic features as 7 independent output clocks, output phase shifting through VCO phases, synchronous outputs, and divider phase shifts.

2.2. Signal Description

Table 2.1. PLL Module Signal Description

Port Name	I/O	Width	Description
Clock and Reset			
refclk_in_i	In	1	Reference clock.
rst_n_i	In	1	PLL reset signal enabled by user from the IP GUI via *PLL Reset Options: Provide PLL Reset*
clkop_o	Out	1	PLL output clock enabled by user from the IP GUI via *CLKOUT [n]: Port Name* set as *CLKOP.*
clkos_o	Out	1	PLL output clock enabled by user from the IP GUI via *CLKOUT [n]: Port Name* set as *CLKOS.*
clkos2_o	Out	1	PLL output clock enabled by user from the IP GUI via *CLKOUT [n]: Port Name* set as *CLKOS2.*
clkos3_o	Out	1	PLL output clock enabled by user from the IP GUI via *CLKOUT [n]: Port Name* set as *CLKOS3.*
clkos4_o	Out	1	PLL output clock enabled by user from the IP GUI via *CLKOUT [n]: Port Name* set as *CLKOS4.*
clkos5_o	Out	1	PLL output clock enabled by user from the IP GUI via *CLKOUT [n]: Port Name* set as *CLKOS5.*
clkophy_o	Out	1	PLL output clock enabled by user from the IP GUI via *CLKOUT [n]: Port Name* set as *CLKOPHY.* This clock is reserved for DDRPHY.
Miscellaneous / Optional Ports			
phasedir_i	In	1	Dynamic Phase direction signal enabled by user from the IP GUI via *Optional Ports: Dynamic Phase Control Ports.* 0 – Phase Advance 1 – Phase Delayed
phasestep_i	In	1	Dynamic Phase step signal enabled by user from the IP GUI via *Optional Ports: Dynamic Phase Control Ports.*
phaseloadreg_i	In	1	Dynamic Phase load signal enabled by user from the IP GUI via *Optional Ports: Dynamic Phase Control Ports.*
phasesel_i [2:0]	In	3	Dynamic Phase clock select signal enabled by user from the IP GUI via *Optional Ports: Dynamic Phase Control Ports.* 0 – clkop_o 1 – clkos_o 2 – clkos2_o 3 – clkos3_o 4 – clkos4_o 5 – clkos5_o 6 – clkophy_o
clkop_i	In	1	Output Clock Enable signals, enabled by user from the IP GUI via *Optional Port Selections: Clock Enable Ports*.
clkos_i	In	1	
clkos2_i	In	1	
clkos3_i	In	1	
clkos4_i	In	1	
clkos5_i	In	1	
clkophy_i	In	1	
lock_o	Out	1	PLL lock signal enabled by user from the IP GUI via *PLL Lock: Provide PLL Lock Signal.*
refclk_out_o	Out	1	Optional signal enabled by user from the IP GUI via *Miscellaneous Ports.* Reference clock output.
div_change_fbkclk_o	Out	1	Optional signal enabled by user from the IP GUI via *Miscellaneous Ports.*

Port Name	I/O	Width	Description
			Feedback divider (NF) count change enables output.
div_change_refclk_o	Out	1	Optional signal enabled by user from the IP GUI via *Miscellaneous Ports.* Reference divider (NR) count change enables output.
slip_fbkclk_o	Out	1	Optional signal enabled by user from the IP GUI via *Miscellaneous Ports.* PLL IP provides two lower-level signals (slip_fbkclk_o and slip_refclk_o) which detect cycle slips between the VCO (i.e. feedback) and reference clocks. A brown-out condition may cause the PLL to lose lock. A brown-out condition occurs when the analog or digital supply voltage that drives the PLL becomes smaller than the specified minimum levels. When a brown-out condition occurs, pulses may be observed on the slip_* signals, indicating an out of lock condition. The LOCK output of the detector circuit will simultaneously output a low signal. The slip_* and LOCK signals, along with a brown-out detector circuit, can be used to force the PLL to go through the reset sequence to re-lock. Note that one should not assume that the PLL will recover to its locked condition after the brown-out condition subsides. It is possible that during the brown-out condition, the PLL loop can become stuck in a state from which it cannot recover without a reset sequence. Therefore, following a brown-out condition, the PLL should always go through a reset sequence to guarantee relock.
slip_refclk_o	Out	1	
outresetack_clkop_o	Out	1	Optional signal enabled by user from the IP GUI via *Miscellaneous Ports.* Internal OUTRESET change occurred output.
outresetack_clkos_o	Out	1	
outresetack_clkos2_o	Out	1	
outresetack_clkos3_o	Out	1	
outresetack_clkos4_o	Out	1	
outresetack_clkos5_o	Out	1	
outresetack_clkophy_o	Out	1	
stepack_clkop_o	Out	1	Optional signal enabled by user from the IP GUI via *Miscellaneous Ports.* Internal STEP change occurred output.
stepack_clkos_o	Out	1	
stepack_clkos2_o	Out	1	
stepack_clkos3_o	Out	1	
stepack_clkos4_o	Out	1	
stepack_clkos5_o	Out	1	
stepack_clkophy_o	Out	1	
LMMI Interface[1] – This is currently not available			
lmmi_clk_i	In	1	LMMI Clock
lmmi_resetn_i	In	1	Reset (active low) Resets the LMM interface. Does not reset the internals of the Hard IP block.
lmmi_request_i	In	1	Start transaction
lmmi_wr_rdn_i	In	1	Write = HIGH, Read = LOW
lmmi_offset_i [4:0]	In	5	Offset (5 bits) – register offset within the secondary register space, starting at offset 0.
lmmi_wdata_i [15:0]	In	16	Write data (16 bits)
lmmi_rdata_o [15:0]	Out	16	Read data (16 bits)
lmmi_rdata_valid_o	Out	1	Read transaction is complete and lmmi_rdata_o contains valid data.
lmmi_ready_o	Out	1	Secondary is ready to start a new transaction. Secondary can insert wait states by holding this signal low.
APB Interface[1] – This is currently not available			

Port Name	I/O	Width	Description
apb_pclk_i	In	1	APB clock
apb_preset_n_i	In	1	APB reset (active low)
apb_paddr_i [4:0]	In	5	APB Address signal
apb_psel_i	In	1	APB Select signal
apb_penable_i	In	1	APB Enable signal
apb_pwrite_i	In	1	APB Direction signal
apb_pwdata_i [15:0]	In	16	APB Write Data signal
apb_pready_o	Out	1	APB Ready signal
apb_prdata_o [15:0]	Out	16	APB Read Data signal
apb_pslverr_o	Out	1	APB Completer Error signal

Notes:

1. Only one of the two interfaces is available as selected by Interface attribute.
   The LMMI and APB interface, which is used to access the PLL registers, is currently not available. Users may refer later on Apps technical notes.

2.3. Attribute Summary

The configurable attributes of the PLL Module are shown in Table 2.2. The attributes can be configured through the IP Catalog's Module/IP wizard of the Lattice Radiant Software.

Table 2.2. Attributes Table

Attribute	Selectable Values	Default	Description
General			
Set Minimum VCO Frequency (MHz)	N/A	800	Display only. Minimum VCO frequency.
Set Maximum VCO Frequency (MHz)	N/A	2500	Display only. Maximum VCO frequency.
Set Parameter Optimization Target	Minimum Jitter, Minimum Power	Minimum Jitter	Set the calculator script to get the PLL parameter that gives either the lowest jitter or lowest power. Low jitter translates to higher VCO frequency. Lowest power translates to lower VCO frequency.
Set Maximum Error Option	Use large multiplication factor to reduce error, Use reasonable tolerance (NF <= 128), Find solution with lowest error, Use specified tolerance value	Find solution with lowest error	Select the tolerance mode that the script will consider when calculating the PLL parameters.
Set Number of Clock Outputs	1 – 7	1	Specify the number of PLL clock outputs.
Enable Fractional Accumulation (Dithering)	Checked, Unchecked	Checked	Enables the fractional feedback divider, otherwise feedback divider will use integer values only.
Enable Spread Spectrum Clock Generation	Checked, Unchecked	Unchecked	Enables Spread Spectrum Clock Generation.
Enable output sync with CLKOP	Checked, Unchecked	Unchecked	
Select Output Divider Path	NA	External Output Divider (1 – 256)	Display only.
Actual VCO Frequency	Calculated	N/A	Display only.

Attribute	Selectable Values	Default	Description
Reference Clock			
Reference Clock: Frequency (MHz)	10 – 800	100	Set the Reference Clock frequency.
Reference Clock: Divider Actual Value	Calculated	N/A	Display only.
Phase Detector Frequency (MHz)	Calculated	N/A	Display only.
Feedback			
Select Feedback Clock	Internal VCO, CLKOP, CLKOS, CLKOS2, CLKOS3, CLKOS4, CLKOS5, CLKOPHY	Internal VCO	Select the feedback clock from the enabled PLL clock outputs or internal VCO. Feedback clock will be internal VCO if Fractional-N or Spread Spectrum Clock is enabled.
Feedback Clock: Actual Divider Value (Float)	Calculated	N/A	Display only (Integer+Fractional).
Feedback Clock: Actual Divider Value (Integer)	Calculated	N/A	Display only.
Feedback Clock: Actual Divider Value (Fractional)	Calculated	N/A	Display only (value/256).
Feedback Clock: Actual Divider Value (Fractional-SSC)	Calculated	N/A	Display only (value/16384).
Spread Spectrum			
Spread Spectrum Profile	Up Spread, Center Spread, Down Spread	Down Spread	Select the spreading profile.
Bandwidth Adjustment Factor	0.5 – 2.0	1	Set the bandwidth adjustment factor.
Desired Modulation Frequency KHz	15 – 4000	30	Set the spreading frequency.
Actual Modulation Frequency KHz	Calculated	N/A	Display only.
Triangle Modulation Depth %	0.0244 – 10.0	2.5	Set the modulation depth.
Actual Triangle Modulation Depth %	Calculated	N/A	Display only.
SSC Minimum Feedback Divider	Calculated	N/A	Display only.
Spreading Slope Control Value	Calculated	N/A	Display only.
Spreading Rate Divider Value	Calculated	N/A	Display only.
Clock Output [n], n = 0 – 6			
CLKOUT [n]: Port Name	CLKOP, CLKOS, CLKOS2, CLKOS3, CLKOS4, CLKOS5, CLKOPHY	CLKOP	Select which PLL clock to configure.
CLKOUT [n]: Bypass	Checked, Unchecked	Unchecked	Bypass the actual divider output and output the reference clock instead.
CLKOUT [n]: Desired Frequency Value (MHz)	3.125 – 2400 MHz	100	Set the desired Output Clock frequency.
CLKOUT [n]: Actual Frequency Value (MHz)	Calculated	N/A	Display Only.
CLKOUT [n]: Actual Divider Value	Calculated	N/A	Display Only.
CLKOUT [n]: Tolerance (%)	0 – 10	0.0	Set the acceptable tolerance for actual vs desired output frequency. Available only if the selected *Maximum Error Option is "Use specified tolerance value".*
CLKOUT [n]: ERROR (PPM)	Calculated	0	Display Only. Difference between desired and actual frequencies.
CLKOUT [n]: Static Phase Shift (Degrees)	0, 45, 90, 135, 180, 225, 270, 315	0	Set the desired clock output phase.

Attribute	Selectable Values	Default	Description
Optional Ports			
Dynamic Phase Control Ports			
Enable Dynamic Phase Ports	Checked, Unchecked	Unchecked	Enable/Disable dynamic phase control ports.
Clock Enable Ports			
CLKOUT [n] Enable Port	Checked, Unchecked	Unchecked	Set to provide clock enable port.
PLL Reset			
Provide PLL Reset	Checked, Unchecked	Unchecked	Set to provide PLL reset port.
PLL Lock			
Provide PLL Lock Signal	Checked, Unchecked	Unchecked	Set to provide PLL lock port.
Enable Fast Lock	Checked, Unchecked	Unchecked	Set the behavior of PLL lock signal.
Miscellaneous Ports			
Enable Misc Port	Checked, Unchecked	Unchecked	Set to provide optional status ports.

3. IP Generation and Evaluation

This section provides information on how to generate the PLL Module using the Lattice Radiant Software and how to run simulation and synthesis. For more details on the Lattice Radiant Software, refer to the Lattice Radiant Software User Guide.

3.1. Licensing the IP

No license is required for this IP module.

3.2. Generating and Synthesizing the IP

Lattice Radiant Software allows you to generate and customize modules and IPs and integrate them into the device architecture.

To generate PLL Module:

1. Create a new Lattice Radiant Software project or open an existing project.
2. In the **IP Catalog** tab, double-click on **PLL** under **Module, Architecture_Modules** category. The **Module/IP Block Wizard** opens as shown in Figure 3.1. Enter values in the **Instance name** and the **Create in** fields and click **Next**.

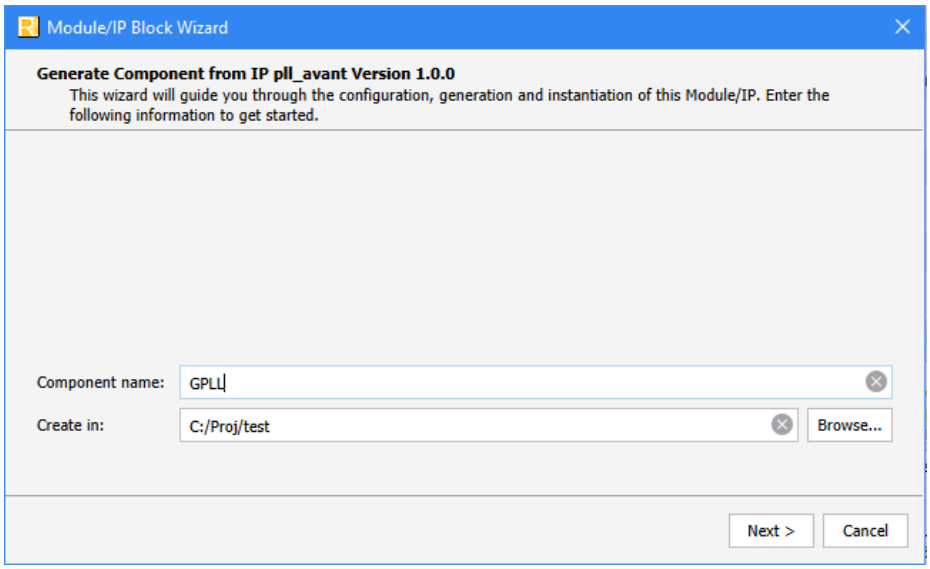

Figure 3.1. Configure Module/IP Block Wizard

3. In the module's dialog box of the **Module/IP Block Wizard** window, customize the selected PLL Module using drop-down menus and checkboxes. As a sample configuration, see Figure 3.2. For configuration options, see the Attributes section.

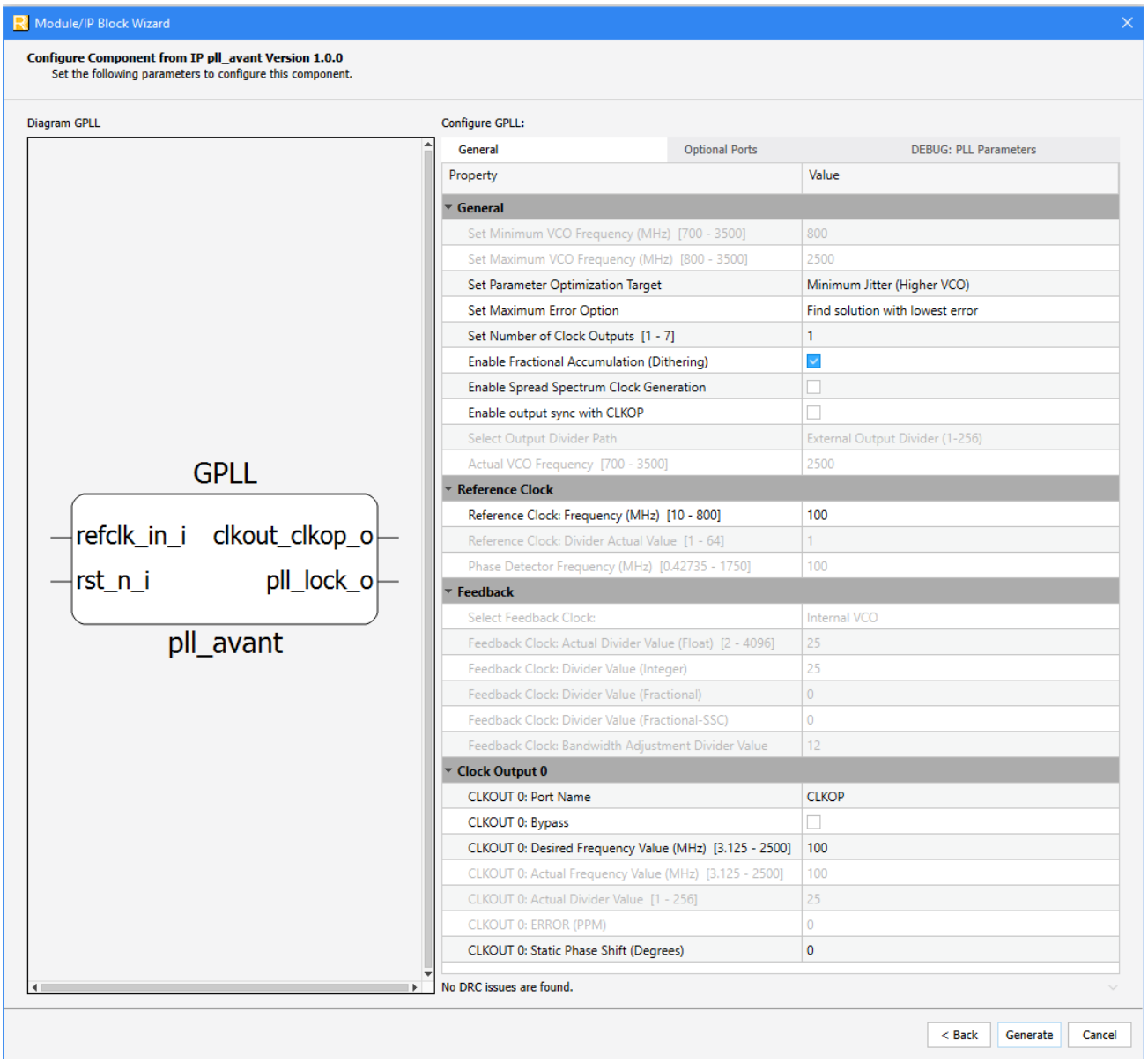

Figure 3.2. Configure User Interface of PLL Module

4. Click **Generate**. The **Check Generating Result** dialog box opens, showing design block messages and results as shown in Figure 3.3.

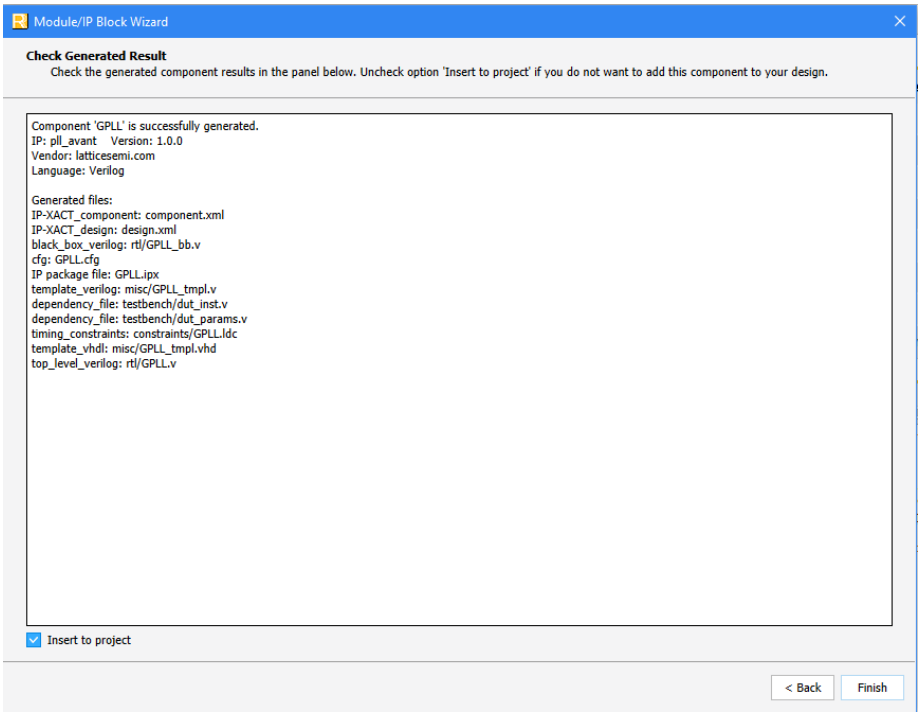

Figure 3.3. Check Generating Result

5. Click **Finish**. All the generated files are placed under the directory paths in the **Create in** and the **Instance name** fields are shown in Figure 3.1.

The generated PLL Module package includes the black box (<Instance Name>_bb.v) and instance templates (<Instance Name>_tmpl.v/vhd) that can be used to instantiate the module in a top-level design. An example RTL top-level reference source file (<Instance Name>.v) that can be used as an instantiation template for the module is also provided. You may also use this top-level reference as the starting template for the top-level for their complete design. The generated files are listed in Table 3.1.

Table 3.1. Generated File List

Attribute	Description
<Instance Name>.ipx	This file contains the information on the files associated to the generated IP.
<Instance Name>.cfg	This file contains the attribute values used in IP configuration.
component.xml	Contains the ipxact:component information of the IP.
design.xml	Documents the configuration attributes of the IP in IP-XACT 2014 format.
rtl/<Instance Name>.v	This file provides an example RTL top file that instantiates the module.
rtl/<Instance Name>_bb.v	This file provides the synthesis black box.
misc/<Instance Name>_tmpl.v misc /<Instance Name>_tmpl.vhd	These files provide instance templates for the module.

3.3. Running the Functional Simulation

Running functional simulation can be performed after the IP is generated and the testbench is added. For this module, a customer testbench is provided.

To add the generated testbench:

1. Go to **File List** tab, right-click **Input Files**.
2. Click Add > Existing Simulation File.
3. A window appears. Open the instance folder **testbench**, then double-click **tb_top.v**.

To run the simulation:

1. Click  button located on the **Toolbar** to initiate **Simulation Wizard**, as shown in Figure 3.4.

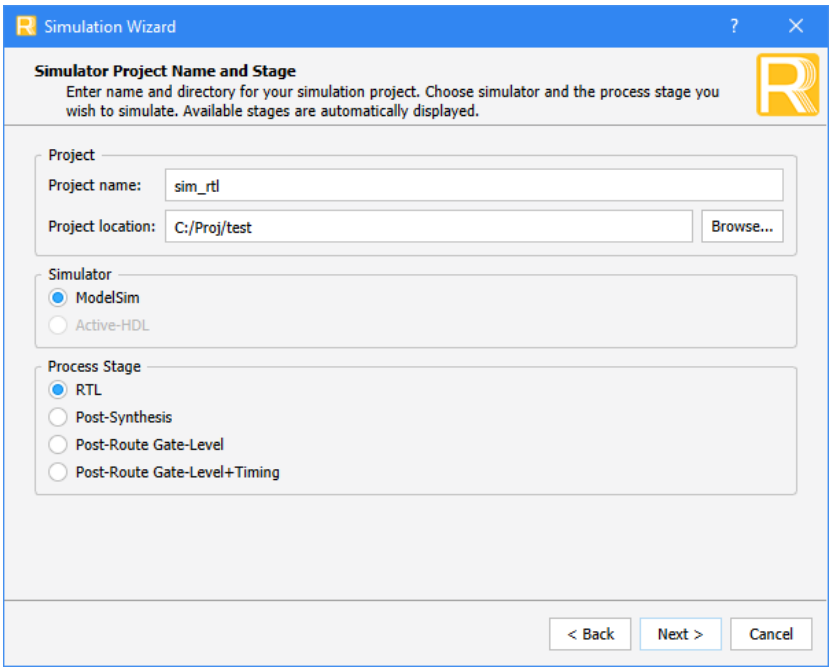

Figure 3.4. Simulation Wizard

2. Click **Next** to open the **Add and Reorder Source** window as shown in Figure 3.5.

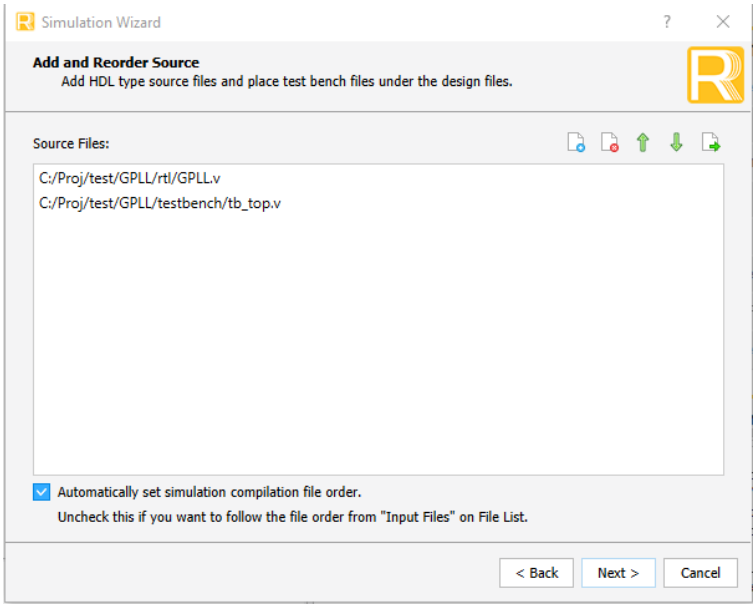

Figure 3.5. Adding and Reordering Source

Note: It is necessary to follow the procedure above until it is fully automated in the Lattice Radiant Software Suite. The results of the simulation in our example are shown in Figure 3.6.

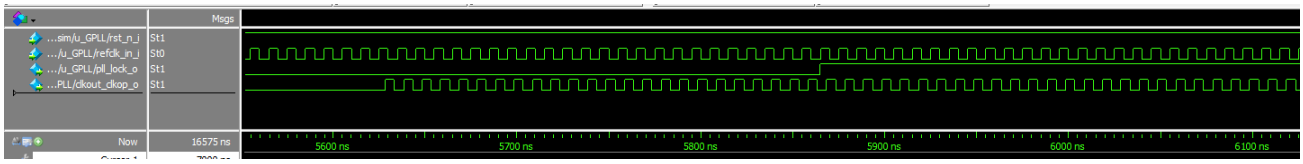

Figure 3.6. Simulation Waveform

3.4. Hardware Evaluation

There is no restriction on the hardware evaluation of this module.

References

For complete information on Lattice Radiant Project-Based Environment, Design Flow, Implementation Flow, and Tasks, as well as on the Simulation Flow, see the Lattice Radiant Software User Guide.

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.0, November 2022

Section	Change Summary
All	Initial release

www.latticesemi.com