AXI4 to AHB-Lite Bridge Module - Lattice Propel Builder

User Guide

FPGA-IPUG-02199-1.0

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
AMBA	Advanced Micro-controller Bus Architecture
AXI	Advanced Extensible Interface Bus
AHB	Advanced High-performance Bus
FPGA	Field Programmable Gate Array
RTL	Register Transfer Level

1. Introduction

The Lattice Semiconductor AXI to AHB-Lite Bridge Module provides an interface between the high-speed AXI and AHB-Lite.

The design is implemented in Verilog HDL. The IP can be configured and based on Table 1.1.

Table 1.1. FPGA Software for IP Configuration, Generation, and Implementation

Supported FPGA Family	IP Configuration and Generation	IP Implementation (Synthesis, Map, Place and Route)
Certus Pro-NX,MachXO5-NX	Lattice Propel Builder software	Lattice Radiant software

1.1. Features

The key features of the AXI to AHB-Lite Bridge Module include:

- Compliance with AMBA AXI4 and AMBA 3 AHB-Lite Protocol
- Support configurable data interface: 8,16,32,64,128,256,512 and 1024
- Support configurable AXI4 ID width: 1 to 11
- Support configurable AXI4 user width: 1 to 128
- Support AXI4 INCR and fixed burst transfers
- Number of supported AHB lite slaves is one.
- Registered output

1.2. Limitations

- AXI4 wrap burst not supported
- AxQOS, AxREGION, AxUSER, AxCACHE and AxLOCK are considered as don't care.
- AxPROT is a pass through to the AHB lite interface

2. Functional Descriptions

2.1. Overview

The Lattice Semiconductor AXI to AHB-Lite Bridge Module is used for interfacing one AXI4 master to one AHB-Lite Slave. When interfacing to multiple AHB-Lite Slaves, this IP should be used together with an AHB-Lite interconnect. The read and write transfers on the AXI4 are converted into equivalent transfers on the AHB-Lite.

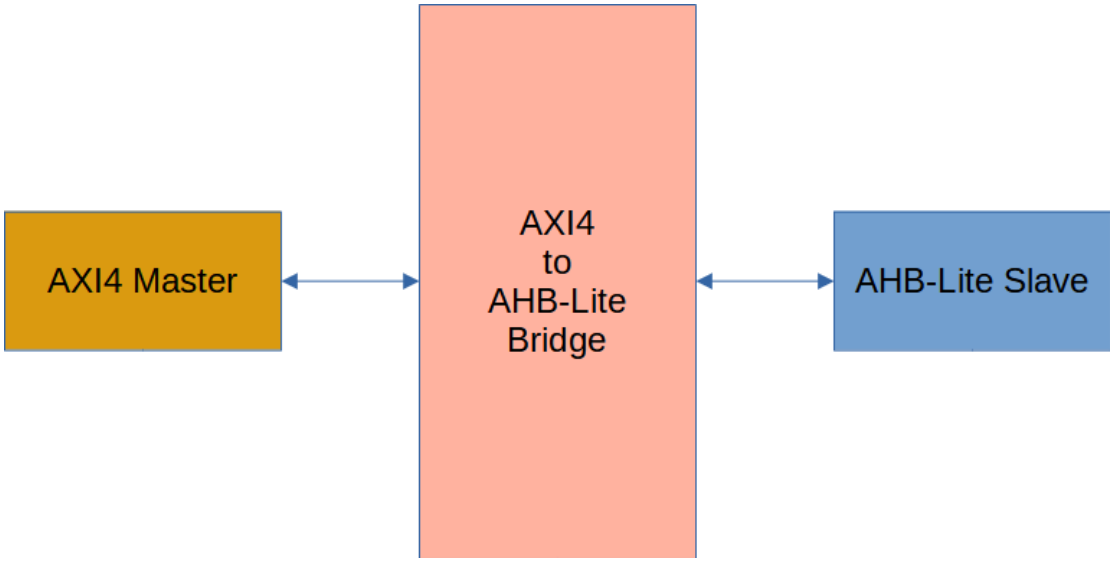

Figure 2.1. AXI4 to AHB-Lite Bridge

2.2. Interface Description

Figure 2.2 shows the interface diagram of the AXI4 to AHB-LITE Bridge Module. The diagram shows all the available ports for the IP core.

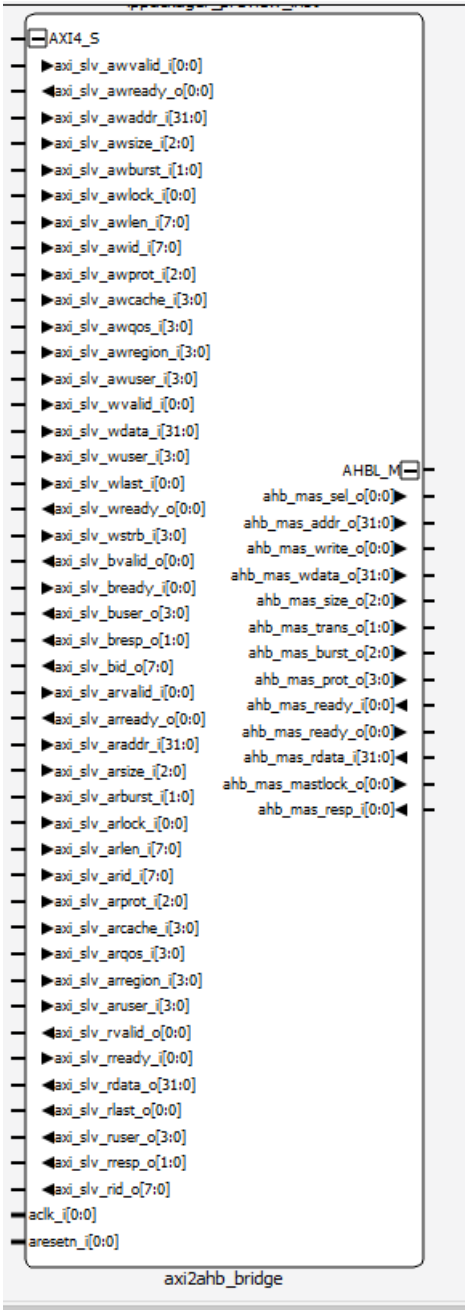

Figure 2.2. AXI4 to AHB-Lite Bridge Module Interface Diagram

Table 2.1. AXI4 to AHB-Lite Bridge Module Signal Description

Pin Name	Direction	Width (Bits)	Description
Clock and Reset			
aclk_i	In	1	AXI4 to AHB-Lite bridge clock.
aresetn_i	In	1	Active low reset.

Pin Name	Direction	Width (Bits)	Description
AXI4 Master Interface (AXI4_S)			
axi_slv_awvalid_i	In	1	Write address valid. This signal indicates that the channel is signaling valid write address and control information.
axi_slv_awaddr_i	In	32	Write address. The write address gives the address of the first transfer in a write burst transaction
axi_slv_awsize_i	In	3	Burst size. This signal indicates the size of each transfer in the burst
axi_slv_awburst_i	In	2	Burst type. The burst type and the size information, determine how the address for each transfer within the burst is calculated
axi_slv_awlen_i	In	8	Burst length. This indicates the number of beats per AXI burst.
axi_slv_awid_i	In	AXI_ID_WIDTH	AXI write ID width.
axi_slv_awlock_i	In	1	Lock type. AXI4: Optional
axi_slv_awcache_i	In	4	Memory type. AXI4: Optional
axi_slv_awprot_i	In	3	Protection type AXI4: Optional
axi_slv_awqos_i	In	4	Quality of Service. AXI4: Optional
axi_slv_awregion_i	In	4	Region AXI4: Optional
axi_slv_awuser_i	In	AXI_USER_WIDTH	User signals. AXI4: Optional
axi_slv_awready_o	Out	1	Write address ready. This signal indicates that the slave is ready to accept an address and associated control signals
axi_slv_wvalid_i	In	1	Write valid. This signal indicates that valid write data and strobes are available
axi_slv_wdata_i	In	AXI_AHB_DATA_WIDTH	Write data.
axi_slv_wlast_i	In	1	Write last. This signal indicates the last transfer in a write burst
axi_slv_wuser_i	In	AXI_USER_WIDTH	User signals. AXI4: Optional
axi_slv_wstrb_i	In	AXI_AHB_DATA_WIDTH/8	Write strobes. This signal indicates which byte lanes hold valid data. There is one write strobe bit for each eight bits of the write data bus
axi_slv_wready_o	Out	1	Write data ready. This signal indicates that the slave is ready to accept write data.
axi_slv_bvalid_o	Out	1	Write response valid. This signal indicates that the channel is signaling a valid write response
axi_slv_bid_o	Out	AXI_ID_WIDTH	Write response ID.
axi_slv_bresp_o	Out	2	Write response. This signal indicates the status of the write transaction

Pin Name	Direction	Width (Bits)	Description
axi_slv_buser_o	Out	AXI_USER_WIDTH	User signals. AXI4: Optional
axi_slv_bready_i	In	1	Response ready. This signal indicates that the master can accept a write response
axi_slv_arvalid_i	In	1	Read address valid. This signal indicates that the channel is signaling valid read address and control information
axi_slv_araddr_i	In	32	Read address. The read address gives the address of the first transfer in a read burst transaction
axi_slv_arsize_i	In	3	Burst size. This signal indicates the size of each transfer in the burst.
axi_slv_arburst_i	In	2	Burst type. The burst type and the size information determine how the address for each transfer within the burst is calculated.
axi_slv_arlen_i	In	8	AXI read burst length. This indicates the number of beats per AXI burst
axi_slv_arid_i	In	AXI_ID_WIDTH	AXI read address ID width.
axi_slv_arlock_i	In	1	Lock type. AXI4: Optional
axi_slv_arcache_i	In	4	Memory type. AXI4: Optional
axi_slv_arprot_i	In	3	Protection type AXI4: Optional
axi_slv_arqos_i	In	4	Quality of Service. AXI4: Optional
axi_slv_arregion_i	In	4	Region AXI4: Optional
axi_slv_aruser_i	In	AXI_USER_WIDTH	User signals. AXI4: Optional
axi_slv_arready_o	Out	1	Read address ready. This signal indicates that the slave is ready to accept an address and associated control signals
axi_slv_rvalid_o	Out	1	Read valid.
axi_slv_rdata_o	Out	AXI_AHB_DATA_WIDTH	Read data.
axi_slv_ruser_o	Out	AXI_USER_WIDTH	User signals. AXI4: Optional
axi_slv_rlast_o	Out	1	Read last. This signal indicates the last transfer in a read burst.
axi_slv_rresp_o	Out	2	Read response. This signal indicates the status of the read transaction
axi_slv_rready_i	In	1	Read ready. This signal indicates that the master can accept the read data and response information
AHB-Lite Interface (AHBL_M)			
ahb_mas_sel_o	Out	1	AHB-Lite slave select.
ahb_mas_addr_o	Out	32	This is the AHB address bus width.
ahb_mas_write_o	Out	1	Indicates the transfer direction, this signal indicates an AHB write access when High and an AHB read access when Low
ahb_mas_wdata_o	Out	AXI_AHB_DATA_WIDTH	Write data. The write data bus transfers data from the master to the slaves during write operations. Width of the port can be 32/64-bit.
ahb_mas_size_o	Out	3	AHB Size of Transfer

Pin Name	Direction	Width (Bits)	Description
ahb_mas_trans_o	Out	2	AHB Transfer Type, which can be NONSEQUENTIAL, SEQUENTIAL, IDLE, or BUSY.
ahb_mas_prot_o	Out	4	Protection type. Indicates the normal, privileged transaction and whether the transaction is a data access or an instruction access. ahb_mas_prot_o is driven with {1'b0, axi_slv_axprot_i}.
ahb_mas_mastlock_o	Out	1	Indicates that the current master is performing a locked sequence of transfers.
ahb_mas_burst_o	Out	3	AHB Burst type. The burst type indicates if the transfer is a single transfer or forms part of a burst. The burst can be incrementing or wrapping.
ahb_mas_ready_o	Out	1	AHB master ready.
ahb_mas_ready_i	In	1	Ready. The AHB slave uses this signal to extend an AHB transfer.
ahb_mas_rdata_i	In	AXI_AHB_DATA_WIDTH	AHB read data driven by slave. Width of the port can be 32/64-bit.
ahb_mas_resp_i	In	1	Transfer Response. When Low, indicates that the transfer status is OKAY. When High, indicates that the transfer status is ERROR.

2.3. Attributes

Table 2.2 provides the list of user-configurable attributes for the AXI4 to AHB-Lite Bridge Module. The attribute values arespecified using the IP core Configuration user interface in the Propel Builder software as shown in Figure 2.3 .

Table 2.2. Attribute Table

Attribute Name	Description
General settings Tab	
AXI_AHB data bus width	Specifies the bit width of AXI and AHB data bus signals.
AXI ID width	Specifies the bit width of AXI ID signals.
AXI user width	Specifies the bit width of AXI user signals.

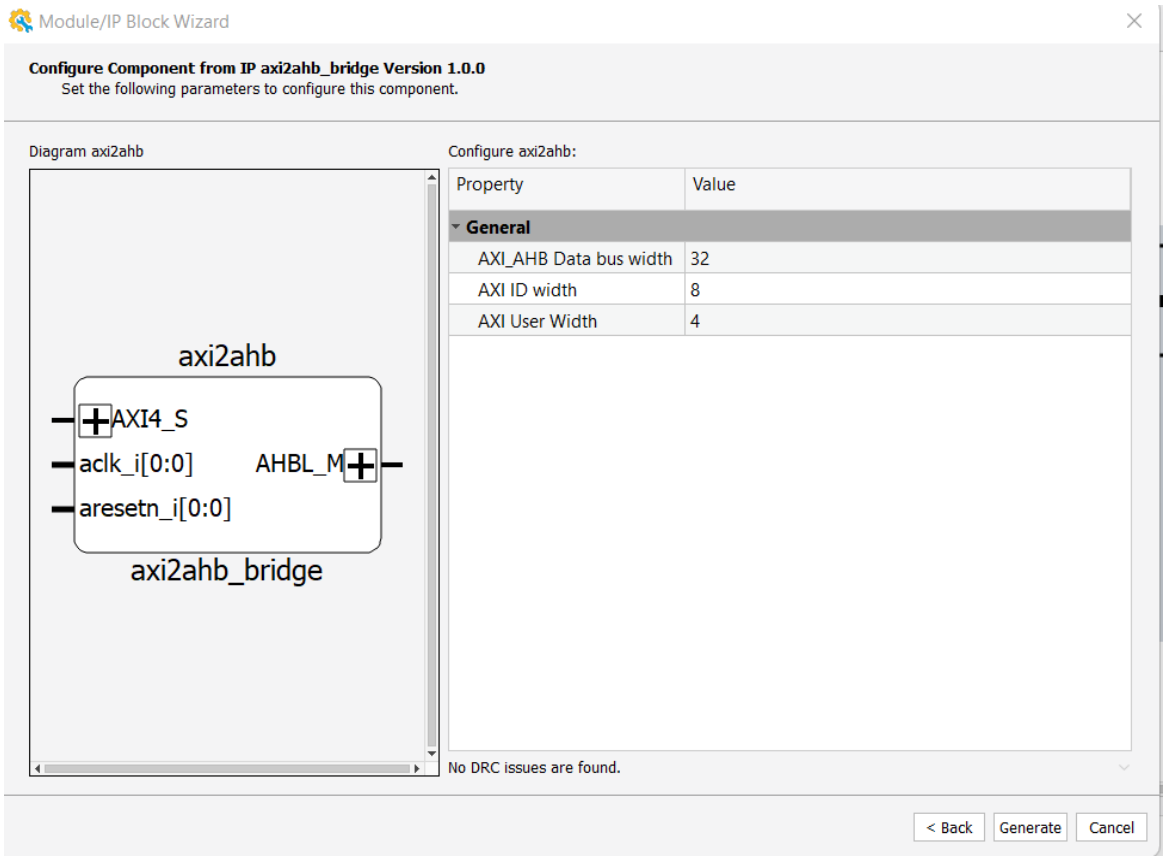

Figure 2.3. AXI4 to AHB-Lite Bridge Module Interface Diagram

Table 2.3. Attribute Name

Attribute Name	Attribute ID	Selectable Values	Default	Dependency on Other Attributes
General Settings tab				
AXI_AHB data bus width	AXI_AHB_DATA_WIDTH	8,16,32,64,128, 256,512,1024	32	-
AXI ID width	AXI_ID_WIDTH	1 to 11	8	-
AXI user width	AXI_USER_WIDTH	1-128	4	-

References

- Certus-Pro NX Web page in latticesemi.com
- AMBA 4 AXI Protocol Specification- “IHI0022H_c_amba_axi_protocol_spec”
- AMBA 3 AHB-Lite protocol specification

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.0, May 2022

Section	Change Summary
All	Initial release

www.latticesemi.com