AXI4 to APB Bridge Module - Lattice Propel Builder

User Guide

FPGA-IPUG-02198-1.0

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
AMBA	Advanced Micro-controller Bus Architecture
AXI	Advanced Extensible Interface Bus
APB	Advanced Peripheral Bus
FPGA	Field Programmable Gate Array
RTL	Register Transfer Level

1. Introduction

The Lattice Semiconductor AXI to APB Bridge Module provides an interface between the high-speed AXI and APB.

The design is implemented in Verilog HDL. The IP can be configured and based on Table 1.1.

Table 1.1. FPGA Software for IP Configuration, Generation, and Implementation

Supported FPGA Family	IP Configuration and Generation	IP Implementation (Synthesis, Map, Place and Route)
Certus Pro-NX	Lattice Propel Builder software	Lattice Radiant software

1.1. Features

The key features of the AXI4 to APB Bridge Module include:

- Compliance with AMBA AXI4 and APB3 Protocol
- Support configurable data bus width: 8,16 and 32
- Support configurable AXI4 ID width: 1 to 11
- Support configurable AXI4 User width: 1 to 128
- Support of AXI4 INCR burst
- Support 32-bit Address width.
- Number of supported APB slave is one
- Registered output

1.2. Assumptions:

- AxQOS, AxREGION, AxCACHE, AxLOCK and AxPROT are considered as don't care.
- AxUSER is passed back as such in the write and read response channels.
- AXI4 wrap and fixed burst not supported
- AXI4 unaligned address is passed as such to the external APB slave during write and read. Based on the implementation of unaligned address in the external APB slave, the data read back from APB slave is passed as such to the AXI4 external master.

2. Functional Descriptions

2.1. Overview

The Lattice Semiconductor AXI4 to APB Bridge core is to connect AXI4 master to APB slave. Read and write transfers on AXI bus are converted into corresponding transfers on the APB.

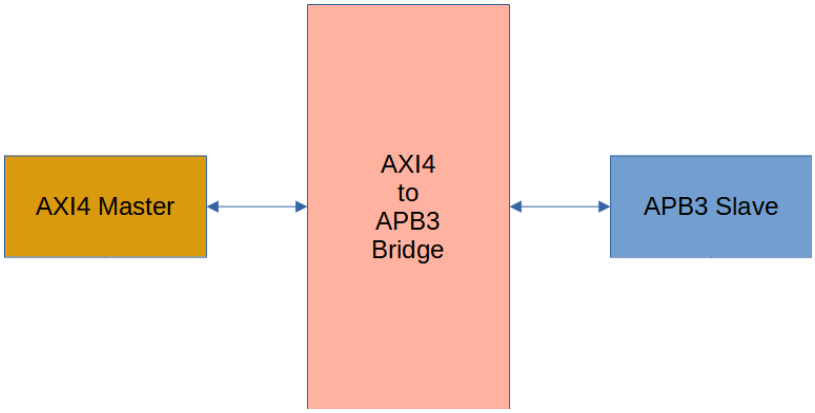

Figure 2.1. AXI4 to APB Bridge

Figure 2.2 shows the interface diagram of the AXI4 to APB Bridge Module. The diagram shows all the available ports for the IP core.

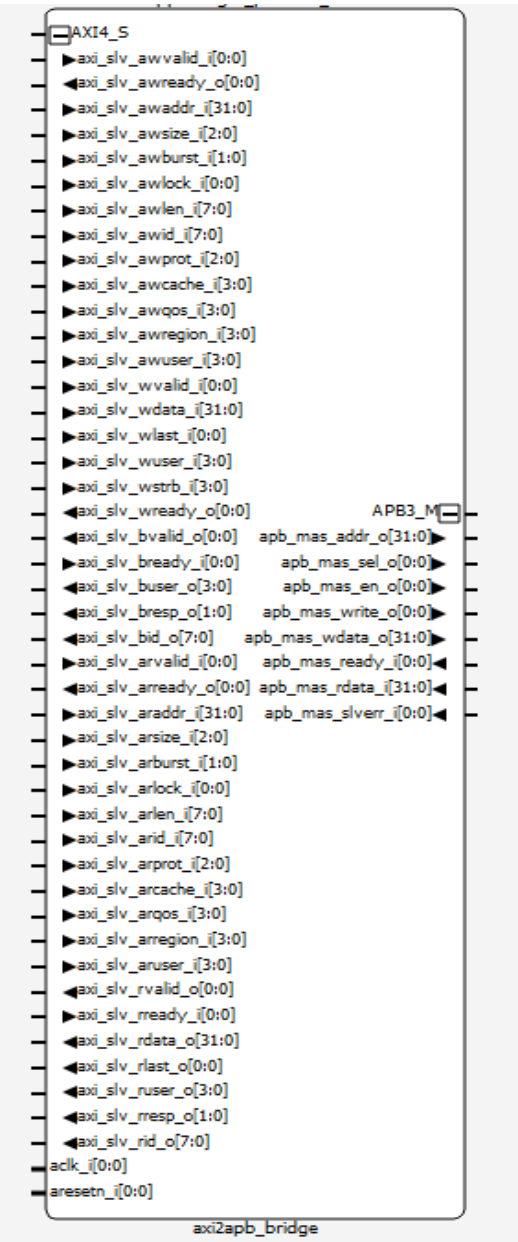

Figure 2.2. AXI4 to APB Bridge Module Interface Diagram

Table 2.1. AXI4 to APB Bridge Module Signal Description

Pin Name	Direction	Width (Bits)	Description
Clock and reset			
aclk_i	In	1	AXI4 to APB bridge clock.
aresetn_i	In	1	Active low reset.

Pin Name	Direction	Width (Bits)	Description
AXI4 slave Interface			
axi_slv_awvalid_i	In	1	Write address valid. This signal indicates that the channel is signaling valid write address and control information.
axi_slv_awaddr_i	In	32	Write address. The write address gives the address of the first transfer in a write burst transaction
axi_slv_awsize_i	In	3	Burst size. This signal indicates the size of each transfer in the burst
axi_slv_awburst_i	In	2	Burst type. The burst type and the size information, determine how the address for each transfer within the burst is calculated
axi_slv_awlen_i	In	8	Burst length. This indicates the number of beats per AXI burst.
axi_slv_awid_i	In	AXI_ID_WIDTH	AXI write ID width.
axi_slv_awlock_i	In	1	Lock type. AXI4: Optional
axi_slv_awcache_i	In	4	Memory type. AXI4: Optional
axi_slv_awprot_i	In	3	Protection type AXI4: Optional
axi_slv_awqos_i	In	4	Quality of Service. AXI4: Optional
axi_slv_awregion_i	In	4	Region AXI4: Optional
axi_slv_awuser_i	In	AXI_USER_WIDTH	User signals. AXI4: Optional
axi_slv_awready_o	Out	1	Write address ready. This signal indicates that the slave is ready to accept an address and associated control signals
axi_slv_wvalid_i	In	1	Write valid. This signal indicates that valid write data and strobes are available
axi_slv_wdata_i	In	AXI_APB_DATA_WIDTH	Write data.
axi_slv_wlast_i	In	1	Write last. This signal indicates the last transfer in a write burst
axi_slv_wstrb_i	In	AXI_APB_DATA_WIDTH/8	Write strobes. This signal indicates which byte lanes hold valid data. There is one write strobe bit for each eight bits of the write data bus

Pin Name	Direction	Width (Bits)	Description
axi_slv_wuser_i	In	AXI_USER_WIDTH	AXI write user width.
axi_slv_wready_o	Out	1	Write data ready. This signal indicates that the slave is ready to accept write data.
axi_slv_bvalid_o	Out	1	Write response valid. This signal indicates that the channel is signaling a valid write response
axi_slv_bid_o	Out	AXI_ID_WIDTH	Write response ID.
axi_slv_buser_o	Out	AXI_USER_WIDTH	Write response User signal.
axi_slv_bresp_o	Out	2	Write response. This signal indicates the status of the write transaction
axi_slv_bready_i	In	1	Response ready. This signal indicates that the master can accept a write response
axi_slv_arvalid_i	In	1	Read address valid. This signal indicates that the channel is signaling valid read address and control information
axi_slv_araddr_i	In	32	Read address. The read address gives the address of the first transfer in a read burst transaction
axi_slv_arsize_i	In	3	Burst size. This signal indicates the size of each transfer in the burst.
axi_slv_arburst_i	In	2	Burst type. The burst type and the size information determine how the address for each transfer within the burst is calculated.
axi_slv_arlen_i	In	8	AXI read burst length. This indicates the number of beats per AXI burst
axi_slv_arid_i	In	AXI_ID_WIDTH	AXI read address ID width.
axi_slv_arlock_i	In	1	Lock type. AXI4: Optional
axi_slv_arcache_i	In	4	Memory type. AXI4: Optional
axi_slv_arprot_i	In	3	Protection type AXI4: Optional
axi_slv_arqos_i	In	4	Quality of Service. AXI4: Optional
axi_slv_arregion_i	In	4	Region AXI4: optional
axi_slv_aruser_i	In	AXI_USER_WIDTH	User signals. AXI4: Optional

Pin Name	Direction	Width (Bits)	Description
axi_slv_arready_o	Out	1	Read address ready. This signal indicates that the slave is ready to accept an address and associated control signals
axi_slv_rvalid_o	Out	1	Read valid. This signal indicates that the channel is signaling the required read data
axi_slv_rdata_o	Out	AXI_APB_DATA_WIDTH	Read data.
axi_slv_rresp_o	Out	2	Read response. This signal indicates the status of the read transfer
axi_slv_ruser_o	Out	AXI_USER_WIDTH	User signals. AXI4
axi_slv_rid_o	Out	AXI_ID_WIDTH	AXI read data ID width.
axi_slv_rlast_o	Out	1	Read last. This signal indicates the last transfer in a read burst.
axi_slv_rready_i	In	1	Read ready. This signal indicates that the master can accept the read data and response information
APB Master Interface			
apb_mas_sel_o	Out	1	APB Select. It indicates slave device is selected and that data transfer is required
apb_mas_en_o	Out	1	APB Enable.
apb_mas_addr_o	Out	32	Address. This is the APB address bus. It can be up to 32 bits wide and is driven by the peripheral bus bridge unit.
apb_mas_write_o	Out	1	APB transfer Direction. This signal indicates an APB write access when High and APB read access when Low
apb_mas_wdata_o	Out	AXI_APB_DATA_WIDTH	APB write data. This bus is driven during write operation
apb_mas_ready_i	In	1	APB Ready. slave use this signal to extend the APB transfer
apb_mas_rdata_i	In	AXI_APB_DATA_WIDTH	APB read data. The selected slave drives this bus during read cycles when Write is LOW.
apb_mas_slverr_i	In	1	APB slave error response. This signal indicates transfer failure.

2.2. Attributes

Table 2.2 provides the list of user-configurable attributes for the AXI4 to APB Bridge Module. The attribute values are specified using the IP core Configuration user interface in the Propel Builder software as shown in Figure 2.3.

Table 2.2. Attribute Table

Attribute Name	Attribute ID	Selectable Values	Default	Dependency on Other Attributes
General Settings tab				
AXI_APB Data width	AXI_APB_DATA_WIDTH	8,16,32	32	-
AXI User width	AXI_USER_WIDTH	1-128	4	-
AXI ID width	AXI_ID_WIDTH	1-11	8	-

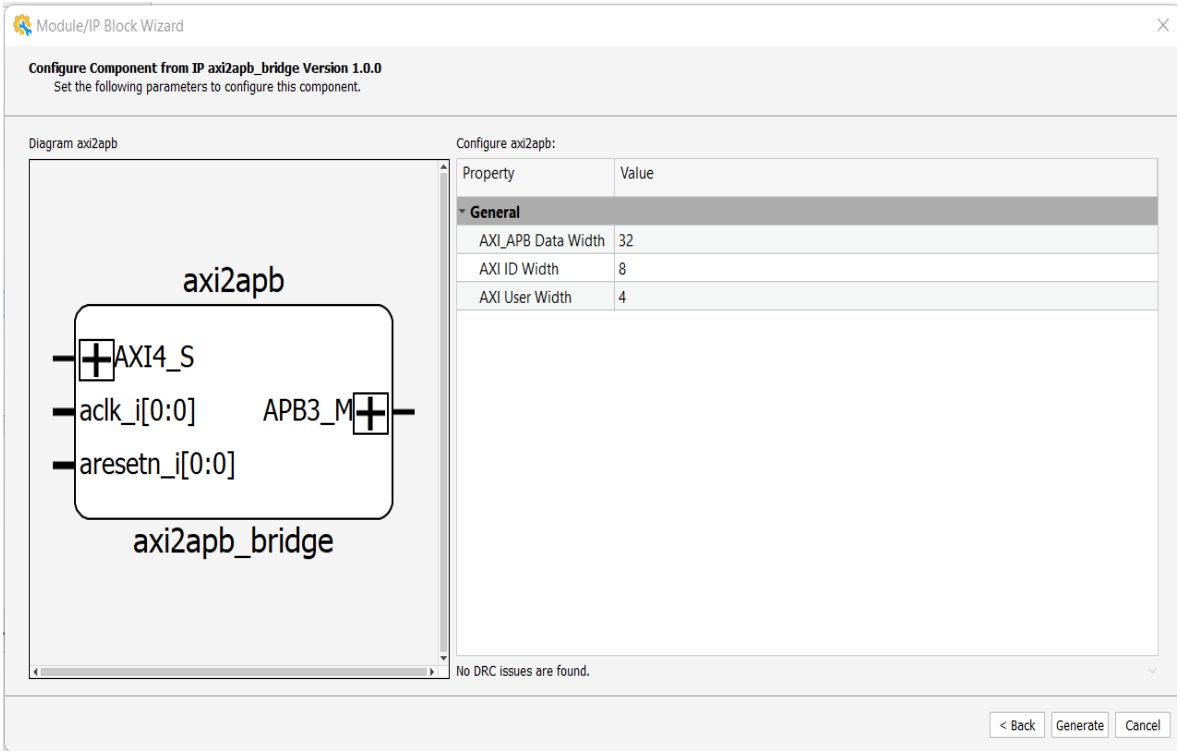

Figure 2.3. AXI4 to APB Bridge Module Configuration User

Table 2.3. Attribute Name

Attribute Name	Description
General Settings Tab	
AXI_APB Data width	This mentions the data bus width of both AXI and APB bus.
AXI User width	This decides the width of AXI user signals (AWUSER, WUSER, BUSER, ARUSER and RUSER)
AXI ID width	This decides the width of AXI AWID, ARID, BID and RID signals.

References

- Lattice Propel 1.0 User Guide
- Certus-Pro NX Web page in latticesemi.com
- AMBA 4 AXI Protocol Specification- “IHI0022H_c_amba_axi_protocol_spec”
- AMBA 3 APB Protocol Specification

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.0, May 2022

Section	Change Summary
All	Initial release

www.latticesemi.com