AXI4 Interconnect Module - Lattice Propel Builder

User Guide

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
AXI	Advanced Extensible Interface
AMBA	Advanced Microcontroller Bus Architecture
FPGA	Field Programmable Gate Array
RTL	Register Transfer Level

1. Introduction

This document provides technical information about AXI Interconnect Module and aims to provide information essential for IP/system developers, verification, and software for integration, testing, and validation.

In general, this document covers design specification from RTL to IP packaging and details the procedures for IP generation and integration.

The design is implemented in System Verilog HDL. The IP can be configured and based on Table 1.1.Table_1_1

Table 1.1. FPGA Software for IP Configuration, Generation, and Implementation

Supported FPGA Family	IP Configuration and Generation	IP Implementation (Synthesis, Map, Place and Route)
Certus Pro-NX	Lattice Propel Builder software	Lattice Radiant software

1.1. Features

The key features of the AXI Interconnect Module include:

- Compliance with AMBA AXI4 and AXI4-Lite Protocol
- Fully parameterized design
- Connect multiple AXI4 masters to multiple memory-mapped AXI4 slaves
- Support of up to 32 AXI4 (or AXI4-Lite) masters and 32 AXI4 (or AXI4-Lite) slaves
- Heterogeneous support - AXI4 and AXI4-lite in single interconnect.
- Configurable data bus width for each interface
- AXI4: 8,16,32, 64, 128, 256, 512, or 1024 width
- AXI4-Lite: 32 or 64 bits
- Address width up to 64-bits [13 to 64]
- Supports AXI4 INCR and FIXED bursts.
- Automatic conversion between interfaces with different data widths.
- Support multiple clock domains
- Automatic conversion for the transactions between interfaces with different clocks.
- Clock domain crossing could be enabled/disabled for each interface.
- Support of fragmented address space of up to eight fragments per external slave
- Full connection between masters and slaves
- External slave side arbitration
- Selectable arbitration scheme:
- Round robin
- Strict priority (Fixed Priority)

1.2. Limitations

- No wrap burst support
- During AXI4 external master request:
- AxQOS, AxREGION, AxUSER, AxCACHE, AxLOCK are ignored while passing to external AXI4-lite slave interface.
- AxQOS, AxREGION, AxUSER, AxCACHE, AxLOCK and AxPROT are passed through as such while passing to external AXI4 slave interface

2. Functional Description

2.1. Overview

The Lattice Semiconductor AXI4 Interconnect is a flexible, versatile and easy-to-use IP with high-performance and low latency interconnect fabric for AMBA 4 AXI/AXI-lite based systems. Any AXI4/AXI4-lite compliant IP can be easily plug-and-play into the system for smooth integration. It supports different data width conversion and clock-domain-crossing. Furthermore, it supports multiple masters with multiple memory-mapped slaves.

It supports AXI OKAY, DECERR (when undefined external slave address region is accessed) and SLVERR (pass through from the external slave) responses.

AXI Interconnect implements the features required for high-performance and low latency systems including:

- Multiple channels
- Single-clock edge operation
- Non-tristate implementation
- Burst transfers in AXI4 interface: INCR burst (1 to 256 beats/burst), Fixed burst (1 to 16 transfers) as per the protocol.
- Wide data bus configurations: 8, 16, 32, 64, 128, 256, 512, or 1024 bits wide for AXI4 interface
- 32 or 64 for AXI4-Lite interface.

Refer to the AMBA 4 AXI Protocol Specification- IHI0022H_c_amba_axi_protocol_spec for more information about the protocol.

AXI Interconnect can be cascaded to implement multi-layer hierarchical interconnect to support large number of masters and slaves. Each master is considered to be on its own layer and isolated from each other, but can share access to the slaves. Each master can access different slaves in parallel. When more than one master tries to access the same slave, external slave-side arbitration is performed by the multi-layer interconnect.

Each port can be configured to support either AXI4 or AXI4-Lite.

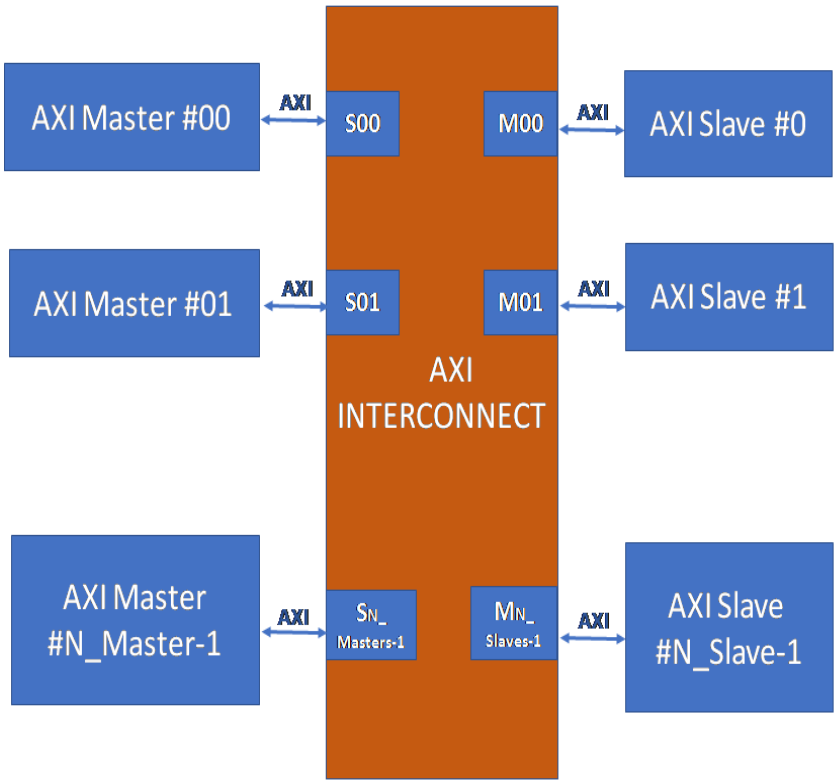

Figure 2.1. AXI Interconnect

2.2. Signal Description

Figure 2.1 shows the interface diagram for the AXI Interconnect Module. The diagram shows all of the available ports for the IP core (except Clock domain crossing clock and reset ports).

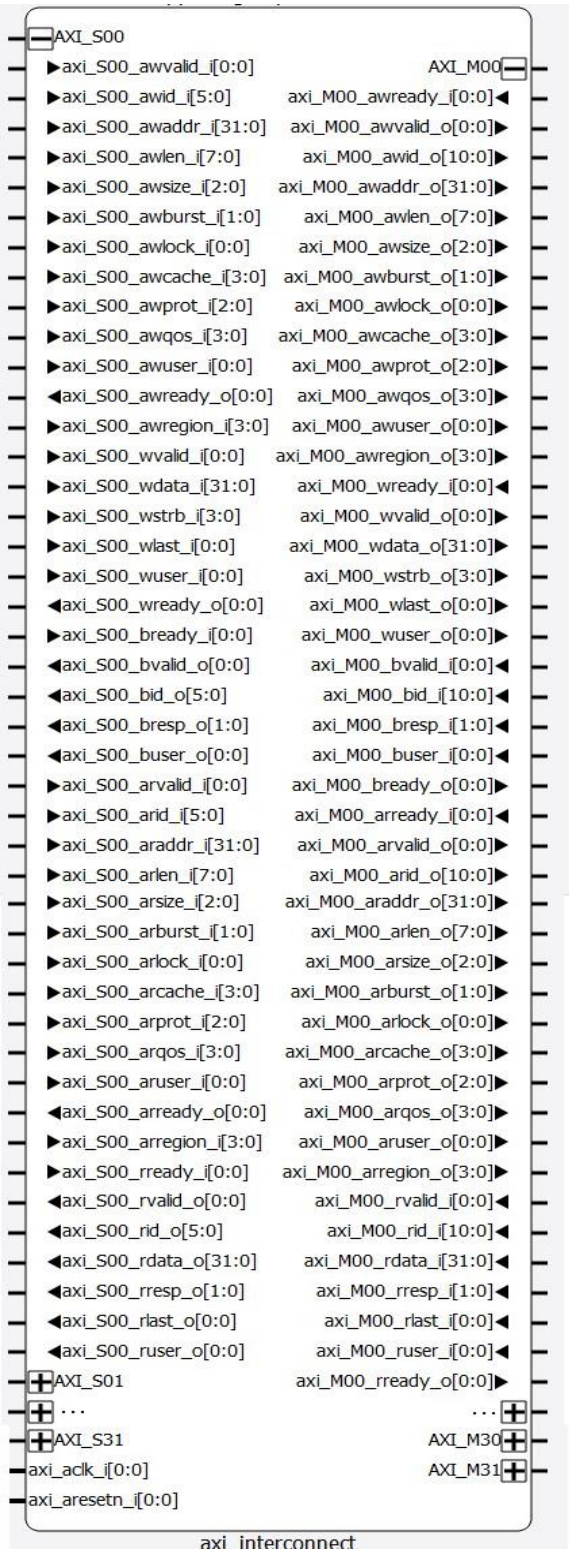

Figure 2.2. AXI Interconnect Module Interface Diagram

Table 2.1. AXI Interconnect Module Signal Description

Pin Name	Direction	Width (Bits)	Description
Clock and Reset			
axi_aclk_i	In	1	AXI clock to AXI Interconnect
axi_aresetn_i	In	1	AXI active LOW reset
AXI Interconnect Slave 00 clock and reset (available if CDC is enabled for this port S00)			
axi_S00_aclk_i**(AL)**	In	1	Input clock to AXI interconnected slave 00 port. It is required only when CDC is enabled for external master 00 port.
axi_S00_aclken_i**(AL)**	In	1	Input clock enable to AXI interconnected slave 00 port. It is required only when CDC is enabled for external master 00 port.
axi_S00_aresetn_i**(AL)**	In	1	Input AXI active Low reset to AXI interconnected slave 00 port. It is required only when CDC is enabled for external master 00 port.
AXI Interconnect Slave xx clock and reset (available if CDC is enabled for this port Sxx)			
axi_Sxx_aclk_i**(AL)**	In	1	Input clock to AXI interconnected slave xx port. It is required only when CDC is enabled for external master xx port.
axi_Sxx_aclken_i**(AL)**	In	1	Input clock enable to AXI interconnected slave xx port. It is required only when CDC is enabled for external master xx port.
axi_Sxx_aresetn_i**(AL)**	In	1	Input AXI active Low reset to AXI interconnected slave xx port. It is required only when CDC is enabled for external master xx port.
AXI Interconnect Slave 00 Interface - connected to external Master 00			
axi_S00_awvalid_i**(AL)**	In	1	Write address valid.
axi_S00_awid_i	In	EXT_MAS_AXI_ID_WIDTH	Write address ID. AXI4: Optional AXI4-Lite: N/A
axi_S00_awaddr_i**(AL)**	In	EXT_MAS_MAX_AXI_ADDR_WIDTH	Write address.
axi_S00_awlen_i	In	8	Burst length, the exact number of transfers in a burst. AXI4: Optional AXI4-Lite: N/A
axi_S00_awsize_i	In	3	Burst size, the size of each transfer in the burst. AXI4: Optional AXI4-Lite: N/A
axi_S00_awburst_i	In	2	Burst type. AXI4: Optional AXI4-Lite: N/A
axi_S00_awlock_i	In	1	Lock type. AXI4: Optional AXI4-Lite: N/A
axi_S00_awcache_i	In	4	Memory type. AXI4: Optional AXI4-Lite: N/A
axi_S00_awprot_i**(AL)**	In	3	Protection type
axi_S00_awqos_i	In	4	Quality of Service. AXI4: Optional AXI4-Lite: N/A

Pin Name	Direction	Width (Bits)	Description
axi_S00_awregion_i	In	4	Region AXI4: required AXI4-Lite: N/A
axi_S00_awuser_i	In	AXI_USER_WIDTH	User signals. AXI4: Optional AXI4-Lite: N/A
axi_S00_awready_o(AL)	Out	1	Write address ready.
axi_S00_wvalid_i(AL)	In	1	Write valid.
axi_S00_wdata_i(AL)	In	EXT_MAS_MAX_AXI_DATA_WIDTH	Write data.
axi_S00_wstrb_i(AL)	In	EXT_MAS_MAX_AXI_DATA_WIDTH/8	Write strobes.
axi_S00_wlast_i	In	1	AXI4 Last write beat/burst. AXI4: Optional AXI4-Lite: N/A
axi_S00_wuser_i	In	AXI_USER_WIDTH	User signal. AXI4: Optional AXI4-Lite: N/A
axi_S00_wready_o(AL)	Out	1	Write ready.
axi_S00_bvalid_o(AL)	Out	1	Write response valid.
axi_S00_bid_o	Out	EXT_MAS_AXI_ID_WIDTH	AXI4: required. AXI4-lite: N/A
axi_S00_bresp_o(AL)	Out	2	Write response.
axi_S00_buser_o	Out	AXI_USER_WIDTH	User signal. AXI4: Optional AXI4-Lite: N/A
axi_S00_bready_i(AL)	In	1	Response ready.
axi_S00_arvalid_i(AL)	In	1	Read address valid.
axi_S00_arid_i	In	EXT_MAS_AXI_ID_WIDTH	Read address ID. AXI4: Optional AXI4-Lite: N/A
axi_S00_araddr_i(AL)	In	EXT_MAS_MAX_AXI_ADDR_WIDTH	Read address.
axi_S00_arlen_i	In	8	Burst length. AXI4: Optional AXI4-Lite: N/A
axi_S00_arsize_i	In	3	Burst size. AXI4: Optional AXI4-Lite: N/A
axi_S00_arburst_i	In	2	Burst type. AXI4: Optional AXI4-Lite: N/A
axi_S00_arlock_i	In	1	Lock type. AXI4: Optional AXI4-Lite: N/A
axi_S00_arcache_i	In	4	Memory type. AXI4: Optional AXI4-Lite: N/A
axi_S00_arprot_i(AL)	In	3	Protection type.

Pin Name	Direction	Width (Bits)	Description
axi_S00_arqos_i	In	4	Quality of Service. AXI4: Optional AXI4-Lite: N/A
axi_S00_arregion_i	In	4	Region AXI4: required AXI4-Lite: N/A
axi_S00_aruser_i	In	AXI_USER_WIDTH	User signal. AXI4: Optional AXI4-Lite: N/A
axi_S00_arready_o(AL)	Out	1	Read address ready.
axi_S00_rvalid_o(AL)	Out	1	Read valid.
axi_S00_rid_o	Out	EXT_MAS_AXI_ID_WIDTH	Read ID. AXI4: required AXI4-Lite: N/A
axi_S00_rdata_o(AL)	Out	EXT_MAS_MAX_AXI_DATA_WIDTH	Read data.
axi_S00_rresp_o(AL)	Out	2	Read response.
axi_S00_rlast_o	Out	1	Last read. AXI4: required AXI4-Lite: N/A
axi_S00_ruser_o	Out	AXI_USER_WIDTH	User signal. AXI4: Optional AXI4-Lite: N/A
axi_S00_rready_i(AL)	In	1	Read ready.
AXI Interconnect Slave xx Interface - connected to external Master xx			
axi_Sxx_awvalid_i(AL)	In	1	Write address valid.
axi_Sxx_awid_i	In	EXT_MAS_AXI_ID_WIDTH	Write address ID. AXI4: Optional AXI4-Lite: N/A
axi_Sxx_awaddr_i(AL)	In	EXT_MAS_MAX_AXI_ADDR_WIDTH	Write address.
axi_Sxx_awlen_i	In	8	Burst length, the exact number of transfers in a burst. AXI4: Optional AXI4-Lite: N/A
axi_Sxx_awsize_i	In	3	Burst size, the size of each transfer in the burst. AXI4: Optional AXI4-Lite: N/A
axi_Sxx_awburst_i	In	2	Burst type. AXI4: Optional AXI4-Lite: N/A
axi_Sxx_awlock_i	In	1	Lock type. AXI4: Optional AXI4-Lite: N/A
axi_Sxx_awcache_i	In	4	Memory type. AXI4: Optional AXI4-Lite: N/A
axi_Sxx_awprot_i(AL)	In	3	Protection type
axi_Sxx_awqos_i	In	4	Quality of Service. AXI4: Optional AXI4-Lite: N/A

Pin Name	Direction	Width (Bits)	Description
axi_Sxx_awregion_i	In	4	Region AXI4: required AXI4-Lite: N/A
axi_Sxx_awuser_i	In	AXI_USER_WIDTH	User signals. AXI4: Optional AXI4-Lite: N/A
axi_Sxx_awready_o(AL)	Out	1	Write address ready.
axi_Sxx_wvalid_i(AL)	In	1	Write valid.
axi_Sxx_wdata_i(AL)	In	EXT_MAS_MAX_AXI_DATA_WIDTH	Write data.
axi_Sxx_wstrb_i(AL)	In	EXT_MAS_MAX_AXI_DATA_WIDTH/8	Write strobes.
axi_Sxx_wlast_i	In	1	AXI4 Last write beat/burst. AXI4: Optional AXI4-Lite: N/A
axi_Sxx_wuser_i	In	AXI_USER_WIDTH	User signal. AXI4: Optional AXI4-Lite: N/A
axi_Sxx_wready_o(AL)	Out	1	Write ready.
axi_Sxx_bvalid_o(AL)	Out	1	Write response valid.
axi_Sxx_bid_o	Out	EXT_MAS_AXI_ID_WIDTH	AXI4: required. AXI4-lite: N/A
axi_Sxx_bresp_o(AL)	Out	2	Write response.
axi_Sxx_buser_o	Out	AXI_USER_WIDTH	User signal. AXI4: Optional AXI4-Lite: N/A
axi_Sxx_bready_i(AL)	In	1	Response ready.
axi_Sxx_arvalid_i(AL)	In	1	Read address valid.
axi_Sxx_arid_i	In	EXT_MAS_AXI_ID_WIDTH	Read address ID. AXI4: Optional AXI4-Lite: N/A
axi_Sxx_araddr_i(AL)	In	EXT_MAS_MAX_AXI_ADDR_WIDTH	Read address.
axi_Sxx_arlen_i	In	8	Burst length. AXI4: Optional AXI4-Lite: N/A
axi_Sxx_arsize_i	In	3	Burst size. AXI4: Optional AXI4-Lite: N/A
axi_Sxx_arburst_i	In	2	Burst type. AXI4: Optional AXI4-Lite: N/A
axi_Sxx_arlock_i	In	1	Lock type. AXI4: Optional AXI4-Lite: N/A
axi_Sxx_arcache_i	In	4	Memory type. AXI4: Optional AXI4-Lite: N/A
axi_Sxx_arprot_i(AL)	In	3	Protection type.

Pin Name	Direction	Width (Bits)	Description
axi_Sxx_arqos_i	In	4	Quality of Service. AXI4: Optional AXI4-Lite: N/A
axi_Sxx_arregion_i	In	4	Region AXI4: required AXI4-Lite: N/A
axi_Sxx_aruser_i	In	AXI_USER_WIDTH	User signal. AXI4: Optional AXI4-Lite: N/A
axi_Sxx_arready_o(AL)	Out	1	Read address ready.
axi_Sxx_rvalid_o(AL)	Out	1	Read valid.
axi_Sxx_rid_o	Out	EXT_MAS_AXI_ID_WIDTH	Read ID. AXI4: required AXI4-Lite: N/A
axi_Sxx_rdata_o(AL)	Out	EXT_MAS_MAX_AXI_DATA_WIDTH	Read data.
axi_Sxx_rresp_o(AL)	Out	2	Read response.
axi_Sxx_rlast_o	Out	1	Last read. AXI4: required AXI4-Lite: N/A
axi_Sxx_ruser_o	Out	AXI_USER_WIDTH	User signal. AXI4: Optional AXI4-Lite: N/A
axi_Sxx_rready_i(AL)	In	1	Read ready.
AXI Interconnect Master 00 clock and reset (available if CDC is enabled for this port M00)			
axi_M00_aclk_i(AL)	In	1	Input clock to AXI interconnected master 00 port. It is required only when CDC is enabled for external slave 00 port.
axi_M00_aclken_i(AL)	In	1	Input clock enable to AXI interconnected master 00 port. It is required only when CDC is enabled for external slave 00 port.
axi_M00_aresetn_i(AL)	In	1	Input AXI active Low reset to AXI interconnected master 00 port. It is required only when CDC is enabled for external slave 00 port.
AXI Interconnect Master yy clock and reset (available if CDC is enabled for this port Myy)			
axi_Myy_aclk_i(AL)	In	1	Input clock to AXI interconnected master yy port. It is required only when CDC is enabled for external slave yy port.
axi_Myy_aclken_i(AL)	In	1	Input clock enable to AXI interconnected master yy port. It is required only when CDC is enabled for external slave yy port.
axi_Myy_aresetn_i(AL)	In	1	Input AXI active Low reset to AXI interconnected master yy port. It is required only when CDC is enabled for external slave yy port.
AXI Interconnect Master 00 Interface - connected to external Slave 00			
axi_M00_awvalid_o(AL)	Out	1	Write address valid.
axi_M00_awid_o	Out	EXT_SLV_AXI_ID_WIDTH	Write address ID. AXI4: required AXI4-Lite: N/A

Pin Name	Direction	Width (Bits)	Description
axi_M00_awaddr_o(AL)	Out	EXT_SLV_MAX_AXI_ADDR_WIDTH	Write address.
axi_M00_awlen_o	Out	8	Burst length, the exact number of transfers in a burst. AXI4: required AXI4-Lite: N/A
axi_M00_awsize_o	Out	3	Burst size, the size of each transfer in the burst. AXI4: required AXI4-Lite: N/A
axi_M00_awburst_o	Out	2	Burst type. AXI4: required AXI4-Lite: N/A
axi_M00_awlock_o	Out	1	Lock type. AXI4: required AXI4-Lite: N/A
axi_M00_awcache_o	Out	4	Memory type. AXI4: required AXI4-Lite: N/A
axi_M00_awprot_o(AL)	Out	3	Protection type.
axi_M00_awqos_o	Out	4	Quality of Service. AXI4: required AXI4-Lite: N/A
axi_M00_awregion_o	Out	4	Region AXI4: required AXI4-Lite: N/A
axi_M00_awuser_o	Out	AXI_USER_WIDTH	User signals. AXI4: required AXI4-Lite: N/A
axi_M00_awready_i(AL)	In	1	Write address ready.
axi_M00_wvalid_o(AL)	Out	1	Write valid.
axi_M00_wdata_o(AL)	Out	EXT_SLV_MAX_AXI_DATA_WIDTH	Write data.
axi_M00_wstrb_o(AL)	Out	EXT_SLV_MAX_AXI_DATA_WIDTH/8	Write strobes.
axi_M00_wlast_o	Out	1	AXI4 Last write beat/burst AXI4: Optional AXI4-Lite: N/A
axi_M00_wuser_o	Out	EXT_SLV_MAX_USER_WIDTH	User signal. AXI4: required AXI4-Lite: N/A
axi_M00_wready_i(AL)	In	1	Write ready.
axi_M00_bvalid_i(AL)	In	1	Write response valid.
axi_M00_bid_i	In	EXT_SLV_AXI_ID_WIDTH	Write response ID AXI4: required. AXI4-lite: N/A
axi_M00_bresp_i(AL)	In	2	Write response.
axi_M00_buser_i	In	AXI_USER_WIDTH	User signal. AXI4: required AXI4-Lite: N/A
axi_M00_bready_o(AL)	Out	1	Response ready.
axi_M00_arvalid_o(AL)	Out	1	Read address valid.

Pin Name	Direction	Width (Bits)	Description
axi_M00_arid_o	Out	EXT_SLV_AXI_ID_WIDTH	Read address ID. AXI4: required AXI4-Lite: N/A
axi_M00_araddr_o(AL)	Out	EXT_SLV_MAX_AXI_ADDR_WIDTH	Read address.
axi_M00_arlen_o	Out	8	Burst length. AXI4: required AXI4-Lite: N/A
axi_M00_arsize_o	Out	3	Burst size. AXI4: required AXI4-Lite: N/A
axi_M00_arburst_o	Out	2	Burst type. AXI4: required AXI4-Lite: N/A
axi_M00_arlock_o	Out	1	Lock type. AXI4: required AXI4-Lite: N/A
axi_M00_arcache_o	Out	4	Memory type. AXI4: required AXI4-Lite: N/A
axi_M00_arprot_o(AL)	Out	3	Protection type.
axi_M00_arqos_o	Out	4	Quality of Service. AXI4: required AXI4-Lite: N/A
axi_M00_arregion_o	Out	4	Region AXI4: required AXI4-Lite: N/A
axi_M00_aruser_o	Out	AXI_USER_WIDTH	User signal. AXI4: required AXI4-Lite: N/A
axi_M00_arready_i(AL)	In	1	Read address ready.
axi_M00_rvalid_i(AL)	In	1	Read valid.
axi_M00_rid_i	In	EXT_SLV_AXI_ID_WIDTH	Read ID. AXI4: required AXI4-Lite: N/A
axi_M00_rdata_i(AL)	In	EXT_SLV_MAX_AXI_DATA_WIDTH	Read data.
axi_M00_rresp_i(AL)	In	2	Read response.
axi_M00_rlast_i	In	1	Last read. AXI4: required AXI4-Lite: N/A
axi_M00_ruser_i	In	AXI_USER_WIDTH	User signal. AXI4: Optional AXI4-Lite: N/A
axi_M00_rready_o(AL)	Out	1	Read ready.
AXI Interconnect Master yy Interface - connected to external Slave yy			
axi_Myy_awvalid_o(AL)	Out	1	Write address valid.
axi_Myy_awid_o	Out	EXT_SLV_AXI_ID_WIDTH	Write address ID. AXI4: required AXI4-Lite: N/A

Pin Name	Direction	Width (Bits)	Description
axi_Myy_awaddr_o(AL)	Out	EXT_SLV_MAX_AXI_ADDR_WIDTH	Write address.
axi_Myy_awlen_o	Out	8	Burst length, the exact number of transfers in a burst. AXI4: required AXI4-Lite: N/A
axi_Myy_awsize_o	Out	3	Burst size, the size of each transfer in the burst. AXI4: required AXI4-Lite: N/A
axi_Myy_awburst_o	Out	2	Burst type. AXI4: required AXI4-Lite: N/A
axi_Myy_awlock_o	Out	1	Lock type. AXI4: required AXI4-Lite: N/A
axi_Myy_awcache_o	Out	4	Memory type. AXI4: required AXI4-Lite: N/A
axi_Myy_awprot_o(AL)	Out	3	Protection type.
axi_Myy_awqos_o	Out	4	Quality of Service. AXI4: required AXI4-Lite: N/A
axi_Myy_awregion_o	Out	4	Region AXI4: required AXI4-Lite: N/A
axi_Myy_awuser_o	Out	AXI_USER_WIDTH	User signals. AXI4: required AXI4-Lite: N/A
axi_Myy_awready_i(AL)	In	1	Write address ready.
axi_Myy_wvalid_o(AL)	Out	1	Write valid.
axi_Myy_wdata_o(AL)	Out	EXT_SLV_MAX_AXI_DATA_WIDTH	Write data.
axi_Myy_wstrb_o(AL)	Out	EXT_SLV_MAX_AXI_DATA_WIDTH/8	Write strobes.
axi_Myy_wlast_o	Out	1	AXI4 Last write beat/burst. AXI4: Optional AXI4-Lite: N/A
axi_Myy_wuser_o	Out	EXT_SLV_MAX_USER_WIDTH	User signal. AXI4: required AXI4-Lite: N/A
axi_Myy_wready_i(AL)	In	1	Write ready.
axi_Myy_bvalid_i(AL)	In	1	Write response valid.
axi_Myy_bid_i	In	EXT_SLV_AXI_ID_WIDTH	Write response ID AXI4: required. AXI4-lite: N/A
axi_Myy_bresp_i(AL)	In	2	Write response.
axi_Myy_buser_i	In	AXI_USER_WIDTH	User signal. AXI4: required AXI4-Lite: N/A
axi_Myy_bready_o(AL)	Out	1	Response ready.
axi_Myy_arvalid_o(AL)	Out	1	Read address valid.

Pin Name	Direction	Width (Bits)	Description
axi_Myy_arid_o	Out	EXT_SLV_AXI_ID_WIDTH	Read address ID. AXI4: required AXI4-Lite: N/A
axi_Myy_araddr_o(AL)	Out	EXT_SLV_MAX_AXI_ADDR_WIDTH	Read address.
axi_Myy_arlen_o	Out	8	Burst length. AXI4: required AXI4-Lite: N/A
axi_Myy_arsize_o	Out	3	Burst size. AXI4: required AXI4-Lite: N/A
axi_Myy_arburst_o	Out	2	Burst type. AXI4: required AXI4-Lite: N/A
axi_Myy_arlock_o	Out	1	Lock type. AXI4: required AXI4-Lite: N/A
axi_Myy_arcache_o	Out	4	Memory type. AXI4: required AXI4-Lite: N/A
axi_Myy_arprot_o(AL)	Out	3	Protection type.
axi_Myy_arqos_o	Out	4	Quality of Service. AXI4: required AXI4-Lite: N/A
axi_Myy_arregion_o	Out	4	Region AXI4: required AXI4-Lite: N/A
axi_Myy_aruser_o	Out	AXI_USER_WIDTH	User signal. AXI4: required AXI4-Lite: N/A
axi_Myy_arready_i(AL)	In	1	Read address ready.
axi_Myy_rvalid_i(AL)	In	1	Read valid.
axi_Myy_rid_i	In	EXT_SLV_AXI_ID_WIDTH	Read ID. AXI4: required AXI4-Lite: N/A
axi_Myy_rdata_i(AL)	In	EXT_SLV_MAX_AXI_DATA_WIDTH	Read data.
axi_Myy_rresp_i(AL)	In	2	Read response.
axi_Myy_rlast_i	In	1	Last read. AXI4: required AXI4-Lite: N/A
axi_Myy_ruser_i	In	AXI_USER_WIDTH	User signal. AXI4: Optional AXI4-Lite: N/A
axi_Myy_rready_o(AL)	Out	1	Read ready.

Notes:

- xx refers to the number of external masters. Possible values [0, 1, …, Total external masters-1]
- yy refers to the number of external slaves. Possible values [0, 1, …, Total external slaves-1]
- AL- When the interface selected is AXI4-lite, only these signals will be part of the AXI4-Lite I/O interface.
- All AXI Master/Slave Interface are compliant with AXI4/AXI4-lite protocol.

Refer to the AMBA 4 AXI Protocol Specification- IHI0022H_c_amba_axi_protocol_spec for the timing diagrams and for more information about the protocol.

2.3. Attributes Summary

Table 2.2 provides the list of user-configurable attributes for the AXI Interconnect Module. The attribute values are specified using the IP core Configuration user interface in the Propel Builder software as shown in Table 2.2 .

Table 2.2. Attributes Table

Attribute Name	Selectable Values	Default	Dependency on Other Attributes
1. General Settings tab			
General			
Total External AXI4 Slaves	1–32	2	Total AXI4 Masters and Total AXI4 Slaves cannot be both 1
Total External AXI4 Masters	1–32	2	
AXI User width	1-128	1	AXI user width
Full Address Decoding up to 4kB	-	checked	-
2. External Master Settings Tab			
2.1 General			
External Master AXI ID width	1-6	6	External master AXI ID width.
AXI Master Max Address Width(bits)	13-64	32	External master maximum AXI address width. Holds maximum of the available external master's address bus width.
AXI Master Max Data Width(bits)	8, 16, 32, 64, 128, 256, 512,1024	32	External master maximum AXI data width. Holds maximum of the available external master's data bus width.
AXI Master Max no. of ID supports	1, 2, 4, 8, 16, 32, 64	64	External Master Maximum number of ID Support Holds maximum of the configured values for different external master.
2.2 External master access Type Settings			
External master AXI access Type <N>	0-2	2	External Master Access Type. Here, <N> = 0 to (Total External AXI4 masters -1) 0 - Write only port 1 - Read only port 2 - Write/Read port
2.3 External master protocol Settings			
External master AXI protocol <N>	AXI4, AXI4-lite	0	AXI protocol supported by the external master. Here, <N> = 0 to (Total External AXI4 masters -1) 0 - AXI4, 1 - AXI4-lite

Attribute Name	Selectable Values	Default	Dependency on Other Attributes
2.4 External master CDC enable Settings			
External master CDC enable <N>	0,1	0	External master CDC enable. Here, <N> = 0 to (Total External AXI4 masters -1) 1- Clock domain crossing enables for the connected external master <N> which is asynchronous to interconnect clock “axi_aclk_i”. 0- CDC is not required for external master<N>
2.5 External master Address Settings			
External master Address width<N>	13-64	32	External master Address width. Here, <N> = 0 to (Total External AXI4 masters -1)
2.6 External Master Data Settings			
External Master Data width <N>	8, 16, 32, 64, 128, 256, 512,1024	32	External master Data width. Here, <N> = 0 to (Total External AXI4 masters -1)
2.7 External Master No. of IDs Support settings			
External Master No. of IDs <N>	1, 2, 4, 8, 16, 32, 64	64	External Master ID’s Here, <N> = 0 to (Total External AXI4 masters -1) Reordering Depth 1: means single thread 2 or more: means multi-thread
2.8 External Master IDs order enable settings			
External Master ID order enable <N>	0,1	0	External Master ID order enable. Here, <N> = 0 to (Total External AXI4 masters -1) To be set to 1, when the external master <N> issues same ID to more than one external slave.
2.9 External master write accept settings			
External Master Write accept<N>	1-16	16	Number of Outstanding Write transactions accepted by external master <N> connected to the AXI interconnect. Here, <N> = 0 to (Total External AXI4 masters -1)

Attribute Name	Selectable Values	Default	Dependency on Other Attributes
2.10 External master read accept settings			
External Master Read accept<N>	1-16	16	Number of Outstanding read transactions accepted by external master<N> connected to the AXI interconnect. Here, <N> = 0 to (Total External AXI4 masters -1)
2.11 External master priority settings			
External Master Priority<N>	Round Robin, Fixed Priority	0	External master <N> priority scheme to choose responses from different external slaves (at write response channel and read response channel) Here, <N> = 0 to (Total External AXI4 masters -1)
2.12 External master 0 Fixed priority settings			
Ext Slave 0 Ext Master 0 Fixed Priority	0 to (Total External AXI4 slaves -1)	0	Ext Slave 0 Ext Master 0 Fixed Priority
….			
Ext Slave <M> Ext Master 0 Fixed Priority	0 to (Total External AXI4 slaves -1)	<M>	Ext Slave <M> Ext Master 0 Fixed Priority Here, <M> = 0 to (Total External AXI4 slaves -1)
2.13 External master <N> Fixed priority settings			
Ext Slave 0 Ext Master N Fixed Priority	0 to (Total External AXI4 slaves -1)	0	Ext Slave 0 Ext Master N Fixed Priority. Here, <N> = Total External AXI4 masters -1
….			
Ext Slave <M> Ext Master N Fixed Priority	0 to (Total External AXI4 slaves -1)	<M>	Ext Slave <M> Ext Master N Fixed Priority. Here, <M> = 0 to (Total External AXI4 slaves -1) Here, <N> = Total External AXI4 masters -1
3. External Slave Settings Tab			
3.1 General			
External Slave AXI ID width	1-6	6	External slave AXI ID width.
AXI Slave Max Address Width(bits)	13-64	32	External slave maximum AXI address width. Holds maximum of the available external slave's address bus width.
AXI Slave Max Data Width(bits)	8, 16, 32, 64, 128, 256, 512,1024	32	External slave maximum AXI data width. Holds maximum of the available external slave's data bus width.

Attribute Name	Selectable Values	Default	Dependency on Other Attributes
AXI Slave Max Fragment count	1-8	8	External Slave Max Fragment count Holds maximum of the available external slave's fragment count.
3.2 External slave access type settings			
External Slave Access Type <M>	0-2	2	External Slave Access Type. Here, <M> = 0 to Total External AXI4 slaves -1 0 - Write only port 1 - Read only port 2 - Write/Read port
3.3 External slave protocol type settings			
External Slave Protocol type <M>	AXI4, AXI4-lite	0	AXI protocol supported by the external slave. Here, <M> = 0 to Total External AXI4 slaves -1
3.4 External slave CDC enable settings			
External slave CDC Enable <M>	0,1	0	External slave CDC enable. Here, <M> = 0 to Total External AXI4 slaves -1 1- Clock domain crossing enables for the connected external slave <M> which is asynchronous to interconnect "axi_aclk_i". 0- CDC is not required for external slave<M>
3.5 External slave address settings			
External Slave Address width <M>	13-64	32	External slave Address width. Here, <M> = 0 to Total External AXI4 slaves -1
3.6 External slave data settings			
External Slave Data width <M>	8, 16, 32, 64, 128, 256, 512,1024	32	External slave Data width. Here, <M> = 0 to Total External AXI4 slaves -1
3.7 External slave write issue settings			
External Slave Write Issue <M>	1-16	16	Number of Outstanding Write transactions issue from each external slave <M> connected to the AXI interconnect. Here, <M> = 0 to Total External AXI4 slaves -1

Attribute Name	Selectable Values	Default	Dependency on Other Attributes
3.8 External slave read issue settings			
External Slave Read Issue <M>	1-16	16	Number of Outstanding read transactions issue from each external slave <M> connected to the AXI interconnect. Here, <M> = 0 to Total External AXI4 slaves -1
3.9 External slave fragment settings			
External slave <M> fragment count	1 to 8	8	External slave fragment count. Here, <M> = 0 to Total External AXI4 slaves -1
3.10 External slave 0 Base address settings			
Base address <F>	0 to ((2^ External Slave Address width 0) - 'h 1000)		Base address for external slave 0 Fragment <F> Here, <F> = 0 to (External slave 0 fragment count-1)
…			
3.11 External slave <M> Base address settings			
Base address <F>	0 to (2^ External Slave Address width <M>) - 'h 1000		Base address for external slave M Fragment <F> Here, <F> = 0 to (External slave M fragment count-1) Here, <M> = Total External AXI4 slaves-1
3.12 External slave 0 End address settings			
End address <F> (1)	'h FFF - (2^ External Slave Address width 0)		End address for external slave 0 Fragment <F> Here, <F> = 0 to (External slave 0 fragment count-1)
…			
3.13 External slave <M> End address settings			
End address <F> (1)	'h FFF - (2^ External Slave Address width 0)		End address for external slave N Fragment <F> Here, <F> = 0 to (External slave M fragment count-1) Here, <M> = Total External AXI4 slaves-1

Attribute Name	Selectable Values	Default	Dependency on Other Attributes
3.14 External slave priority settings			
External Slave Priority <M>	Round Robin, Fixed Priority	0	External slave <M> priority scheme to choose request from different external masters (at write address and read address channel) Here, <M> = 0 to Total External AXI4 slaves -1
3.15 External slave 0 Fixed priority settings			
Ext Master 0 Ext Slave 0 Fixed Priority	0 to (Total External AXI4 masters -1)	0	Ext Master 0 Ext Slave 0 Fixed Priority
….			
Ext Master <N> Ext Slave 0 Fixed Priority	0 to (Total External AXI4 masters -1)	<N>	Ext Master <N> Ext Slave 0 Fixed Priority Here, <N> = 0 to (Total External AXI4 masters -1)
3.16 External slave <M> Fixed priority settings			
Ext Master 0 Ext Slave M Fixed Priority	0 to (Total External AXI4 masters -1)	0	Ext Master 0 Ext Slave <M> Fixed Priority Here, <M> = Total External AXI4 slaves-1
….			
Ext Master <N> Ext Slave M Fixed Priority	0 to (Total External AXI4 masters -1)	<N>	Ext Master <N> Ext Slave <M> Fixed Priority Here, <M> = Total External AXI4 slaves-1 Here, <N> = 0 to (Total External AXI4 masters -1)

Note:

1. Minimum size for each of the external slave fragments must be a multiple of 4KB.
   Example:
   - Slave 0 fragment 0 base address = ‘h0000
   - Slave 0 fragment 0 end address = ‘h0FFF
   - Slave 0 fragment 1 base address = ‘h1000
   - Slave 0 fragment 1 end address = ‘h1FFF

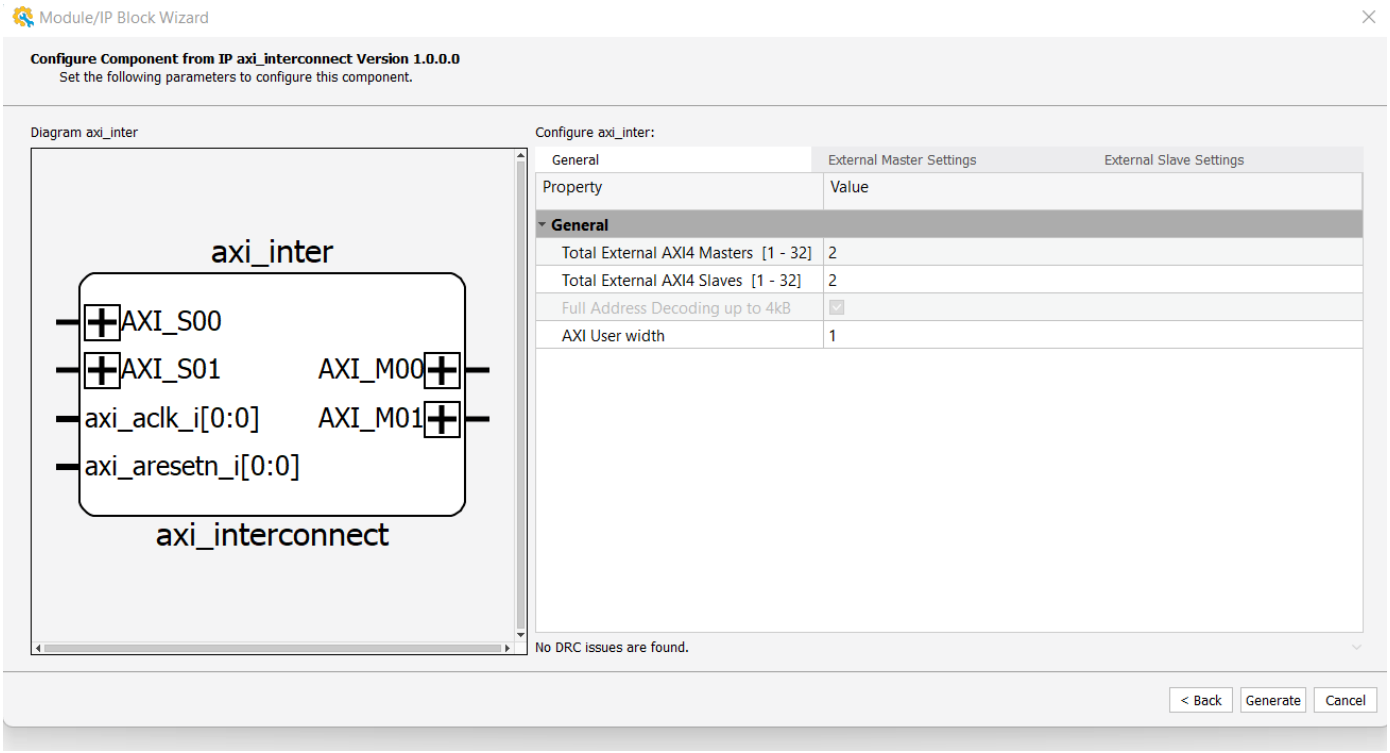

Figure 2.3. AXI Interconnect Module Configuration User Interface

Table 2.3. Attributes Description

Attribute Name	Description
1. General Settings tab	
General	
Total External AXI4 Slaves	Total external AXI4 Masters.
Total External AXI4 Masters	Total external AXI4 Slaves.
AXI User width	AXI user width. This is the common bit width for all the AXI4 interfaces
2. External Master Settings Tab	
2.1 General	
External Master AXI ID width	External master AXI ID width. This holds the maximum ID bit width required by the external master port interfaces.
AXI Master Max Address Width(bits)	External master maximum AXI address width. Holds maximum of the available external master's address bus width.
AXI Master Max Data Width(bits)	External master maximum AXI data width. Holds maximum of the available external master's data bus width.
AXI Master Max no. of ID supports	External Master Maximum number of ID Support Holds maximum of the configured values for different external master.
2.2 External master access Type Settings	
External master AXI access Type <N>	External Master WO/RO/WR access type. Here, <N> = 0 to (Total External AXI4 masters -1) 0 - Write only port 1 - Read only port 2 - Write/Read port

Attribute Name	Description
2.3 External master protocol Settings	
External master AXI protocol <N>	AXI protocol supported by the external master N. Here, <N> = 0 to (Total External AXI4 masters -1) The supported protocol types are AXI4 and AXI4-lite.
2.4 External master CDC enable Settings	
External master CDC enable <N>	External master port interface <N> clock domain crossing enable/disable. This is enabled when external master port interface <N> is asynchronous to the AXI interconnect clock axi_aclk_i Here, <N> = 0 to (Total External AXI4 masters -1).
2.5 External master Address Settings	
External master Address width<N>	External master Address width. Here, <N> = 0 to (Total External AXI4 masters -1). This is used for the configuration of each of the external master port address width.
2.6 External Master Data Settings	
External Master Data width <N>	External master Data width. Here, <N> = 0 to (Total External AXI4 masters -1) This is used for the configuration of each of the external master port data bus width.
2.7 External Master No. of IDs Support settings	
External Master No. of IDs <N>	Number of different AXI4 IDs supported by external master <N> Here, <N> = 0 to (Total External AXI4 masters -1) Reordering Depth 1: means single thread 2 or more: means multi-thread
2.8 External Master IDs order enable settings	
External Master ID order enable <N>	ID order enable/disable for the external master <N> Here, <N> = 0 to (Total External AXI4 masters -1) When same ID is issued to more than one external slave by an external master <N>, then AXI interconnect ensures that the write/read responses from different slaves are passed in the order of reception of requests received from the external master <N>.
2.9 External master write accept settings	
External Master Write accept<N>	Number of Outstanding Write transactions accepted by external master <N> connected to the AXI interconnect. Here, <N> = 0 to (Total External AXI4 masters -1)
2.10 External master read accept settings	
External Master Read accept<N>	Number of Outstanding read transactions accepted by external master<N> connected to the AXI interconnect. Here, <N> = 0 to (Total External AXI4 masters -1)

Attribute Name	Description
2.11 External master priority settings	
External Master Priority<N>	External master <N> priority scheme to choose responses from different external slaves (at write response channel and read response channel) Here, <N> = 0 to (Total External AXI4 masters -1). The available priority schemes are round robin and fixed priority.
2.12 External master 0 Fixed priority settings	
Ext Slave <M> Ext Master 0 Fixed Priority	This is enabled when external master 0 is set to fixed priority. This configures the order of fixed priority to be followed between different external slaves for external master 0. Ext Slave <M> Ext Master 0 Fixed Priority Here, <M> = 0 to (Total External AXI4 slaves -1)
2.13 External master <N> Fixed priority settings	
Ext Slave <M> Ext Master N Fixed Priority	This is enabled when external master N is set to fixed priority. This configures the order of fixed priority to be followed between different external slaves for external master N. Ext Slave <M> Ext Master N Fixed Priority. Here, <M> = 0 to (Total External AXI4 slaves -1) Here, <N> = Total External AXI4 masters -1
3. External Slave Settings Tab	
3.1 General	
External Slave AXI ID width	External slave AXI ID width. This holds the maximum ID bit width required by the external slave port interfaces.
AXI Slave Max Address Width(bits)	External slave maximum AXI address width. Holds maximum of the available external slave's address bus width.
AXI Slave Max Data Width(bits)	External slave maximum AXI data width. Holds maximum of the available external slave's data bus width.
AXI Slave Max Fragment count	External Slave Max Fragment count Holds maximum of the available external slave's fragment count.
3.2 External slave access type settings	
External Slave Access Type <M>	External slave WO/RO/WR access type. Here, <M> = 0 to (Total External AXI4 slaves -1) 0 - Write only port 1 - Read only port 2 - Write/Read port
3.3 External slave protocol type settings	
External Slave Protocol type <M>	AXI protocol supported by the external slave M. Here, <M> = 0 to (Total External AXI4 slaves -1) The supported protocol types are AXI4 and AXI4-lite.

Attribute Name	Description
3.4 External slave CDC enable settings	
External slave CDC Enable <M>	External slave port interface <M> clock domain crossing enable/disable. This is enabled when external slave port interface <M> is asynchronous to the AXI interconnect clock axi_aclk_i Here, <M> = 0 to (Total External AXI4 slaves -1).
3.5 External slave address settings	
External Slave Address width <M>	External slave Address width. Here, <M> = 0 to (Total External AXI4 slaves -1). This is used for the configuration of each of the external slave port address width.
3.6 External slave data settings	
External Slave Data width <M>	External slave data bus width. Here, <M> = 0 to (Total External AXI4 slaves -1). This is used for the configuration of each of the external slave port data bus width.
3.7 External slave write issue settings	
External Slave Write Issue <M>	Number of Outstanding Write transactions issue by each external slave <M> connected to the AXI interconnect. Here, <M> = 0 to Total External AXI4 slaves -1
3.8 External slave read issue settings	
External Slave Read Issue <M>	Number of Outstanding read transactions issue by each external slave <M> connected to the AXI interconnect. Here, <M> = 0 to Total External AXI4 slaves -1
3.9 External slave fragment settings	
External slave <M> fragment count	Number of fragments per external slave interface. Here, <M> = 0 to Total External AXI4 slaves -1 This fragment count should not exceed the AXI slave maximum fragment count.
3.10 External slave <M> Base address settings	
Base address <F>(1)	Base address for external slave <M> Fragment <F> Here, <F> = 0 to (External slave M fragment count-1)
3.11 External slave <M> End address settings	
End address <F> (2)	End address for external slave <M> Fragment <F> Here, <F> = 0 to (External slave M fragment count-1)
3.12 External slave priority settings	
External Slave Priority <M>	External slave <M> priority scheme to choose requests from different external masters (at write and read address channel) Here, <M> = 0 to (Total External AXI4 slaves -1). The available priority schemes are round robin and fixed priority.

Attribute Name	Description
3.13 External slave 0 Fixed priority settings	
Ext Master <N> Ext Slave 0 Fixed Priority	This is enabled when external slave 0 is set to fixed priority. This configures the order of fixed priority to be followed between different external masters for external slave 0. Ext Master <N> Ext Slave 0 Fixed Priority Here, <N> = 0 to (Total External AXI4 masters -1)
3.14 External slave <M> Fixed priority settings	
Ext Master <N> Ext Slave M Fixed Priority	This is enabled when external slave M is set to fixed priority. This configures the order of fixed priority to be followed between different external masters for external slave M. Ext Master <N> Ext Slave M Fixed Priority Here, <N> = 0 to (Total External AXI4 masters -1)

Notes:

- The base address has to be multiple of 4KB (i.e., 2^12). i.e., 0, ‘h1000,’h2000 etc.
- The end address has to be multiple of 4KB-1. i.e., ‘h FFF, ‘h1FFF etc.
- The address range per fragment starts from the Base address and end at the End address. This address range should be non-overlapping between different fragments across the external slaves.

2.4. Use Models

The AXI Interconnect Module connects one or more AXI4/AXI4-lite master devices to one or more AXI4/AXI4-lite slave devices.

Each connected AXI master device could either be:

- A device that originates AXI4/AXI4-lite transactions (endpoint master) or
- A master interface of an upstream AXI Interconnect core being cascaded.

Similarly, each connected AXI4/AXI4-lite slave device could either be:

- The final target of AXI4/AXI4-lite transactions (endpoint slave) or
- A slave interface of a downstream AXI Interconnect core being cascaded

In general, AXI Interconnect Module can be configured for the following connectivity patterns:

- Single Master Interconnect – refer to the Singe master interconnect section.
- Multi-Master Interconnect – refer to multi-master interconnect section.

An example of Single Master Interconnect application is shown in Figure 2.4. The arrows in the figure are AXI4/AXI4-lite interface connections, where M stands for an AXI master port, and S stands for an AXI slave port. The AXI interface type can be configured as either AXI4 or AXI4-lite.

In this example, the Instruction port of the CPU is directly connected to one port of Dual Port Memory while the Data port of the CPU is connected to the slave port of Single Master Interconnect. This connection allows parallel instruction fetch and data access execution. The master ports of Single Master Interconnect are connected to one port of Dual Port Memory, AXI2AHB Bridge, AXI2APB Bridge and LPDDR4 MC. This allows the CPU Data port to access the said slaves.

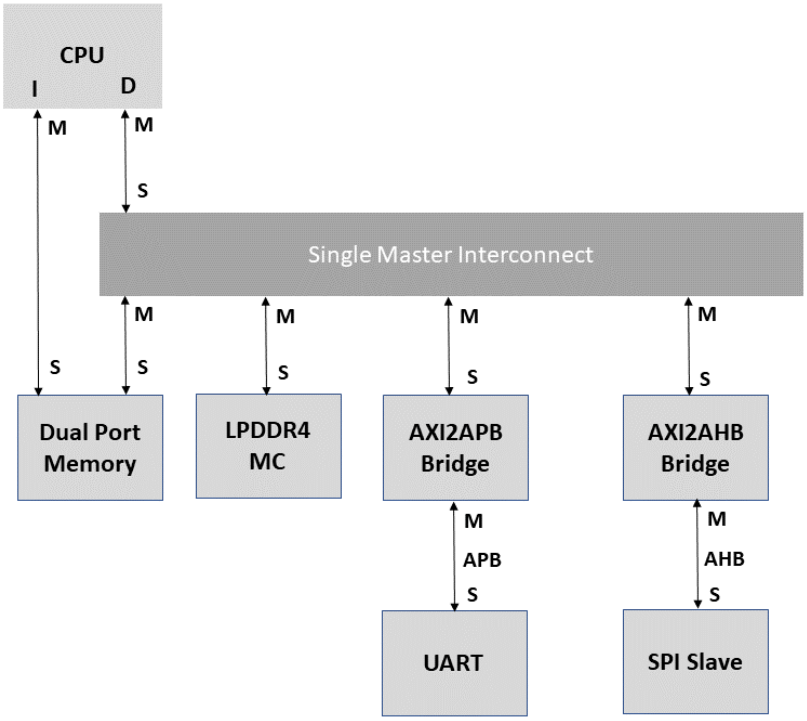

Figure 2.4. Example of Single Master Interconnect Application

An example of Multi-Master Interconnect application is shown in Figure 2.5. This is similar to Figure 2.4 with the addition of DMA IP. In this example, DMA is configured to have one AXI4 master port for reading and writing data to Memory and one AXI4-Lite slave port for register access by the CPU.

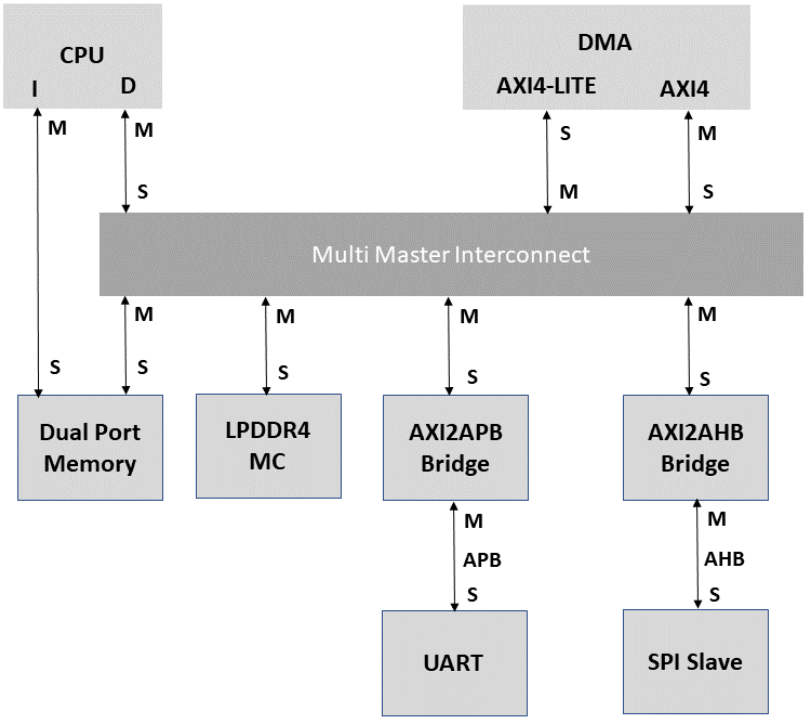

Figure 2.5. Example of Multi-Master Interconnect Application

2.4.1. Default Slave

When a transfer is attempted to an address that does not map to an external slave, the default slave provides DECERR response.

References

- AMBA 4 AXI Protocol Specification- “IHI0022H_c_amba_axi_protocol_spec”
- Certus-Pro NX Web page in latticesemi.com

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.0, May 2022

Section	Change Summary
All	Initial release

www.latticesemi.com