DDR 7:1 Module - Lattice Radiant Software

User Guide

FPGA-IPUG-02189-1.1

November 2022

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
GDDR	Generic Double Date
GUI	Graphical User Interface
I/O	Input/Output
RTL	Register Transfer Level

1. Introduction

The Lattice Semiconductor Generic Double Data Rate 7:1 Input/Output (GDDR 7:1 I/O) Module is designed to be used mainly for Flat-panel Display interface.

1.1. Features

Key features of the Generic Double Data Rate 7:1 Input/Output Module include:

- Receive and Transmit Interface up to 1050 Mbps
- 1-bit to 16-bit data bus width
- Optional bit word alignment and data delay control (for Receive Interface only)

1.2. Conventions

1.2.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.2.2. Signal Names

Signal names that end with:

- _*n* are active low
- _*i* are input signals
- _*o* are output signals
- _*io* are bi-directional input/output signals

2. Functional Description

2.1. Overview

GDDR 7:1 I/O Module is a specific case of Generic DDR I/O Module designed to be used for Flat-panel Display interface.

Table 2.1 provides a summary of GDDR 7:1 I/O Interfaces.

Table 2.1. Available GDDR 7:1 I/O Module Interfaces

Feature	Description	Comments
GDDRX71_RX.ECLK	Generic DDR 7:1 Receive Interface	Supports bypassed and dynamic data path delay. Optional BW_ALIGN support soft logic. Optional Data Delay Control support soft logic. Required GDDR_SYNC support soft logic.
GDDRX71_TX.ECLK	Generic DDR 7:1 Transmit Interface	Supports bypassed data path delay. Required GDDR_SYNC support soft logic.

Notes:

- G – Generic
- _RX – Receive interface
- _TX – Transmit interface
- ECLK – Uses edge clock clocking resource

Table 2.2. Summary of the Soft Logic

Module	Description
GDDR_SYNC	Needed to tolerate large skew between stop and reset input.
BW_ALIGN	The soft IP is used to perform bit and word alignment using PLL's dynamic phase shift interface and dynamic DELAY adjustment.

Figure 2.1 presents top-level diagram describing GDDR 7:1 I/O Module.

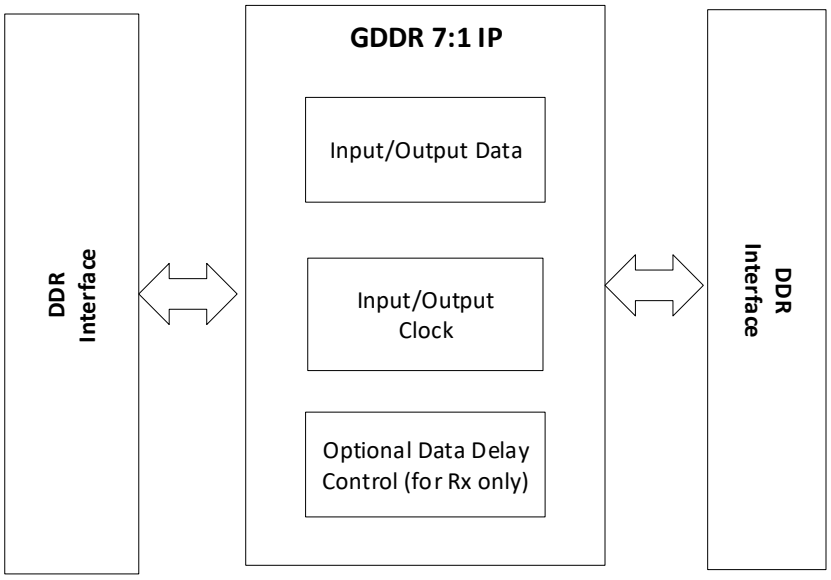

Figure 2.1. GDDR 7:1 I/O Soft IP Top-level Block Diagram

2.2. Functional Diagrams

2.2.1. GDDRX71_RX.ECLK

This is a specialized receive interface (called 7:1 LVDS, FPD-Link, or OpenLDI) using 1:7 gearing and ECLK. The input clock coming in is multiplied 3.5X using a PLL. The multiplied clock is used to capture the data at the receive IDDR71 module.

Figure 2.2 and Figure 2.4 describe the GDDR 7:1 I/O Receive Interface with Data Delay Control option disabled.

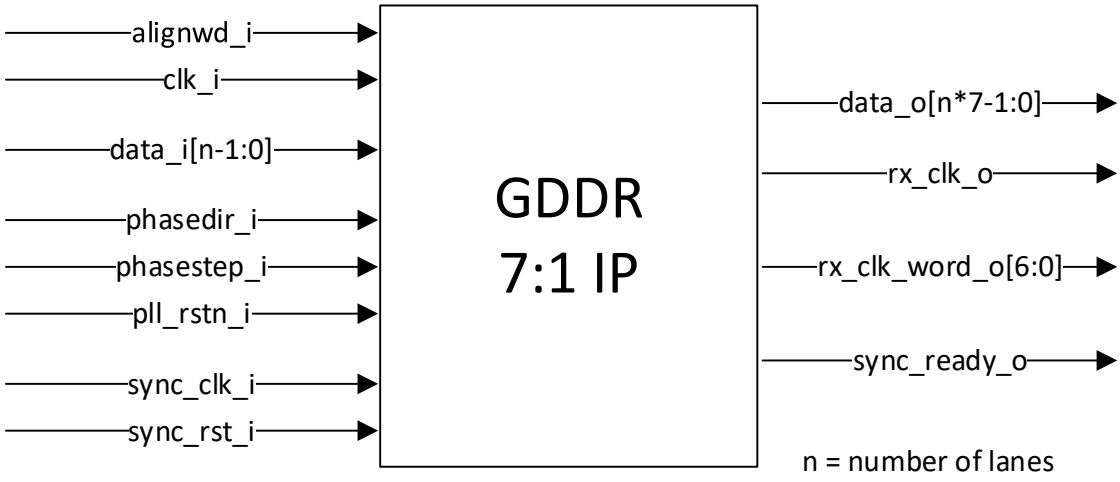

Figure 2.2. GDDRX71_RX.ECLK with GDDR_SYNC and GPLL (without BW_ALIGN) Block Diagram

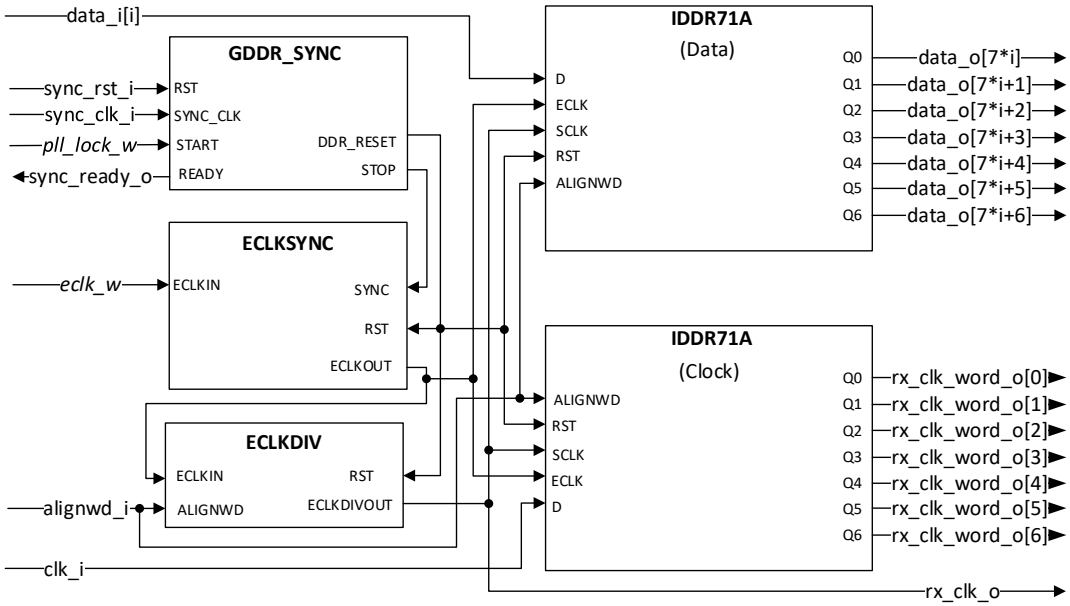

Figure 2.3. GDDRX71_RX.ECLK with GDDR_SYNC and GPLL (without BW_ALIGN) Interface

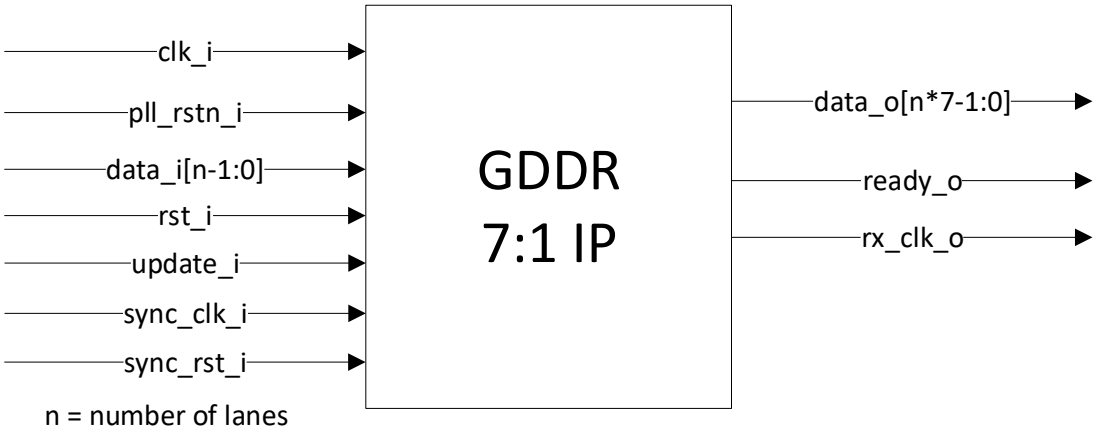

Figure 2.4. GDDRX71_RX.ECLK with GDDR_SYNC, GPLL and BW_ALIGN Block Diagram

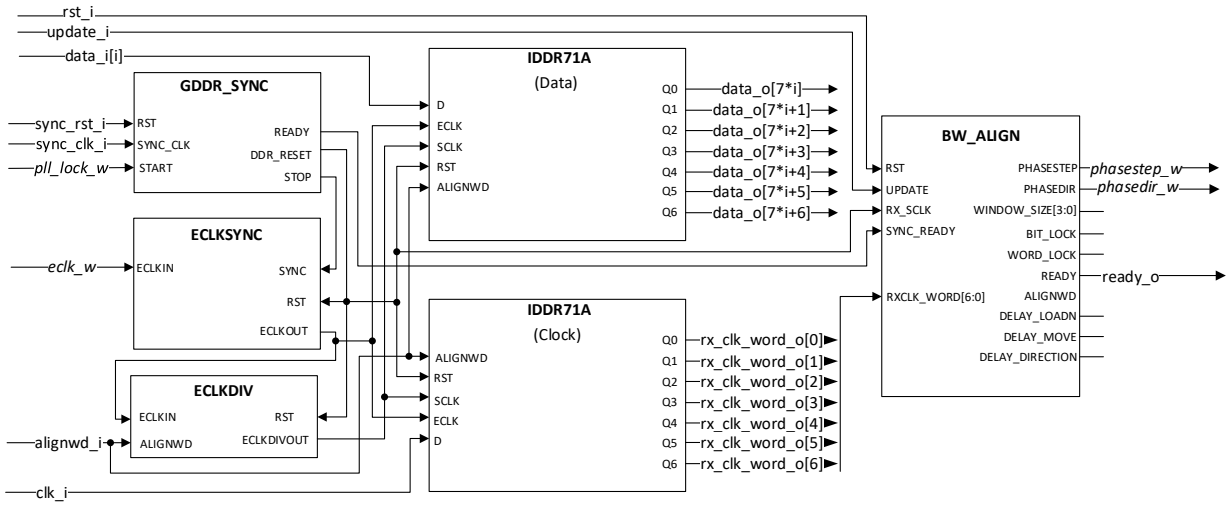

Figure 2.5. GDDRX71_RX.ECLK with GDDR_SYNC, GPLL and BW_ALIGN Interface

Figure 2.6 describes GDDR 7:1 I/O Receive Interface with Data Delay Control option enabled.

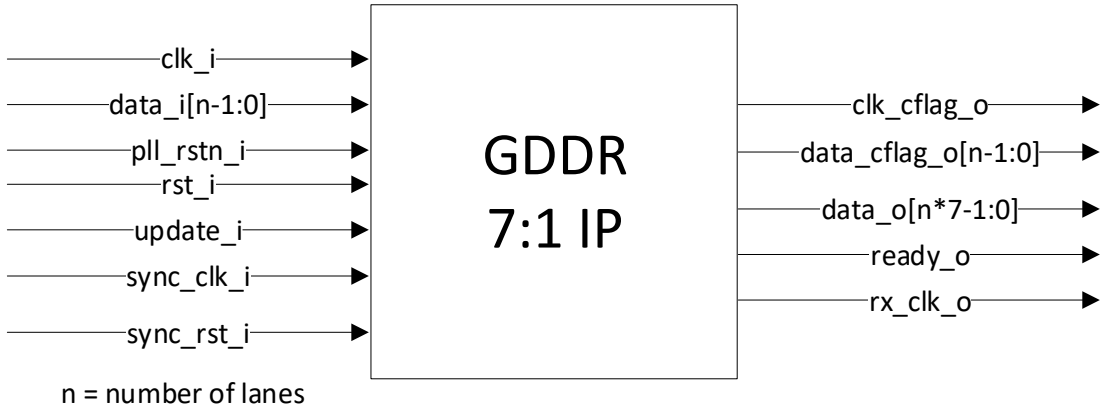

Figure 2.6. GDDRX71_RX.ECLK with GDDR_SYNC, GPLL, BW_ALIGN and Data Delay Control Block Diagram

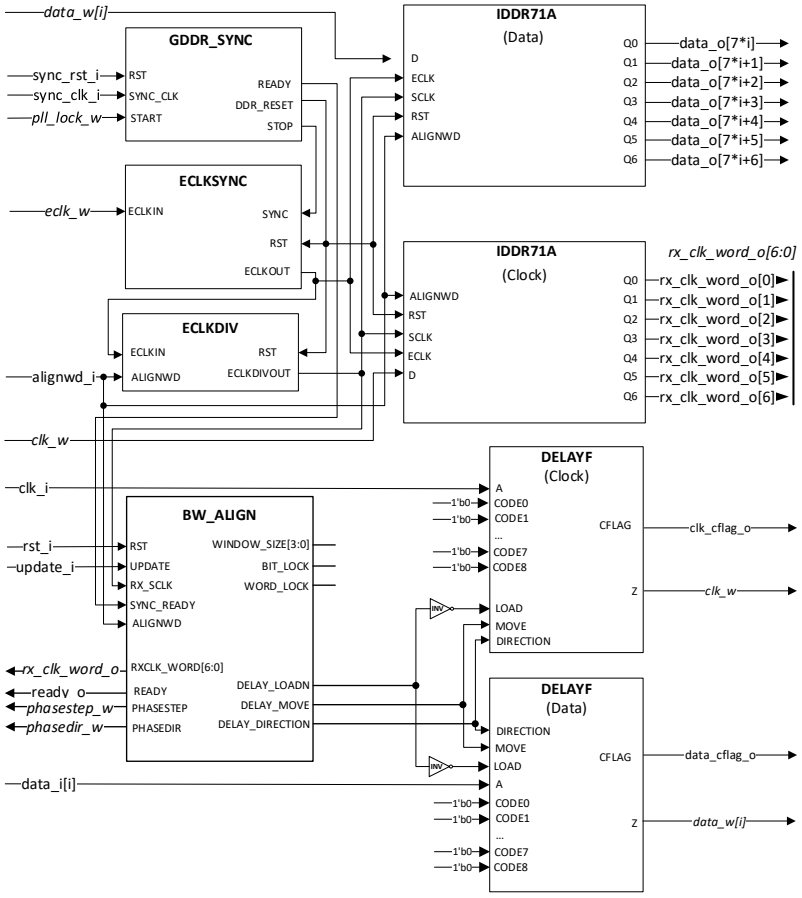

Figure 2.7. GDDRX71_RX.ECLK with GDDR_SYNC, GPLL, BW_ALIGN and Data Delay Control Interface

Figure 2.8 shows the PLL used on GDDR 7:1 I/O Receive Interface. When “Bit and Word Alignment” is enabled, phasedir_i and phasestep_i connects from phasedir_w and phasestep_w consecutively of Figure 2.5 and Figure 2.7.

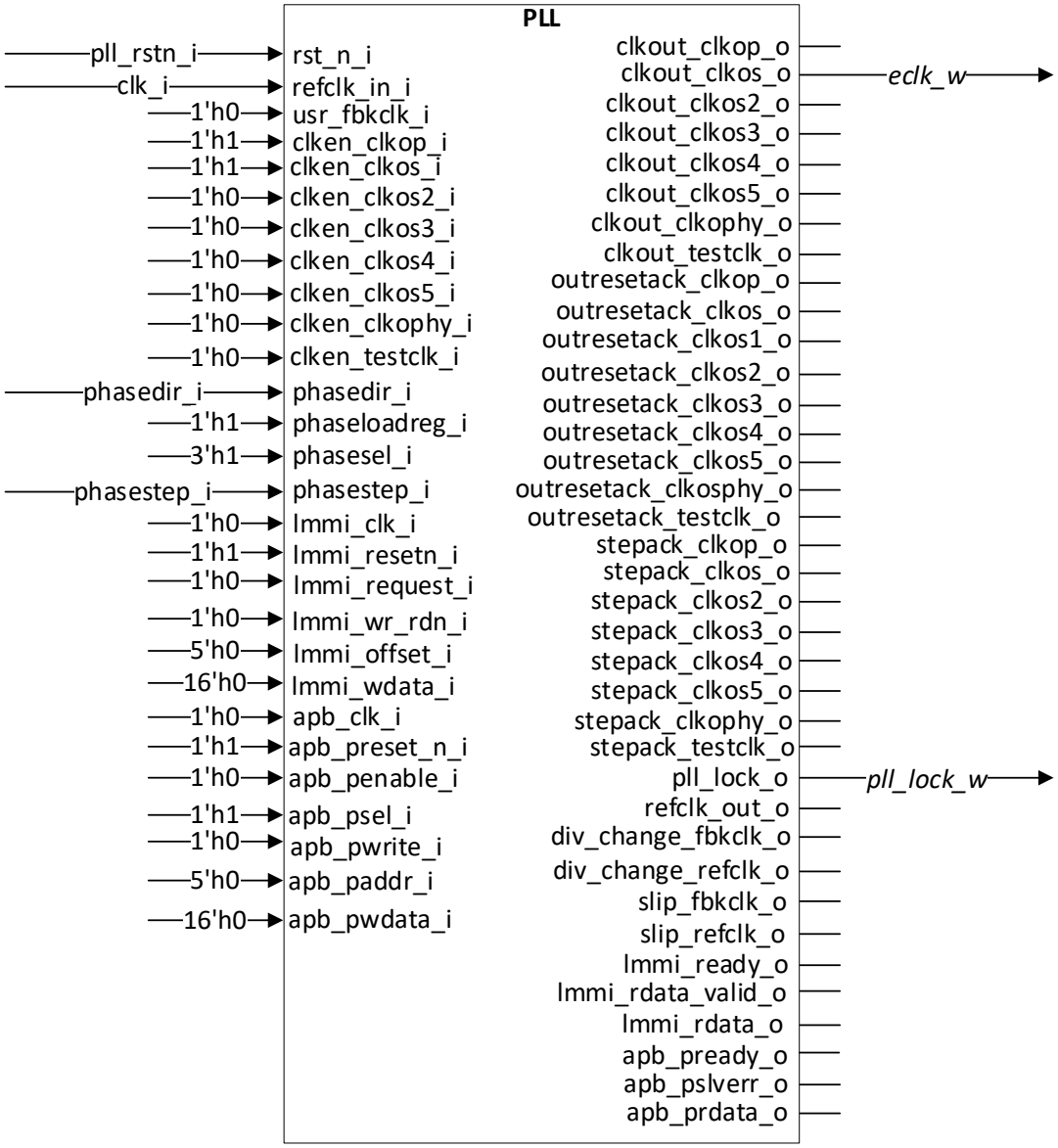

Figure 2.8. PLL of GDDRX71_RX.ECLK

2.2.2. RX Output Data Mapping

Bus Width = 2

data_i[1:0] = a[1:0], b[1:0], c[1:0], d[1:0], e[1:0], f[1:0], g[1:0]

data_o[7*2-1:0] = {g[1:0],f[1:0], e[1:0], d[1:0], c[1:0], b[1:0], a[1:0]}

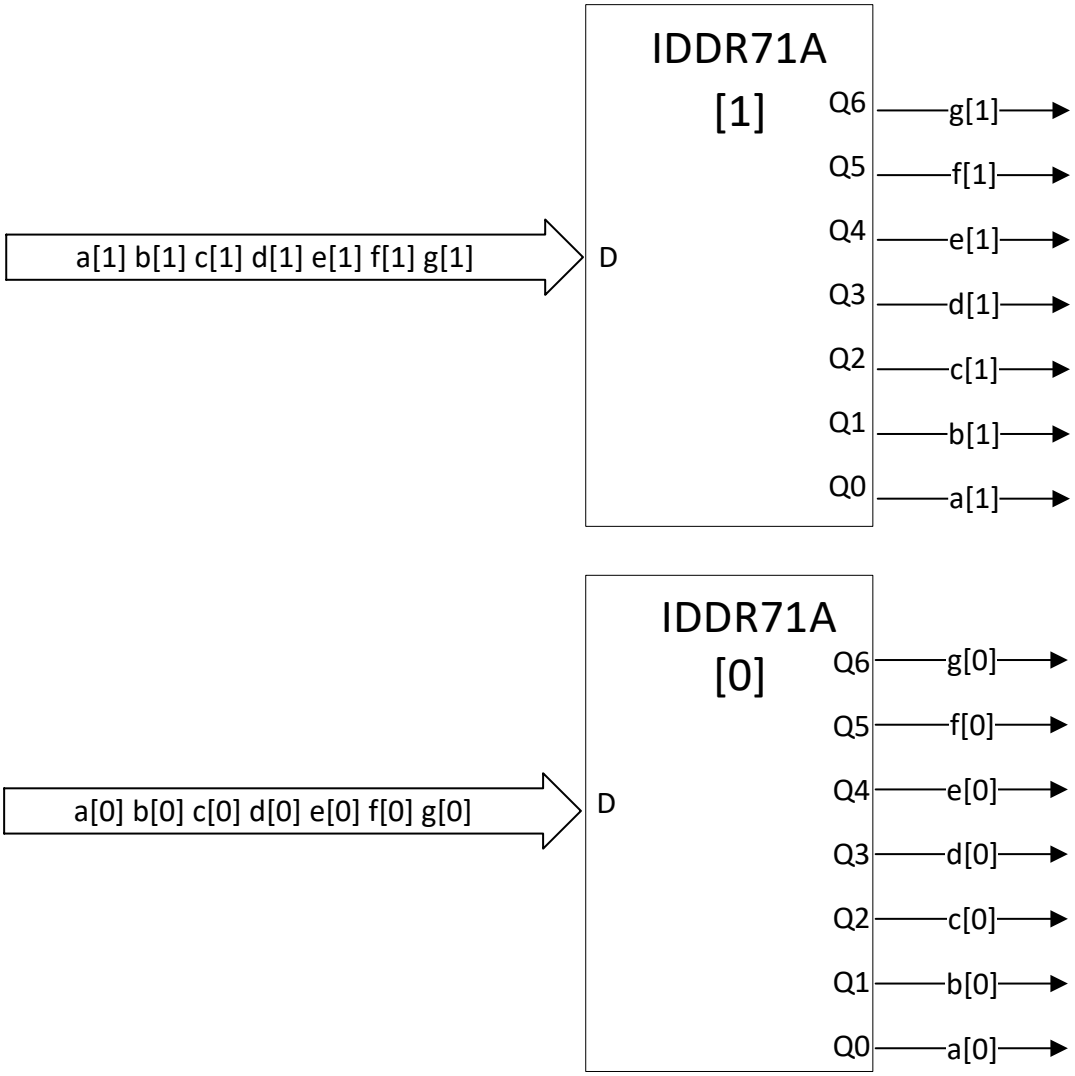

Figure 2.9. Rx Output Data Mapping

As shown in Figure 2.9, for GDDR71 Rx configuration, when Bus Width is 2 bits, the IP generates two IDDR71A modules (in our example for X3.5, the number of data_i batches is seven.)

The first batch of incoming data_i[a1:a0] is captured on the rising edge of the fast clock. The next batch of data_i[b1:b0] is captured on the falling edge of the fastest clock and so on.

In the figure, this translates to the batch of the input data's slowest bits data_i[g1:g0] being placed on the data_o vector's highest bits [13:12]. Similarly, data_i[f1:f0] bits are placed on data_o[11:10] and so on. The sum of all the IDDR71 outputs is a data_o[13:0] vector.

2.2.3. GDDRX71_TX.ECLK

This is a specialized transmit interface (called 7:1 LVDS, FPD-Link, or OpenLDI) using 7:1 gearing and ECLK. The output clock going out is divided by 3.5X using ECLKDIV. The multiplied clock is used to capture the data at the ODDR71 module. Transmit side for the 7:1 LVDS interface DDR using the 7:1 gearing with ECLK. The clock output is aligned to the data output.

Figure 2.10 describes GDDR 7:1 I/O Transmit Interface.

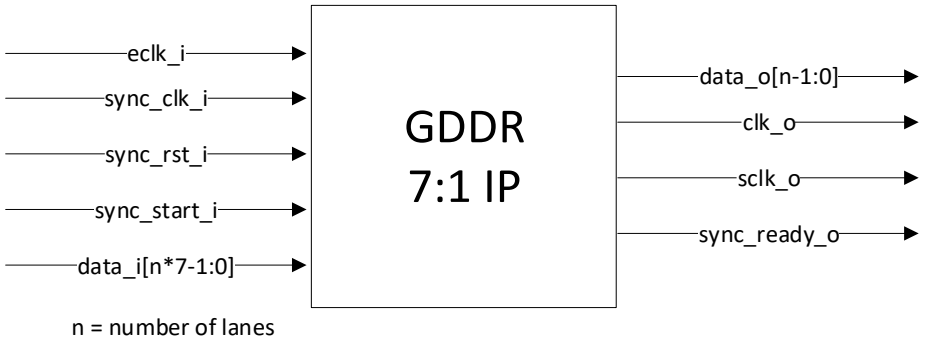

Figure 2.10. GDDRX71_TX.ECLK Static Delay Block Diagram

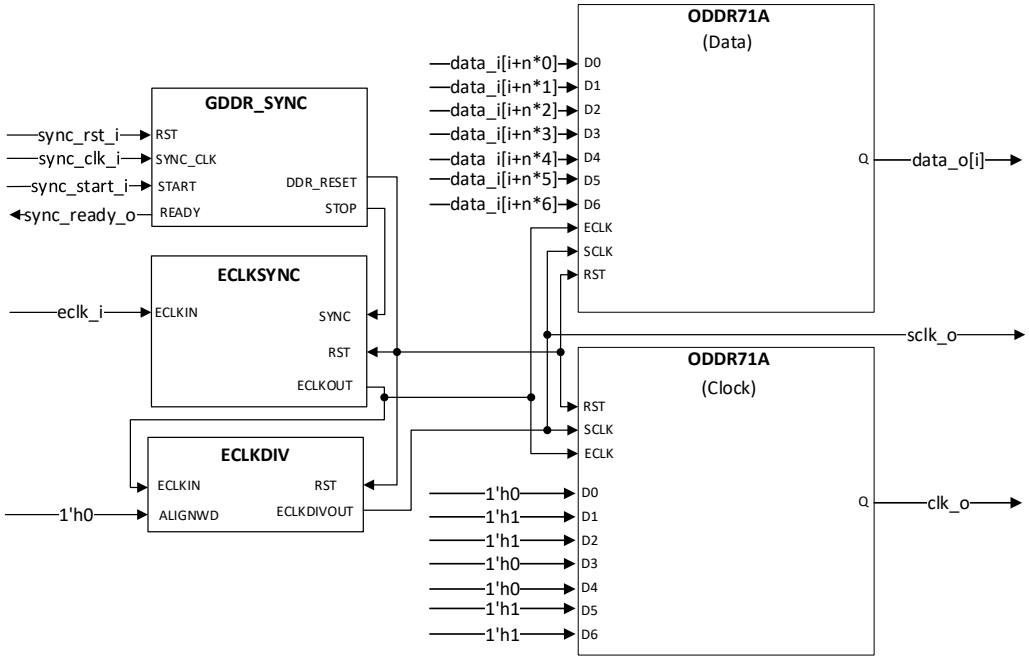

Figure 2.11. GDDRX71_TX.ECLK Static Delay Interface

2.2.4. TX Input Data Mapping

Bus Width = 4
data_i [7 * 4 - 1 : 0]
data_o [4-1:0]

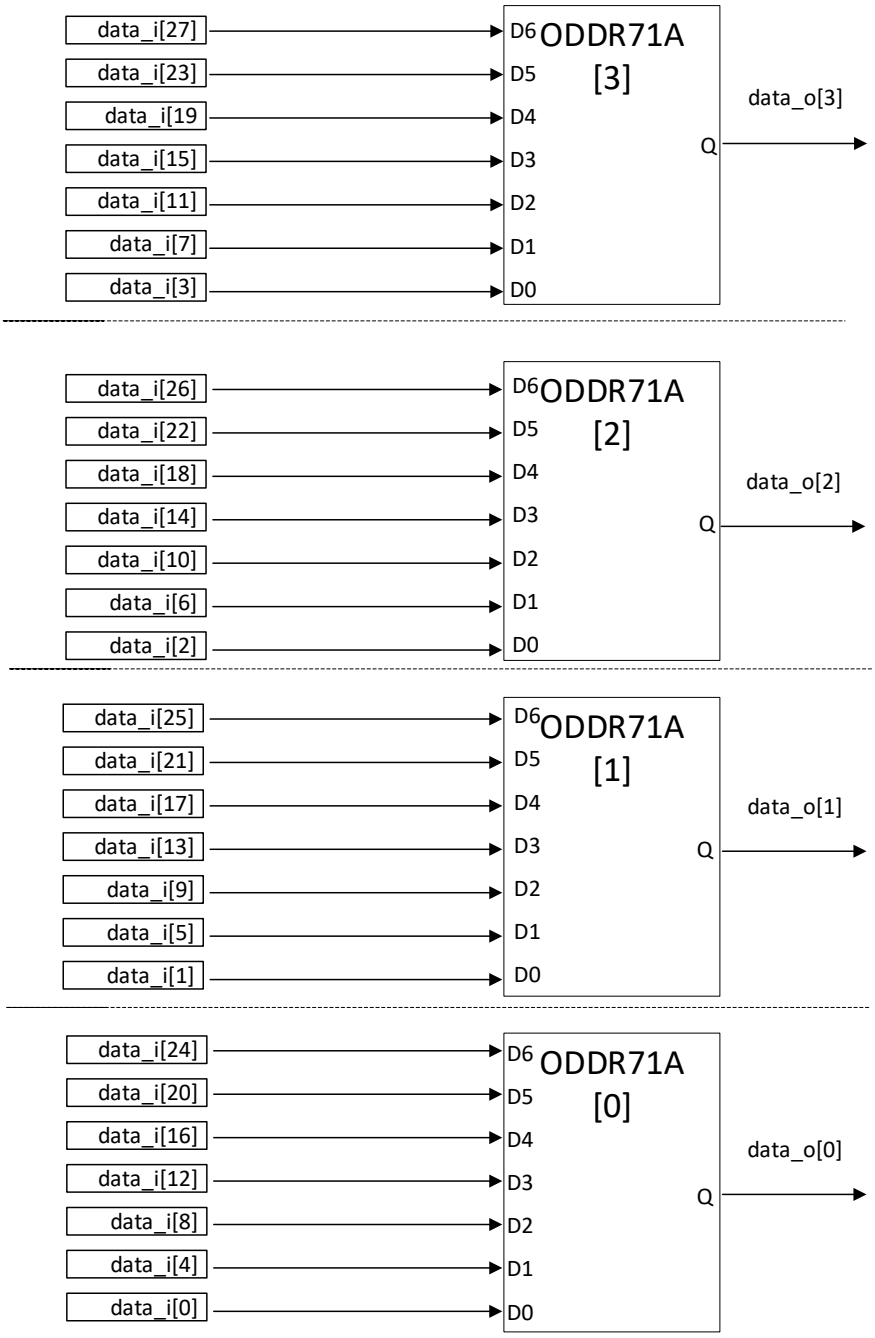

Figure 2.12. Tx Input Data Mapping

As shown in Figure 2.12, for GDDR 7:1 Tx configuration, when Bus Width is 4 bits, the IP generates four ODDR71A modules. The entire input data is broken down into 7 groups, each group with the size of 4 bits. The group with the fastest bits data_i[3:0] is transmitted first, followed by data_i[7:4] and so on.

2.3. Signal Description

Table 2.3. GDDR 7:1 I/O Module Receive Signal Description

Port Name	Direction	Width(bits)	Description
Clock and Reset			
rx_clk_o	OUT	1	Clock output for Receive interface. Divided RX clock form 7:1 RX interface produced by ECLKDIV. This is only available when *Enable Bit and Word Alignment Soft IP* is enabled.
sync_clk_i	IN	1	Startup clock. This cannot be the RX_CLK or divided version. It can be another low-speed continuously running clock. For example, an oscillator clock.
sync_rst_i	IN	1	Active high reset signal.
rst_i	IN	1	Active high reset signal when *Enable Bit and Word Alignment Soft IP* is enabled.
User Interface			
pll_rstn_i	IN	1	Active low reset of internal PLL. This is available only when *Interface Type* is Receive.
phasedir_i	IN	1	Phase rotation direction of internal PLL. This is available only when *Interface Type* is Receive, *Enable Bit and Word Alignment Soft IP* is disabled, and *Enable Data Delay Control* is disabled.
phasestep_i	IN	1	Rotate phase of internal PLL. This is available only when *Interface Type* is Receive, *Enable Bit and Word Alignment Soft IP* is disabled, and *Enable Data Delay Control* is disabled.
update_i	IN	1	Start bit and word alignment, or restart the procedure if optimization is needed again. This is available only when *Interface Type* is Receive and *Enable Bit and Word Alignment Soft IP* is enabled.
alignwd_i	IN	1	This signal is used for word alignment. It shifts word by one bit. This is only available when *Enable Bit and Word Alignment Soft IP* is disabled.
data_o	OUT	n*7	Received input data to fabric.
sync_ready_o	OUT	1	Indicate that startup is finished and RX circuit is ready to operate. Only available when *Enable Bit and Word Alignment Soft IP* is disabled.
ready_o	OUT	1	Indicates alignment is done, startup is finished and RX circuit is ready to operate. This is only available when *Enable Bit and Word Alignment Soft IP* is enabled.
rx_clk_word_o	OUT	7	Valid receiver clock word size allowance. Parallel data output. Only available when *Enable Bit and Word Alignment Soft IP* is disabled.
data_cflag_o	OUT	n	Underflow or overflow flag to indicate the minimum or maximum data path delay adjustment is reached. This is available only when *Interface Type* is Receive, *Enable Bit and Word Alignment Soft IP* is enabled, and *Enable Data Delay Control* is enabled.
clk_cflag_o	OUT	1	Underflow or overflow flag to indicate minimum or maximum clock path delay adjustment is reached. This is available only when *Interface Type* is Receive, *Enable Bit and Word Alignment Soft IP* is enabled, and *Enable Data Delay Control* is enabled.
I/O Pad Interface			
clk_i	IN	1	Clock input signal from I/O.
data_i	IN	n	Data input signal from I/O.

Note: n = number of lanes.

Table 2.4. GDDR 7:1 I/O Module Transmit Signal Description

Port Name	Direction	Width(bits)	Description
Clock and Reset			
eclk_i	IN	1	Transmit data sampling clock.
sclk_o	OUT	1	Clock output for *Interface Type* is Transmit.
sync_clk_i	IN	1	Low speed continuously running clock input.
sync_rst_i	IN	1	Active high reset signal.
User Interface			
data_i	IN	n*7	Transmit output data going to I/O.
sync_ready_o	OUT	1	Indicate that startup is finished and TX circuit is ready to operate.
sync_start_i	IN	1	Waits for the PLL lock signal to start the synchronization.
I/O Pad Interface			
clk_o	OUT	1	Clock output signal to I/O.
data_o	OUT	n	Data output signal to I/O.

Note: n = number of lanes

2.4. Attribute Summary

Table 2.5 provides a list of user-configurable attributes for the GDDR 7:1 I/O Module. Attributes settings are specified using GDDR 7:1 I/O Module Configuration user interface in Lattice Radiant.

Table 2.5. Attributes Table

Attribute	Selectable Values	Default	Dependency on other Attributes	Additional Requirements
Interface Type	Receive, Transmit	Receive	—	—
Bus Width	1–16	8	—	—
Interface Bandwidth (Mbps)	70-1050	945	—	—
Clock Frequency (MHz)	10–150	135	*Bandwidth/7*	Display for information only
Enable Bit and Word Alignment Soft IP	Checked, Unchecked	Unchecked	*Interface Type = Receive*	—
Enable Data Delay Control	Checked, Unchecked	Unchecked	*Interface Type = Receive* and *Enable Bit and Word Alignment Soft IP* is checked	—

Note: The attributes can be configured from the General Tab of the Lattice Radiant Software user interface.

Table 2.6 below presents attribute description.

Table 2.6. Attributes Description

Attribute Name	Description
Interface Type	RECEIVE or TRANSMIT interface type
Bus Width	Total number of lanes/bus width
Interface Bandwidth (Mbps)	Interface Clock Frequency
Enable Bit and Word Alignment Soft IP	Optional bit and word alignment Soft IP (BW_ALIGN) module. The bit alignment module centers the edge clock to the middle of the data eye and the word alignment module is used to achieve the 7-bit word alignment.
Enable Data Delay Control	When enabled, BW_ALIGN Soft IP module automatically controls the movement of the data on DELAY module.

3. IP Generation, Simulation, and Validation

This section provides information on how to generate the IP using the Lattice Radiant Software, and how to run simulation and synthesis. For more details on the Lattice Radiant Software, refer to the Lattice Radiant Software User Guide.

3.1. Generating the IP

The Lattice Radiant Software allows you to customize and generate modules and IPs and integrate them into the device's architecture. The procedure for generating the GDDR 7:1 I/O module in Lattice Radiant Software is described below.

To generate GDDR 7:1 I/O Module:

1. Create a new Lattice Radiant Software project or open an existing project.
2. In the **IP Catalog** tab, double-click on **GDDR 7:1** under **Module, Architecture_Modules, I/O** category. The **Module/IP Block Wizard** opens as shown in Figure 3.1. Enter values in the **Component name** and the **Create in** fields and click **Next**.

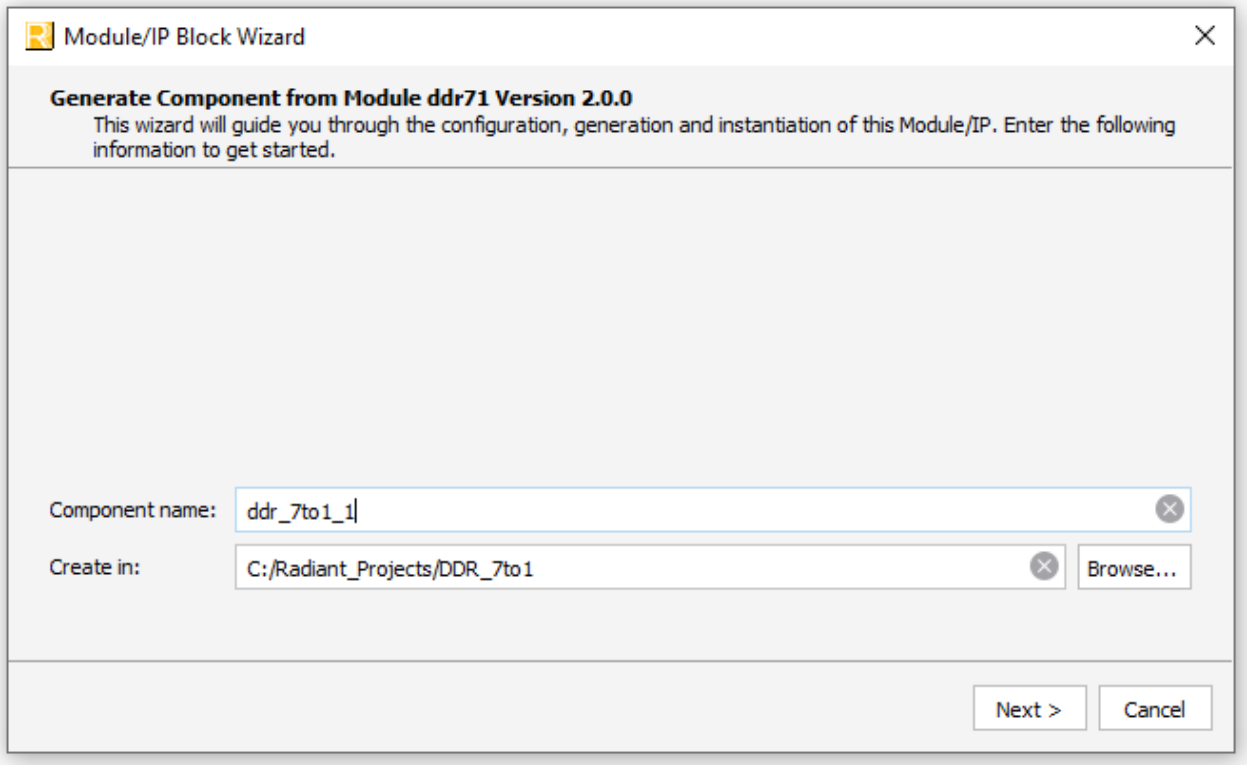

Figure 3.1. Module/IP Block Wizard

3. In the module's dialog box of the **Module/IP Block Wizard** window, customize the selected GDDR 7:1 I/O module using drop-down menus and check boxes. As a sample configuration, see Figure 3.2. For configuration options, see the Attribute Summary section.

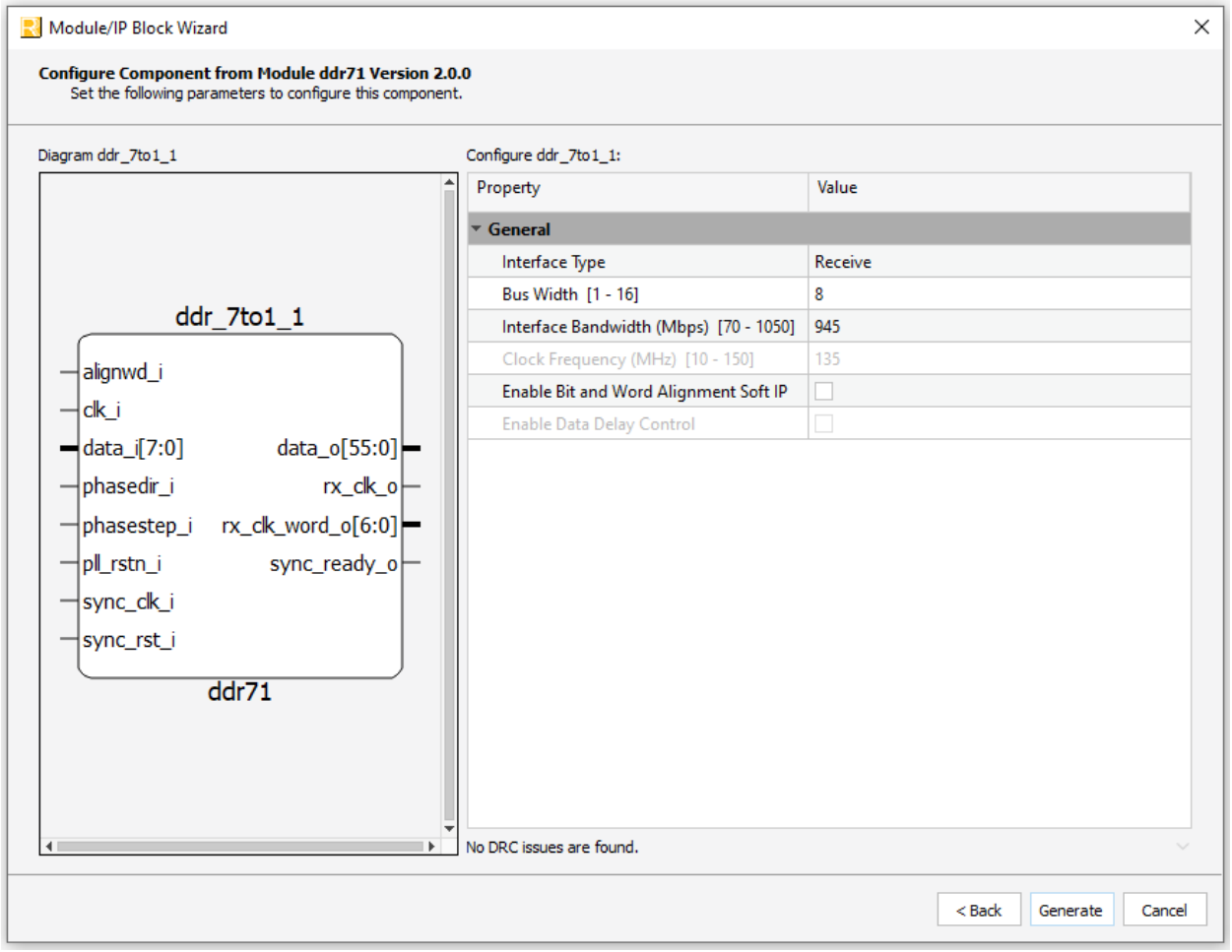

Figure 3.2. Configure Block of GDDR 7:1 I/O Module

4. Click **Generate**. The **Check Generated Result** dialog box opens, showing design block messages and results as shown in Figure 3.3.

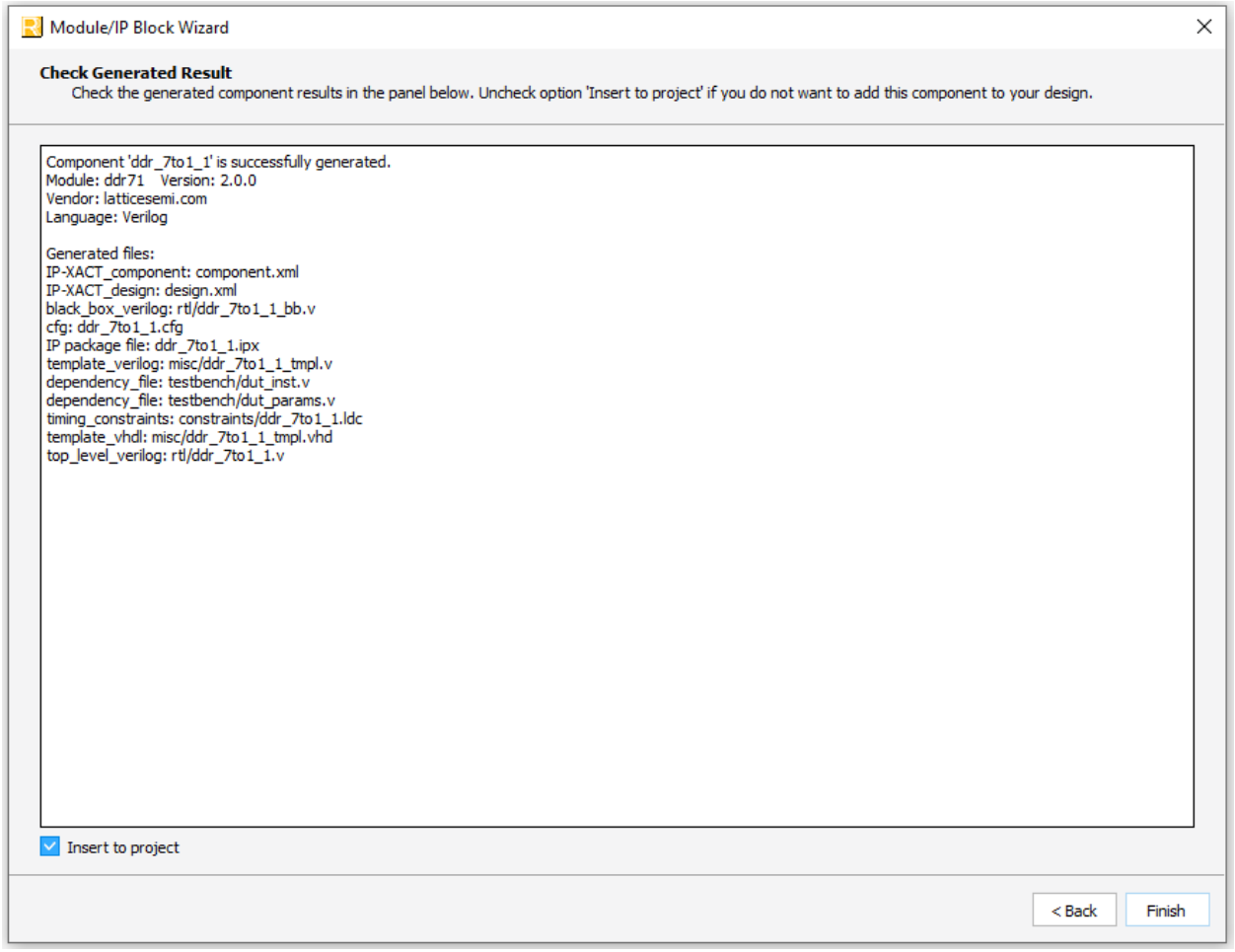

Figure 3.3. Check Generated Result

5. Click the **Finish** button. All the generated files are placed under the directory paths in the **Create in** and the **Component name** fields shown in Figure 3.1.

The generated GDDR 7:1 I/O module package includes the black box (<Instance Name>_bb.v) and instance templates (<Instance Name>_tmpl.v/vhd) that can be used to instantiate the module in a top-level design. An example RTL top-level reference source file (<Instance Name>.v) that can be used as an instantiation template for the module is also provided. You may also use this top-level reference as the starting template for the top-level for their complete design. The generated files are listed in Table 3.1.

Table 3.1. Generated File List

Attribute	Description
<Instance Name>.ipx	This file contains the information on the files associated to the generated IP.
<Instance Name>.cfg	This file contains the parameter values used in IP configuration.
component.xml	Contains the ipxact:component information of the IP.
design.xml	Documents the configuration parameters of the IP in IP-XACT 2014 format.
rtl/<Instance Name>.v	This file provides an example RTL top file that instantiates the module.
rtl/<Instance Name>_bb.v	This file provides the synthesis black box.
misc/<Instance Name>_tmpl.v misc /<Instance Name>_tmpl.vhd	These files provide instance templates for the module.
testbench/tb_top.v	Test bench template; you can edit this to match your specific needs.
testbench/dut_params.v	Instantiated version of the <IP_name>.v file for simulation use
testbench/dut_ints.v	Top level parameters of the generated RTL file

3.2. Running Functional Simulation

After the IP is generated, running functional simulation can be performed using different available simulators. The default simulator already has pre-compiled libraries ready for simulation. Choosing a non-default simulator however, may require additional steps.

To run functional simulation using the default simulator:

1. Click the  button located on the **Toolbar** to initiate **Simulation Wizard**, as shown in Figure 3.4.

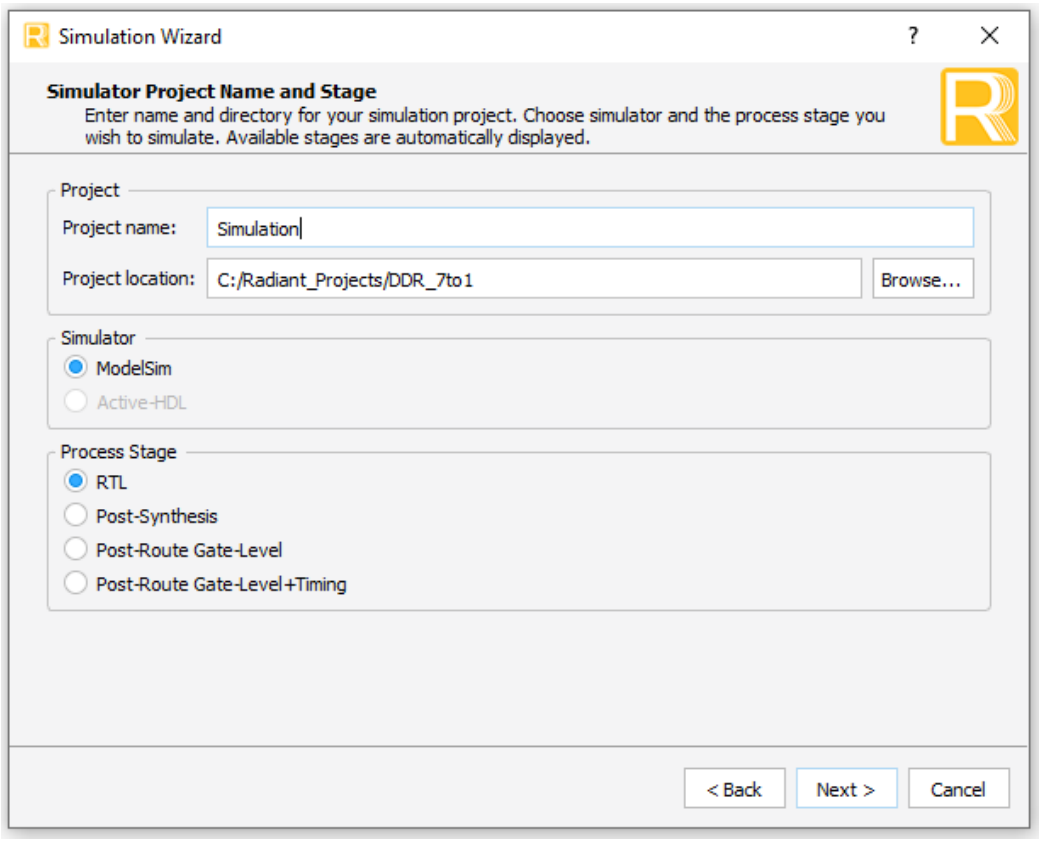

Figure 3.4. Simulation Wizard

2. Click **Next** to open the **Add and Reorder Source** window as shown in Figure 3.5.

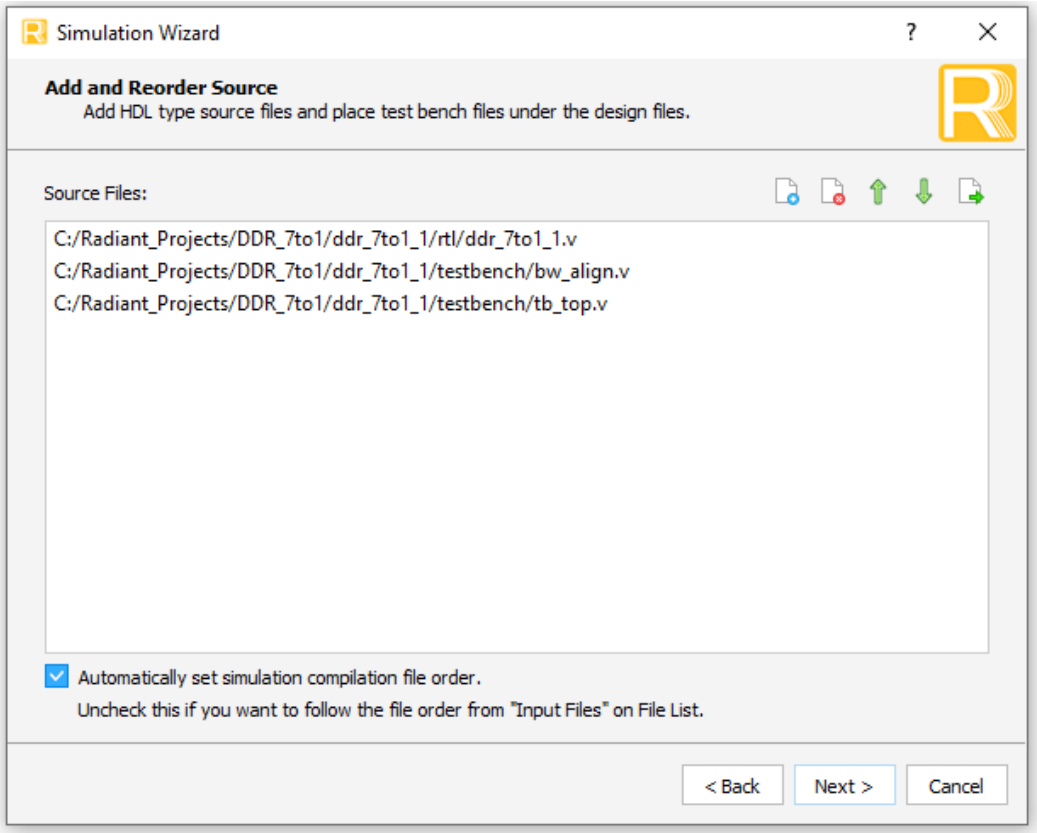

Figure 3.5. Adding and Reordering Source

3. Click **Next**. The Summary window is shown. Click **Finish** to run the simulation.

Note: It is necessary to follow the procedure above until it is fully automated in the Lattice Radiant Software Suite.

The results of the simulation in our example are provided in Figure 3.6.

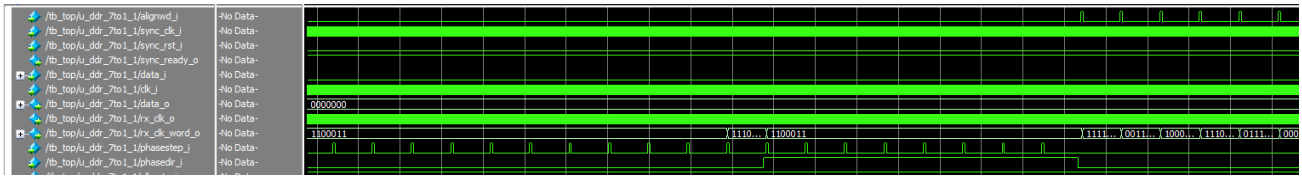

Figure 3.6. Simulation Waveform

3.3. IP Evaluation

There is no restriction on the IP evaluation of this module.

Appendix A. Resource Utilization

DDR 7:1 module resource utilization are shown on Table A.1 and Table A.2 using LAV-AT-500E-3LFG1156I and LAV-AT-500E-1LFG1156I devices with Synplify Pro of Lattice Radiant software. Default configuration is used and some attributes are changed from the default value to show the effect on the resource utilization.

Table A.1. Resource Utilization using LAV-AT-500E-3LFG1156I

Configuration	Clk Fmax (MHz)[1]	Registers	LUTs[2]	EBRs	DSPs
Interface Type is Receive, Interface Bandwidth is 1050Mbps, others are default	150	12	25	0	0
Interface Type is Transmit, Interface Bandwidth is 1050Mbps, others are default	150	12	25	0	0

1. Fmax is generated when the FPGA design only contains the DDR7:1 module and the target frequency is 150 MHz. DDR7:1 module supports up to 1050 MHz ECLK and 150 MHz SCLK only. These values may be reduced when user logic is added to the FPGA design.
2. The distributed RAM utilization is accounted for in the total LUT4s utilization. The actual LUT4 utilization is distribution among logic, distributed RAM, and ripple logic.

Table A.2. Resource Utilization using LAV-AT-500E-1LFG1156I

Configuration	Clk Fmax (MHz)[1]	Registers	LUTs[2]	EBRs	DSPs
Interface Type is Receive, Interface Bandwidth is 1050Mbps, others are default	150	12	25	0	0
Interface Type is Transmit, Interface Bandwidth is 1050Mbps, others are default	150	12	25	0	0

1. Fmax is generated when the FPGA design only contains the DDR7:1 module and the target frequency is 150 MHz. DDR7:1 module supports up to 1050 MHz ECLK and 150 MHz SCLK only. These values may be reduced when user logic is added to the FPGA design.
2. The distributed RAM utilization is accounted for in the total LUT4s utilization. The actual LUT4 utilization is distribution among logic, distributed RAM, and ripple logic.

References

For complete information on Lattice Radiant Project-Based Environment, Design Flow, Implementation Flow and Tasks, as well as on the Simulation Flow, see the Lattice Radiant Software User Guide.

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.1, November 2022

Section	Change Summary
Appendix A. Resource Utilization	Added Resource Utilization section.

Revision 1.0, November 2022

Section	Change Summary

Functional Description	In Table 2.3. GDDR 7:1 I/O Module Receive Signal Description:
	• Revised the description for the signal sync_clk_i
	• Added the following User Interface signals and their details:
	  • pll_rstn_i
	  • phasedir_i
	  • phasestep_i
	  • update_i
	  • data_cflag_o
	  • clk_cflag_o

IP Generation, Simulation, and Validation	• Revised the title from 'IP Generation and Evaluation' to 'IP Generation, Simulation, and Validation' • Deleted the section 'Licensing the IP' • Revised the title of section 3.1 from 'Generation and Synthesis' to 'Generating the IP' • Revised the figures Figure 3.1. Module/IP Block Wizard, Figure 3.2. Configure Block of GDDR 7:1 I/O Module, and Figure 3.3. Check Generated Result • Revised the title of section 3.3 from 'Hardware Evaluation' to 'IP Evaluation'

Revision 0.80, May 2022

Section	Change Summary
All	Initial release

www.latticesemi.com