Avant DDR Generic Module - Lattice Radiant Software

User Guide

FPGA-IPUG-02188-1.0

October 2022

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Tables

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
FPGA	Field Programmable Gate Array
GDDR	Generic Double Data Rate
I/O	Input/Output
RTL	Register Transfer Level
SDR	Single Data Rate

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1. Introduction

The Lattice Semiconductor Generic Double Data Rate Input/Output (GDDR I/O) Module is designed to be used in a wide range of applications in which high-speed data transfer is required.

1.1. Features

The key features of Generic Double Data Rate Input/Output (GDDR I/O) Module include:

- Receive and Transmit Interface up to 1800 Mbps
- Supported gearing: X1, X2, X4, X5
- Selectable I/O type
  - Single-ended or Differential Signaling
- 1-bit to 256-bit data bus width
- 100 MHz to 900 MHz clock frequency
  - 100 MHz to 250 MHz for X1 Gearing
  - 100 MHz to 600 MHz for X2 Gearing
  - 100 MHz to 900 MHz for X4 and X5 Gearing
- Clock-data relationship options:
  - Edge-to-edge
  - Centered
- Data Path Delay that includes following options:
  - Bypass
  - Static Default (Receive Interface only)
  - Dynamic Default (Receive Interface only)
  - Static User-defined
  - Dynamic User-defined
- Includes GDDR_SYNC soft IP logic
- Tri-state control (Transmit Interface only)

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1.2. Conventions

1.2.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.2.2. Signal Names

Signal names that end with:

- _*n* are active low
- _*i* are input signals
- _*o* are output signals
- _*io* are bidirectional input/output signals

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2. Functional Description

2.1. Overview

The GDDR I/O Module is directly connected to the memory interface providing all required DDR ports for memory access. It converts the single data rate (SDR) data to DDR data for write operations and performs the DDR to SDR conversion for read operations. This I/O module utilizes the dedicated FPGA DDR I/O logic and is designed to reliably drive and capture data on the memory interface. DDR interfaces capture data on both rising and falling edges of the clock, thus doubling performance. Table 2.1 provides a summary of GDDR I/O Interface.

Table 2.1. Available GDDR I/O Module Interfaces

Feature	Description	Comments
GDDRX1_RX.SCLK.Centered	Generic DDR 2:1 Receive Centered Interface	Supports bypassed, static, and dynamic data path delay.
GDDRX1_RX.SCLK.Aligned	Generic DDR 2:1 Receive Aligned Interface	Supports bypassed, static, and dynamic data path delay. Supports dynamic clock path delay. Required RX_SYNC support soft logic. Using DDRDLL and DLLDEL.
GDDRX2_RX.ECLK.Centered	Generic DDR 4:1 Receive Centered Interface	Supports bypassed, static and dynamic data path delay. Required GDDR_SYNC support soft logic.
GDDRX2_RX.ECLK.Aligned	Generic DDR 4:1 Receive Aligned Interface	Supports bypassed, static and dynamic data path delay. Supports dynamic clock path delay. Required RX_SYNC support soft logic. Using DDRDLL and DLLDEL.
GDDRX4_RX.ECLK.Centered	Generic DDR 8:1 Receive Centered Interface	Supports bypassed, static, and dynamic data path delay. Required GDDR_SYNC support soft logic.
GDDRX4_RX.ECLK.Aligned	Generic DDR 8:1 Receive Aligned Interface	Supports bypassed, static, and dynamic data path delay. Supports dynamic clock path delay. Required RX_SYNC support soft logic. Using DDRDLL and DLLDEL.
GDDRX5_RX.ECLK.Centered	Generic DDR 10:1 Receive Centered Interface	Supports bypassed, static, and dynamic data path delay. Required GDDR_SYNC support soft logic.
GDDRX5_RX.ECLK.Aligned	Generic DDR 10:1 Receive Aligned Interface	Supports bypassed, static, and dynamic data path delay. Supports dynamic clock path delay. Required RX_SYNC support soft logic. Using DDRDLL and DLLDEL.
GDDRX1_TX.SCLK.Centered	Generic DDR 2:1 Transmit Centered Interface	Supports bypassed and dynamic data path delay. Supports tri-state control.
GDDRX1_TX.SCLK.Aligned	Generic DDR 2:1 Transmit Aligned Interface	Supports bypassed and dynamic data path delay. Supports tri-state control.
GDDRX2_TX.ECLK.Centered	Generic DDR 4:1 Transmit Centered Interface	Supports bypassed and dynamic data path delay. Supports tri-state control. Required GDDR_SYNC support soft logic.
GDDRX2_TX.ECLK.Aligned	Generic DDR 4:1 Transmit Aligned Interface	Supports bypassed and dynamic data path delay. Supports tri-state control. Required GDDR_SYNC support soft logic.
GDDRX4_TX.ECLK.Centered	Generic DDR 8:1 Transmit Centered Interface	Supports bypassed and dynamic data path delay. Supports tri-state control. Required GDDR_SYNC support soft logic.
GDDRX4_TX.ECLK.Aligned	Generic DDR 8:1 Transmit Aligned Interface	Supports bypassed and dynamic data path delay. Supports tri-state control. Required GDDR_SYNC support soft logic.
GDDRX5_TX.ECLK.Centered	Generic DDR 10:1 Transmit Centered Interface	Supports bypassed and dynamic data path delay. Supports tri-state control. Required GDDR_SYNC support soft logic.
GDDRX5_TX.ECLK.Aligned	Generic DDR 10:1 Transmit Aligned Interface	Supports bypassed and dynamic data path delay. Supports tri-state control. Required GDDR_SYNC support soft logic.

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Table 2.2. Summary of GDDR Support Soft Logic

Feature	Description
GDDR_SYNC	Needed to tolerate large skew between stop and reset input.
RX_SYNC	Used to break up the DDRDLL to DLLDEL clock loop for aligned interface.

The following notes apply to Table 2.1 and Table 2.2:

- G – Generic
- _RX – Receive interface
- _TX – Transmit interface
- .SCLK – Uses SCLK (primary clock) clocking resource
- .ECLK – Uses ECLK (edge clock) clocking resource
- DDRX1 – DDR X1 gearing I/O Register
- DDRX2 – DDR X2 gearing I/O Registers
- DDRX4 – DDR X4 gearing I/O Registers
- DDRX5 – DDR X5 gearing I/O Registers
- .Centered – Clock is centered to the data when coming into the device
- .Aligned – The clock is coming in edge aligned to the Data

Figure 2.1 illustrates top-level design of GDDR I/O Soft IP.

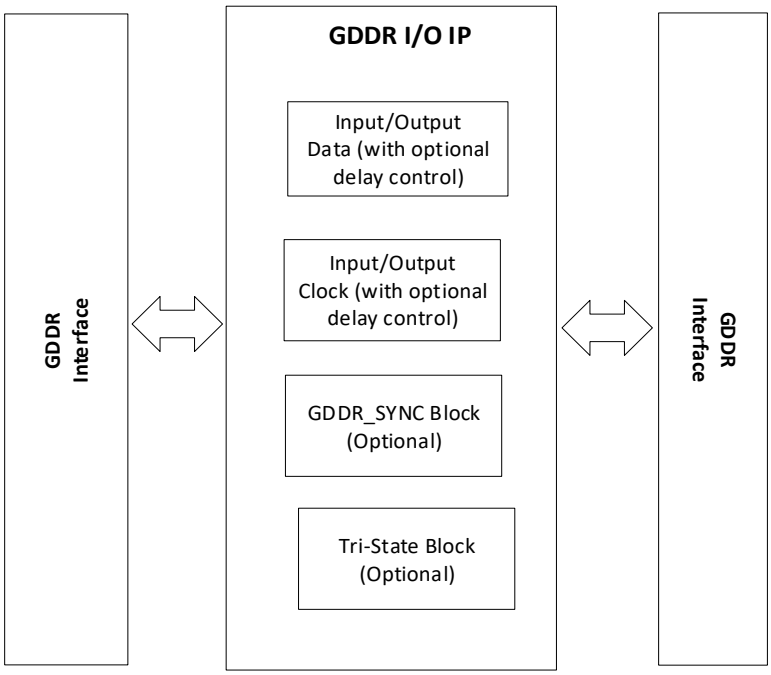

Figure 2.1. GDDR I/O Module Top-level Block Diagram

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2.2. Functional Diagrams

2.2.1. GDDRX1_RX.SCLK.Centered

This is a generic receive interface using X1 gearing and SCLK. The input clock is centered relative to the data. This interface can be used for DDR data rates below 500 Mb/s.

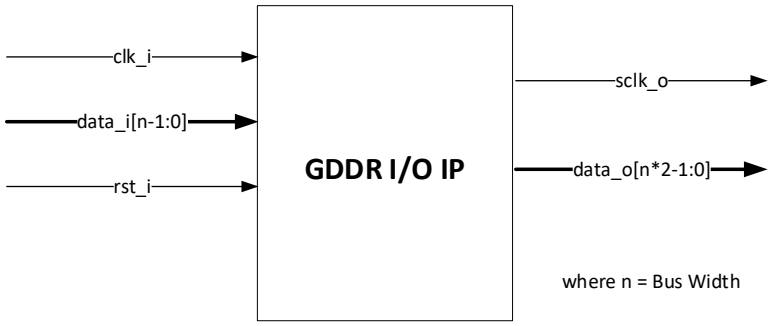

Figure 2.2. GDDRX1_RX.SCLK.Centered Bypass/Static Default/Static User-defined Delay Block Diagram

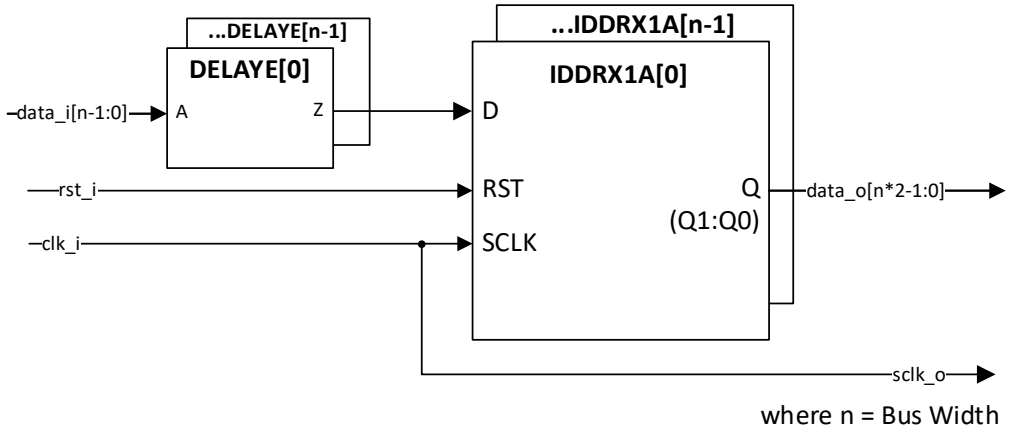

Figure 2.3. GDDRX1_RX.SCLK.Centered Bypass/Static Default/Static User-defined Delay Interface

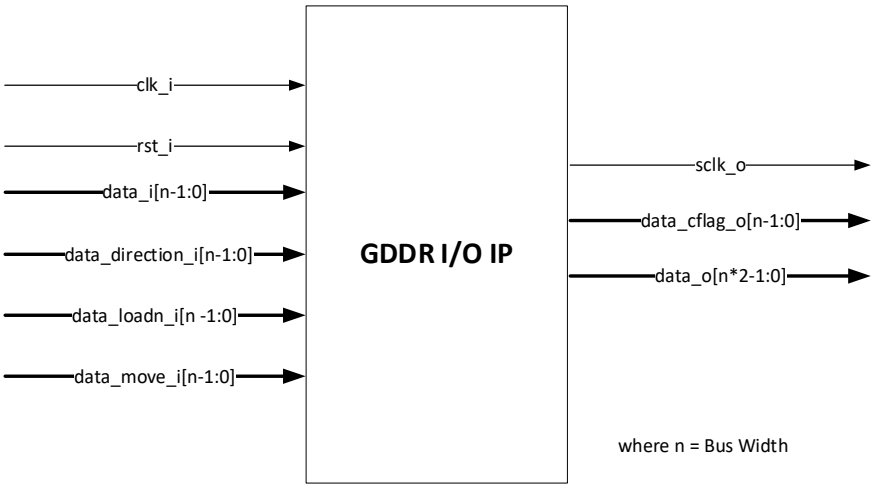

Figure 2.4. GDDRX1_RX.SCLK.Centered Dynamic Default/Dynamic User-defined Delay Block Diagram

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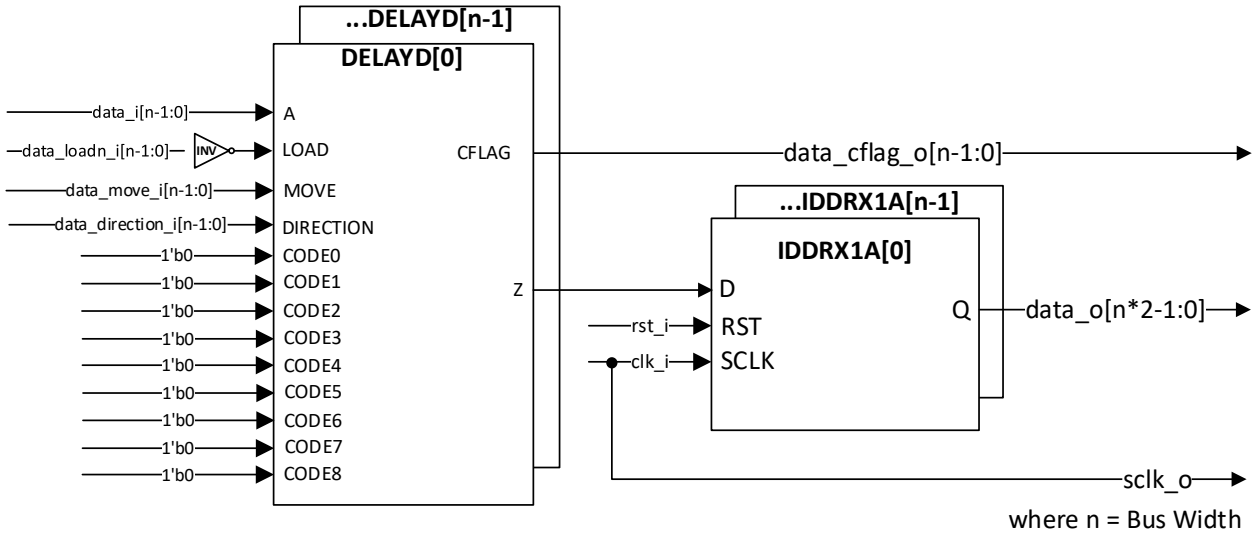

Figure 2.5. GDDRX1_RX.SCLK.Centered Dynamic Default/Dynamic User-defined Delay Interface

2.2.2. GDDRX1_RX.SCLK.Aligned

This is a generic receive interface using X1 gearing and SCLK. The input clock is edge aligned to the data. This interface can be used for DDR data rates up to 500 Mb/s.

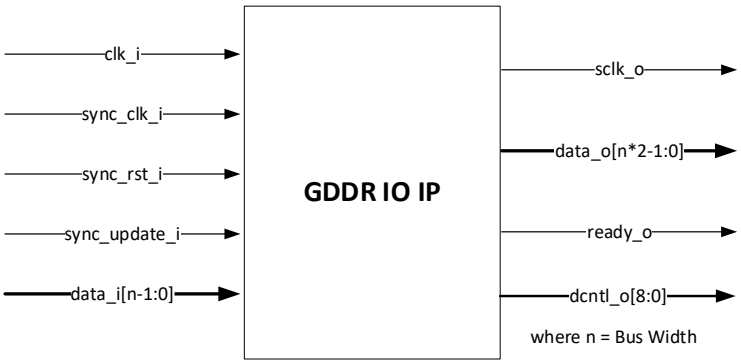

Figure 2.6. GDDRX1_RX.SCLK.Aligned Bypass/Static Default/Static User-defined Delay Block Diagram

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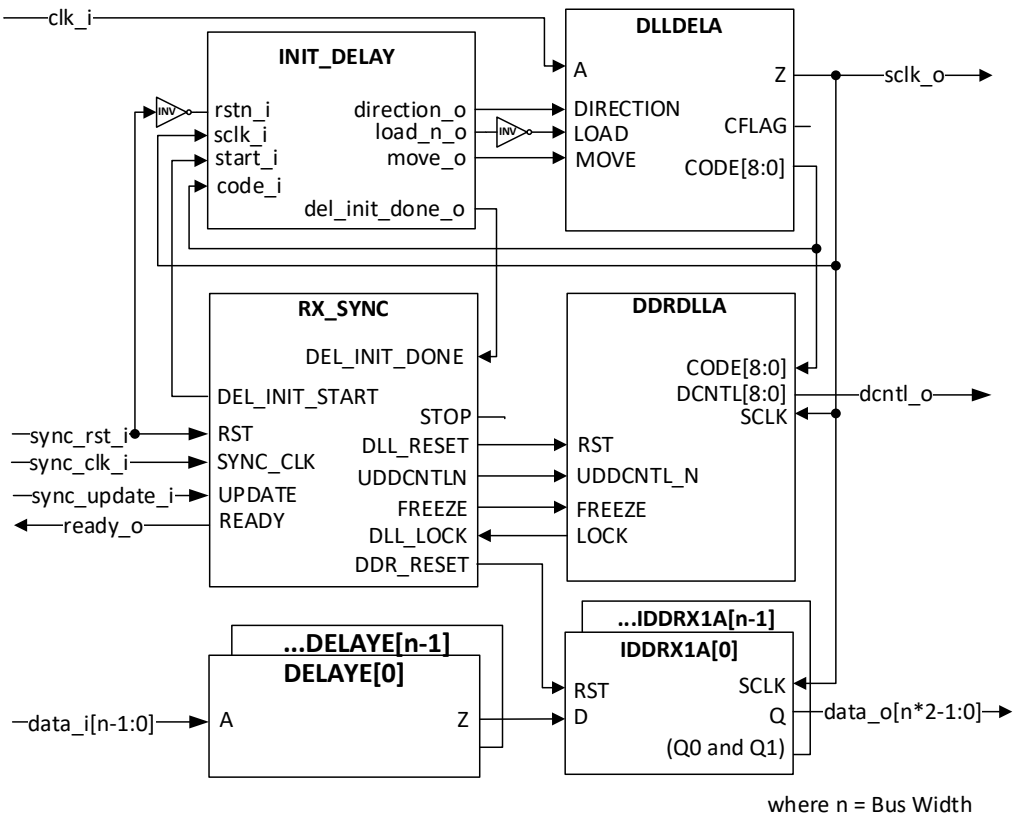

Figure 2.7. GDDRX1_RX.SCLK.Aligned Bypass/Static Default/Static User-defined Interface

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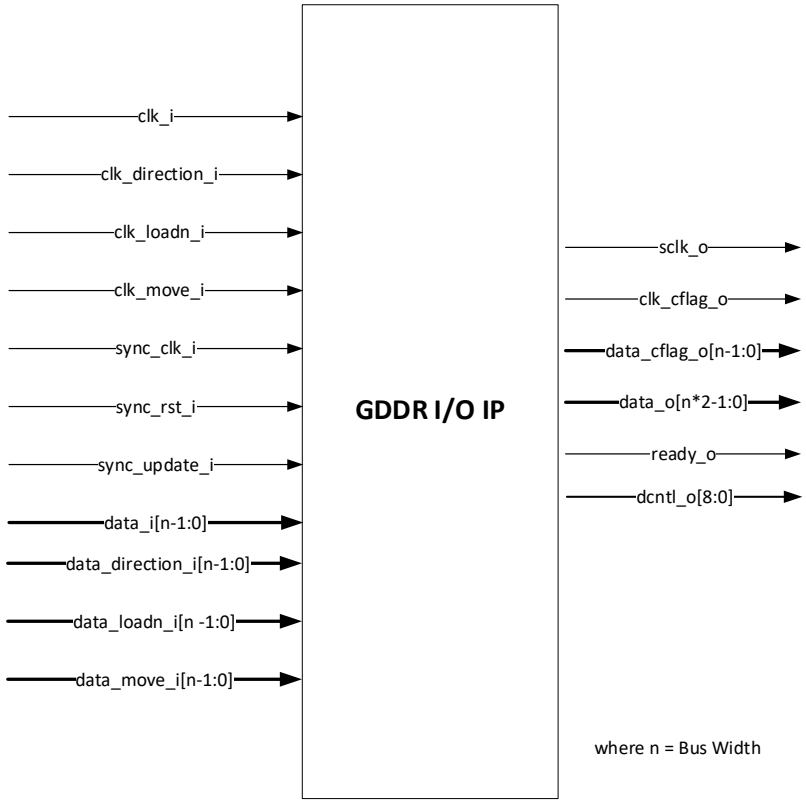

Figure 2.8. GDDRX1_RX.SCLK.Aligned Dynamic Default/User-Defined (Data) and Dynamic User-defined Delay (Clock) Block Diagram

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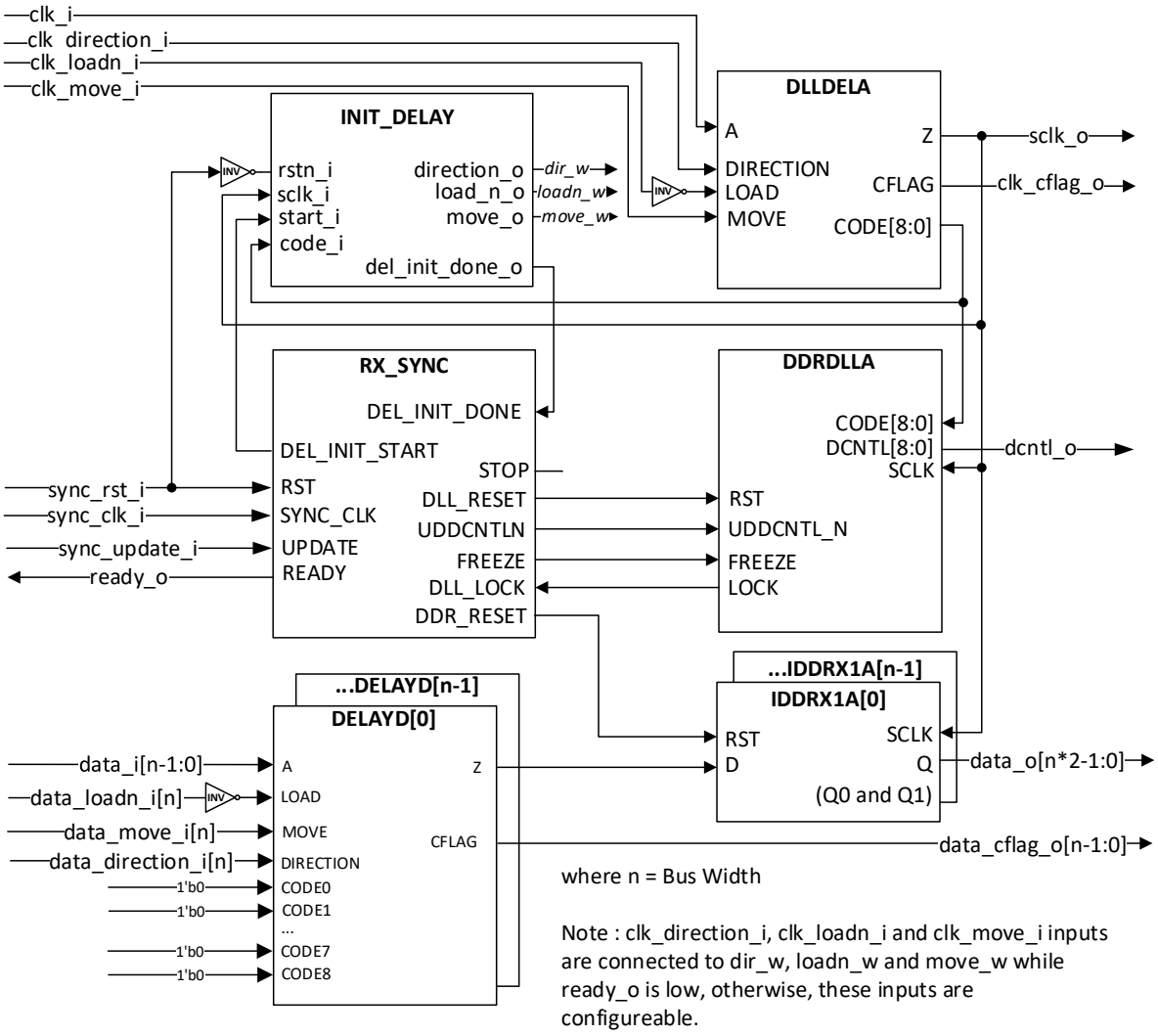

Figure 2.9. GDDRX1_RX.SCLK.Aligned Dynamic Default/User-Defined (Data) and Dynamic User-defined Delay (Clock) Interface

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2.2.3. GDDRX2/4/5_RX.ECLK.Centered

These are generic receive interfaces using X2, X4, or X5 gearing and Edge Clock Tree (ECLK). The input clock is centered relative to the data. These interfaces must be used for DDR data rates above 500 Mb/s.

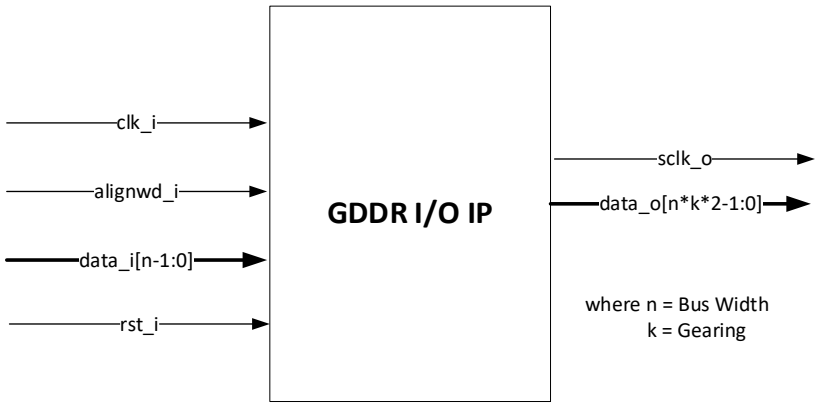

Figure 2.10. GDDRX2/4/5_RX.ECLK.Centered Bypass/Static Default/Static User-defined Delay Block Diagram

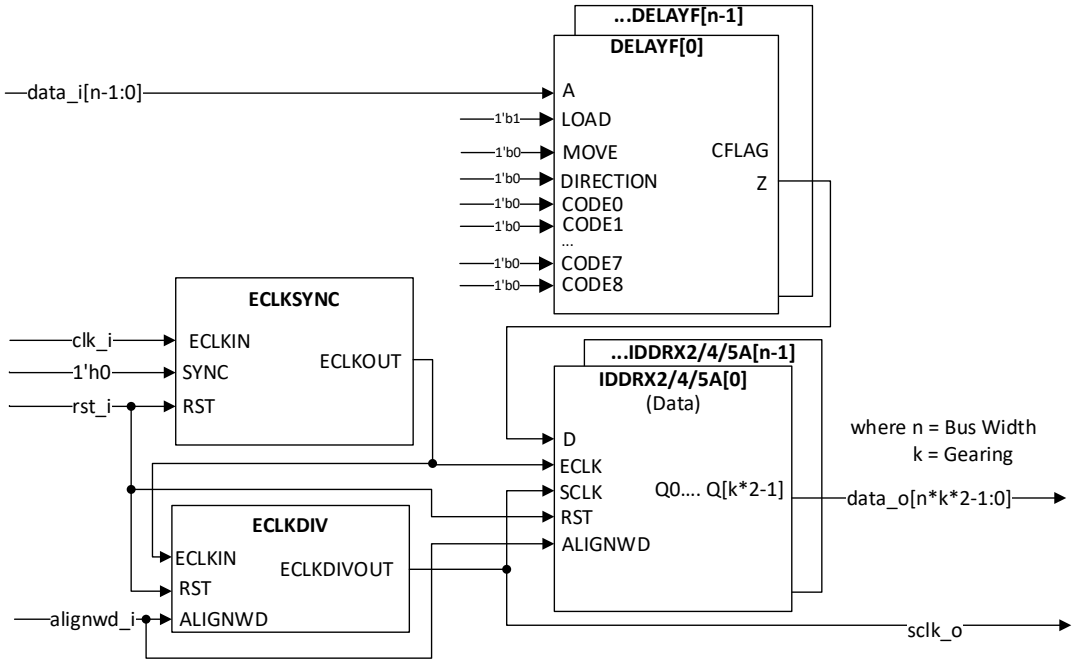

Figure 2.11. GDDRX2/4/5_RX.ECLK.Centered Bypass/Static Default/Static User-defined Delay Interface

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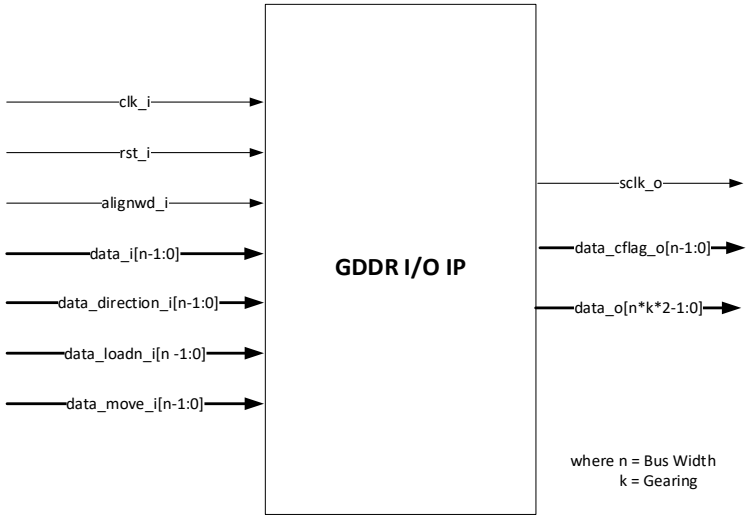

Figure 2.12. GDDRX2/4/5_RX.ECLK.Centered Dynamic Default/Dynamic User-defined Delay Block Diagram

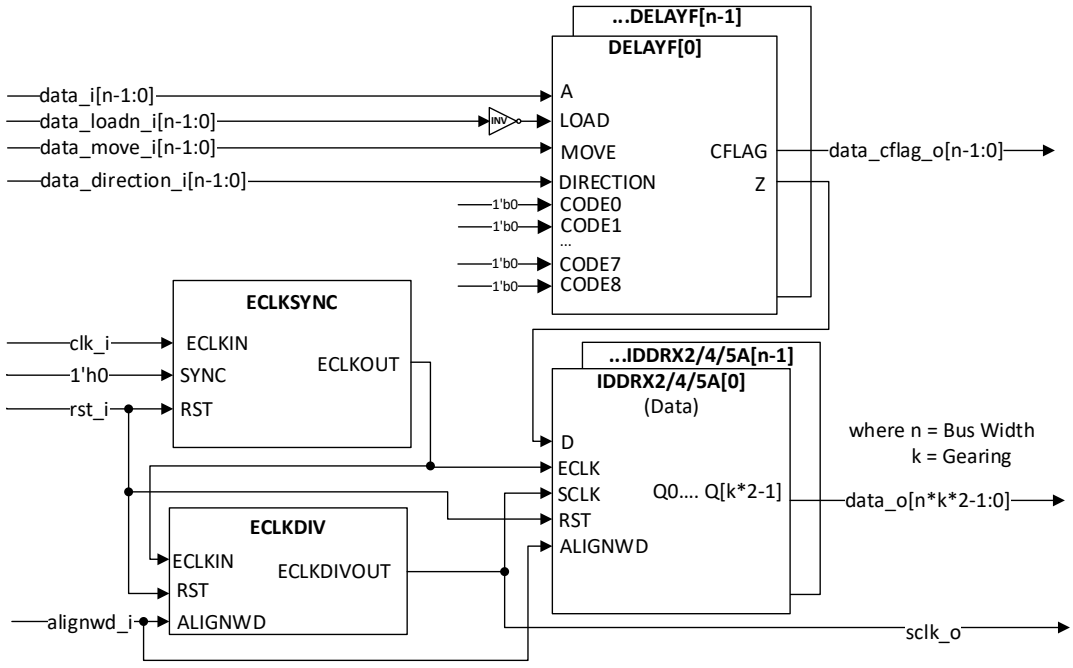

Figure 2.13. GDDRX2/4/5_RX.ECLK.Centered Dynamic Default/Dynamic User-defined Delay Interface

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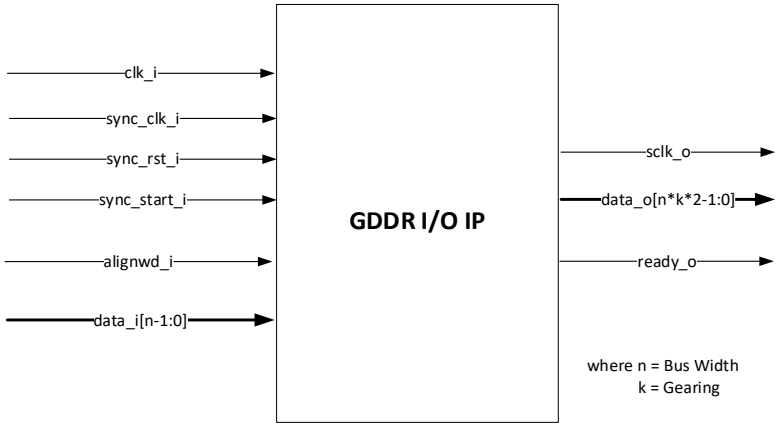

Figure 2.14. GDDRX2/4/5_RX.ECLK.Centered Bypass/Static Default/Static User-defined Delay with GDDR_SYNC Block Diagram

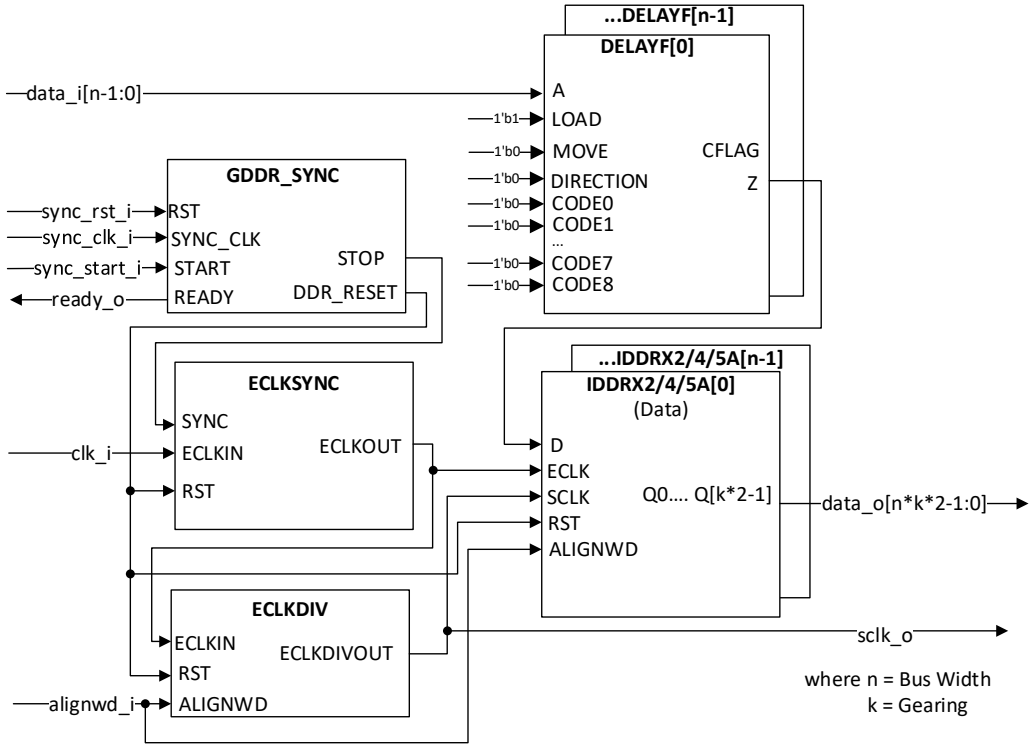

Figure 2.15. GDDRX2/4/5_RX.ECLK.Centered Bypass/Static Default/Static User-defined Delay with GDDR_SYNC Interface

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2.2.4. GDDRX2/4/5_RX.ECLK.Aligned

These are generic receive interfaces using X2, X4, or X5 gearing and Edge Clock Tree (ECLK). The input clock is edge aligned to the data. These interfaces must be used for DDR data rates above 500 Mb/s.

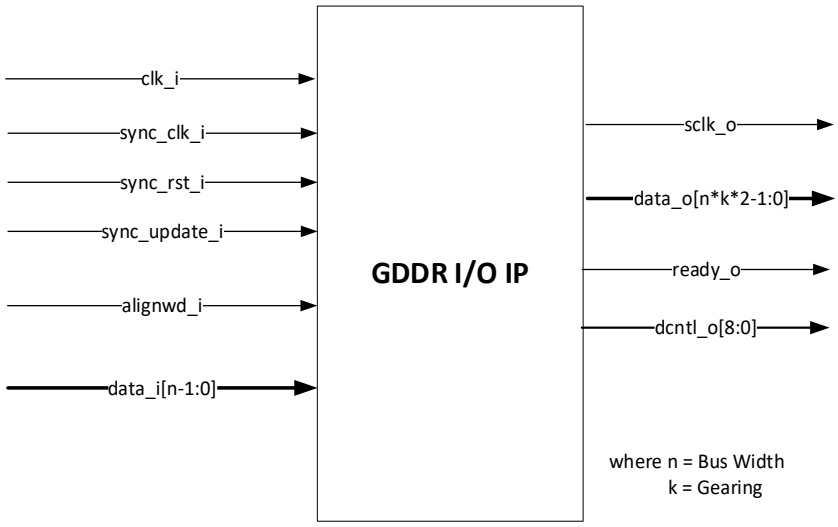

Figure 2.16. GDDRX2/4/5_RX.ECLK.Aligned Bypass/Static Default/Static User-defined Delay Block Diagram

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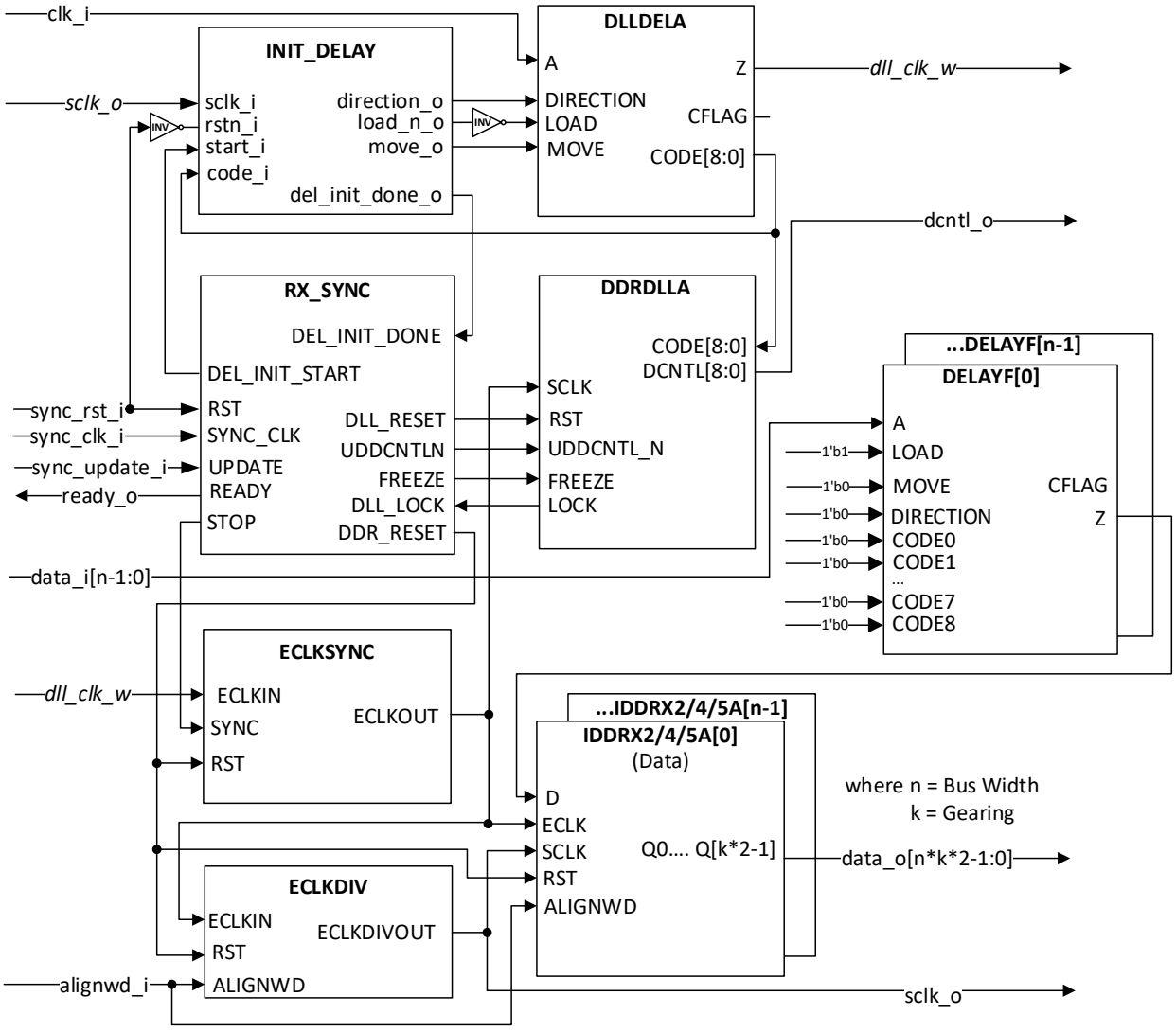

Figure 2.17. GDDRX2/4/5_RX.ECLK.Aligned Bypass/Static Default/Static User-defined Interface

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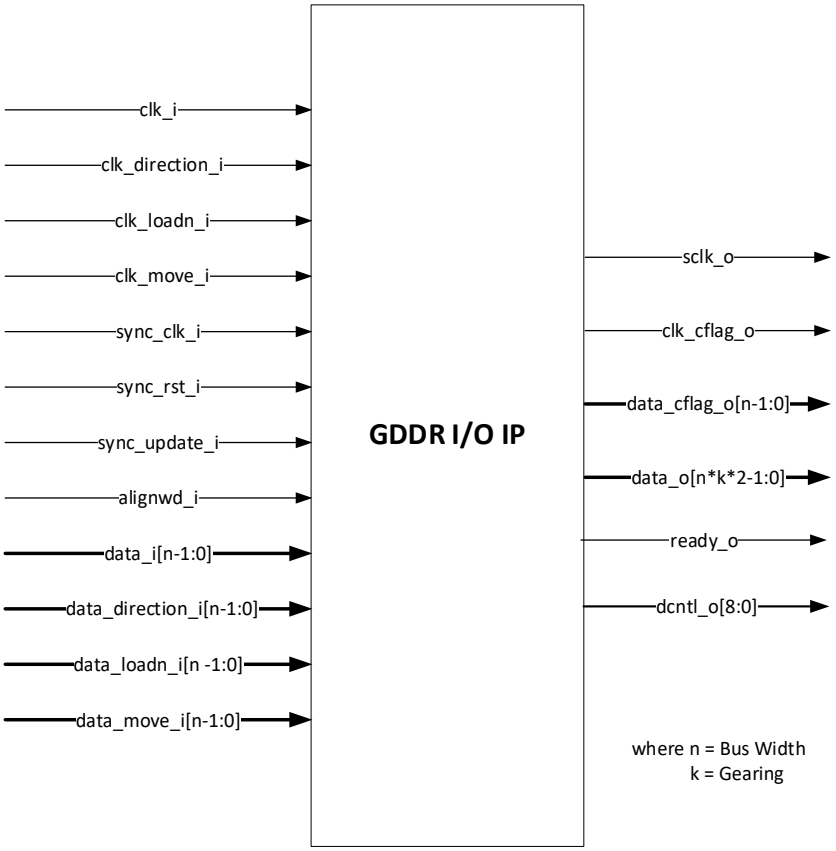

Figure 2.18. GDDRX2/4/5_RX.ECLK.Aligned Dynamic Default/Dynamic User-defined Delay Block Diagram

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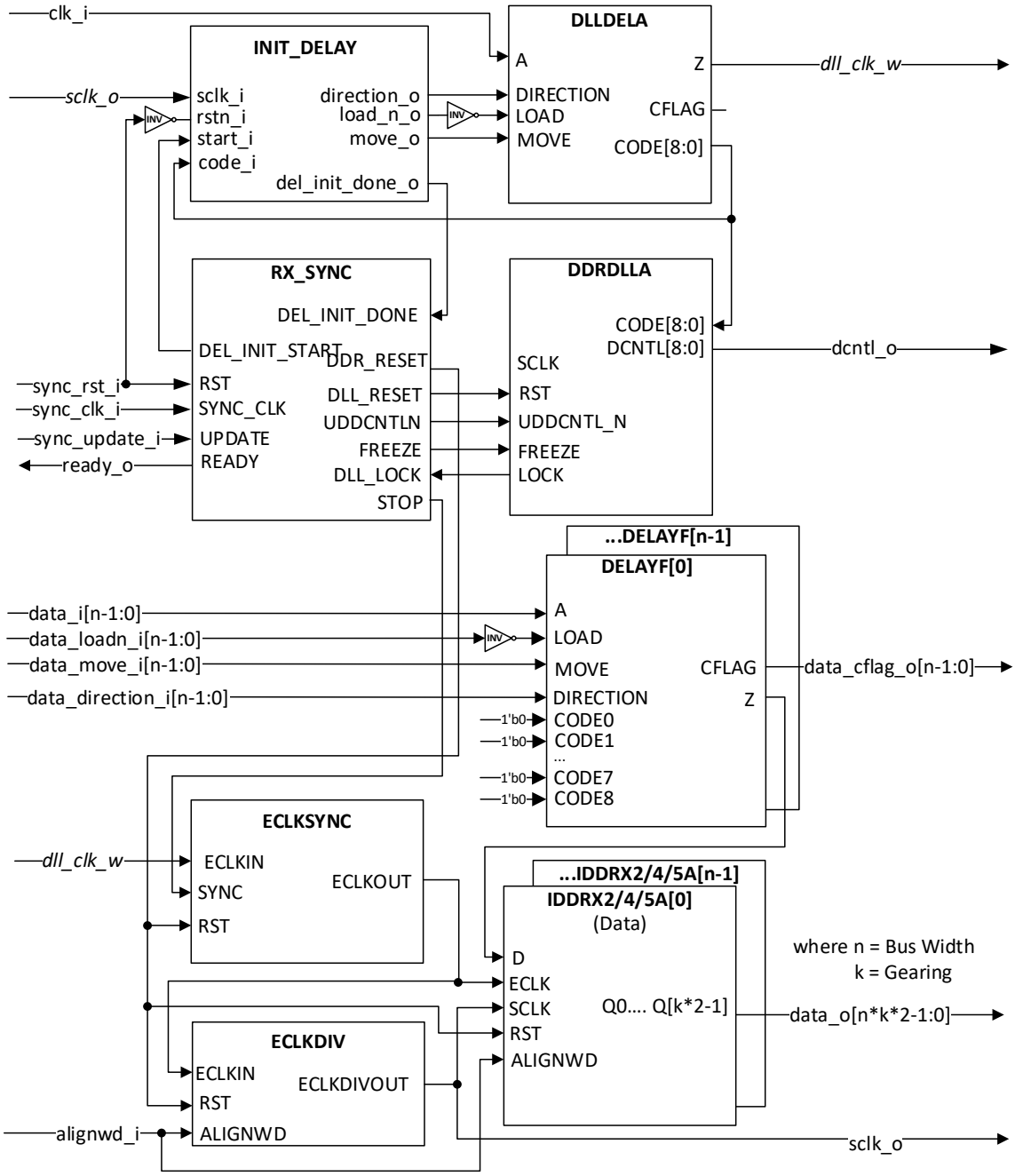

Figure 2.19. GDDRX2/4/5_RX.ECLK.Aligned Dynamic Default/Dynamic User-defined Delay Interface

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2.2.5. GDDRX1_TX.SCLK.Centered

This is a generic transmit interface using X1 gearing and SCLK. The input clock is centered relative to the data. This interface can be used for DDR data rates below 500 Mb/s.

The clock used to generate the clock output is delayed 90 degrees to center the data at the output side.

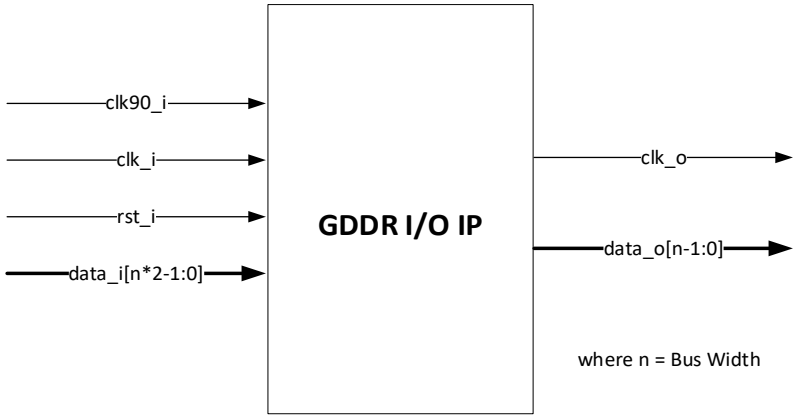

Figure 2.20. GDDRX1_TX.SCLK.Centered Bypass/Static User-defined Delay Block Diagram

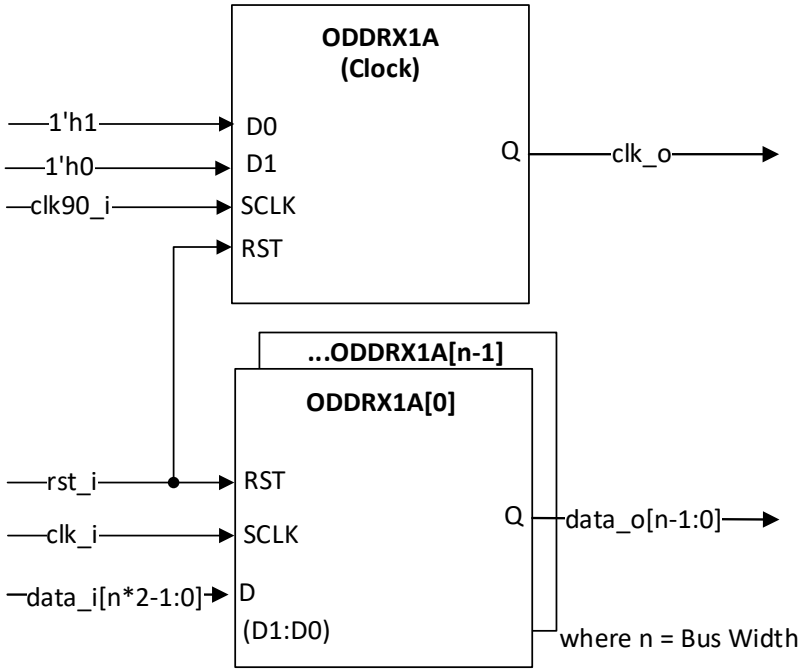

Figure 2.21. GDDRX1_TX.SCLK.Centered Bypass Interface

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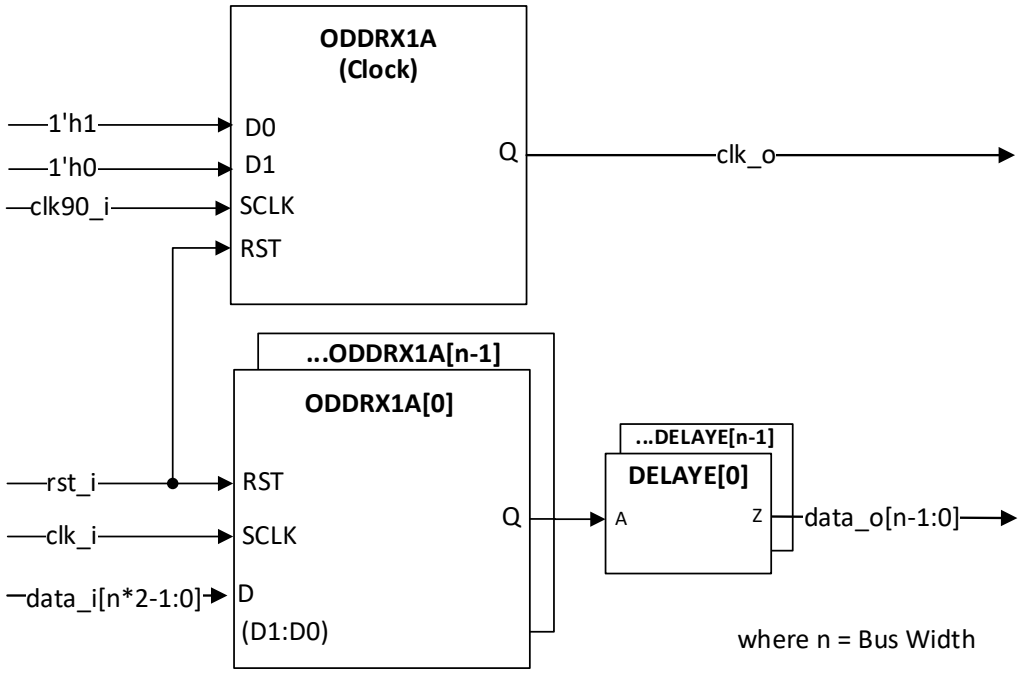

Figure 2.22. GDDRX1_TX.SCLK.Centered Static User-defined Delay Interface

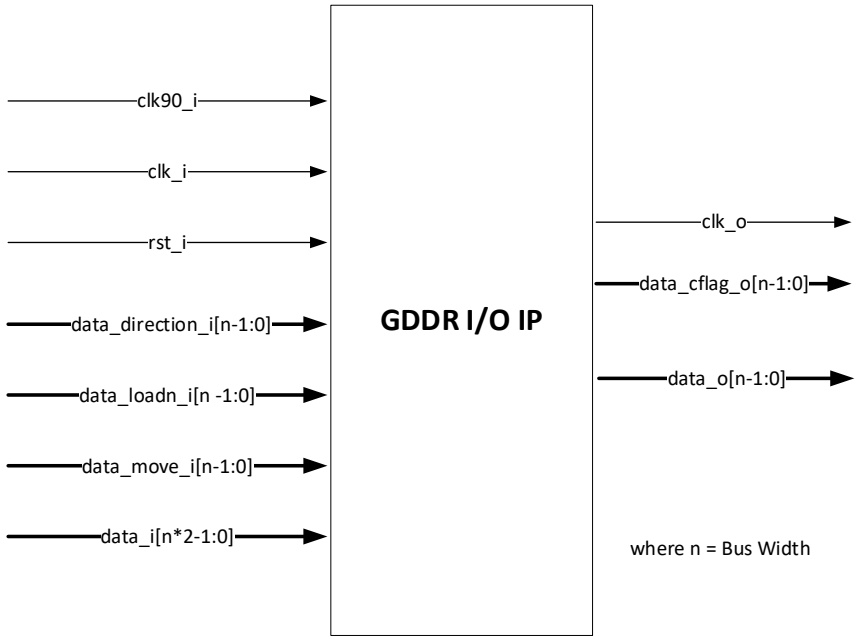

Figure 2.23. GDDRX1_TX.SCLK.Centered Dynamic User-defined Delay Block Diagram

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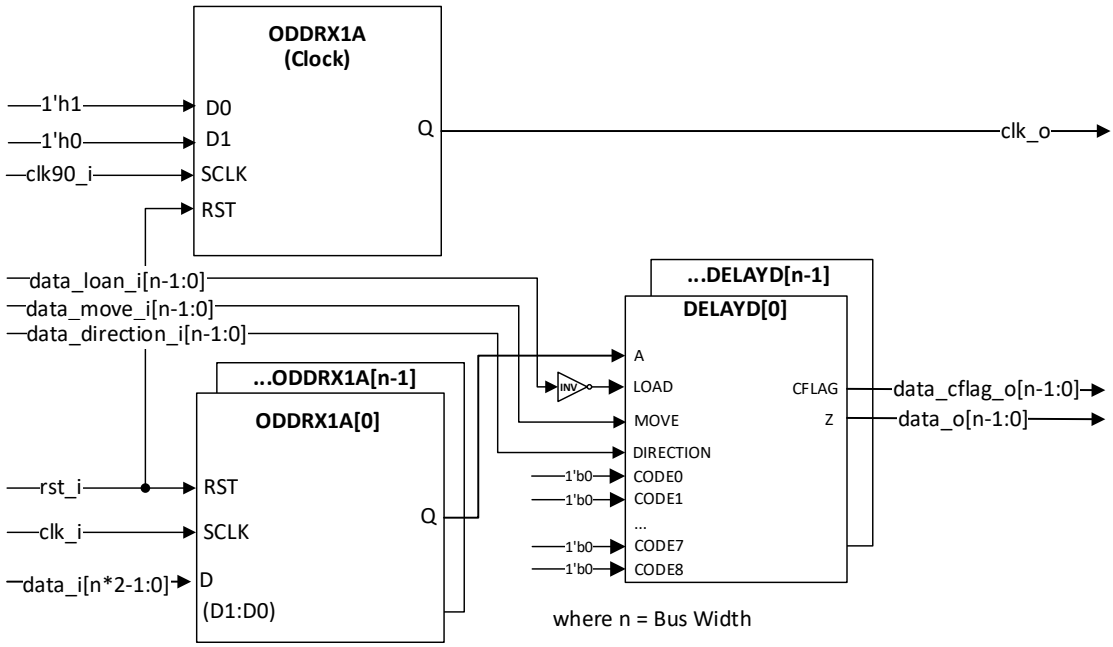

Figure 2.24. GDDRX1_TX.SCLK.Centered Dynamic User-defined Delay Interface

2.2.6. GDDRX1_TX.SCLK.Aligned

This is a generic transmit interface using X1 gearing and SCLK. The input clock is edge aligned to the data. This interface can be used for DDR data rates up to 500 Mb/s.

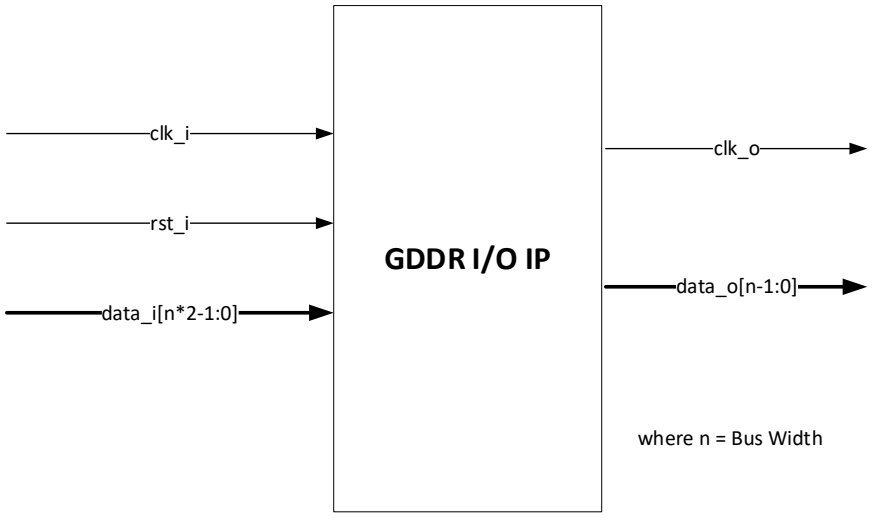

Figure 2.25. GDDRX1_TX.SCLK.Aligned Bypass/Static User-defined Delay Block Diagram

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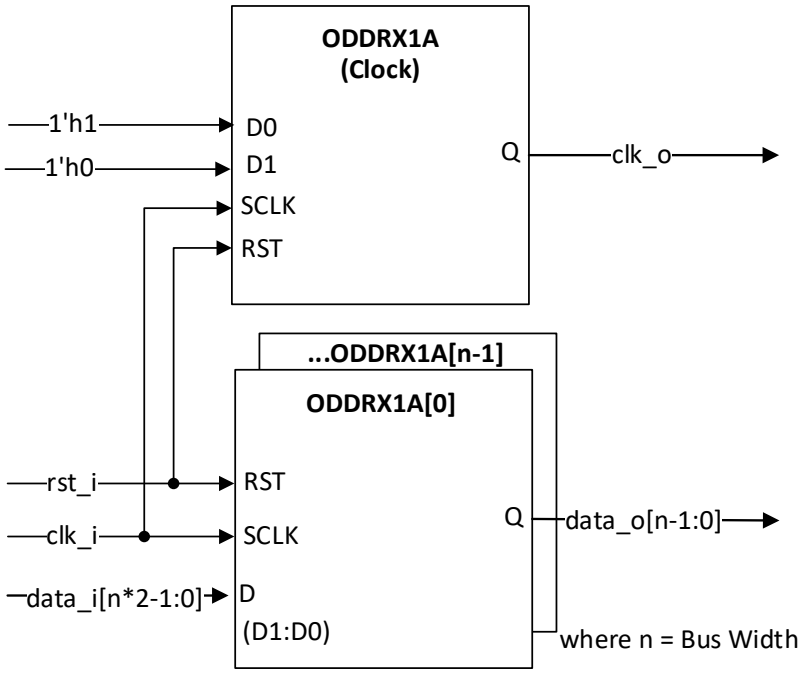

Figure 2.26. GDDRX1_TX.SCLK.Aligned Bypass Interface

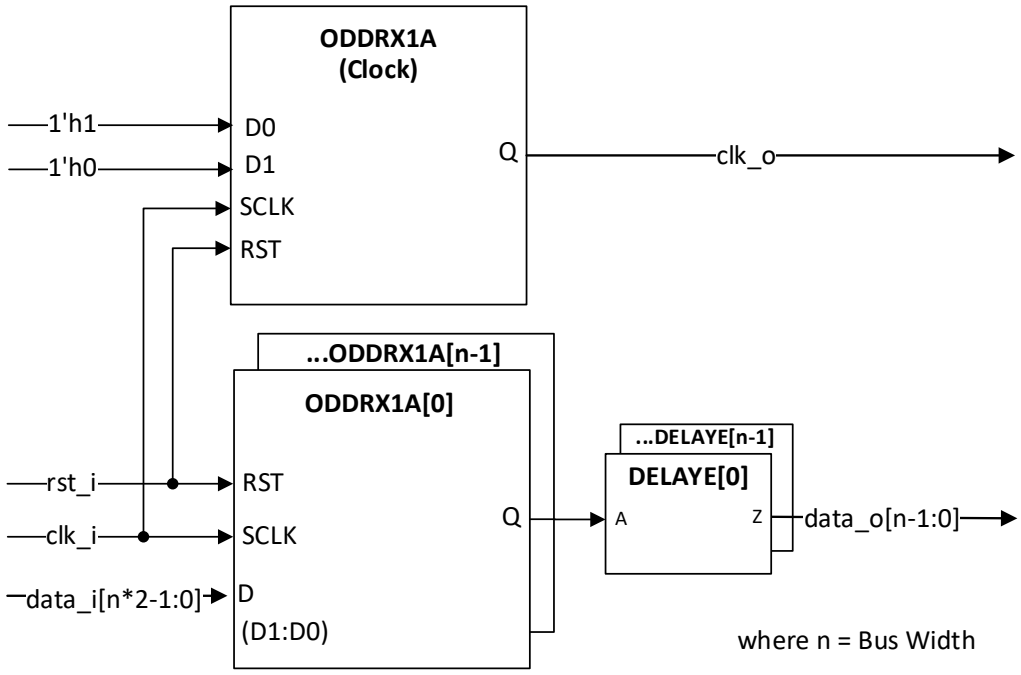

Figure 2.27. GDDRX1_TX.SCLK.Aligned Static User-defined Delay Interface

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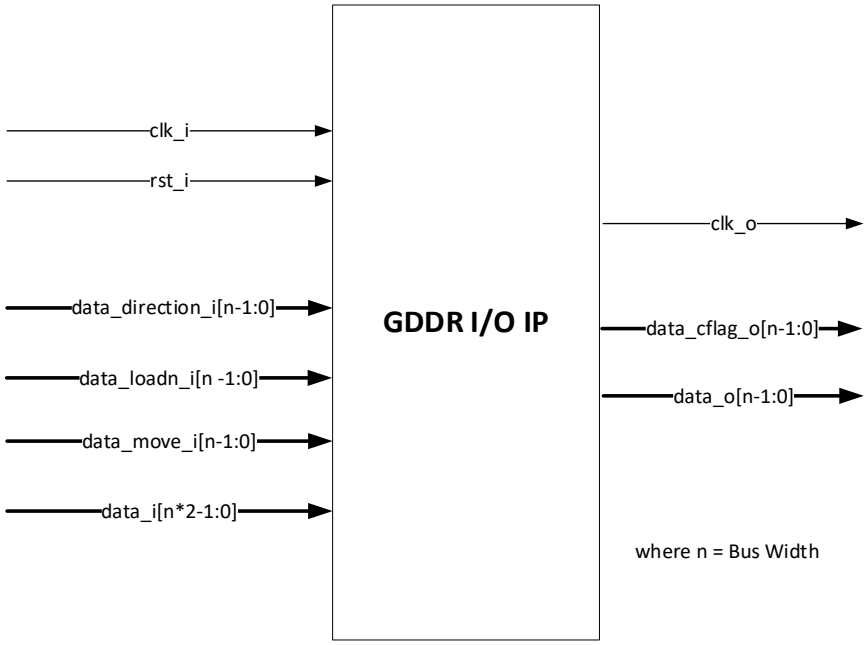

Figure 2.28. GDDRX1_TX.SCLK.Aligned Dynamic User-defined Delay Block Diagram

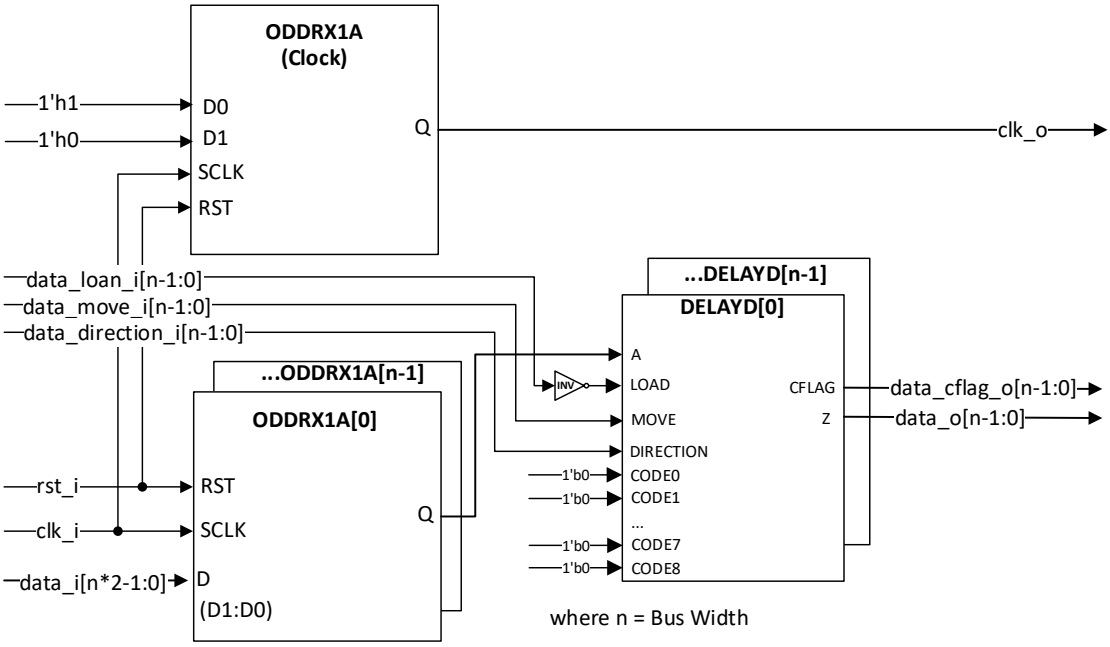

Figure 2.29. GDDRX1_TX.SCLK.Aligned Dynamic User-defined Delay Interface

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2.2.7. GDDRX2/4/5_TX.ECLK.Centered

These are generic transmit interfaces using X2, X4, or X5 gearing and Edge Clock Tree (ECLK). The input clock is centered relative to the data. These interfaces must be used for DDR data rates above 500 Mb/s.

The clock used to generate the clock output is delayed 90 degrees to center the data at the output side.

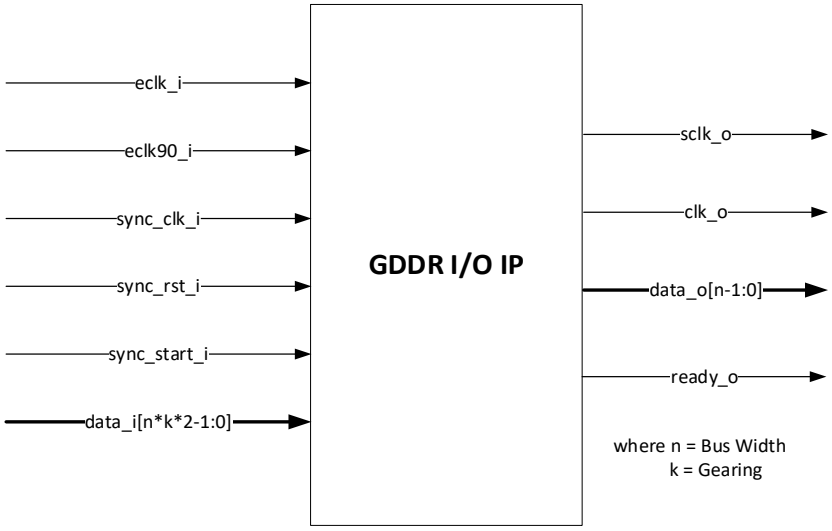

Figure 2.30. GDDRX2/4/5_TX.ECLK.Centered Bypass/Static User-defined Delay (with GDDR_SYNC) Block Diagram

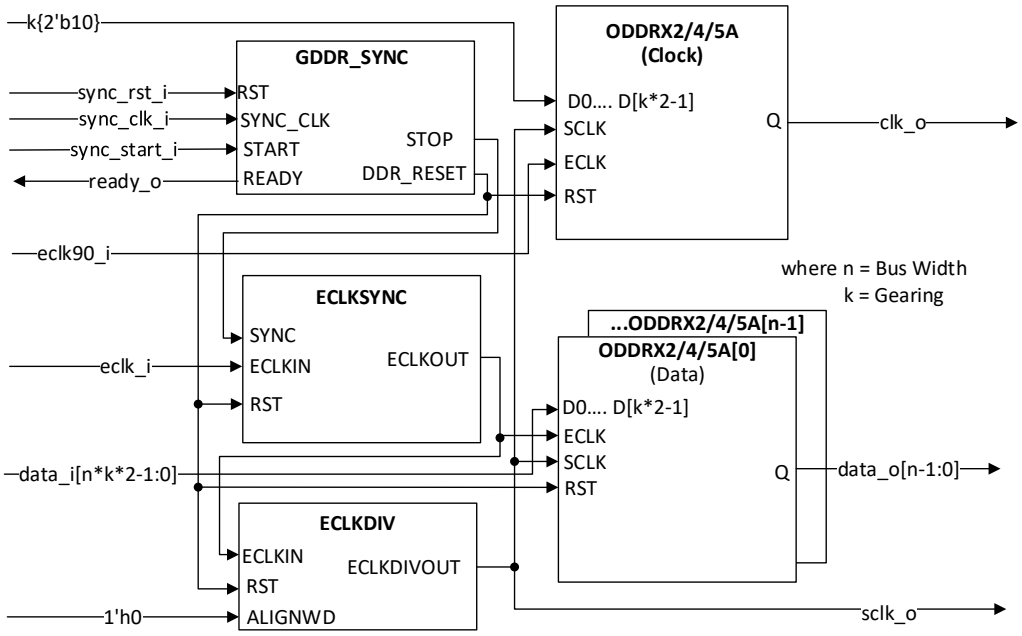

Figure 2.31. GDDRX2/4/5_TX.ECLK.Centered Bypass (with GDDR_SYNC) Interface

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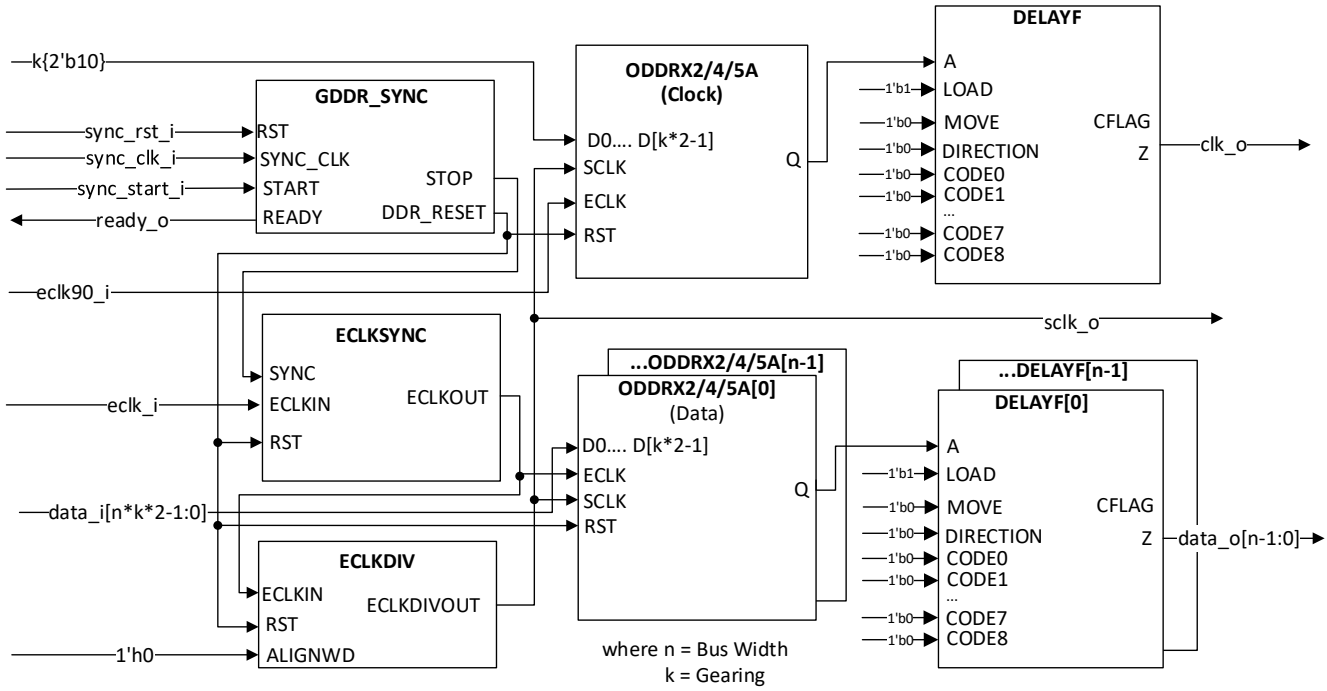

Figure 2.32. GDDRX2/4/5_TX.ECLK.Centered Static User-defined Delay (with GDDR_SYNC) Interface

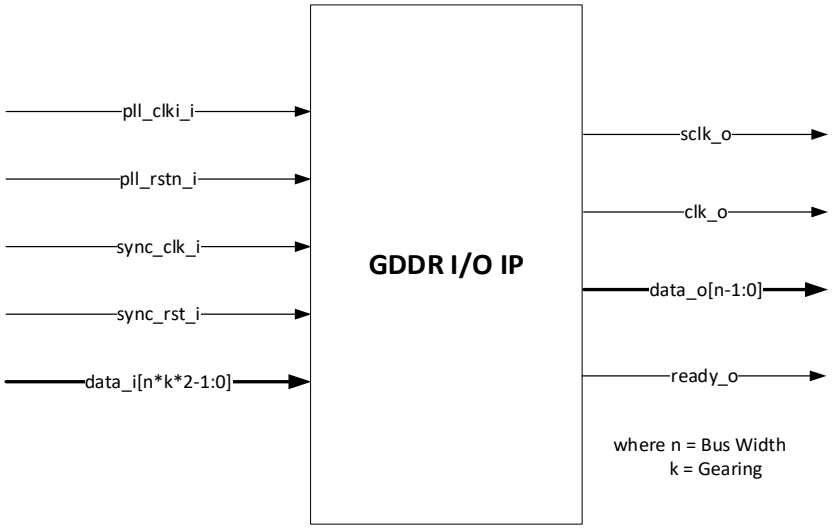

Figure 2.33. GDDRX2/4/5_TX.ECLK.Centered Bypass/Static User-defined Delay with PLL Block Diagram

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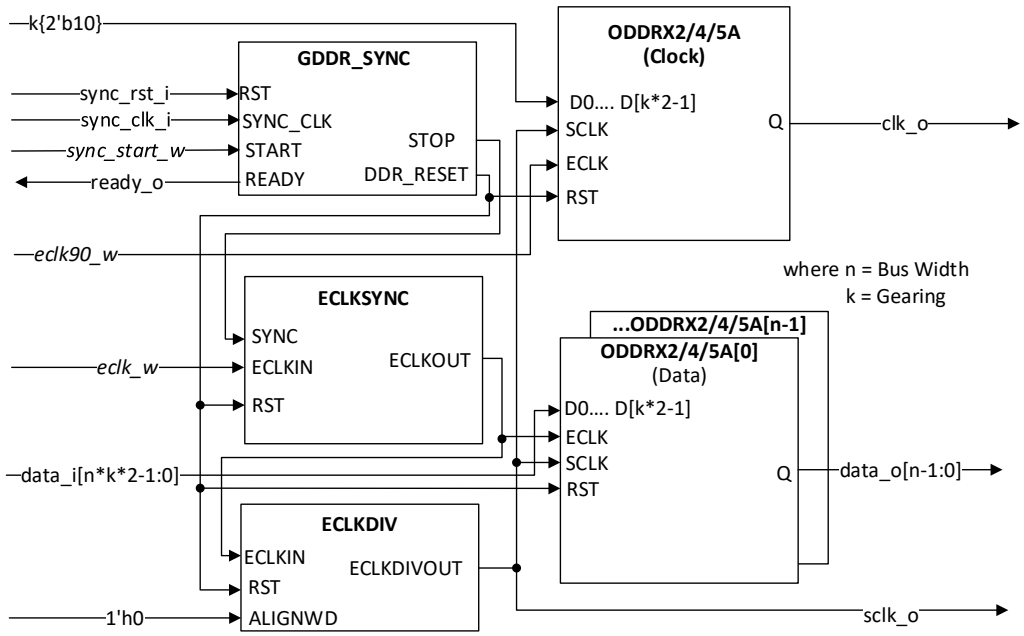

Figure 2.34. GDDRX2/4/5_TX.ECLK.Centered Bypass for PLL Interface

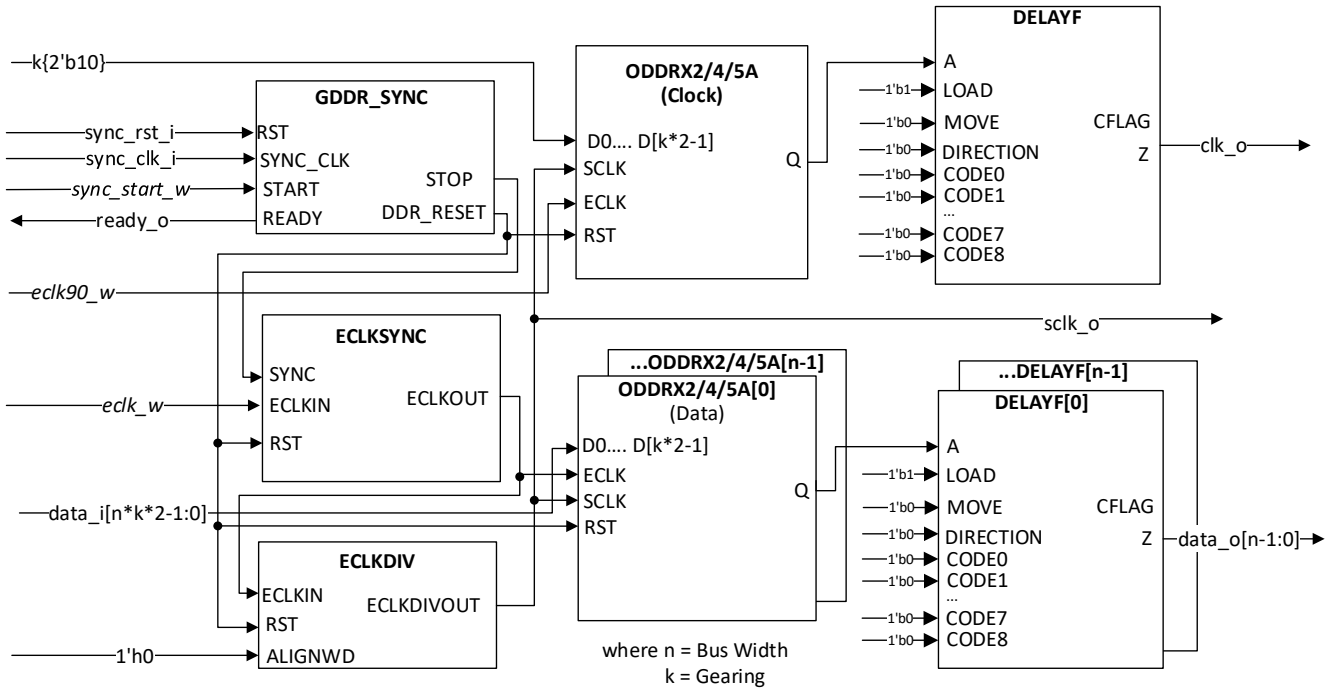

Figure 2.35. GDDRX2/4/5_TX.ECLK.Centered Static User-defined Delay for PLL Interface

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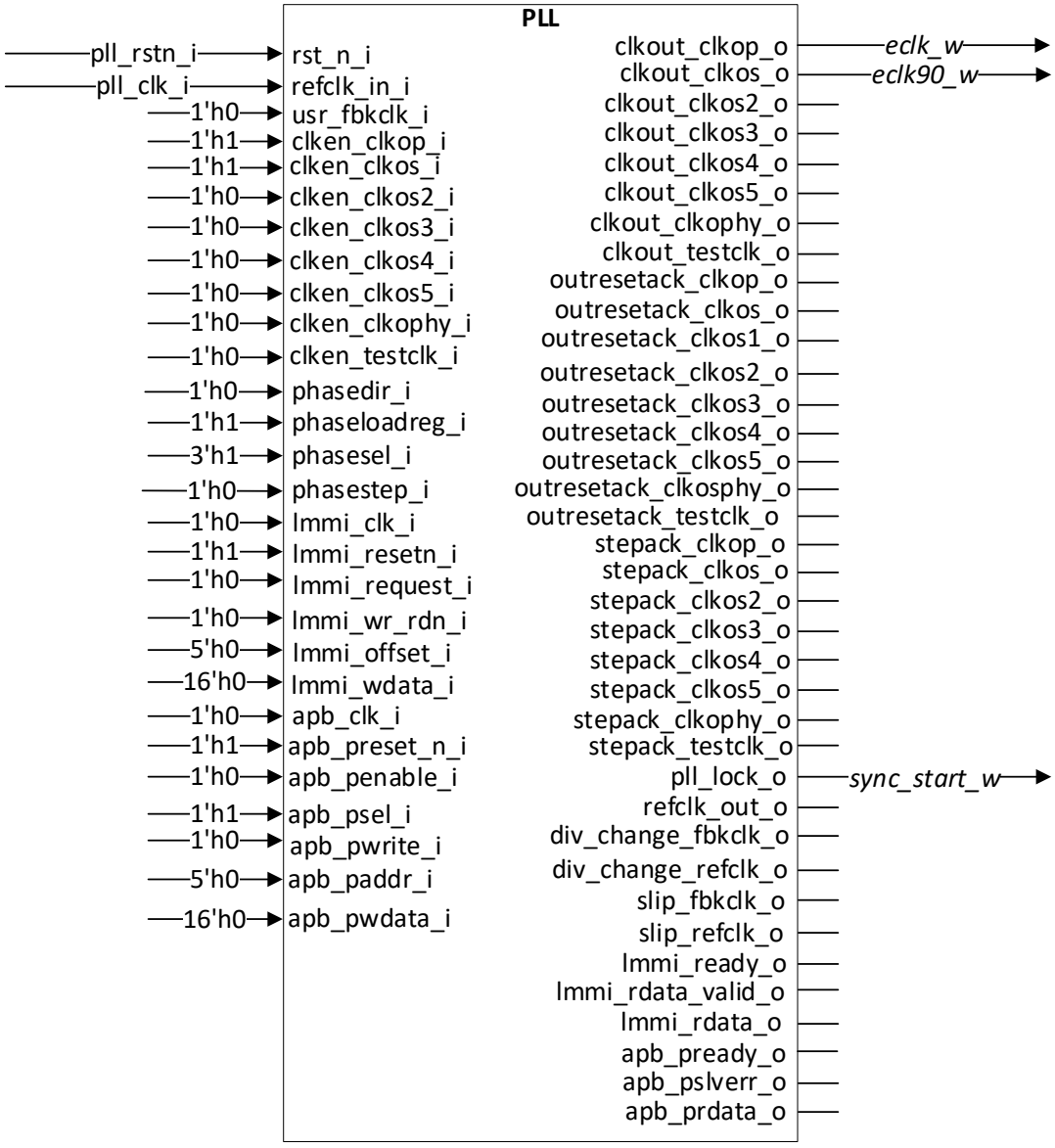

Figure 2.36. GDDRX2/4/5_TX.ECLK.Centered Bypass/Static User-defined Delay PLL Interface

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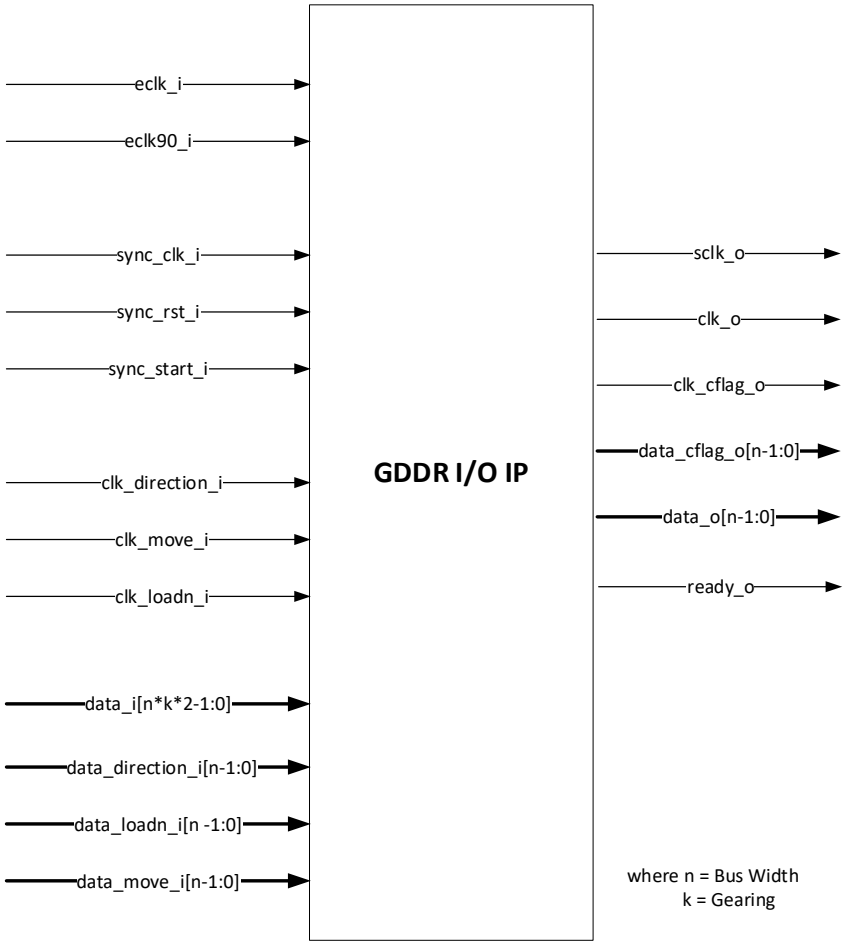

Figure 2.37. GDDRX2/4/5_TX.ECLK.Centered Dynamic User-defined Delay (with GDDR_SYNC) Block Diagram

The diagram presented in Figure 2.37 is true for both; Tristate Control enabled and disabled cases (with outen_n_i present in the Tristate Control enabled case).

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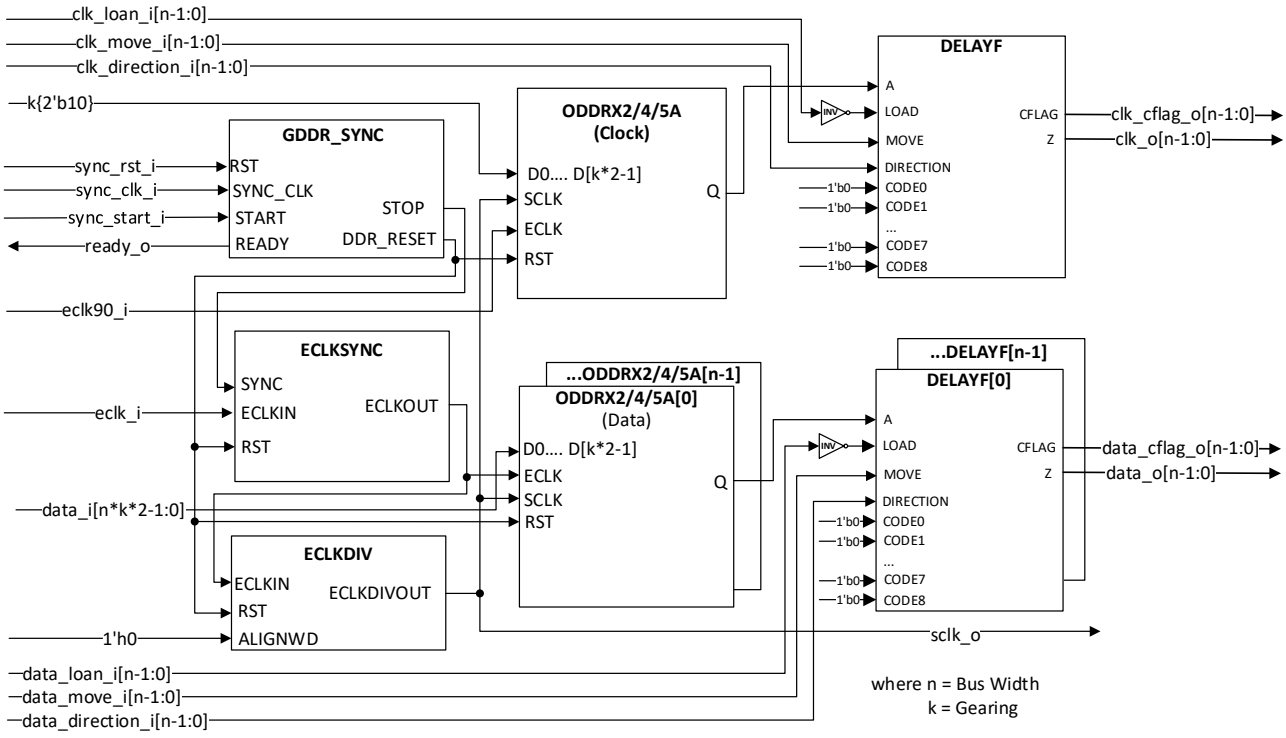

Figure 2.38. GDDRX2/4/5_TX.ECLK.Centered Dynamic User-defined Delay (with GDDR_SYNC) Block Diagram

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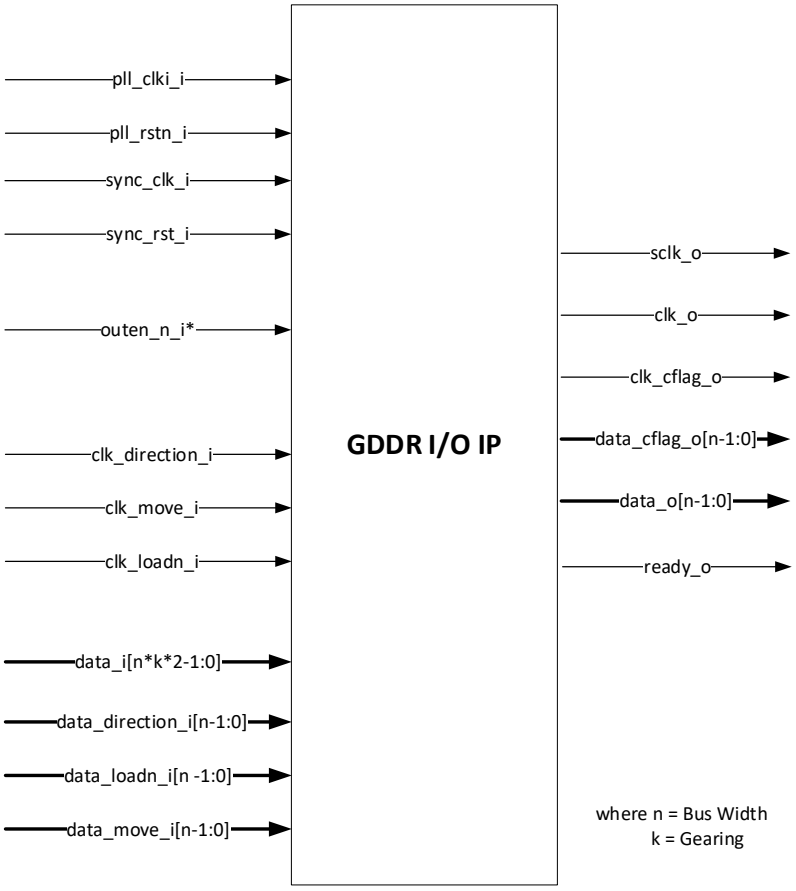

***Note:** Present only for Tristate Control Enabled case.

Figure 2.39. GDDRX2/4/5_TX.ECLK.Centered Dynamic User-defined Delay with PLL

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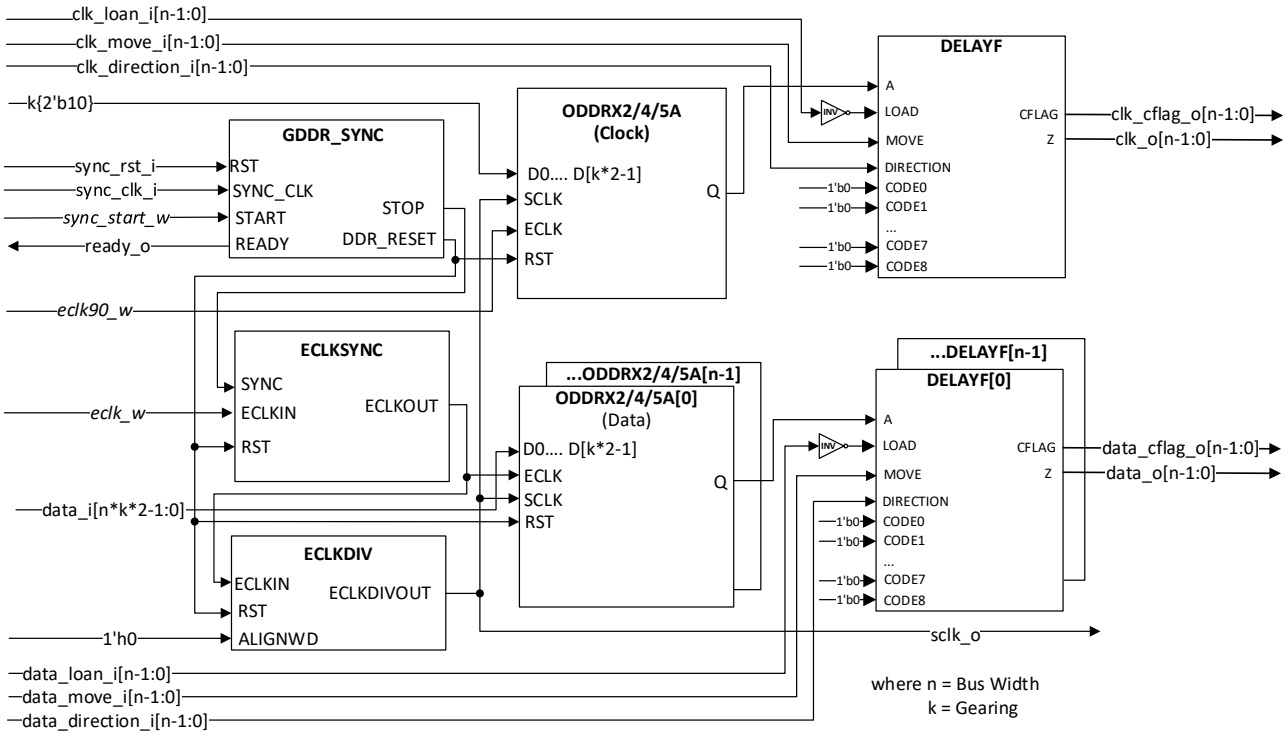

Figure 2.40. GDDRX2/4/5_TX.ECLK.Centered Dynamic User-defined Delay for PLL Interface

Figure 2.40 connects to Figure 2.36 for PLL interface.

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2.2.8. GDDRX2/4/5_TX.ECLK.Aligned

These are generic transmit interfaces using X2, X4, or X5 gearing and Edge Clock Tree (ECLK). The input clock is edge aligned to the data. These interfaces must be used for DDR data rates above 500 Mb/s.

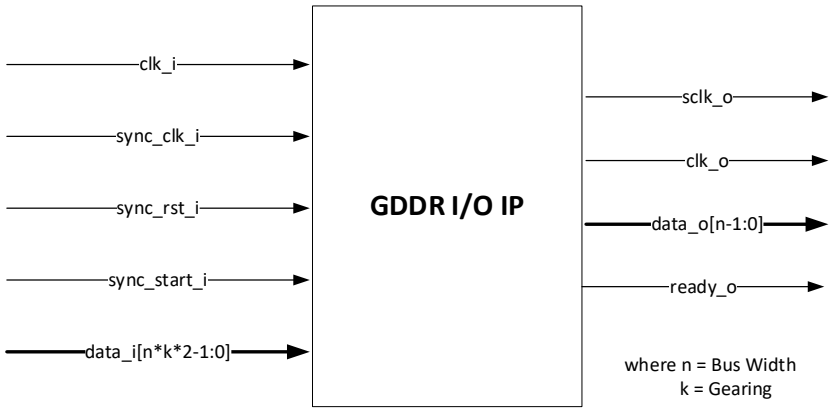

Figure 2.41. GDDRX2/4/5_TX.ECLK.Aligned Bypass/Static User-defined Delay GDDR_SYNC Enabled Block Diagram

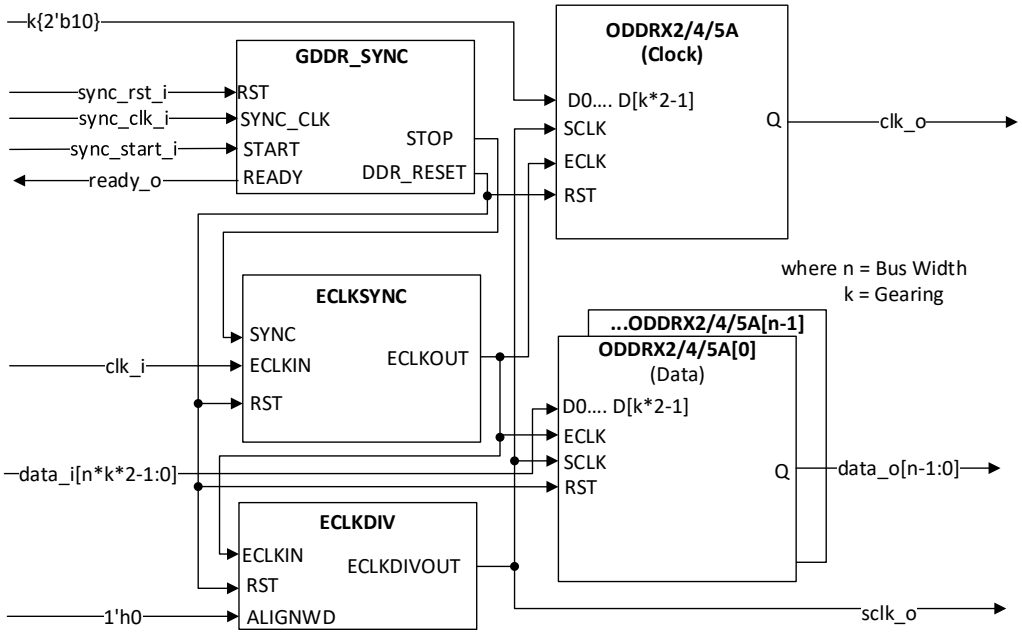

Figure 2.42. GDDRX2/4/5_TX.ECLK.Aligned Bypass with GDDR_SYNC Enabled Interface

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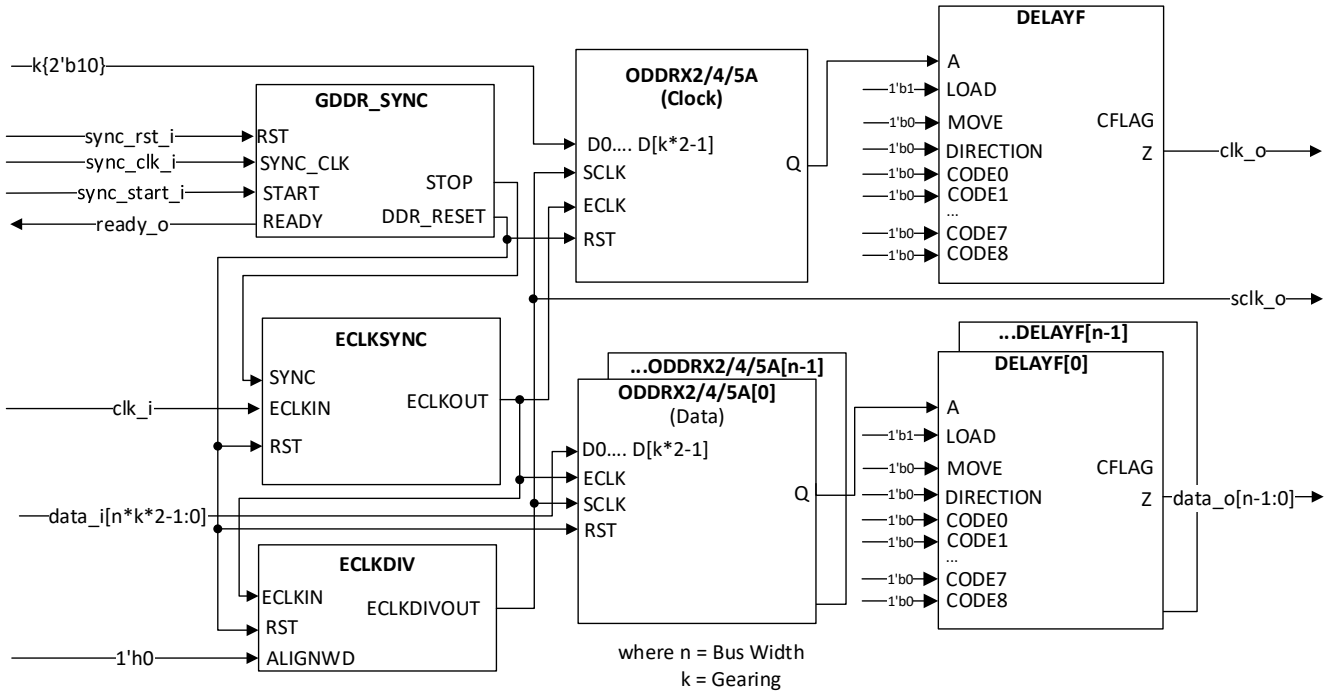

Figure 2.43. GDDRX2/4/5_TX.ECLK.Aligned Static User-defined Delay with GDDR_SYNC Enabled Block Diagram

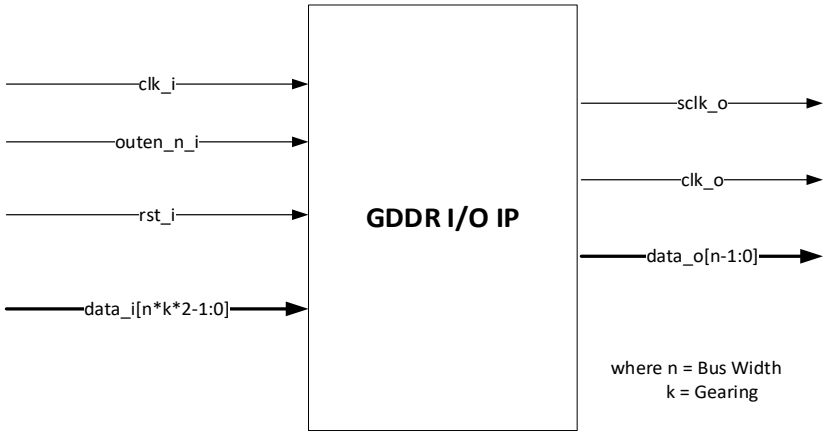

Figure 2.44. GDDRX2/4/5_TX.ECLK.Aligned Bypass/Static User-defined Delay Tristate Control Enabled Block Diagram

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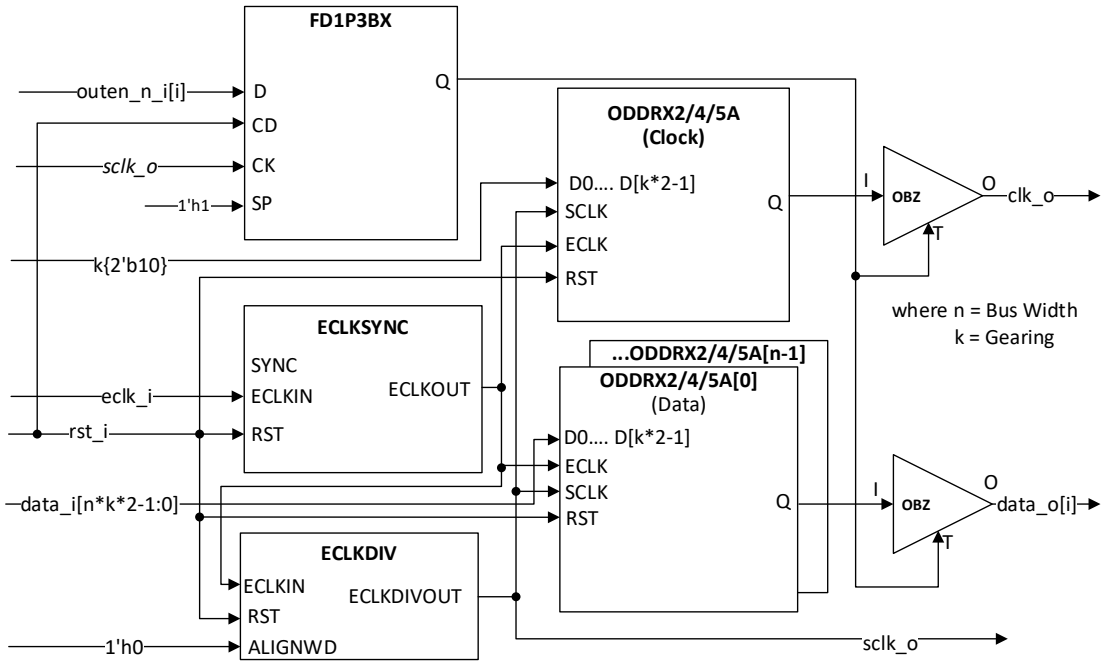

Figure 2.45. GDDRX2/4/5_TX.ECLK.Aligned Bypass Tristate Control Enabled Block Diagram

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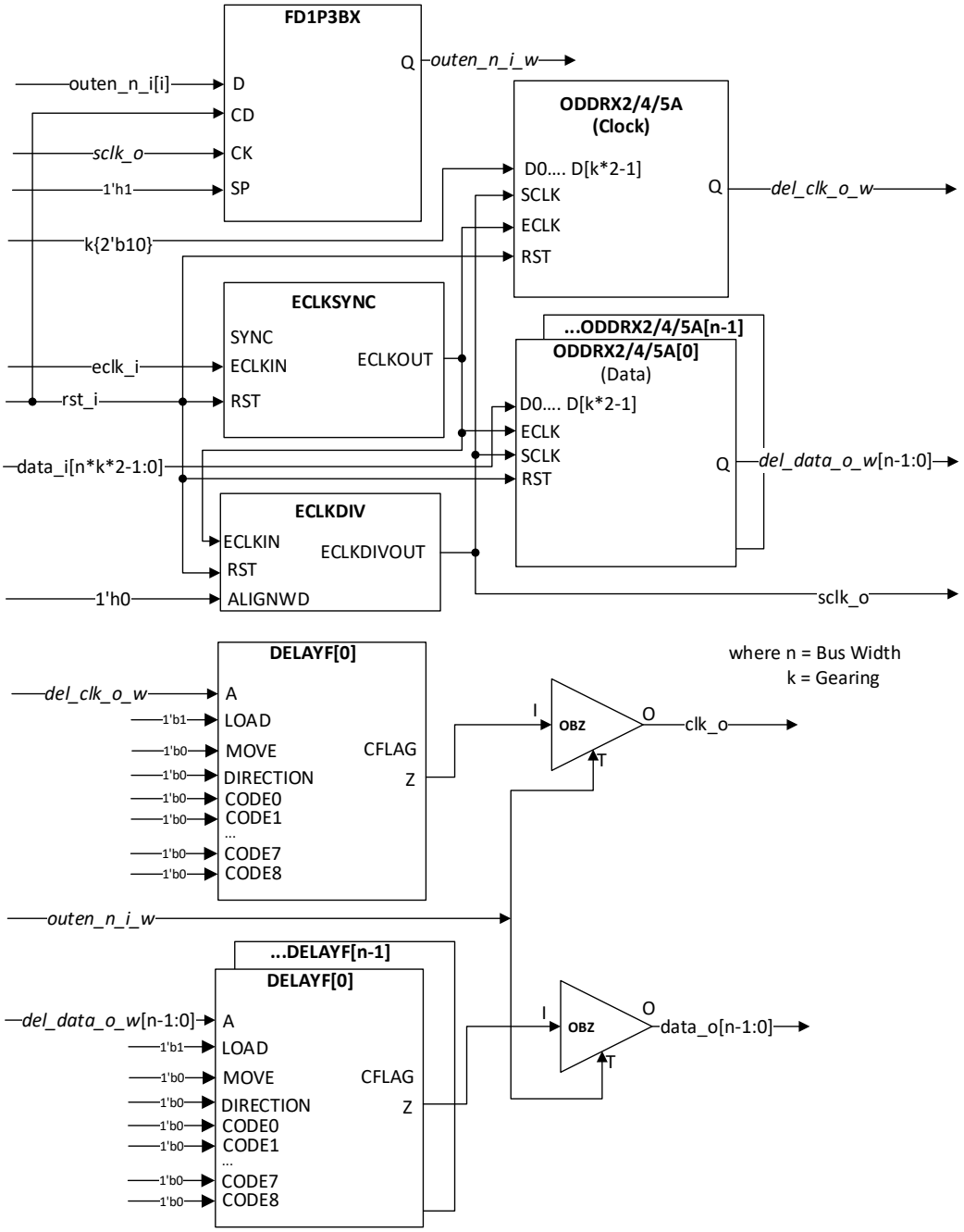

Figure 2.46. GDDRX2/4/5_TX.ECLK.Aligned Static User-defined Delay Tristate Control Enabled Block Diagram

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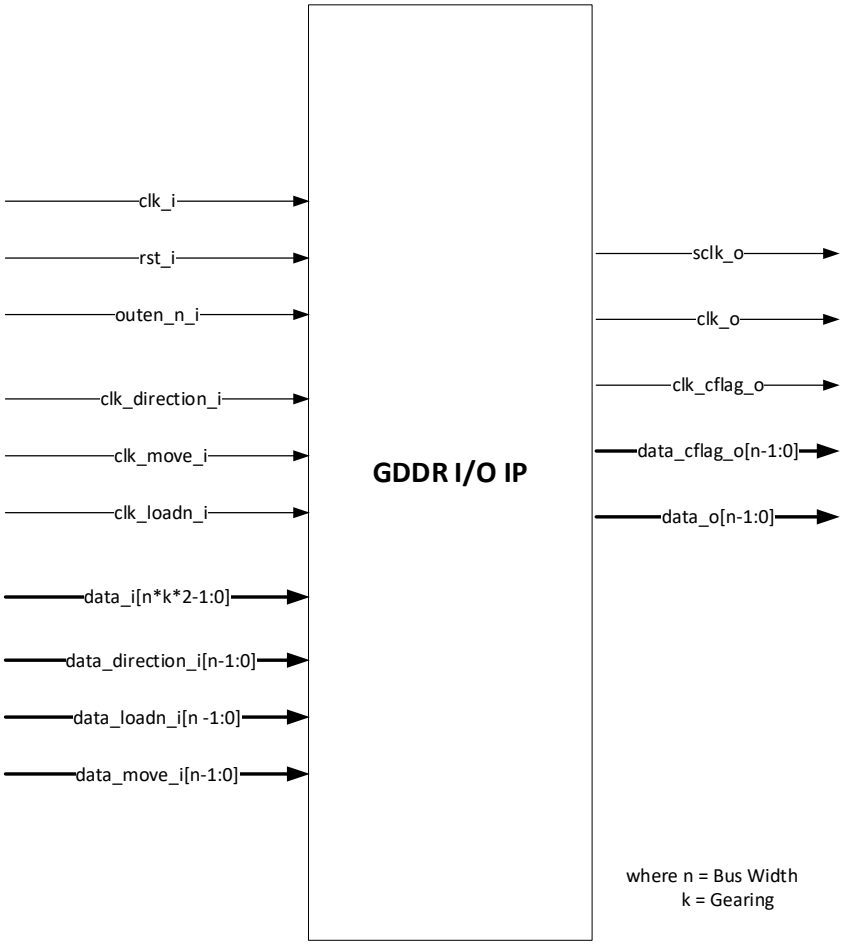

Figure 2.47. GDDRX2/4/5_TX.ECLK.Aligned Dynamic User-defined Delay Block Diagram

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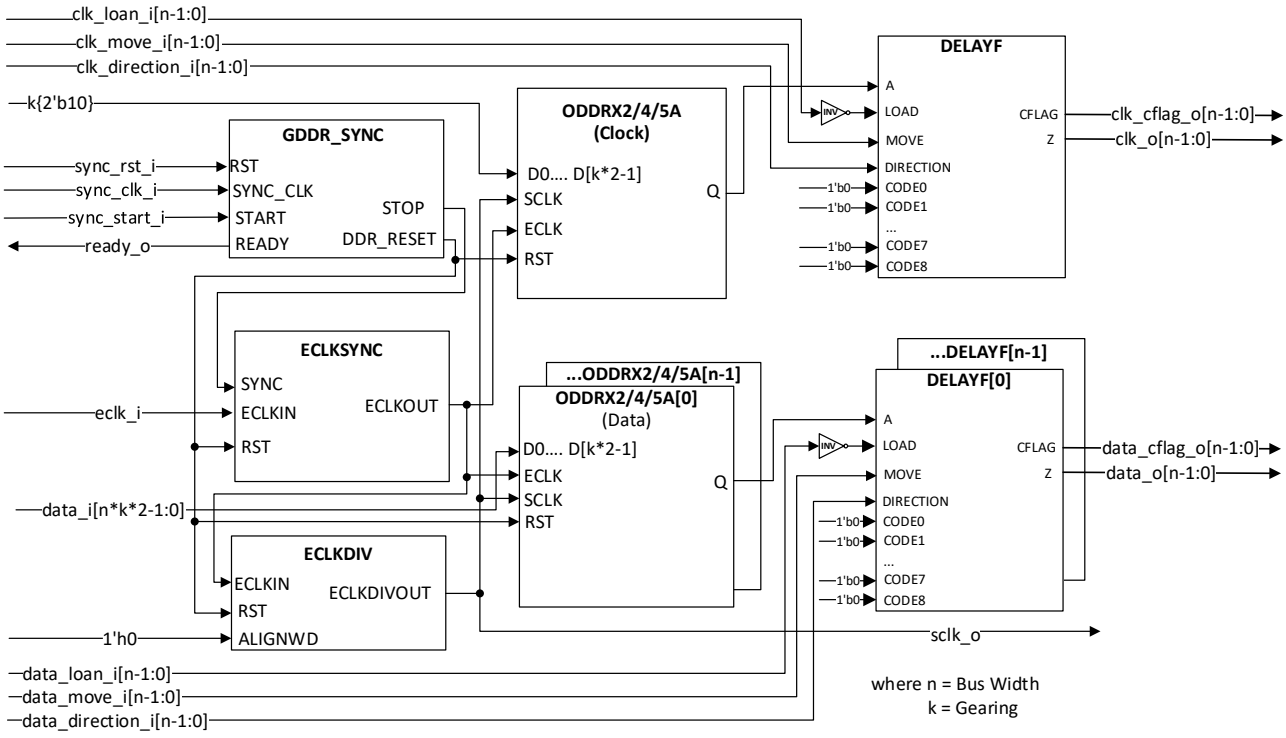

Figure 2.48. GDDRX2/4/5_TX.ECLK.Aligned Dynamic User-defined Delay Interface

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2.3. GDDR Behavior

2.3.1. RX Output Data Mapping

Bus Width = 4

Gearing = X2

data_i[4-1:0] = a[3:0], b[3:0], c[3:0], d[3:0]

data_o[2× 2×4-1:0] = {d[3:0], c[3:0], b[3:0], a[3:0]}

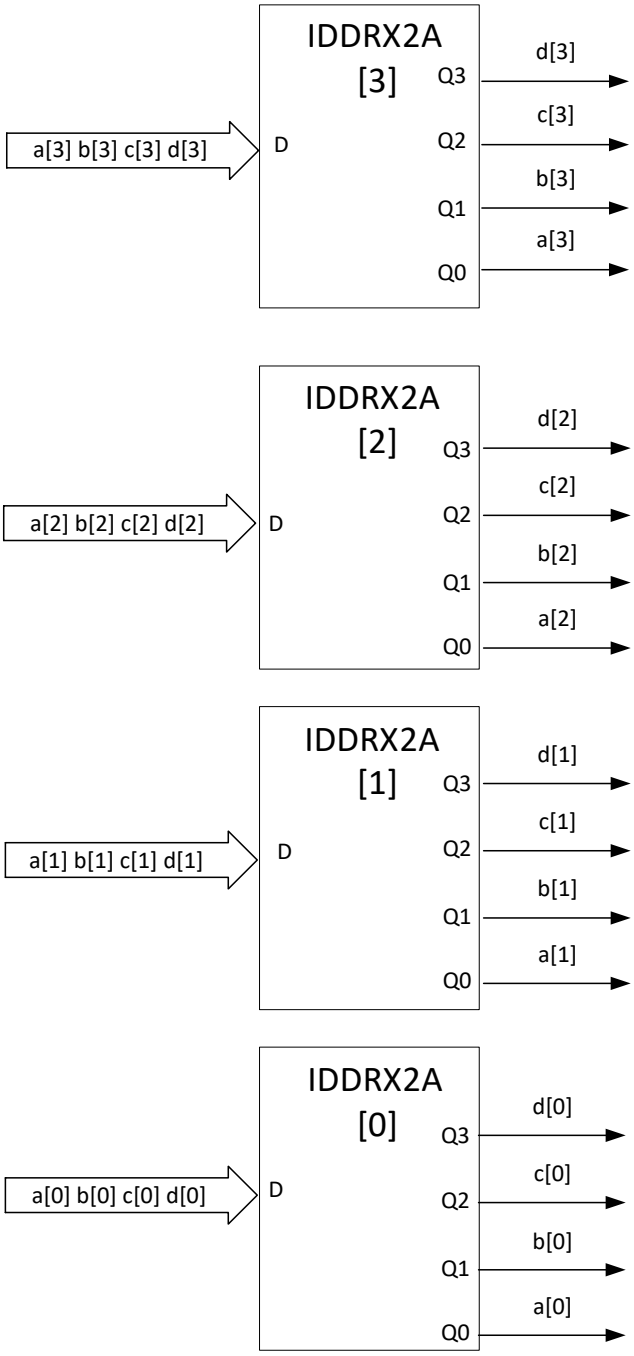

Figure 2.49. Rx Output Data Mapping Illustration

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As seen in Figure 2.49, for GDDR Rx configuration, when Bus Width is 4 bits, the IP generates four IDDRX2A modules (in our example for X2 gearing, the number of data_i batches is four.)

First batch of incoming data_i[a3:a0] is captured on the rising edge of the fast clock. The next batch of data_i[b3:b0] is captured on the falling edge of the fastest clock and so on.

In the picture above, this translates to the batch of the input data's slowest bits data_i[d3:d0] being placed on the data_o vector's highest bits [15:12]. Similarly, data_i[c3:c0] bits are placed on data_o[11:8] and so on. The sum of all the IDDRX2As outputs is a data_o[15:0] vector.

2.3.2. TX Input Data Mapping

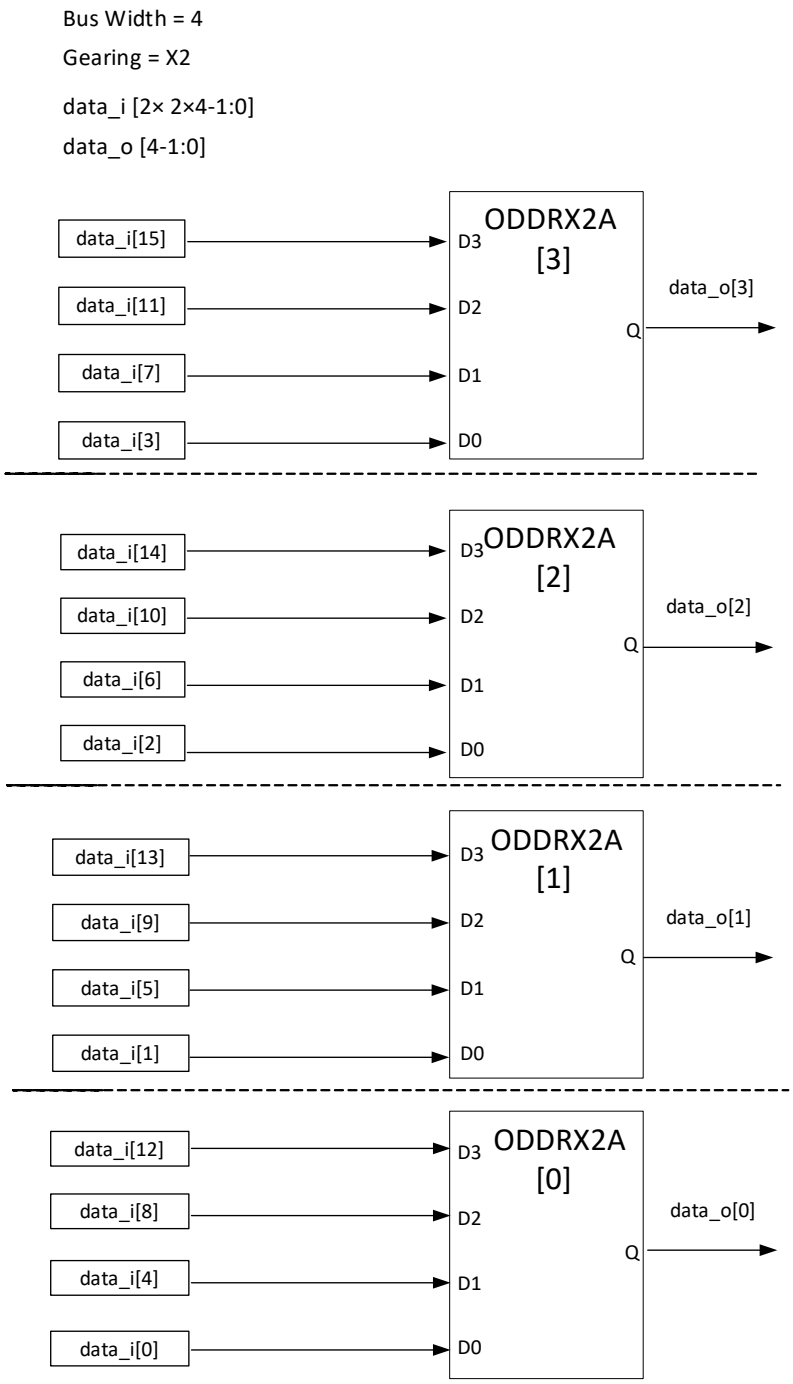

Figure 2.50. Tx Input Data Mapping Illustration

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As seen in Figure 2.50, for GDDR Tx configuration, when Bus Width is 4 bits, the IP generates four ODDRX2A modules. The entire input data is being broken down into four groups, each group the size of (gearing*2) bits. The group of the fastest bits data_i[3:0] is being transmitted first, followed by data_i[7:4] and so on.

2.4. Signal Description

Table 2.3. GDDR I/O Module Receive Signal Description

Port Name	Direction	Width (Bits)	Description
Clock and Reset			
clk_o	OUT	1	Received data sampling clock
rst_i	IN	1	Active high reset signal
sclk_o	OUT	1	Clock output for receive interface
sync_clk_i	IN	1	RX_SYNC/GDDR_SYNC low speed continuously running clock input
sync_rst_i	IN	1	RX_SYNC/GDDR_SYNC active HIGH reset signal
User Interface			
data_o	OUT	n * k	Received input data to fabric
alignwd_i	IN	1	This signal is used for word alignment. It shifts word by one bit. Only available for X2, X4, and X5 gearing ratio.
data_loadn_i	IN	n	Active low signal to reset data path delay setting to default. Only available during dynamic user-defined data path delay.
data_move_i	IN	n	Increments or decrements data path delay setting depending on data_direction_i. Only available during dynamic user-defined data path delay.
data_direction_i	IN	n	*1* to decrease data path delay; *0* to increase data path delay. Only available during dynamic user-defined data path delay.
data_cflag_o	OUT	n	Underflow or overflow flag to indicate minimum or maximum data path delay adjustment is reached. Only available during dynamic user-defined data path delay.
clk_loadn_i	IN	1	Active low signal to reset clock delay setting for clock to default. Only available during dynamic clock delay enabled.
clk_move_i	IN	1	Increments or decrements clock delay setting depending on clk_direction_i. Only available during dynamic clock delay enabled.
clk_direction_i	IN	1	*1* to decrease clock delay; *0* to increase clock delay. Only available during dynamic clock delay enabled.
clk_cflag_o	OUT	1	Underflow or overflow flag to indicate minimum or maximum clock delay adjustment is reached. Only available during dynamic clock delay enabled.
sync_update_i	IN	1	Used to restart sync process. ready_o goes low and waits for the sync process to finish before going high again.
sync_start_i	IN	1	Start the sync process. Must be high during all synchronization process.
ready_o	OUT	1	Indicate that startup is finished and RX circuit is ready to operate.
I/O Pad Interface			
clk_i	IN	1	Clock input signal from I/O
data_i	IN	n	Data input signal from I/O.

Note: n = number of lanes, k = 2(X1), 4(X2), 8(X4), and 10(X5).

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Table 2.4. GDDR I/O Module Transmit Signal Description

Port Name	Direction	Width (Bits)	Description
Clock and Reset			
rst_i	IN	1	Active high reset signal
clk_i	IN	1	Transmit data sampling clock. Only available when PLL instantiation is disabled.
clk90_i	IN	1	90-degree shifted for transmit clock generation.
sclk_o	OUT	1	Clock output for transmit interface. For X2, X4, and X5 configurations only.
eclk_i	IN	1	Transmit data sampling clock. Only available when PLL instantiation is disabled. For centered X2, X4, and X5 configurations.
eclk90_i	IN	1	90-degree shifted for transmit clock generation. For centered X2, X4 and X5 configurations.
sync_clk_i	IN	1	GDDR_SYNC low speed continuously running clock input
sync_rst_i	IN	1	GDDR_SYNC reset signal
User Interface			
data_i	IN	n × k	Transmit output data going to I/O
outen_n_i	IN	1	Active low signal output enable
data_loadn_i	IN	n	Active low signal to reset data path delay setting to default. Only available during dynamic user-defined data path delay.
data_move_i	IN	n	Increments or decrements data path delay setting depending on data_direction_i. Only available during dynamic user-defined data path delay.
data_direction_i	IN	n	*1* to decrease data path delay; *0* to increase data path delay. Only available during dynamic user-defined data path delay.
data_cflag_o	OUT	n	Underflow or overflow flag to indicate minimum or maximum data path delay adjustment is reached. Only available during dynamic user-defined data path delay.
clk_loadn_i	IN	1	Active LOW signal to reset clock delay setting for clock to default. Only available during dynamic clock delay enabled.
clk_move_i	IN	1	Increments or decrements clock delay setting depending on clk_direction_i. Only available during dynamic clock delay enabled.
clk_direction_i	IN	1	*1* to decrease clock delay; *0* to increase clock delay. Only available during dynamic clock delay enabled.
lock_o	OUT	1	PLL lock output signal. Only available when PLL instantiation is enabled.
ready_o	OUT	1	Indicate that startup is finished and TX circuit is ready to operate.
sync_start_i	IN	1	Used to re-start sync process. ready_o goes low and wait for sync process to finish before going high again.
I/O Pad Interface			
clk_o	OUT	1	Clock output signal to I/O
data_o	OUT	n	Data output signal to I/O.

Note: n = number of lanes, k = 2(X1), 4(X2), 8(X4), and 10(X5).

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2.5. Attribute Summary

Table 2.5 provides a list of user configurable attributes for the GDDR I/O Module. Attribute settings are specified using GDDR I/O Module Configuration user interface in Lattice Radiant.

Table 2.5. Attributes Table

Attribute	Selectable Values	Default	Dependency on Other Attributes
Interface Type	Transmit, Receive	Receive	—
I/O Standard for this Interface	(Legal Combination Table)	LVDS	—
Gearing Ratio	X1, X2, X4, X5	X1	X1 is available if *Clock Frequency <= 250 MHz* X2 is available if *Clock Frequency <= 600 MHz* X4 and X5 are available if *Clock Frequency <= 900 MHz*
Bus Width for this Interface	1 - 256	8	—
Clock to Data Relations on the Pins	Edge-to-Edge, Centered	Edge-to-Edge	—
Interface	GDDRX1_RX.SCLK.Aligned GDDRX1_RX.SCLK.Centered GDDRX1_TX.SCLK.Aligned GDDRX1_TX.SCLK.Centered GDDRX2_RX.ECLK.Aligned GDDRX2_RX.ECLK.Centered GDDRX2_TX.ECLK.Aligned GDDRX2_TX.ECLK.Centered GDDRX4_RX.ECLK.Aligned GDDRX4_RX.ECLK.Centered GDDRX4_TX.ECLK.Aligned GDDRX4_TX.ECLK.Centered GDDRX5_RX.ECLK.Aligned GDDRX5_RX.ECLK.Centered GDDRX5_TX.ECLK.Aligned GDDRX5_TX.ECLK.Centered	GDDRX1_RX.SCLK.Aligned	For display information only.
Data Path Delay	Bypass, Static Default, Dynamic Default, Static User-defined, Dynamic User-defined	Bypass	*Static Default* and *Dynamic Default* are supported for *Interface Type == Receive*
Fine Delay Value for User-defined	0 - Maximum Fine Delay	0	*Data Path Delay == Static User-defined* or *Dynamic User-defined* Maximum Fine Delay = (1/ *Clock Frequency*)/14ps Note: In silicon, targeted delay step is 12.5 ps. In functional simulation, delay step that can be observed is 10ps. Meanwhile 14ps is the observed delay step on timing characterization.
Clock Path Delay	Fixed Dynamic	Fixed	*Data Path Delay == Dynamic Default* or *Data Path Delay == Dynamic User-defined*
Include GDDR_SYNC	Checked, Not checked	Not checked	*Interface Type == Receive*, *Clock to Data Relationship on the Pins == Centered*, *Gearing Ratio* != *X1* and *Data Path Delay* != *Dynamic Default* nor *Dynamic User-defined* *Interface Type == Transmit*, *Clock to Data Relationship on the Pins == Edge-to-edge*, *Gearing Ratio* != *X1*, *Data Path Delay* !=

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Attribute	Selectable Values	Default	Dependency on Other Attributes
			Dynamic Default nor *Dynamic User-defined* and *Tristate Control == Disabled*
Enable Tristate Control	Checked, Not checked	Not checked	*Interface Type == Transmit*, *Clock to Data Relationship on the Pins == Centered*, *Gearing Ratio* != *X1* and *Data Path Delay == Dynamic Default* or *Dynamic User-defined* and *Clock Path Delay == Dynamic* *Interface Type == Transmit*, *Clock to Data Relationship on the Pins == Edge-to-edge*, *Gearing Ratio != X1* and *Data Path Delay != Dynamic Default nor Dynamic User-defined* and *Clock Path Delay != Dynamic*
Clock Frequency for this Interface (MHz)	100-900	150	Selectable maximum value is based on Gearing setting.
Bandwidth for this Interface (Mbits/s)	Calculated	2400	2*(Clock Frequency for this Interface)*(Bus Width for this Interface)
Enable PLL Instantiation	Checked, Not checked	Not checked	*Interface Type == Transmit,'Clock to Data Relationship on the Pins == Centered, Gearing Ratio* != *X1*
PLL Input Clock Frequency (MHz)	10 – Max Value	25	Enable PLL Instantiation is checked. Max Value = *Clock Frequency for this Interface* if *Clock Frequency <= 800 MHz* else Max Value= 800 MHz
PLL Output Clock Frequency Actual Value (MHz)	Calculated	150	—
PLL Output Clock Tolerance (%)	0.0, 0.1, 0.2, 0.5, 1.0, 2.0, 5.0, 10.0	0.0	Enable PLL Instantiation is checked.

Note: All attributes can be configured from the General tab of the Lattice Radiant Software user interface.

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Table 2.6 presents attribute description.

Table 2.6. Attribute Description

Attribute	Description
Interface Type	Selects interface type as Receive or Transmit.
I/O Standard for this Interface	List of Single-ended or Differential I/O supported.
Gearing Ratio	Selects gearing ratio as X1, X2, X4, or X5.
Bus Width for this Interface	Total number of lanes/bus width.
Clock to Data Relations on the Pins	Selects clock to data relationship as Edge-to-edge or Centered.
Interface	Summarizes the interface to be used.
Data Path Delay	Selects among Bypass, Static Default, Static User-defined, Dynamic Default or Dynamic User-defined. Allows user to set default data path fine delay value when selected as user-defined.
Fine Delay Value for User-defined	Default data path fine delay setting. Only valid when Data Path Delay is Static User-defined or Dynamic User-defined. Ideally, a 9-bit binary string, 12.5 ps per step max_fine_delay = 511 × 12.5 ps = 6387.5ps Note: The silicon is designed to have 12.5ps delay per step but on simulation, only 10ps can be observed.
Clock Path Delay	Fixed or dynamic addition of clock path delay.
Include GDDR_SYNC	Enables usage of GDDR_SYNC support soft logic.
Enable Tristate Control	Enable Tri-State Control instantiation.
Clock Frequency for this Interface (MHz)	Clock frequency to be used in selected interface.
Enable PLL Instantiation	Enables usage of existing PLL module.
PLL Input Clock Frequency (MHz)	Value of PLL input clock frequency
PLL Output Clock Frequency Actual Value (MHz)	Value of PLL output clock frequency
PLL Output Clock Tolerance (%)	Percentage on allowable difference of the actual to desired value.

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3. IP Generation, Simulation, and Validation

This section provides information on how to generate the IP using the Lattice Radiant software, and how to run simulation, synthesis, and hardware evaluation. For more details on the Lattice Radiant software, refer to the Lattice Radiant software user guide.

3.1. Generating the IP

The Lattice Radiant software allows user to customize and generate modules and IPs and integrate them into the device's architecture. The procedure for generating the GDDR I/O Module in Lattice Radiant software is described below.

To generate GDDR I/O Module:

1. Create a new Lattice Radiant Software project or open an existing project.
2. In the **IP Catalog** tab, double-click on **DDR_Generic** under **Module, Architecture_Modules, IO** category. The **Module/IP Block Wizard** opens as shown in Figure 3.1. Enter values in the **Component name** and the **Create in** fields and click **Next**.

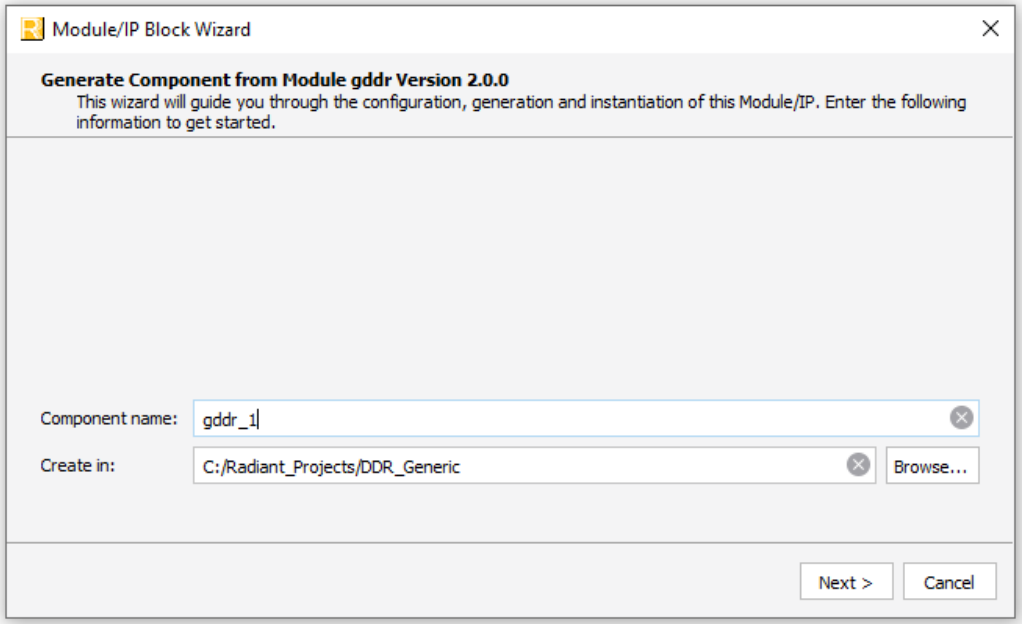

Figure 3.1. Module/IP Block Wizard

3. In the module's dialog box of the **Module/IP Block Wizard** window, customize the selected GDDR I/O Module using drop-down menus and check boxes. As a sample configuration, see Figure 3.2. For configuration options, see the Attribute Summary section.

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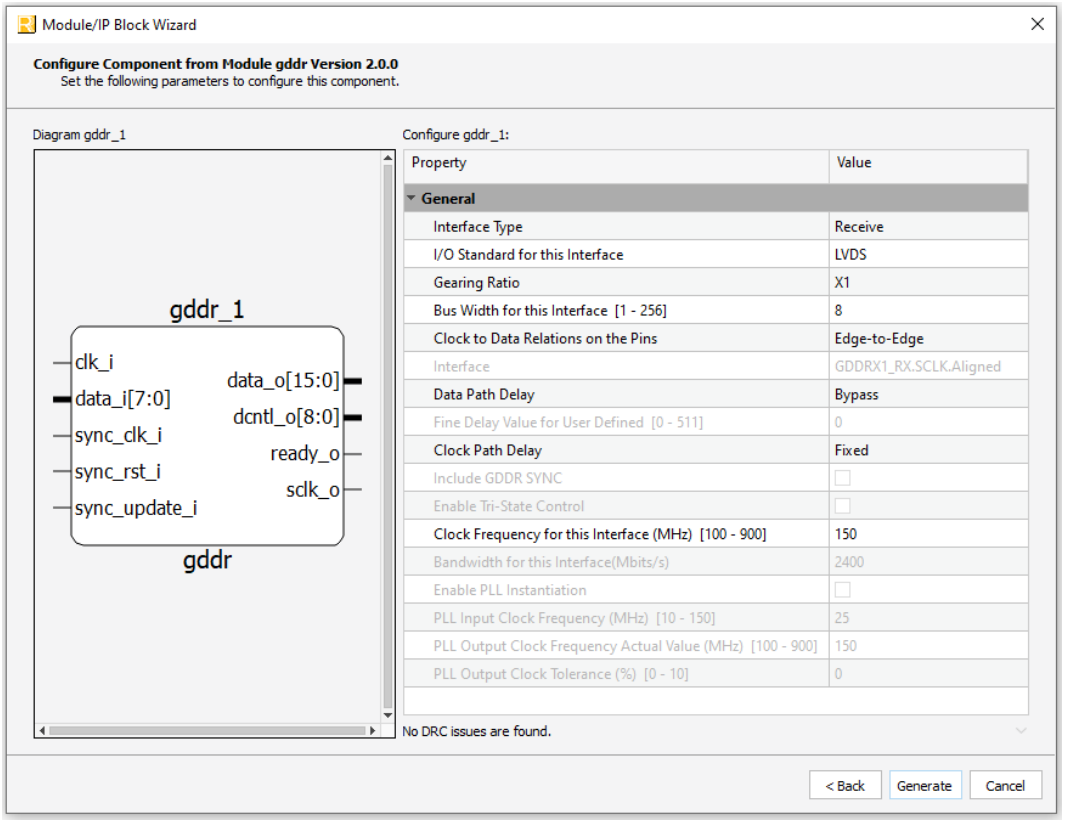

Figure 3.2. Configure Block of GDDR I/O Module

4. Click **Generate**. The **Check Generated Result** dialog box opens, showing design block messages and results as shown in Figure 3.3.

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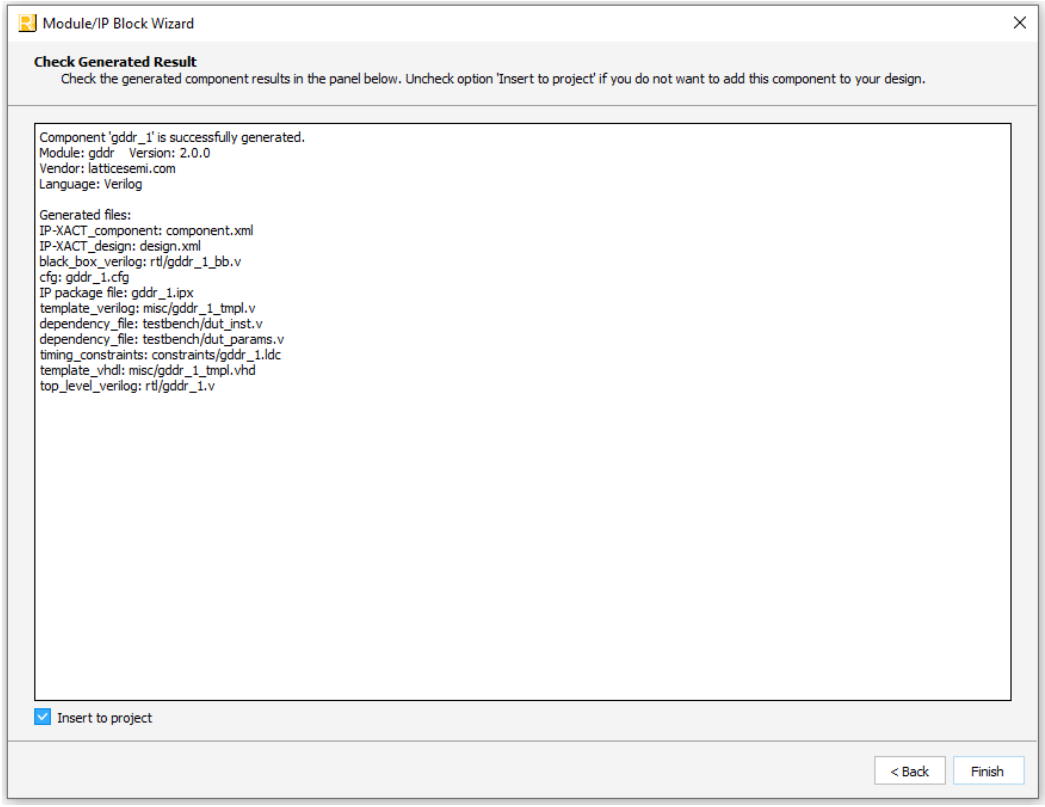

Figure 3.3. Check Generated Result

5. Click the **Finish** button. All the generated files are placed under the directory paths in the **Create in** and the **Component name** fields shown in Figure 3.1.

The generated GDDR I/O module package includes the black box (<Instance Name>_bb.v) and instance templates (<Instance Name>_tmpl.v/vhd) that can be used to instantiate the module in a top-level design. An example RTL top-level reference source file (<Instance Name>.v) that can be used as an instantiation template for the module is also provided. user may also use this top-level reference as the starting template for the top-level for their complete design. The generated files are listed in Table 3.1.

Table 3.1. Generated File List

Attribute	Description
<Instance Name>.ipx	This file contains the information on the files associated to the generated IP.
<Instance Name>.cfg	This file contains the parameter values used in IP configuration.
component.xml	Contains the ipxact:component information of the IP.
design.xml	Documents the configuration parameters of the IP in IP-XACT 2014 format.
rtl/<Instance Name>.v	This file provides an example RTL top file that instantiates the module.
rtl/<Instance Name>_bb.v	This file provides the synthesis black box.
misc/<Instance Name>_tmpl.v misc /<Instance Name>_tmpl.vhd	These files provide instance templates for the module.
testbench/tb_top.v	Test bench template; user can edit this to match the specific needs.
testbench/dut_params.v	Instantiated version of the <IP_name>.v file for simulation use
testbench/dut_ints.v	Top level parameters of the generated RTL file

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3.2. Running Functional Simulation

After the IP is generated, running functional simulation can be performed using different available simulators. The default simulator already has pre-compiled libraries ready for simulation. Choosing a non-default simulator, however, may require additional steps.

To run functional simulation using the default simulator:

1. Click the button located on the **Toolbar** to initiate **Simulation Wizard**, as shown in Figure 3.4.

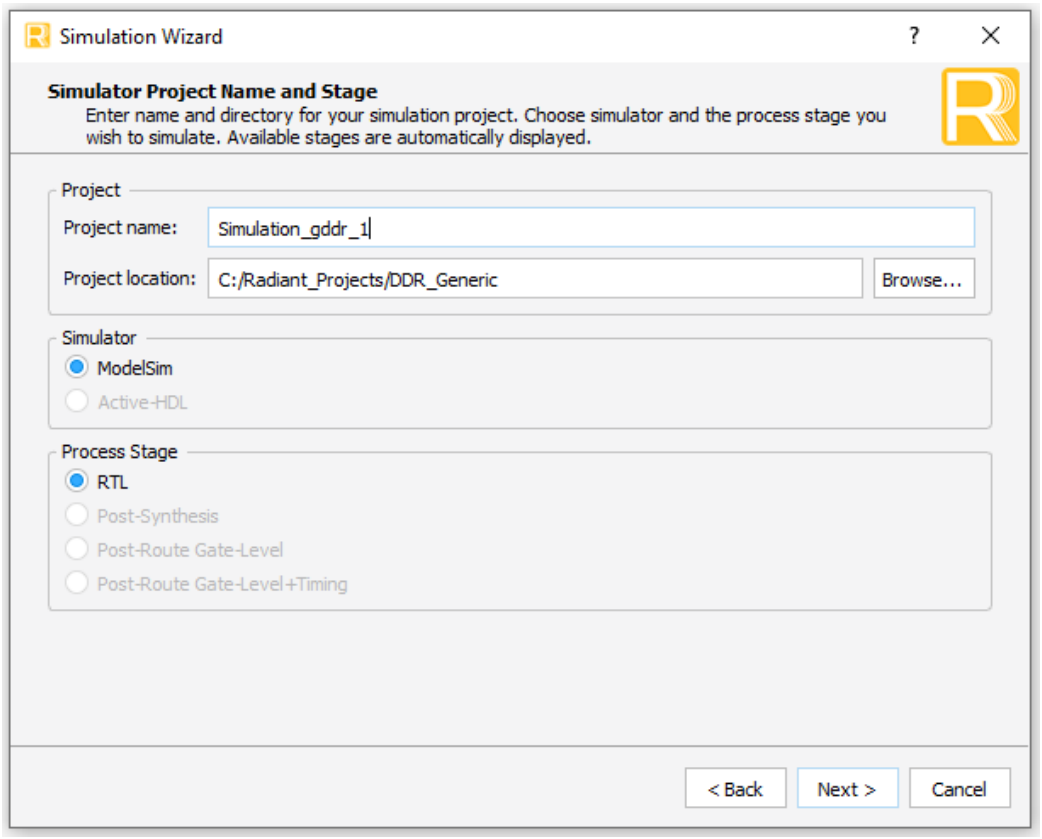

Figure 3.4. Simulation Wizard

2. Click **Next** to open the **Add and Reorder Source** window as shown in Figure 3.5.

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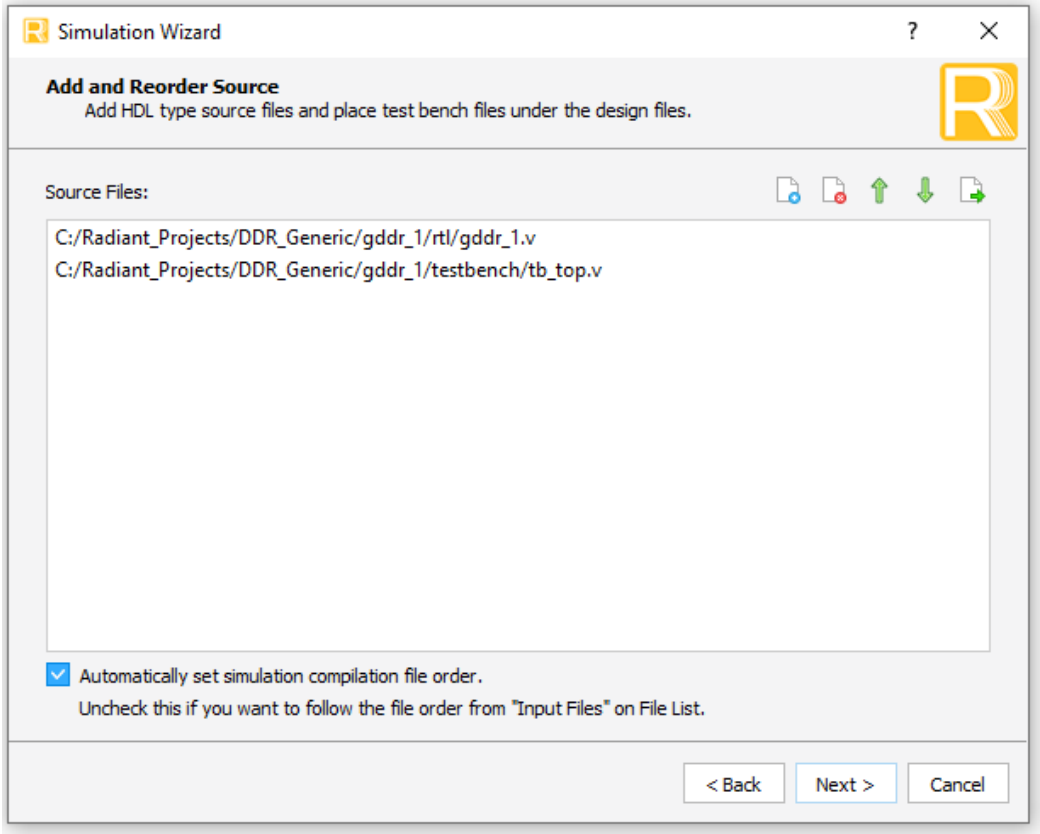

Figure 3.5. Adding and Reordering Source

3. Click **Next**. The Summary window is shown. Click **Finish** to run the simulation.

Note: It is necessary to follow the procedure above until it is fully automated in the Lattice Radiant Software Suite.

The results of the simulation in our example are provided in Figure 3.6.

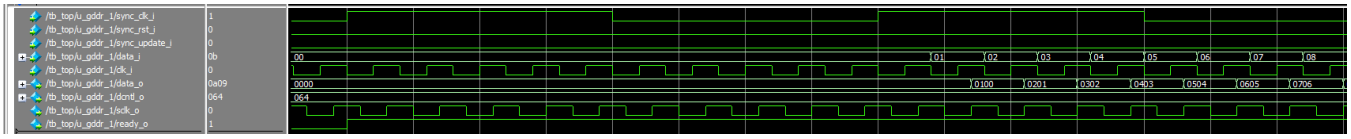

Figure 3.6. Simulation Waveform

3.3. IP Evaluation

There is no restriction on the IP evaluation of this module.

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Appendix A. Resource Utilization

Table A.1 and Table A.2 shows resource utilization of DDR Generic configurations using LAV-AT-500E-3LFG1156I and LAV-AT-500E-1LFG1156I devices with Synplify Pro of Lattice Radiant software. Default configuration is used and some attributes are changed from the default value to show the effect on the resource utilization.

Table A.1. Resource Utilization using LAV-AT-500E-3LFG1156I

Configuration	Clk Fmax (MHz)[1]	Registers	LUTs[2]	EBRs	DSPs
8-bit Receive X1 Edge-to-Edge Bypass	250	44	108	0	0
8-bit Receive X2 Centered Bypass	300	0	0	0	0
16-bit Receive X4 Edge-to-Edge Static Default	225	44	112	0	0
4-bit Receive X5 Centered Dynamic Default	180	0	4	0	0
8-bit Transmit X1 Edge-to-Edge Bypass	250	0	0	0	0
16-bit Transmit X2 Centered Bypass	300	12	25	0	0
16-bit Transmit X4 Centered Static User Defined with 10 Fine Delay value	225	12	25	0	0
4-bit Transmit X5 Centered Dynamic User Defined	180	12	30	0	0

Notes:

1. Fmax is generated when the FPGA design only contains the Generic DDR module and the target frequency is 200 MHz for X1, X2, and X4 gearing and 180 MHz for X5 gearing. Generic DDR module supports SCLK frequency up to 250MHz for X1, 300 MHz for X2, 225 MHz for X4 and 180 MHz for X5 gearing. The obtained Fmax values may be reduced when user logic is added to the FPGA design.
2. The *distributed RAM utilization* is accounted for in the total LUT4s utilization. The actual LUT4 utilization is distribution among logic, *distributed RAM*, and *ripple logic*.

Table A.2. Resource Utilization using LAV-AT-500E-1LFG1156I

Configuration	Clk Fmax (MHz)[1]	Registers	LUTs[2]	EBRs	DSPs
8-bit Receive X1 Edge-to-Edge Bypass	250	44	108	0	0
8-bit Receive X2 Centered Bypass	300	0	0	0	0
16-bit Receive X4 Edge-to-Edge Static Default	225	44	112	0	0
4-bit Receive X5 Centered Dynamic Default	180	0	4	0	0
8-bit Transmit X1 Edge-to-Edge Bypass	250	0	0	0	0
16-bit Transmit X2 Centered Bypass	300	12	25	0	0
16-bit Transmit X4 Centered Static User Defined with 10 Fine Delay value	225	12	25	0	0
4-bit Transmit X5 Centered Dynamic User Defined	180	12	30	0	0

Notes:

1. Fmax is generated when the FPGA design only contains the Generic DDR module and the target frequency is 200 MHz for X1, X2, and X4 gearing and 180 MHz for X5 gearing. Generic DDR module supports SCLK frequency up to 250MHz for X1, 300 MHz for X2, 225 MHz for X4 and 180 MHz for X5 gearing. The obtained Fmax values may be reduced when user logic is added to the FPGA design.
2. The *distributed RAM utilization* is accounted for in the total LUT4s utilization. The actual LUT4 utilization is distribution among logic, *distributed RAM*, and *ripple logic*.

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References

For complete information on Lattice Radiant Project-Based Environment, Design Flow, Implementation Flow and Tasks, as well as on the Simulation Flow, see the Lattice Radiant software user guide.

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Revision History

Revision 1.0, October 2022

Section	Change Summary
Functional Description	Updated below figures: • Figure 2.11. GDDRX2/4/5_RX.ECLK.Centered Bypass/Static Default/Static User-defined Delay Interface • Figure 2.15. GDDRX2/4/5_RX.ECLK.Centered Bypass/Static Default/Static User-defined Delay with GDDR_SYNC Interface • Figure 2.17. GDDRX2/4/5_RX.ECLK.Aligned Bypass/Static Default/Static User-defined Interface • Figure 2.32. GDDRX2/4/5_TX.ECLK.Centered Static User-defined Delay (with GDDR_SYNC) Interface • Figure 2.35. GDDRX2/4/5_TX.ECLK.Centered Static User-defined Delay for PLL Interface • Figure 2.43. GDDRX2/4/5_TX.ECLK.Aligned Static User-defined Delay with GDDR_SYNC Enabled Block Diagram • Figure 2.46. GDDRX2/4/5_TX.ECLK.Aligned Static User-defined Delay Tristate Control Enabled Block Diagram
IP Generation, Simulation, and Validation	Updated below figures: • Figure 3.1. Module/IP Block Wizard • Figure 3.2. Configure Block of GDDR I/O Module • Figure 3.3. Check Generated Result
Resource Utilization	Added Appendix A. Resource Utilization section.

Revision 0.8, May 2022

Section	Change Summary
All	Initial release.

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