Avant SDR Module - Lattice Radiant Software

User Guide

FPGA-IPUG-02187-1.0

October 2022

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
RTL	Register Transfer Level
SDR	Single Data Rate

1. Introduction

The Lattice Semiconductor Single Data Rate Input/Output (SDR I/O) Module is designed to be used in a wide range of applications in which fast data transmission is required.

1.1. Features

The key features of Single Data Rate Input/Output (SDR I/O) Module include:

- Receive and Transmit Interface of up to 250 Mbps
- Selectable I/O type
  - Single-ended or Differential Signaling
- 1-bit to 256-bit data bus width
- 1 MHz to 250 MHz clock frequency
- Data Path Delay that includes following options:
  - Bypass
  - Static Default (Receive Interface only)
  - Dynamic Default (Receive Interface only)
  - Static User-Defined
  - Dynamic User-Defined
- Tristate control (Transmit Interface only)
- Clock inversion (Receive Interface only)

1.2. Conventions

1.2.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.2.2. Signal Names

Signal names that end with:

- *_n* are active low
- *_i* are input signals
- *_o* are output signals
- *_io* are bi-directional input/output signals

2. Functional Description

2.1. Overview

Table 2.1. SDR I/O Module Interfaces

Feature	Description	Comments
GIREG_RX.SCLK	SDR Receive Interface	Supports bypassed, static, and dynamic data path delay. Supports clock inversion logic
GOREG_TX.SCLK	SDR Transmit Interface	Supports bypassed, static, and dynamic data path delay. Supports tristate control.

Notes:

- G – Generic
- IREG – SDR input I/O register
- OREG – SDR output I/O register
- _RX – Receive interface
- _TX – Transmit interface
- .SCLK – Uses SCLK (primary clock) clocking resource

SDR GIREG_RX.SCLK interface is used when a simple input register is required for the design. The clock input to the input register can be optionally inverted if required. These interfaces always use SCLK.

SDR GOREG_TX.SCLK interface is used for an SDR data output implementation with tight specifications on clock out to data out skew. The same clock is used for both data and clock generation.

Single Data Rate applications capture data on one edge of a clock only.

Figure 2.1 presents a top-level block diagram of SDR I/O Module.

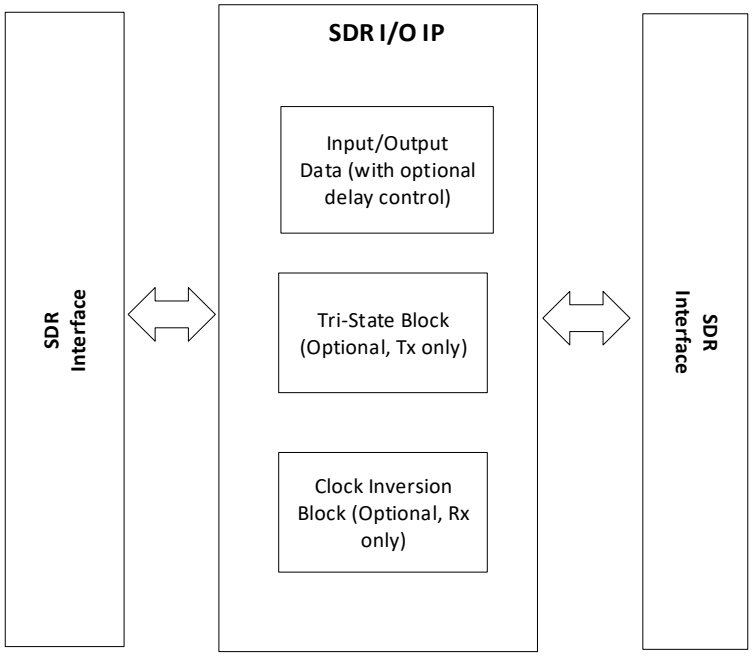

Figure 2.1. SDR I/O Module Top Level Block Diagram

2.2. Functional Diagrams

2.2.1. GIREG_RX.SCLK

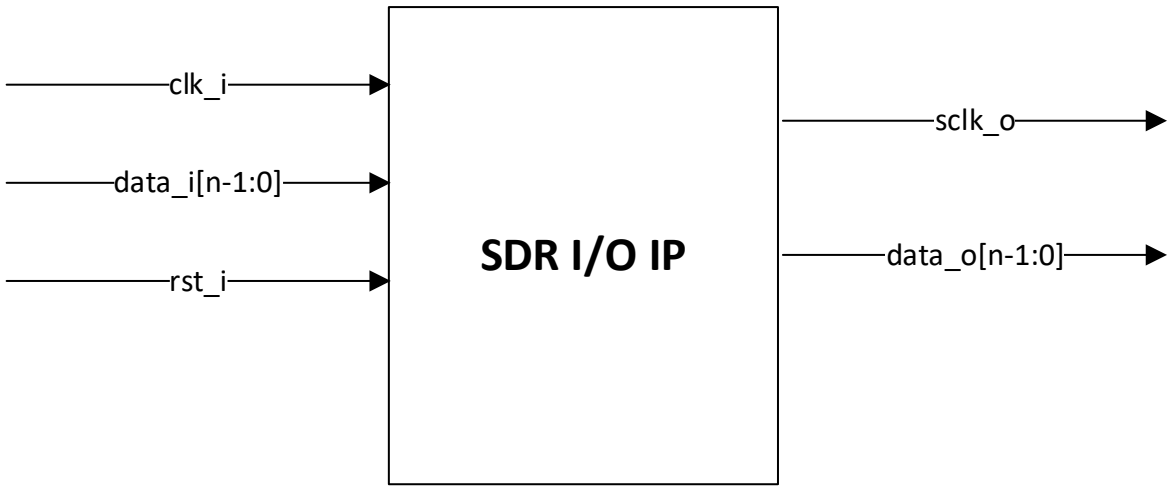

Figure 2.2. GIREG_RX.SCLK Bypass/Static Default/Static User-Defined Delay Block Diagram

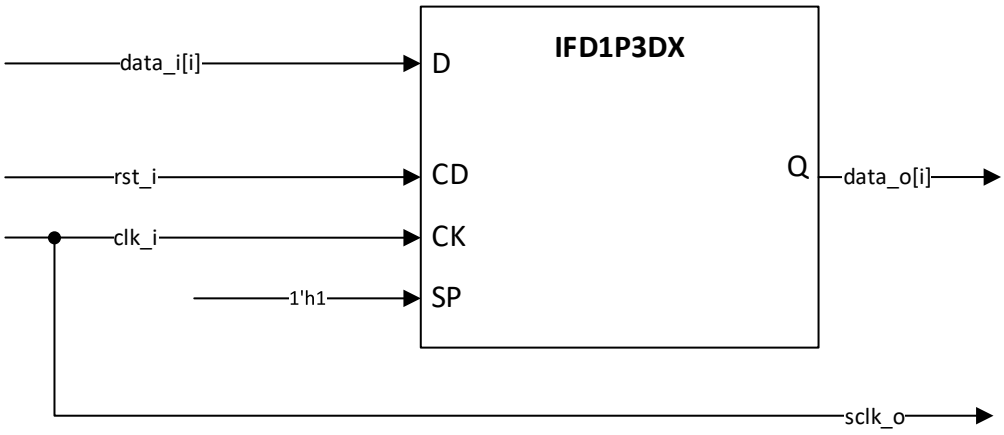

Figure 2.3. GIREG_RX.SCLK Bypass Interface

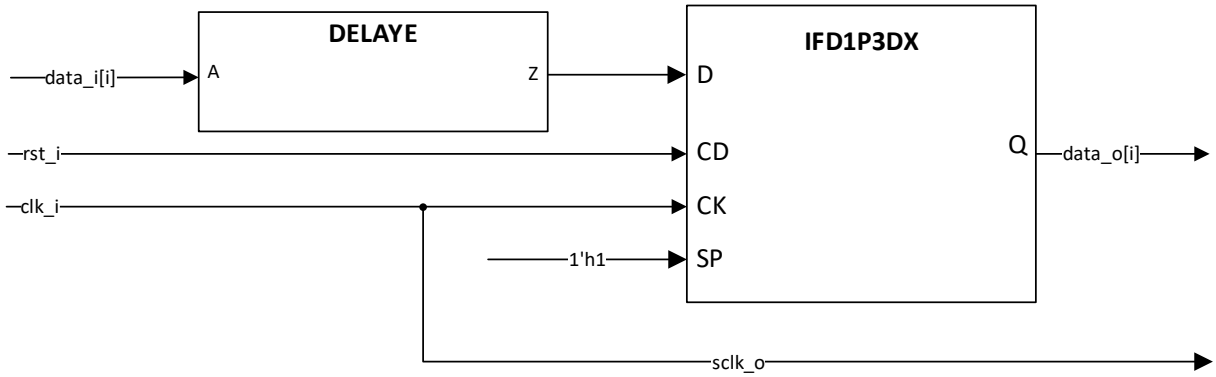

Figure 2.4. GIREG_RX.SCLK Static Default/Static User-Defined Delay Interface

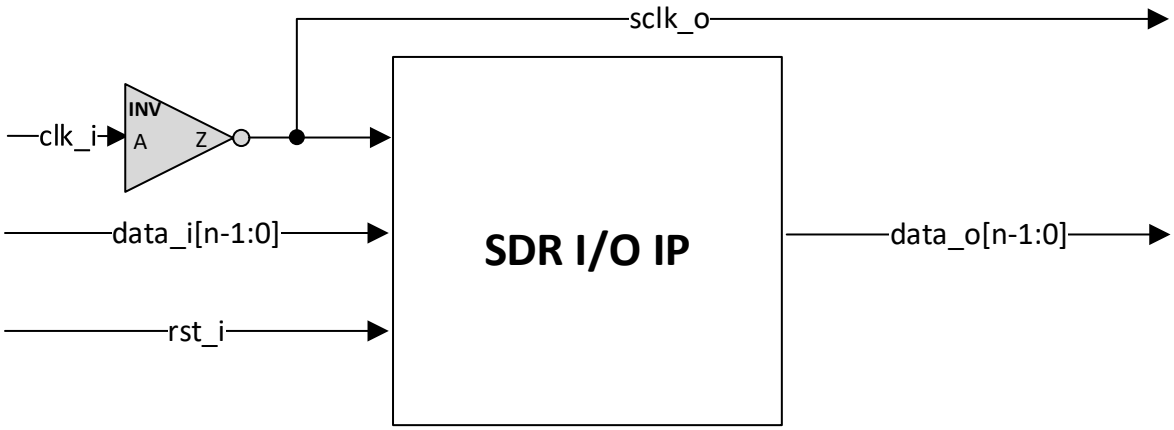

Figure 2.5. GIREG_RX.SCLK Bypass/Static Default/Static User-Defined Delay Inversion Enabled Block Diagram

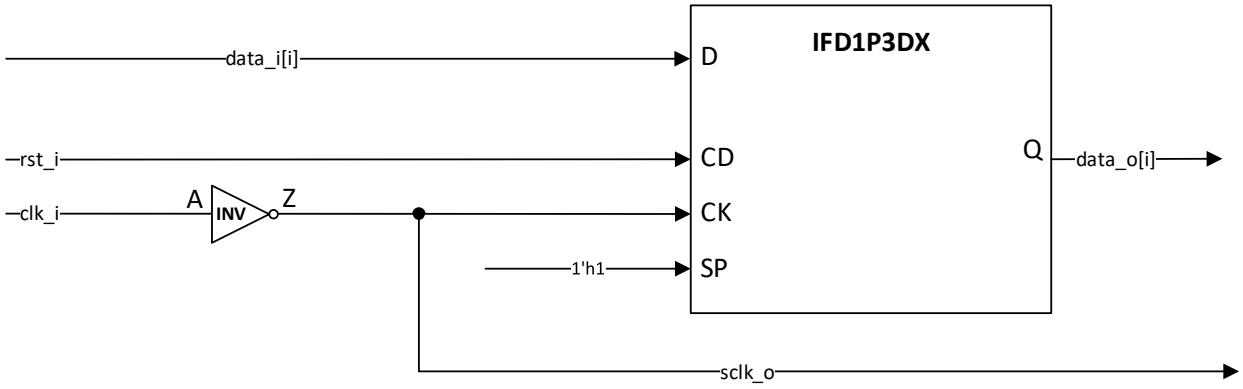

Figure 2.6. GIREG_RX.SCLK Bypass Inversion Enabled Interface

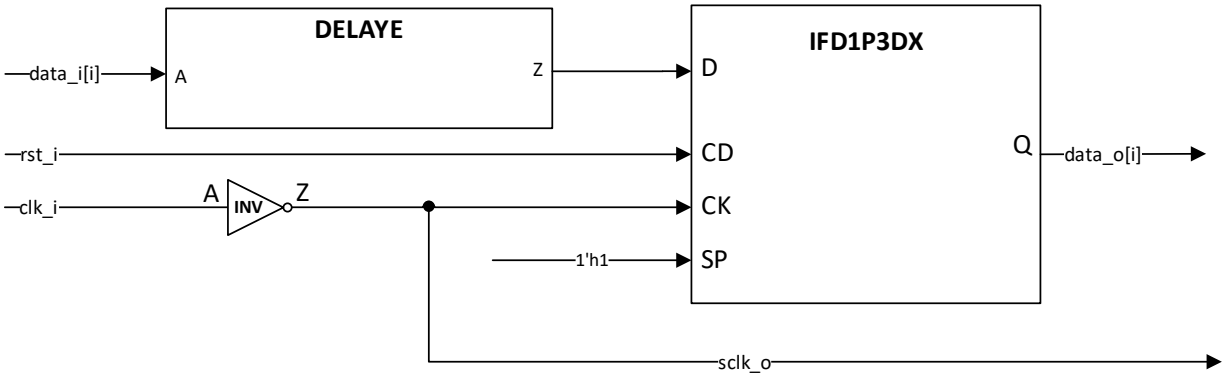

Figure 2.7. GIREG_RX.SCLK Static Default/Static User-Defined Delay Inversion Enabled Interface

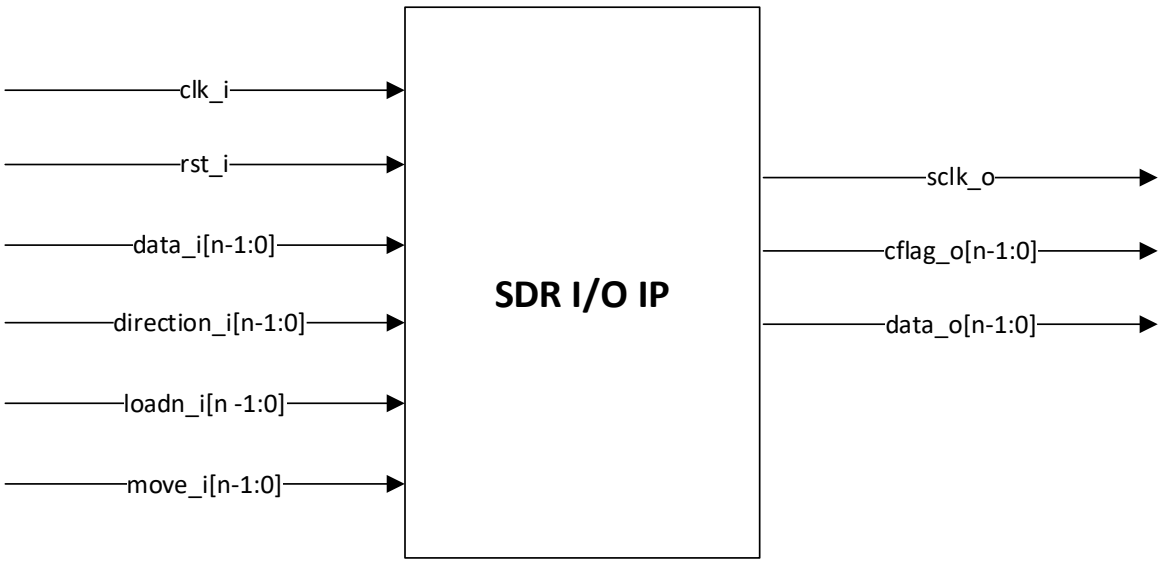

Figure 2.8. GIREG_RX.SCLK Dynamic Default/Dynamic User-Defined Delay Block Diagram

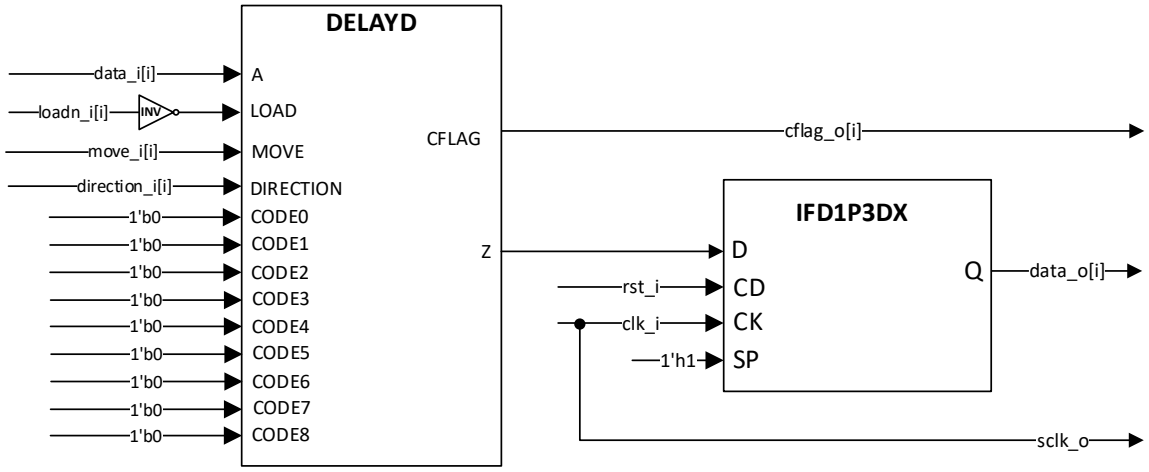

Figure 2.9. GIREG_RX.SCLK Dynamic Default/Dynamic User-Defined Delay Interface

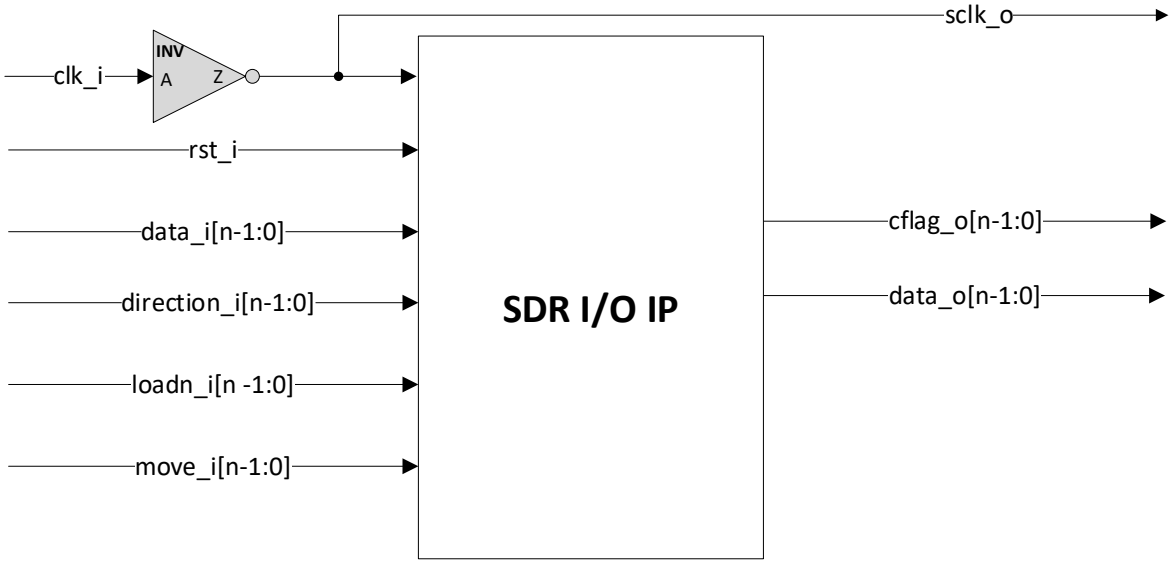

Figure 2.10. GIREG_RX.SCLK Dynamic Default/Dynamic User-Defined Delay Inversion Enabled Block Diagram

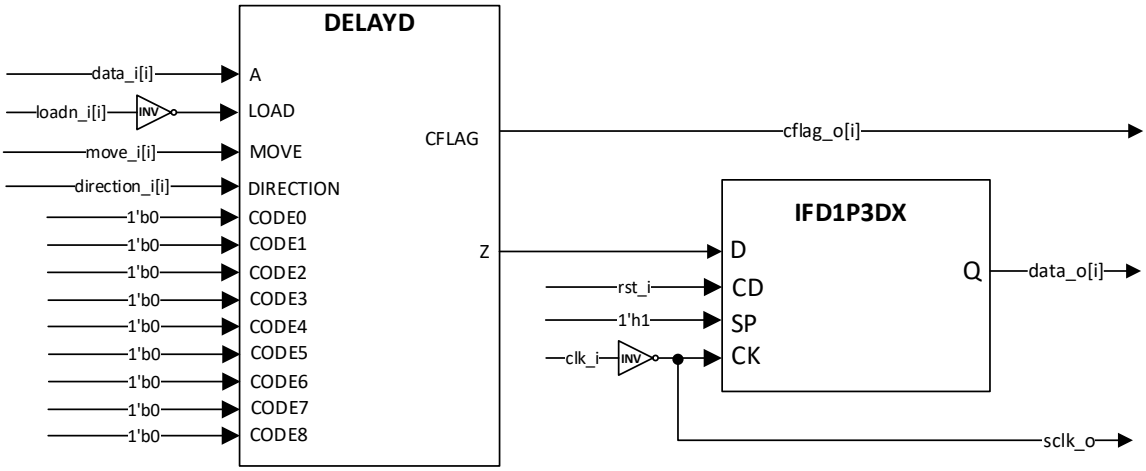

Figure 2.11. GIREG_RX.SCLK Dynamic Default/Dynamic User-Defined Delay Inversion Enabled Interface

2.2.2. GOREG_TX.SCLK

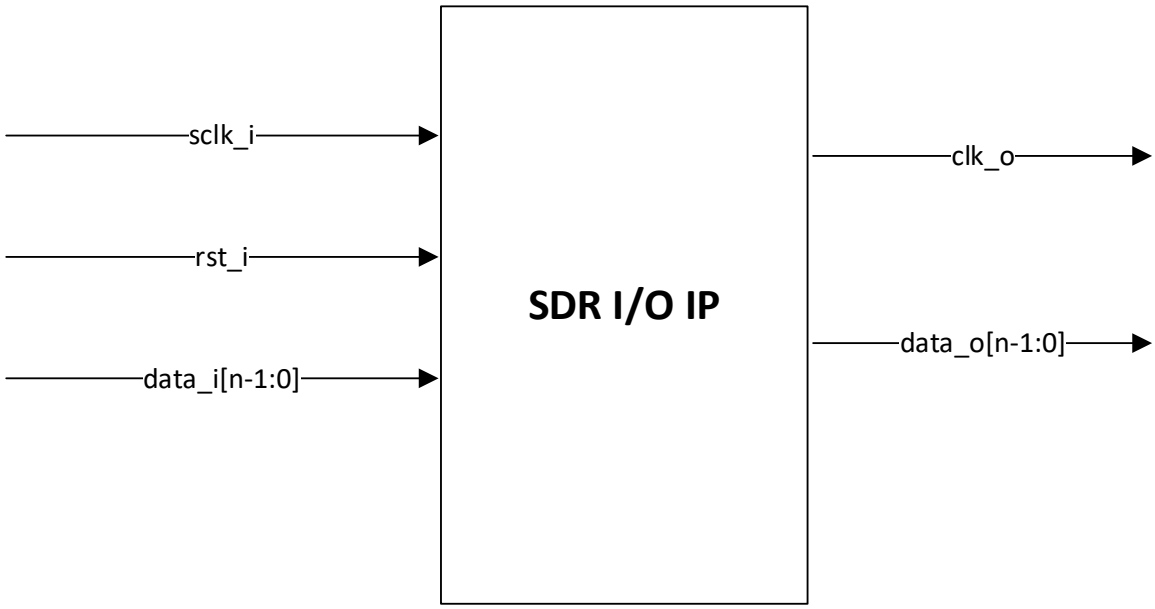

Figure 2.12. GOREG_TX.SCLK Bypass/Static User-Defined Delay Block Diagram

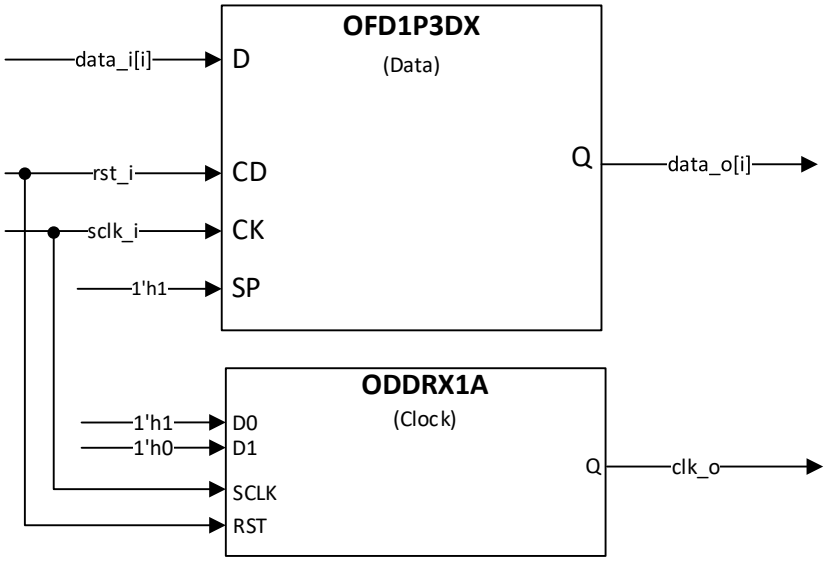

Figure 2.13. GOREG_TX.SCLK Bypass Interface

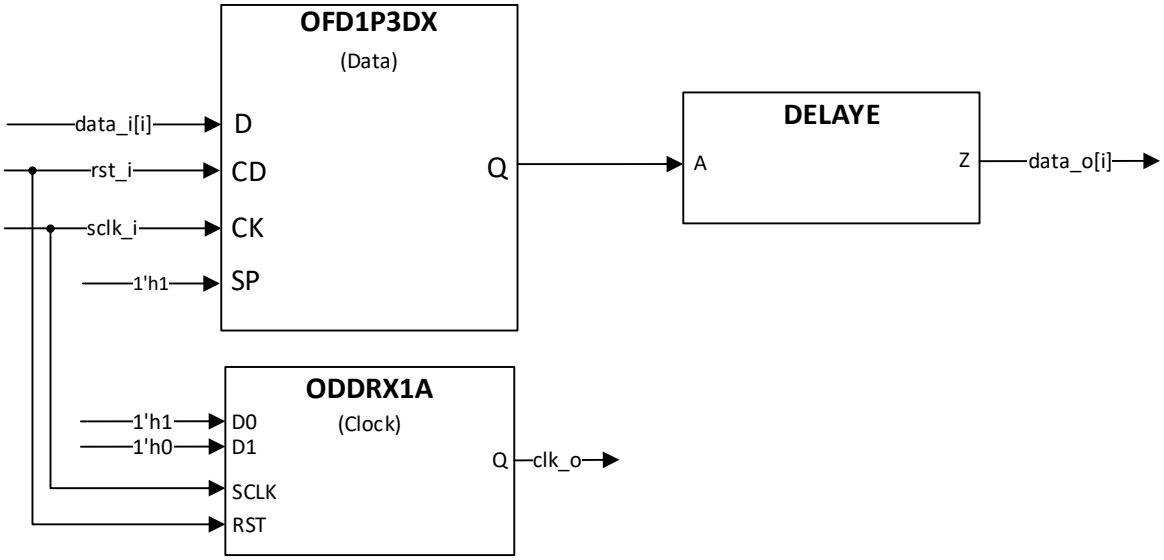

Figure 2.14. GOREG_TX.SCLK Static User-Defined Delay Interface

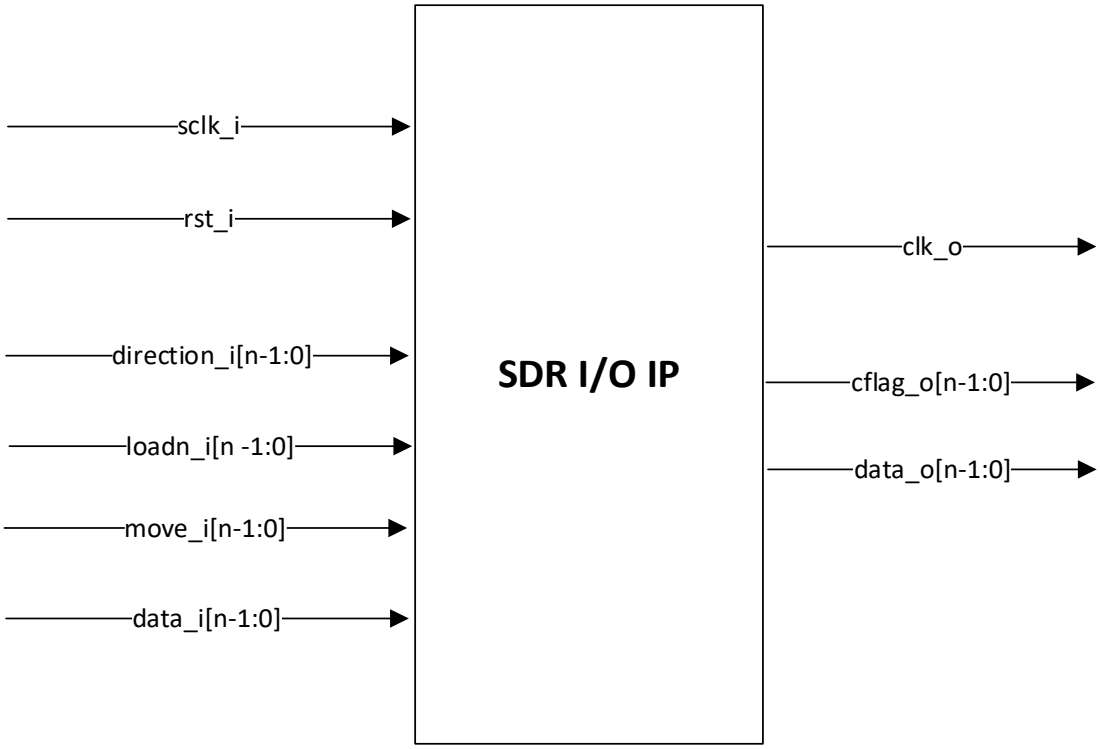

Figure 2.15. GOREG_TX.SCLK Dynamic User-Defined Delay Block Diagram

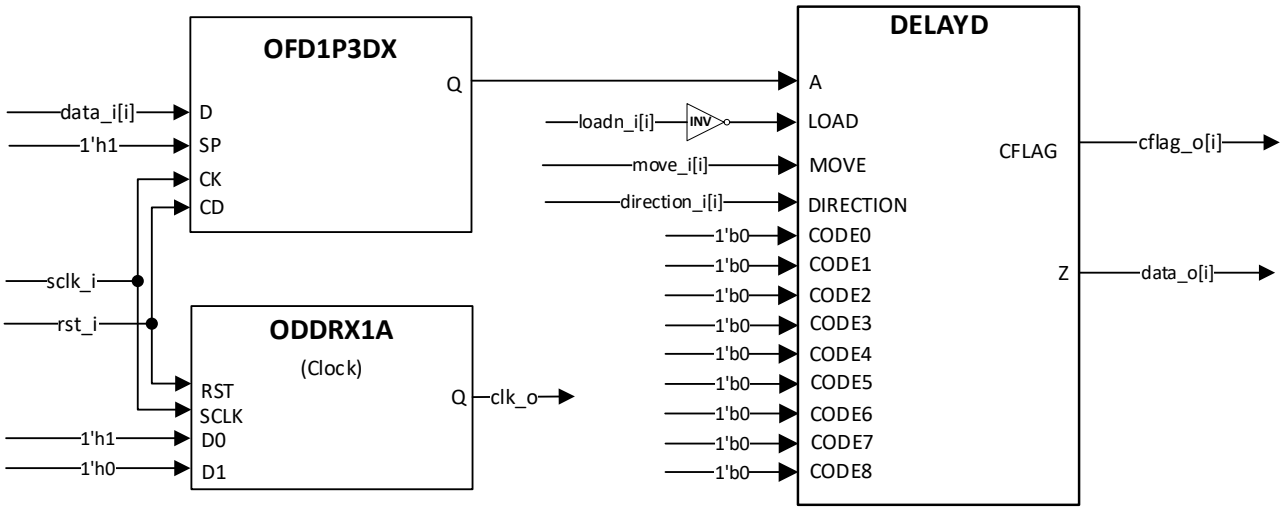

Figure 2.16. GOREG_TX.SCLK Dynamic User-Defined Delay Interface

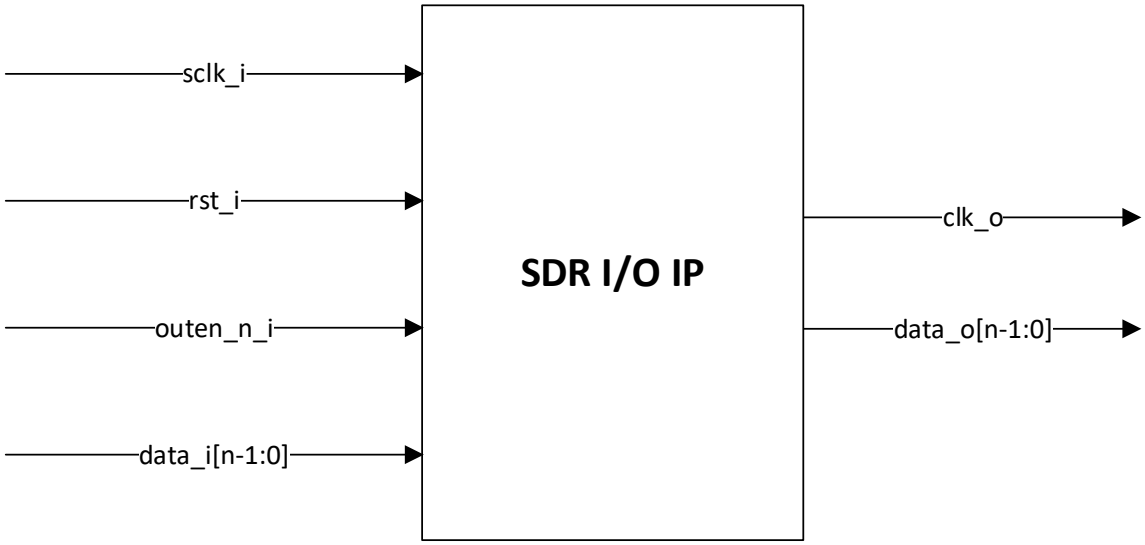

Figure 2.17. GOREG_TX.SCLK Bypass Delay/Static User Defined Delay Tristate Control Enabled Block Diagram

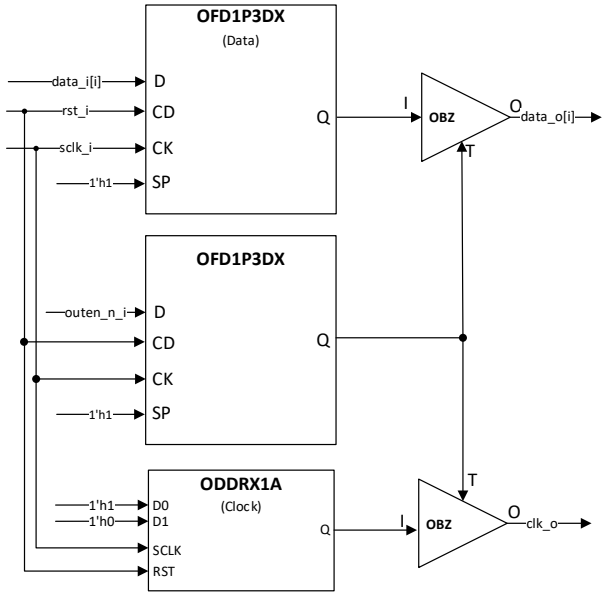

Figure 2.18. GOREG_TX.SCLK Bypass Delay Tristate Control Enabled Interface

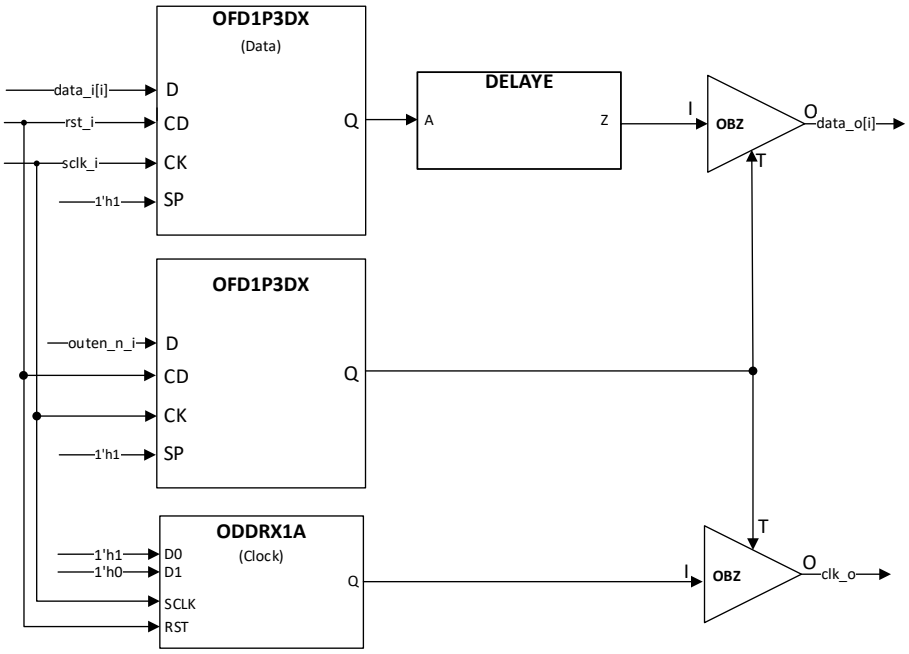

Figure 2.19. GOREG_TX.SCLK Static User Defined Delay Tristate Control Enabled Interface

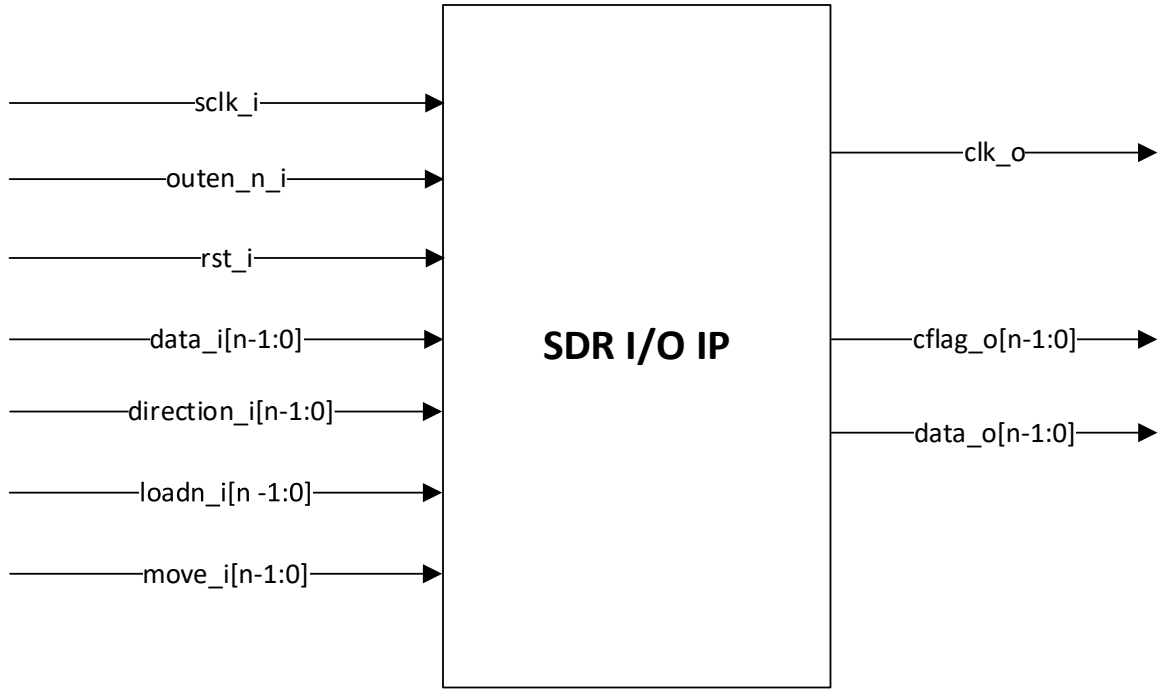

Figure 2.20. GOREG_TX.SCLK Dynamic User Defined Delay Tristate Control Enabled Block Diagram

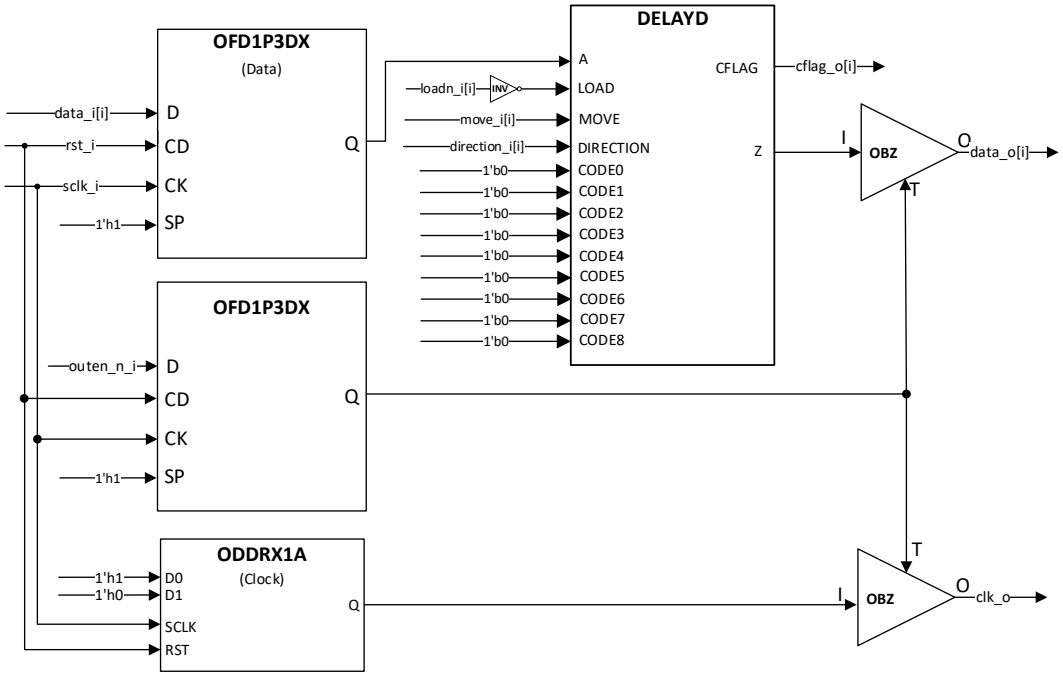

Figure 2.21. GOREG_TX.SCLK Dynamic User Defined Delay Tristate Control Enabled Interface

2.3. Signal Description

Table 2.2. SDR I/O Module Receive Signal Description

Port Name	Direction	Description
Clocks and Reset		
rst_i	In	Active high reset signal.
sclk_o	Out	Received data sampling clock
User Interface		
data_o[n-1:0]	Out	Received input data to fabric.
loadn_i[n-1:0]	In	Active low signal to reset data path delay setting to default. Only available during dynamic default or dynamic user-defined data path delay.
move_i[n-1:0]	In	Increments or decrements data path delay setting depending on direction_i. Only available during dynamic default or dynamic user-defined data path delay.
direction_i[n-1:0]	In	*1* to decrease and *0* to increase data path delay. This is only available during dynamic default or dynamic user-defined data path delay.
cflag_o[n-1:0]	Out	Underflow or overflow flag to indicate that minimum or maximum data path delay adjustment is reached. This is only available during dynamic default or dynamic user-defined data path delay.
I/O Pad Interface		
clk_i	In	Clock input signal from I/O.
data_i[n-1:0]	In	Data input signal from I/O.

Note: n = number of lanes/bus width.

Table 2.3. SDR I/O Module Transmit Signal Description

Port Name	Direction	Description
Clocks and Reset		
rst_i	In	Active high reset signal.
sclk_i	In	Transmit data sampling clock.
User Interface		
data_i[n-1:0]	In	Transmit output data going to I/O.
outen_n_i	In	Active low signal output enable. Only available when Tri-State mode is enabled.
loadn_i[n-1:0]	In	Active low signal to reset data path delay setting to default. Only available during dynamic default or dynamic user-defined data path delay.
move_i[n-1:0]	In	Increments or decrements data path delay setting depending on direction_i. Only available during dynamic default or dynamic user-defined data path delay.
direction_i[n-1:0]	In	*1* to decrease and *0* to increase data path delay. This is only available during dynamic default or dynamic user defined data path delay.
cflag_o[n-1:0]	Out	Underflow or overflow flag to indicate that minimum or maximum data path delay adjustment is reached. This is only available during dynamic default or dynamic user-defined data path delay.
I/O Pad Interface		
clk_o	Out	Clock output signal to I/O.
data_o[n-1:0]	Out	Data output signal to I/O.

Note: n = number of lanes/bus width.

2.3. Attribute Summary

Table 2.4 provides a list of user configurable attributes for the SDR I/O Module. Attribute settings are specified using SDR I/O Module Configuration user interface in Lattice Radiant.

Table 2.4. Attributes Table

Attribute	Selectable Values	Default	Dependency on other Attributes	Additional Requirements
Interface Type	Receive, Transmit	Receive	—	—
I/O Standard for this Interface	(Legal Combination Table)	LVDS	—	—
Bus Width for this Interface	1 – 256	8	—	—
Data Path Delay	Bypass, Static Default, Dynamic Default, Static User Defined, Dynamic User Defined	Bypass	*Static Default* and *Dynamic Default* are supported for *Interface Type* == *Receive*	—
Fine Delay Value for User Defined	0 – Maximum Fine Delay	0	*Data Path Delay* == *Static User Defined* or *Dynamic User Defined* Maximum Fine Delay = (1/ *Clock Frequency*)/14ps Note: In silicon, targeted delay step is 12.5 ps. In functional simulation, delay step that can be observed is 10ps. Meanwhile 14ps is the observed delay step on timing characterization.	—
Enable Tristate Control	Checked, Not checked	Not checked	*Interface Type* == *Transmit*	—
Enable Clock Inversion	Checked, Not	Not	*Interface Type* == *Receive*	—

Attribute	Selectable Values	Default	Dependency on other Attributes	Additional Requirements
	checked	checked		
Clock Frequency for this Interface (MHz)	1 – 250	200	—	—
Bandwidth for this Interface (Mbits/s)	Calculated	1600	Clock Frequency × Bus Width	Display for information only

Note: All attributes can be configured from the General tab of the Lattice Radiant Software user interface.

Table 2.5 shows the description of the attributes used on SDR I/O module.

Table 2.5. Attributes Description

Attribute Name	Description
Interface Type	Selects interface type as Receive or Transmit.
I/O Standard for this Interface	List of Single-ended or Differential I/O supported.
Bus Width for this Interface	Total number of lanes/bus width.
Data Path Delay	Selects among Bypass, Static Default, Static User Defined, Dynamic Default or Dynamic User Defined. Allows setting default data path fine delay value when selected as Static User Defined or Dynamic User Defined.
Fine Delay Value for User Defined	Default data path fine delay setting. This is only valid when Data Path Delay is Static User Defined or Dynamic User Defined. For STATIC mode, value overrides the default delay setting. For DYNAMIC mode, this is the initial value of the fine delay element. Ideally, a 9-bit binary string, 12.5 ps per step. max_fine_delay = 511 × 12.5 ps = 6387.5ps Note: The silicon is designed to have 12.5ps delay per step but on simulation, only 10ps can be observed.
Enable Tristate Control	Tristate enabled during transmission.
Enable Clock Inversion	Clock Inversion enabled. If enabled, received data sampling clock signal is inversed.
Clock Frequency for this Interface (MHz)	Clock frequency to be used in selected interface.

3. IP Generation and Evaluation

This section provides information on how to generate the IP using the Lattice Radiant Software, and how to run simulation, synthesis, and hardware evaluation. For more details on the Lattice Radiant Software, refer to the Lattice Radiant Software User Guide.

3.1. Licensing the IP

No license is required for this module.

3.2. Generation and Synthesis

The Lattice Radiant Software allows you to customize and generate modules and IPs and integrate them into the device's architecture. The procedure for generating the SDR I/O module in Lattice Radiant Software is described below.

To generate SDR I/O Module:

1. Create a new Lattice Radiant Software project or open an existing project.
2. In the **IP Catalog** tab, double-click on **SDR** under **Module, Architecture_Modules, IO** category. The **Module/IP Block Wizard** opens as shown in Figure 3.1. Enter values in the **Component name** and the **Create in** fields and click **Next**.

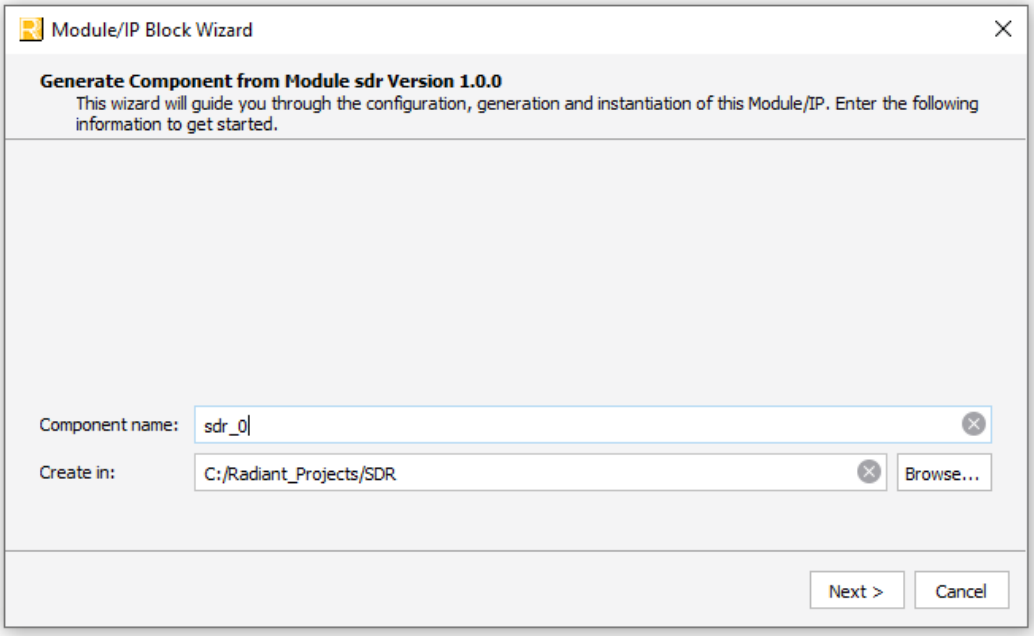

Figure 3.1. Module/IP Block Wizard

3. In the module's dialog box of the **Module/IP Block Wizard** window, customize the selected SDR I/O module using drop-down menus and check boxes. As a sample configuration, see Figure 3.2. For configuration options, see the Attribute Summary section.

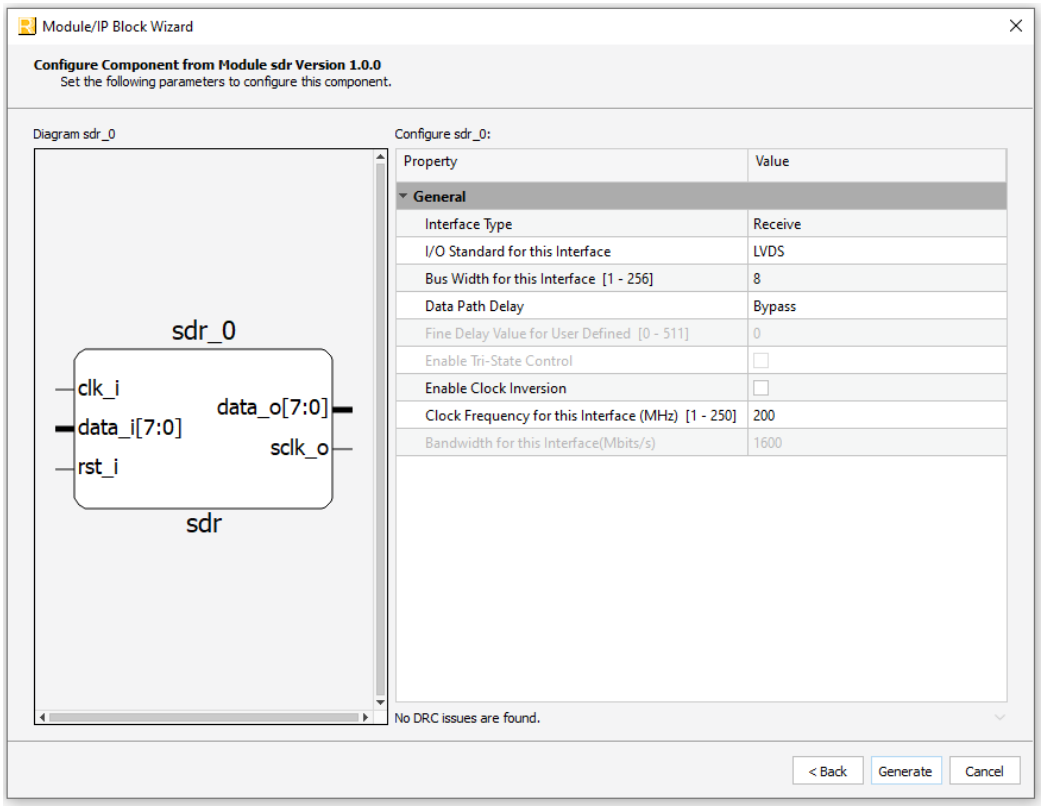

Figure 3.2. Configure Block of SDR I/O Module

4. Click **Generate**. The **Check Generated Result** dialog box opens, showing design block messages and results as shown in Figure 3.3.

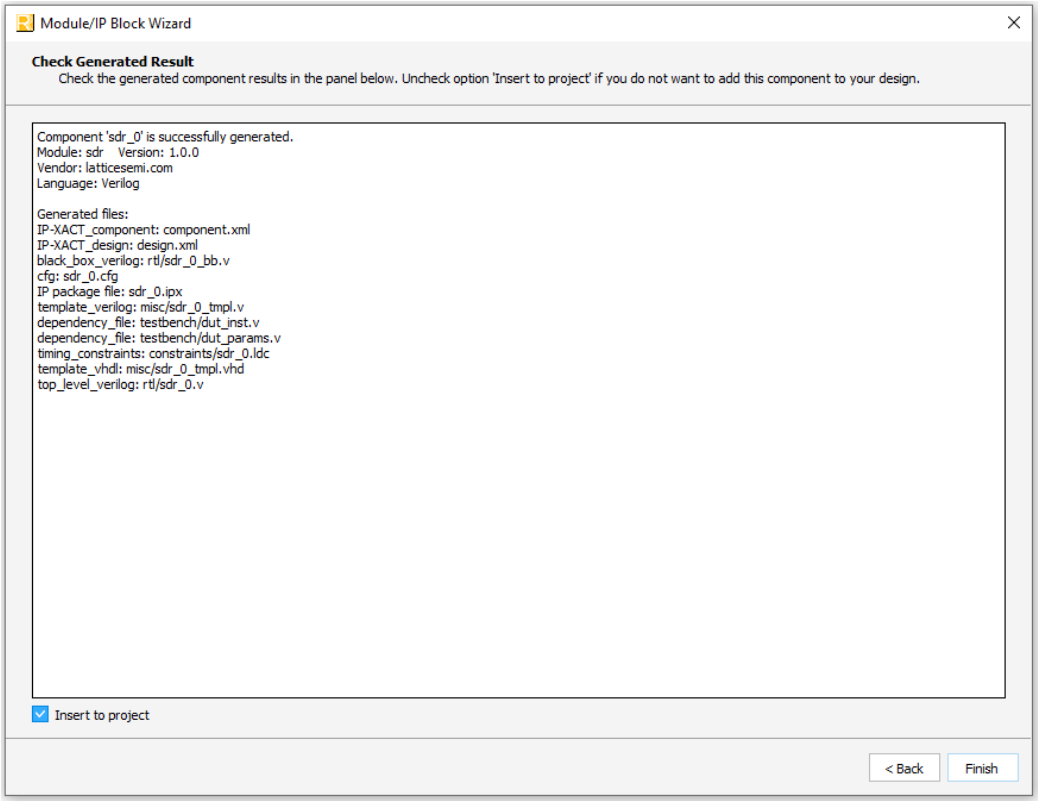

Figure 3.3. Check Generated Result

5. Click the **Finish** button. All the generated files are placed under the directory paths in the **Create in** and the **Component name** fields shown in Figure 3.1.

The generated SDR I/O module package includes the black box (<Instance Name>_bb.v) and instance templates (<Instance Name>_tmpl.v/vhd) that can be used to instantiate the module in a top-level design. An example RTL top-level reference source file (<Instance Name>.v) that can be used as an instantiation template for the module is also provided. You may also use this top-level reference as the starting template for the top-level for their complete design. The generated files are listed in Table 3.1.

Table 3.1. Generated File List

Attribute	Description
<Instance Name>.ipx	This file contains the information on the files associated to the generated IP.
<Instance Name>.cfg	This file contains the parameter values used in IP configuration.
component.xml	Contains the ipxact:component information of the IP.
design.xml	Documents the configuration parameters of the IP in IP-XACT 2014 format.
rtl/<Instance Name>.v	This file provides an example RTL top file that instantiates the module.
rtl/<Instance Name>_bb.v	This file provides the synthesis black box.
misc/<Instance Name>_tmpl.v misc /<Instance Name>_tmpl.vhd	These files provide instance templates for the module.
testbench/tb_top.v	Test bench template; you can edit this to match your specific needs.
testbench/dut_params.v	Instantiated version of the <IP_name>.v file for simulation use
testbench/dut_ints.v	Top level parameters of the generated RTL file

3.3. Running Functional Simulation

After the IP is generated, running functional simulation can be performed using different available simulators. The default simulator already has pre-compiled libraries ready for simulation. Choosing a non-default simulator, however, may require additional steps.

To run functional simulation using the default simulator:

1. Click the  button located on the **Toolbar** to initiate **Simulation Wizard**, as shown in Figure 3.4.

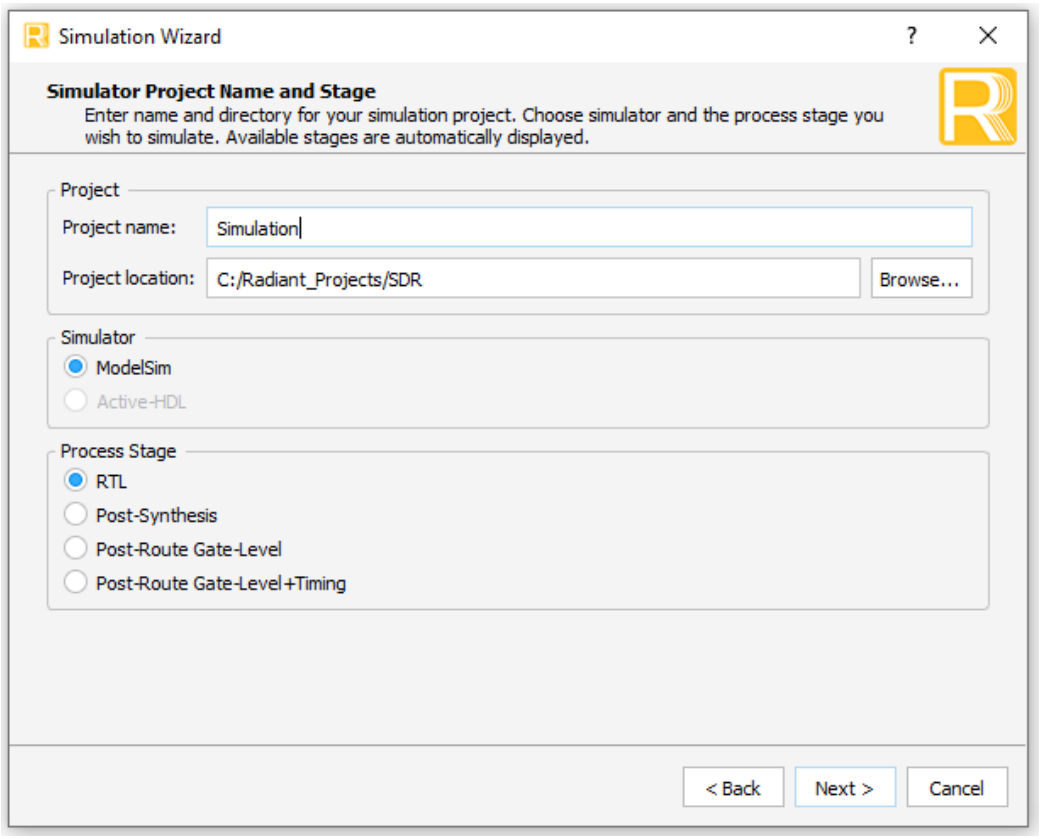

Figure 3.4. Simulation Wizard

2. Click **Next** to open the **Add and Reorder Source** window as shown in Figure 3.5.

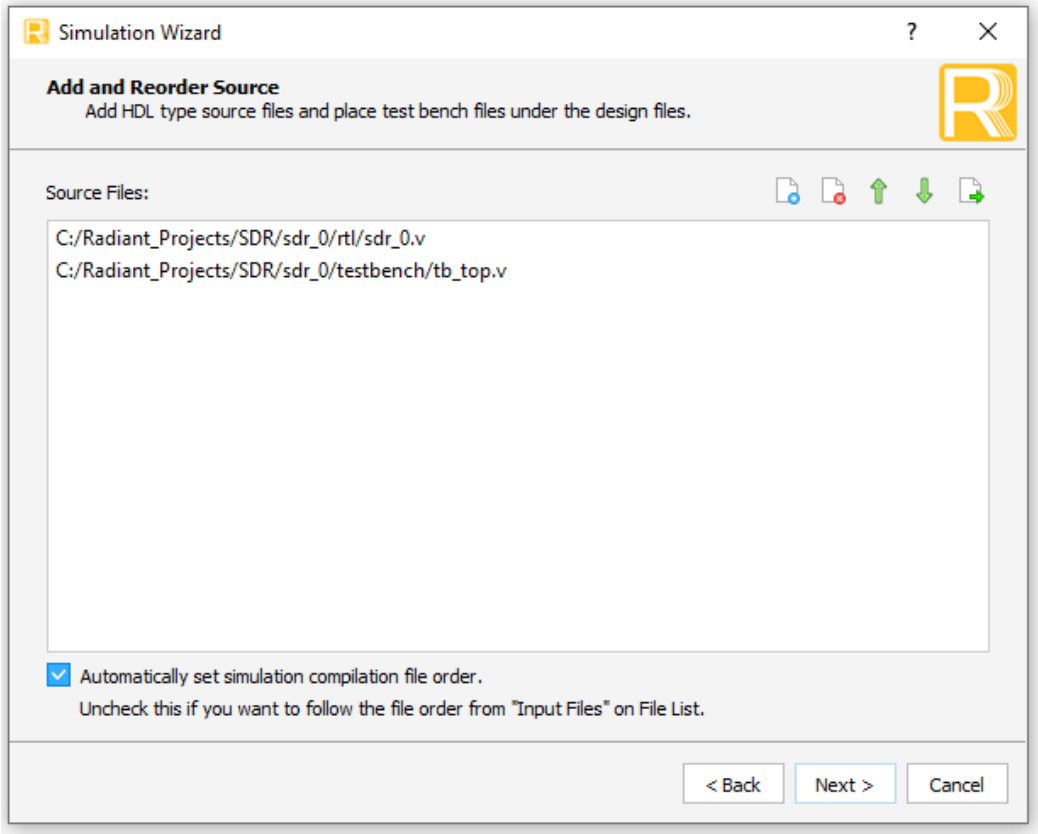

Figure 3.5. Adding and Reordering Source

3. Click **Next**. The Summary window is shown. Click **Finish** to run the simulation.

Note: It is necessary to follow the procedure above until it is fully automated in the Lattice Radiant Software Suite.

The results of the simulation in our example are provided in Figure 3.6.

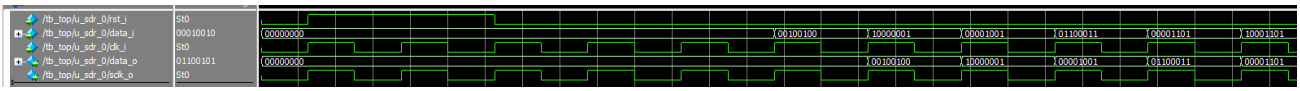

Figure 3.6. Simulation Waveform

3.4. Hardware Evaluation

There is no restriction on the hardware evaluation of this module.

Appendix A. Resource Utilization

The SDR module resource utilization is shown in Table A.1 using LAV-AT-500E-1LFG672C device with Lattice Synthesis Engine of Lattice Radiant software 2022.1. Default configuration is used, and some attributes are changed from the default value to show the effect on the resource utilization.

Table A.1. Resource Utilization

Configuration	Clk Fmax (MHz)[1]	Registers	LUTs[2]	EBRs	DSPs
Default	200	16	9	0	0
Data Path Delay = Static User Defined, Fine Delay Value = 10, others = Default	200	16	9	0	0
Interface Type = Transmit, others = Default	200	16	9	0	0
Interface Type = Transmit, Data Path Delay = Dynamic User Defined, Fine Delay Value = 10, others = Default	200	16	17	0	0

Notes:

1. Fmax is generated when the FPGA design only contains the SDR module, and the target frequency is 200 MHz. These values may be reduced when user logic is added to the FPGA design.
2. The *distributed RAM* utilization is accounted for in the total LUT4s utilization. The actual LUT4 utilization is distribution among *logic, distributed RAM*, and *ripple logic*.

References

For complete information on Lattice Radiant Project-Based Environment, Design Flow, Implementation Flow and Tasks, as well as on the Simulation Flow, see the Lattice Radiant Software User Guide.

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.0, October 2022

Section	Change Summary
Resource Utilization	Added Appendix A. Resource Utilization section.

Revision 0.8, May 2022

Section	Change Summary
All	Initial release.

www.latticesemi.com