SubLVDS Image Sensor Receiver IP Core

User Guide

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Inclusive Language

This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
APB	Advanced Peripheral Bus
AXI4-Stream	Advanced eXtensible Interface 4 Stream
EAV	End of Active Video
LSE	Lattice Synthesis Engine
LVDS	Low-Voltage Differential Signaling
SAV	Start of Active Video
Sub-LVDS	A reduced-voltage form of LVDS signaling
RX	Receive

1. Introduction

The Lattice Semiconductor SubLVDS Image Sensor Receiver IP Core converts double data rate interface to pixel clock domain. The SubLVDS interface is primarily used in image sensors. It has one clock pair and more than one data pairs. The number of data pairs varies, depending on bandwidth requirement.

Compared to the LVDS Interface, SubLVDS:

- has lower common mode that is 0.9 V, while the common mode for LVDS is 1.25 V;
- is typically powered by 1.8 V supply, while LVDS uses 2.5 V supply;
- has lower differential swing that is ±150 mV, while the differential swing for LVDS is ±175 mV;
- is a source synchronous interface, the clock pair is running at the same rate as the data. This is not a 7:1 interface;
- has the clock center-aligned with the data.

1.1. Quick Facts

Table 1.1 provides the quick facts about the SubLVDS Image Sensor Receiver IP Core.

Table 1.1. SubLVDS Image Sensor Receiver IP Core Quick Facts

IP Requirements	Supported FPGA Families	Lattice Avant™, MachXO5™-NX, CrossLink™-NX, CertusPro™-NX, Certus™-NX
Resource Utilization	Targeted Devices	LAV-AT-E70, LAV-AT-G70, LAV-AT-X70, LFMXO5-25, LFMXO5-55T, LFMXO5-100T, LIFCL-40, LIFCL-33, LIFCL-17, LFCPNX-100, LFD2NX-40, LFD2NX-17
	Supported User Interface	Native Interface, APB Interface, and AXI4-Stream Transmit Interface. See the Signal Description section.
	Resources	See Table A.1 and Table A.2.
Design Tool Support	Lattice Implementation	IP Core v1.x.x - Lattice Radiant Software 2.1 or later IP Core v1.2.x - Lattice Radiant Software 3.2 IP Core v1.3.x - Lattice Radiant Software 2023.1 IP Core v1.4.x - Lattice Radiant Software 2023.1
	Synthesis	Lattice Synthesis Engine
		Synopsys® Synplify Pro® for Lattice
	Simulation	For the list of supported simulators, see the Lattice Radiant Software User Guide.

1.2. Features

The key features of the SubLVDS Image Sensor Receiver IP Core include:

- Supports 4, 6, 8, 10, 12, 14, or 16 data lanes from an image sensor.
- Supports 10-bit (RAW10) or 12-bit (RAW12) pixel widths.
- Supports gearing of 8 and 16. The gearing 16 option is only for 4-lane configuration.
- Supports APB Interface for register access and AXI4-Stream Transmit Interface.
- Can generate XVS and XHS for image sensors operating in Passive mode.

1.3. Conventions

1.3.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL. This includes radix indications and logical operators. The most significant bit within the pixel data is the highest index.

1.3.2. Signal Names

Signal names that end with:

- *_n* are active low
- *_i* are input signals
- *_o* are output signals
- *_io* are bi-directional signals

1.3.3. Attribute Names

Attribute names in this document are formatted in title case and italicized (*Attribute Name*).

2. Functional Description

2.1. Overview

The SubLVDS Image Sensor Receiver IP Core converts double data rate interface into pixel clock domain. The input interface of the design consists of a data bus and a clock in SubLVDS interface format. The output interface consists of a 10-bit or 12-bit multi-pixel data, frame valid, line valid, data valid and a pixel clock with a gearing of 1:8 or 1:16.

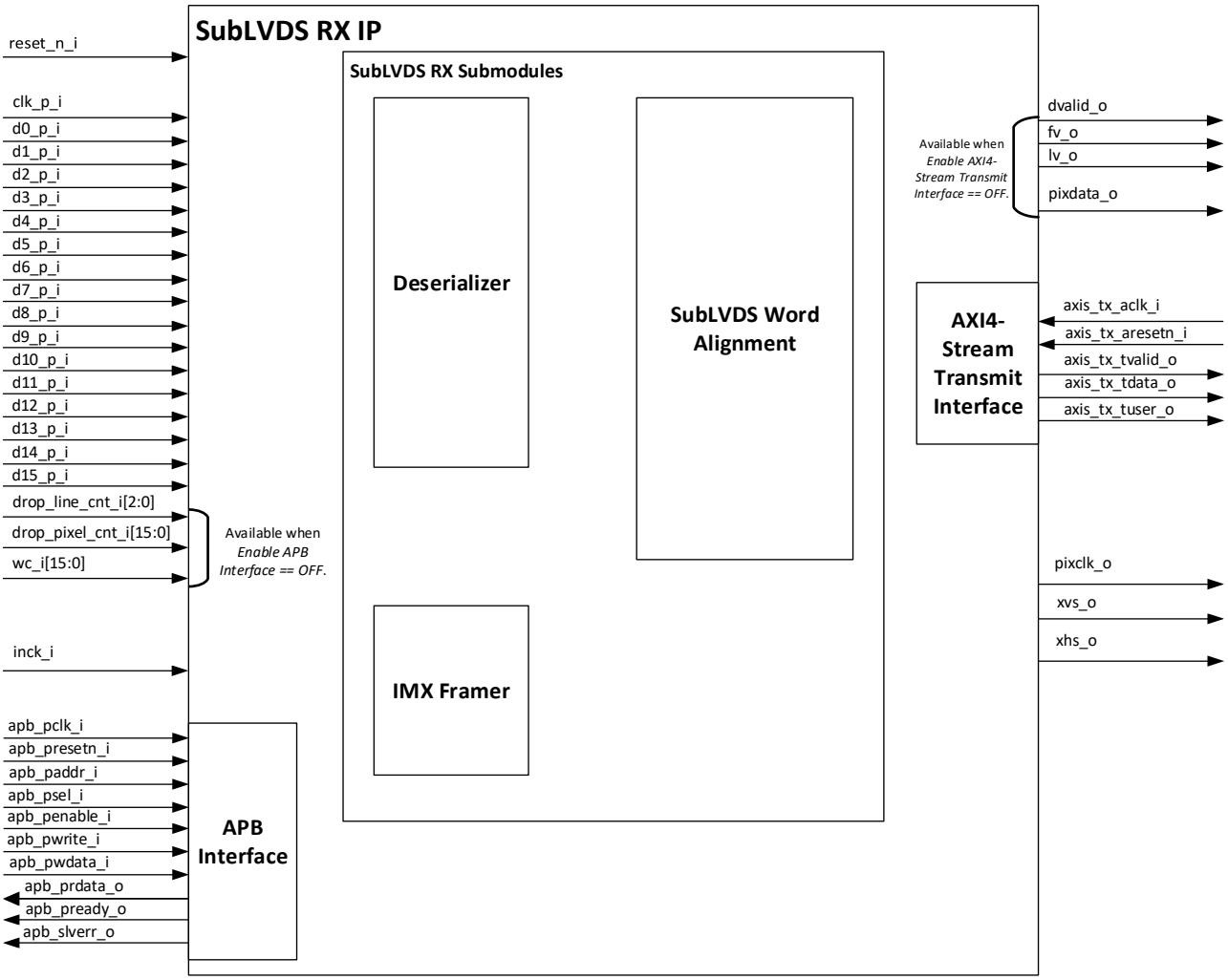

Figure 2.1. SubLVDS Image Sensor Receiver IP Core Top Level Block Diagram

2.2. Signal Description

Table 2.1 lists top-level input and output signals and their descriptions for the SubLVDS Image Sensor Receiver IP Core.

Table 2.1. SubLVDS Image Sensor Receiver IP Core Signal Description

Port Name	I/O	Width	Description
Native Interface Ports			
reset_n_i	In	1	System active low asynchronous reset
inck_i	In	1	IMX Framer input clock. This clock is shared with the Sony Image Sensor.
clk_p_i	In	1	Positive subLVDS input clock to subLVDS RX
d0_p_i	In	1	Positive subLVDS input data lane 0 to subLVDS RX
d1_p_i	In	1	Positive subLVDS input data lane 1 to subLVDS RX
d2_p_i	In	1	Positive subLVDS input data lane 2 to subLVDS RX
d3_p_i	In	1	Positive subLVDS input data lane 3 to subLVDS RX
d4_p_i	In	1	Positive subLVDS input data lane 4 to subLVDS RX
d5_p_i	In	1	Positive subLVDS input data lane 5 to subLVDS RX
d6_p_i	In	1	Positive subLVDS input data lane 6 to subLVDS RX
d7_p_i	In	1	Positive subLVDS input data lane 7 to subLVDS RX
d8_p_i	In	1	Positive subLVDS input data lane 8 to subLVDS RX
d9_p_i	In	1	Positive subLVDS input data lane 9 to subLVDS RX
d10_p_i	In	1	Positive subLVDS input data lane 10 to subLVDS RX
d11_p_i	In	1	Positive subLVDS input data lane 11 to subLVDS RX
d12_p_i	In	1	Positive subLVDS input data lane 12 to subLVDS RX
d13_p_i	In	1	Positive subLVDS input data lane 13 to subLVDS RX
d14_p_i	In	1	Positive subLVDS input data lane 14 to subLVDS RX
d15_p_i	In	1	Positive subLVDS input data lane 15 to subLVDS RX
drop_line_cnt_i[2]	In	3	Number of dropped lines
drop_pixel_cnt_i[2]	In	16	Number of dropped pixels
wc_i[2]	In	16	Word count
dvalid_o[3]	Out	1	Data valid detection signal, indicates valid pixel data.
fv_o[3]	Out	1	Frame valid detection signal, indicates valid frame.
lv_o[3]	Out	1	Line valid detection signal, indicates a valid line.
pixclk_o	Out	1	Pixel clock generated form the CLKDIV
pixdata_o[3]	Out	BUS_WIDTH*LANE_WIDTH[1]	Pixel data coming from the parser module. Multi-pixel data bus.
xvs_o	Out	1	Sony passive readout vertical control signal
xhs_o	Out	1	Sony passive readout horizontal control signal
APB Completer Interface Ports[4]			
apb_pclk_i	In	1	An external clock with a maximum frequency of 144 MHz
apb_presetn_i	In	1	APB active low reset
apb_paddr_i	In	32	APB address
apb_psel_i	In	1	APB completer select
apb_penable_i	In	1	APB completer enable
apb_pwrite_i	In	1	APB completer write
apb_pwdata_i	In	32	APB write data
apb_prdata_o	Out	32	APB read data
apb_pready_o	Out	1	APB ready
apb_pslverr_o	Out	1	APB completer error
AXI4-Stream Transmitter Interface Ports[5]			

Port Name	I/O	Width	Description
axis_tx_aclk_i	In	1	AXI4-Stream Transmit clock with the same frequency as the pixel clock generated from CLKDIV
axis_tx_aresetn_i	In	1	AXI4-Stream Transmit active low reset
axis_tx_tvalid_o	Out	1	AXI4-Stream Transmit valid mapped from *dvalid_o* signal from the Native Interface
axis_tx_tdata_o	Out	192	AXI4-Stream Transmit data-in mapped from *pixdata_o* signal from the Native Interface
axis_tx_tuser_o	Out	2	AXI4-Stream Transmit user-defined output mapped from *fv_o* and *lv_o* signals from the Native Interface

Note:

1. BUS_WIDTH depends on *Data Type*. When *Data Type* == RAW10, if *RX Gear* == 8, BUS_WIDTH == 10 else BUS_WIDTH == 20. When *Data Type* == RAW12, if *RX Gear* == 8, BUS_WIDTH == 12 else BUS_WIDTH == 24. LANE_WIDTH is equal to *Number of RX Lanes*.
2. The port is available when Enable APB Interface == OFF.
3. The port is available when Enable AXI4-Stream Transmit Interface == OFF.
4. These ports are available when Enable APB Interface == ON.
5. These ports are available when Enable AXI4-Stream Transmit Interface == ON.

2.3. Attribute Summary

Table 2.2 lists the parameters used to generate the SubLVDS Image Sensor Receiver IP Core. Table 2.3 describes each attribute.

Table 2.2. Attributes Table

Attribute	Selectable Values	Default	Dependency on Other Attributes
General			
Receiver			
Number of RX Lanes	4, 6, 8, 10, 12, 14, 16	4	—
RX Gear	8, 16	8	—
Clock			
RX Line Rate	160 – 1500	160	*Number of RX Lanes, RX Gear*
SubLVDS Clock Frequency (MHz)	Calculated	80	*RX Line Rate*/2
Pixel Clock Frequency (MHz)	Calculated	20	*Pixel Clock Frequency* = 2*(*SubLVDS Clock Frequency*/*RX Gear*)
Data			
Dropped Line Mode	Static, Dynamic	Dynamic	—
Dropped Line Count	0 – 7	0	*Dropped Line Mode == Static*
Dropped Pixel Mode	Static, Dynamic	Dynamic	—
Dropped Pixel Count	0 – 65535	0	*Dropped Pixel Mode == Static*
Word Count Mode	Static, Dynamic, Off	Dynamic	—
Word Count	0 – 65535	0	*Word Count Mode == Static*
Miscellaneous			
Enable APB Interface	ON, OFF	OFF	—
Enable AXI4-Stream Transmit Interface	ON, OFF	OFF	—
Video			
Video Packet			
Data Type	RAW10, RAW12	RAW10	—
IMX Framer Settings			
Image Sensor Mode	Active, Passive	Active	—
V_TOTAL	2 - 4095	10	*Image Sensor Mode == Passive*
H_TOTAL	0 - 4095	1285	*Image Sensor Mode == Passive*
V_H_BLANK	0 - 4095	2	*Image Sensor Mode == Passive*

Note:

1. Consistent with Lattice Semiconductor inclusive language policy, the terms *active* and *passive* are used in place of the original terms in the Sony Image Sensor Framer document. The technical definitions remain the same.

Table 2.3. Attributes Description

Attribute	Description
General	
Receiver	
Number of RX Lanes	Generates subLVDS I/O.
RX Gear	Specifies the RX gearing. Only the 4-lane configuration has the option to choose between *RX Gear == 8* or *RX Gear == 16*.
Clock	
RX Line Rate	Target *RX Line Rate* per lane
	1500 Mbps maximum line rate is supported in Jedi-D1 Flip-chip packages only. For non-flip-chip package, the maximum line rate is 1250 Mbps.
SubLVDS Clock Frequency (MHz)	SubLVDS clock Automatically computed based on the target *RX Line Rate*.
Pixel Clock Frequency (MHz)	Pixel clock Automatically computed based on the target *RX Line Rate*.
Data	
Dropped Line Mode	Allows you to choose between *Static* (predetermined values for the number of dropped lines) and *Dynamic* (you can determine the values via an added port) Modes.
Dropped Line Count	Determines the number of lines to be dropped at the start of the frame.
Dropped Pixel Mode	Allows you to choose between *Static* (predetermined values for the number of dropped pixels) and *Dynamic* (you can determine the values via an additional port) Modes.
Dropped Pixel Count	Crops the number of pixels after SAV (the OPB and OPB ignore pixels). Refer to the Sony IMX sensor specification for information on these pixels. The input value should be equal to the desired number of pixels to drop/*Number of RX Lanes*. For example, to drop 8 pixels when *Number of RX Lanes* == 4, the input to *Dropped Pixel Count* should be 2.
Word Count Mode	Allows you to choose between *Static* (predetermined values for the word count), *Dynamic* (user determines values via an additional port) and *Off* (logic not used) Modes.
Word Count	Number of active video pixels per line after the dropped pixels (when *Dropped Pixel Count* > 0). Reducing this effectively drops the OPB ignore bits right before the EAV. Kindly refer to the Sony IMX sensor specification for information on these pixels. If *Word Count* == 0 and *Dropped Pixel Count* == 0, the total number of pixels coming out of the design is the total number of active pixels sent by sensor + EAV pixels. The input value should be equal to the desired total number of pixels/*Number of RX Lanes*. For example, if the desired total number of pixels is 40 and Number of RX Lane == 4, *Word Count* should be 10.
Video	
Miscellaneous	
Enable APB Interface	If this interface is *ON*, the APB Interface is used instead of the Native SubLVDS Rx Interface.
Enable AXI4-Stream Transmit Interface	If this interface is *ON*, the AXI4-Stream Transmit Interface is used instead of the Native SubLVDS Rx Interface.
Video Packet	
Data Type	Selects desired data type.
IMX Framer Settings	
Image Sensor Mode	Sets the mode of the image sensor. In passive mode, it enables the IMX framer.
V_TOTAL	Sets the number of lines XVS is driven high. Only available when *Image Sensor Mode == Passive*.
H_TOTAL	Sets the number of INCK clocks XHS is driven high. Only available when *Image Sensor Mode == Passive*.
V_H_BLANK	Sets the number of INCK clocks XVS and XHS are driven low. Only available when *Image Sensor Mode == Passive*.

2.4. Modules Description

2.4.1. Clock, Reset and Initialization

Active low reset is used in the design with synchronous release. Resets for each clock domain are synchronized to their respective clock domains.

The system reset, reset_n_i, is synchronized to the pixel clock domain and it serves as a reset source for the SubLVDS Word Alignment module.

No special reset sequence is required in this IP.

The RX clock input, clk_p_i, is from an external source (image sensor) and should be connected to a dedicated SubLVDS edge clock pin. The Deserializer block generates a pixel clock, pixclk_o, with a gearing of 1:8 or 1:16 for the pixel data.

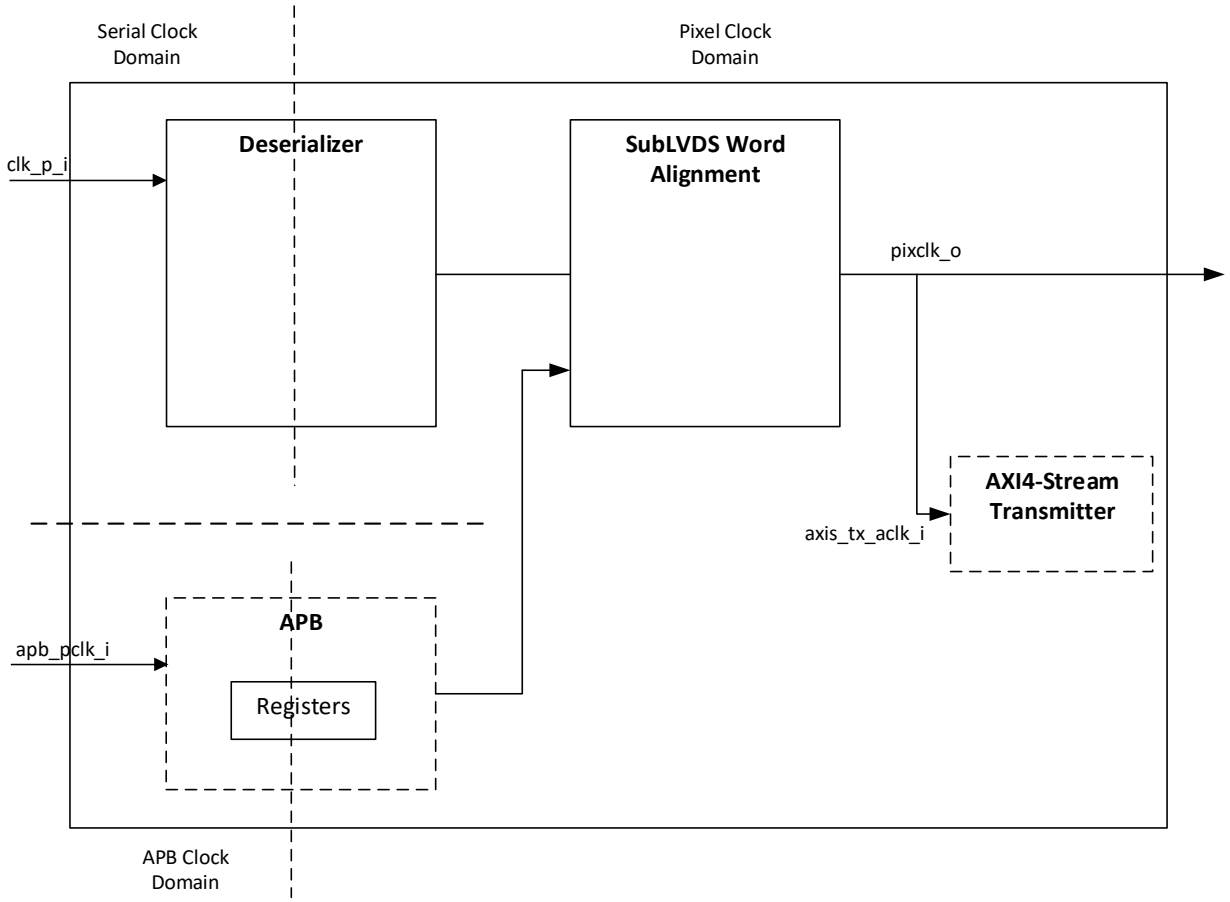

Figure 2.2. Clock Domain Crossing Block Diagram

Table 2.4. Clock Domain Crossing

Clock Domain Crossing	Handling Approach
SubLVDS Serial Clock to Pixel Clock	1:8/1:16 gearbox DDR Hard IP

The general formula for computing the required clocks of the system:

RX Line Rate (total) = total pixels (active + blanking) ∗ frame rate ∗ bits per pixel

RX Line Rate (per lane) = *RX Line Rate* (total)/*Number of RX lanes*

RX input clock = *RX Line Rate* (per lane)/2

Pixel clock = RX input clock/*RX Gear*

Note: gearing = 4 if 1:8 gearing; gearing = 8 if 1:16 gearing.

2.4.2. SubLVDS Image Sensor Receiver IP Core Submodules

The SubLVDS RX IP consists of the Deserializer module, the SubLVDS Word Alignment module, the IMX Framer module, an optional APB Interface module, and an optional AXI4-Stream Transmitter Interface module.

The Deserializer block converts each double data rate lane (d*_p_i signals) to a single data rate 8-bit or 16-bit at a slower operating speed within a system.

The word alignment module receives the 8-bit (1:8 gearing) or 16-bit (1:16 gearing) deserialized data (deser_q_o signal) and converts it to 10-bit or 12-bit pixel data according to the set configuration of data type (RAW10 or RAW12). The output of the module is a multi-pixel bus (pixdata_o), pixel clock (pixclk_o), dvalid_o, fv_o, and lv_o control signals.

The IMX Framer module is used for Image Sensors that operate in the Passive mode only.

Figure 2.3 shows the detailed block diagram of the SubLVDS Image Sensor Receiver IP Core when both the APB and AXI4-Stream Transmitter interfaces are not enabled. Figure 2.4 shows the detailed block diagram of the SubLVDS Image Sensor Receiver IP Core when the APB interface is enabled. Figure 2.5 shows the detailed block diagram of the SubLVDS Image Sensor Receiver IP Core when the AXI4-Stream Transmitter interface is enabled. Figure 2.6 shows the detailed block diagram of the SubLVDS Image Sensor Receiver IP Core when both the APB and AXI4-Stream Transmitter interfaces are enabled.

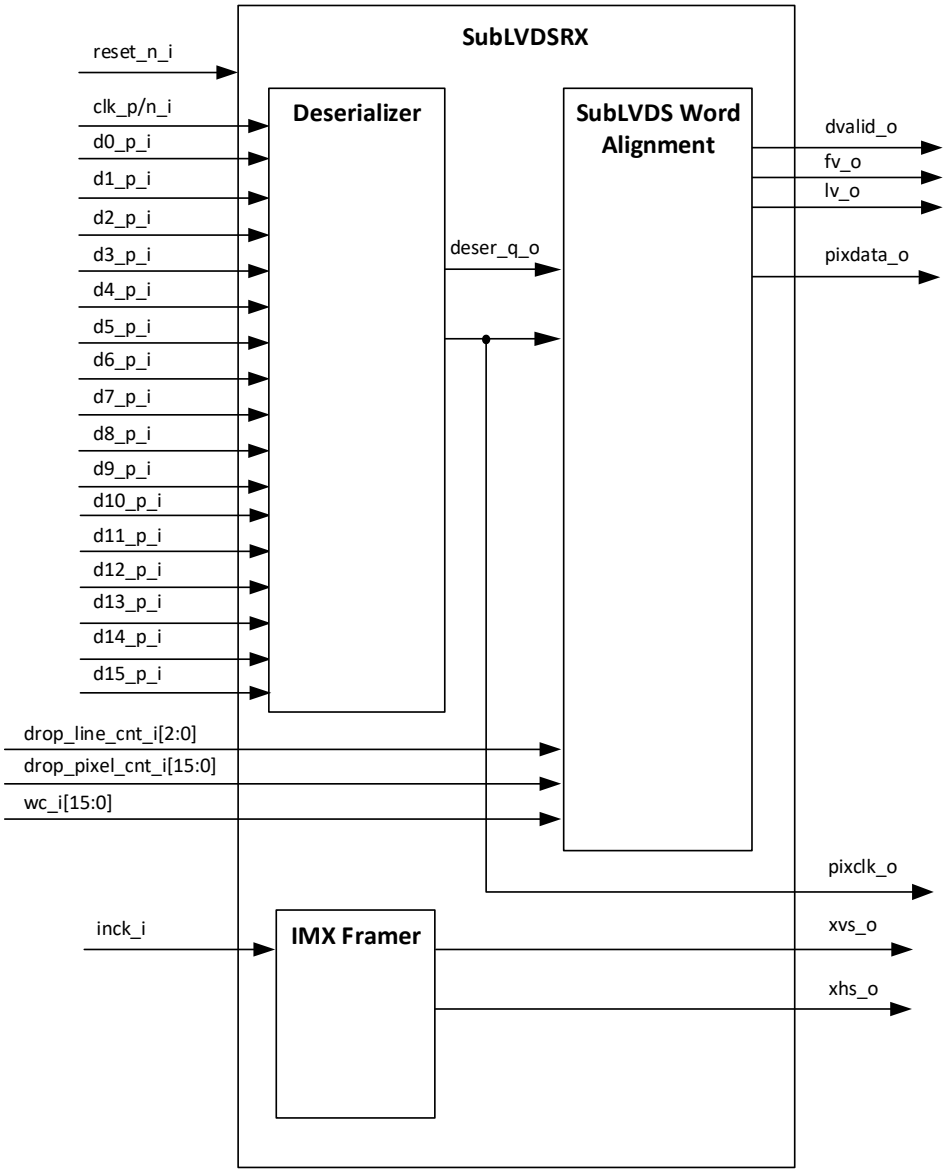

Figure 2.3. SubLVDS Image Sensor Receiver IP Core Detailed Block Diagram (APB and AXI4-Stream Transmitter Interfaces not Enabled)

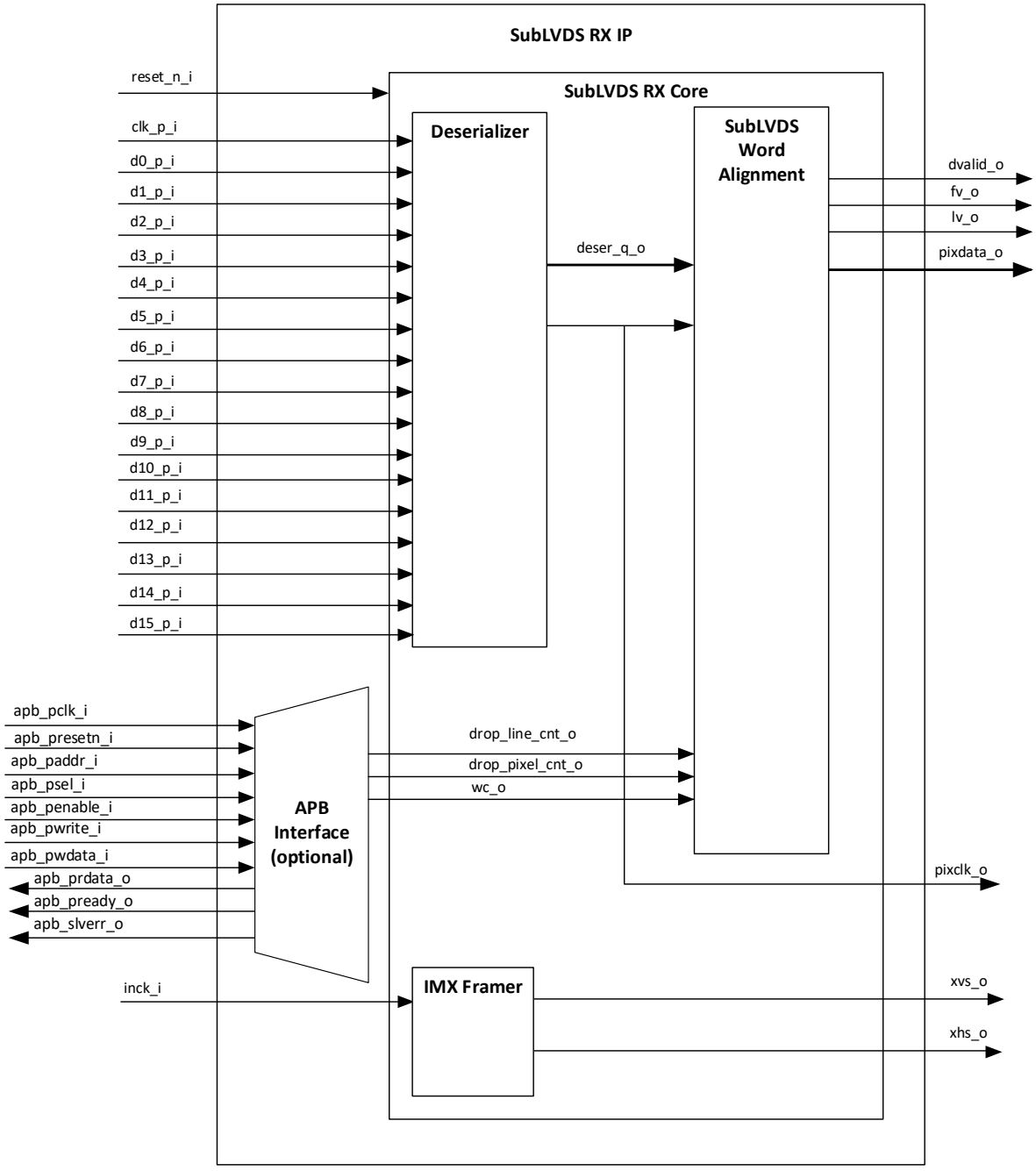

Figure 2.4. SubLVDS Image Sensor Receiver IP Core Detailed Block Diagram (APB Interface Enabled)

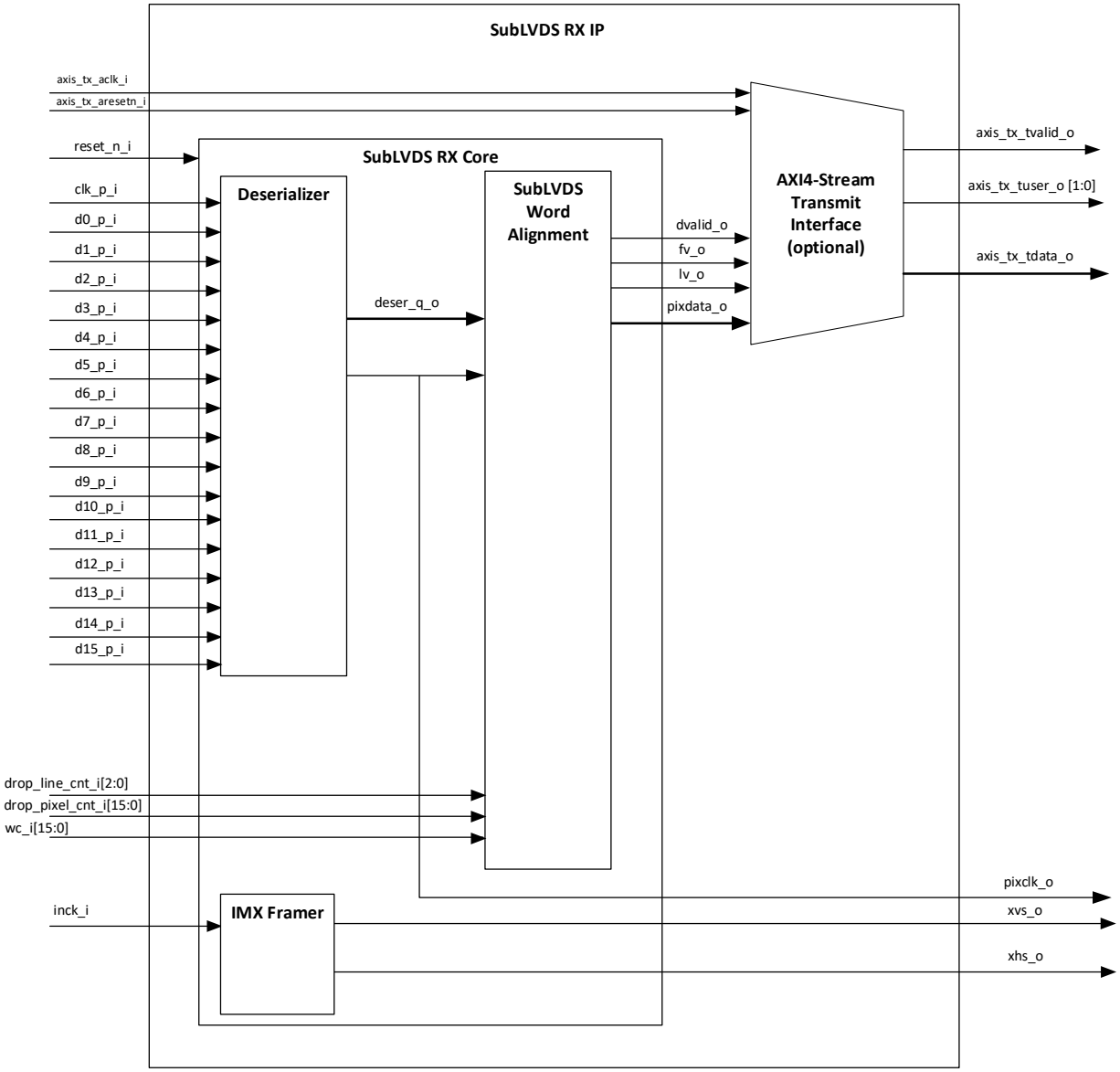

Figure 2.5. SubLVDS Image Sensor Receiver IP Core Detailed Block Diagram (AXI4-Stream Transmitter Interface Enabled)

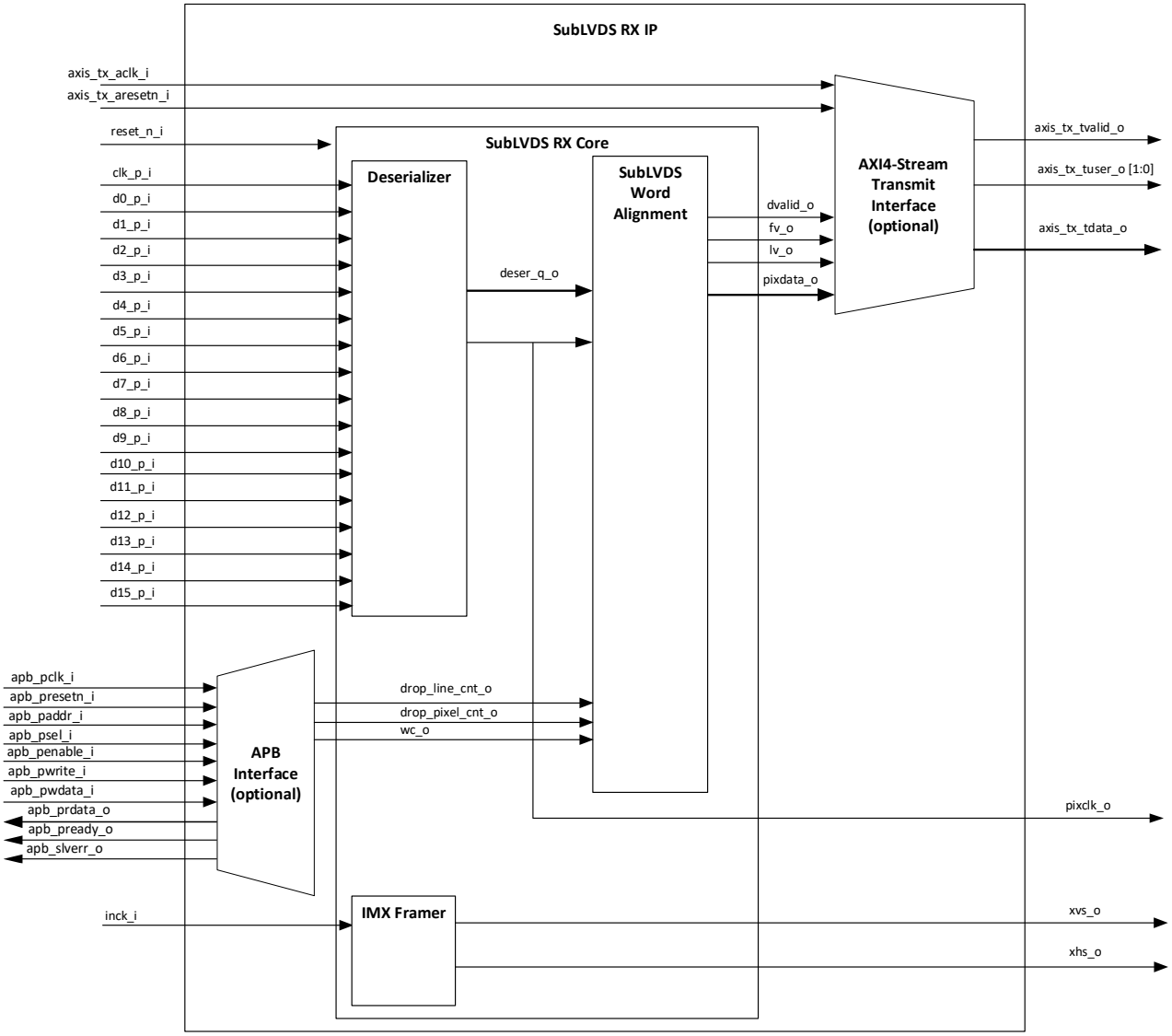

Figure 2.6. SubLVDS Image Sensor Receiver IP Core Detailed Block Diagram (APB and AXI4-Stream Interfaces Enabled)

2.5. Register Descriptions

All registers are accessed through the APB Interface. Access Types of each register are defined in Table 2.5.

Table 2.5. Access Types

Access Types	Behavior on Read Access	Behavior on Write Address
RW	Returns register value	Updates register value.
RSVD	Returns 0	Ignores write access.

2.5.1. Configuration Registers

The design maintains configuration registers summarized in Table 2.6.

Table 2.6. Summary of Registers

Offset	Register Name	Access	Description
0x000	DROP_PIXEL_CNT	RW	Register for the number of dropped pixels
0x004	DROP_LINE_CNT	RW	Register for the number of dropped lines
0x008	WC	RW	Register for word count

2.5.1.1. DROP_PIXEL_CNT Register

This register records the number of dropped pixels when APB is enabled.

Table 2.7. DROP_PIXEL_CNT Register

Bit	Label	Description	Default
[31:16]	RSVD	Reserved bits	0
[15:0]	drop_pixel_cnt_o	Number of dropped pixels	0

2.5.1.2. DROP_LINE_CNT Register

This register records the number of dropped lines when APB is enabled.

Table 2.8. DROP_LINE_CNT Register

Bit	Label	Description	Default
[31:3]	RSVD	Reserved bits	0
[2:0]	drop_line_cnt_o	Number of dropped lines	0

2.5.1.3. WC Register

This register records the word count when APB is enabled.

Table 2.9. WC Register

Bit	Label	Description	Default
[31:16]	RSVD	Reserved bits	0
[15:0]	wc_o	Number of dropped lines	0

If the APB Interface is not enabled, then the internal signals listed below turn to top-level input signals.

- drop_line_cnt_i
- drop_pixel_cnt_i
- wc_i

2.6. AXI4-Stream Transmit Interface

The AXI4-Stream Transmit Interface provides the transmission of pixel data. AXI4-Stream data valid acts as an enable signal and the data is driven on the AXI transmit data bus.

2.6.1. Default Normal Transmission

Figure 2.7 shows the default normal transmission when using the AXI4-Stream Interface:

- T0: *axis_tx_tuser_o*[1:0] and *axis_tx_tvalid_o* are asserted to indicate the start of valid data transmission.
- T1: *axis_tx_tuser_o*[0] is de-asserted to indicate the end of valid data transmission.

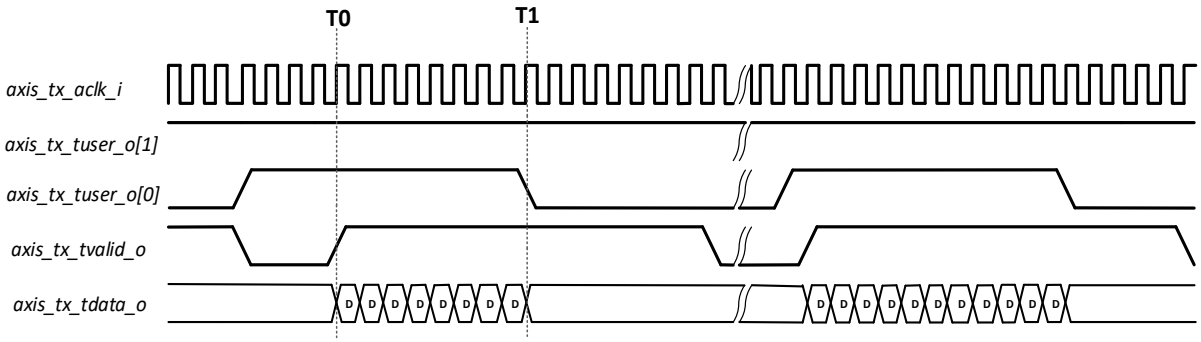

Figure 2.7. Default Normal Transmission

2.6.2. Custom Transmission

AXI4-Stream Transmission only allows data width in multiples of 8 (refer to AMBA 4 AXI4-Stream Protocol version 1.0 for the operation). In this transmission, data padding is used when the Number of Rx Lanes == 6, 10, and 14 for the Data Type == RAW10.

Figure 2.8 shows the timing diagram of custom transmission when using the AXI4-stream Interface.

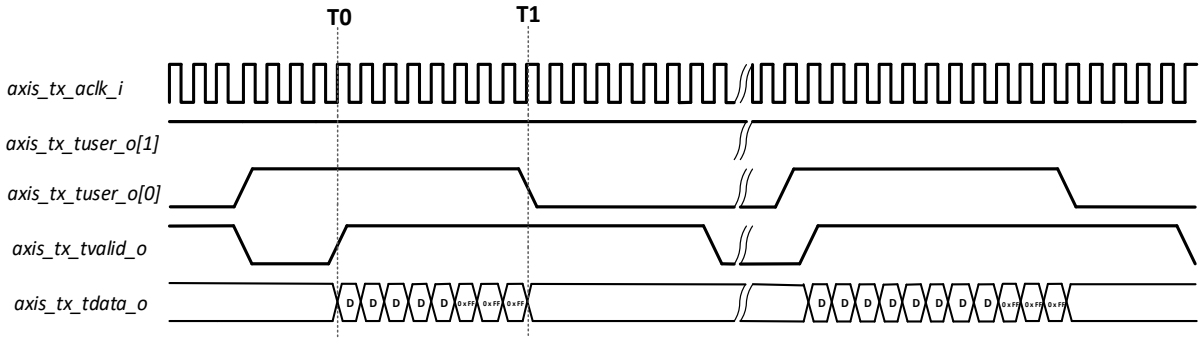

Figure 2.8. Custom Transmission

If the AXI4-Stream Transmitter is not enabled, then the internal signals listed below turns to top-level input signals.

- pixdata_o
- fv_o
- lv_o
- dvalid_o

2.7. Timing Specifications

Figure 2.9 shows the timing of SubLVDS Image Sensor Receiver IP Core input interface. It shows the sync signal and data output timing during 10-bit length serial received from the image sensor.

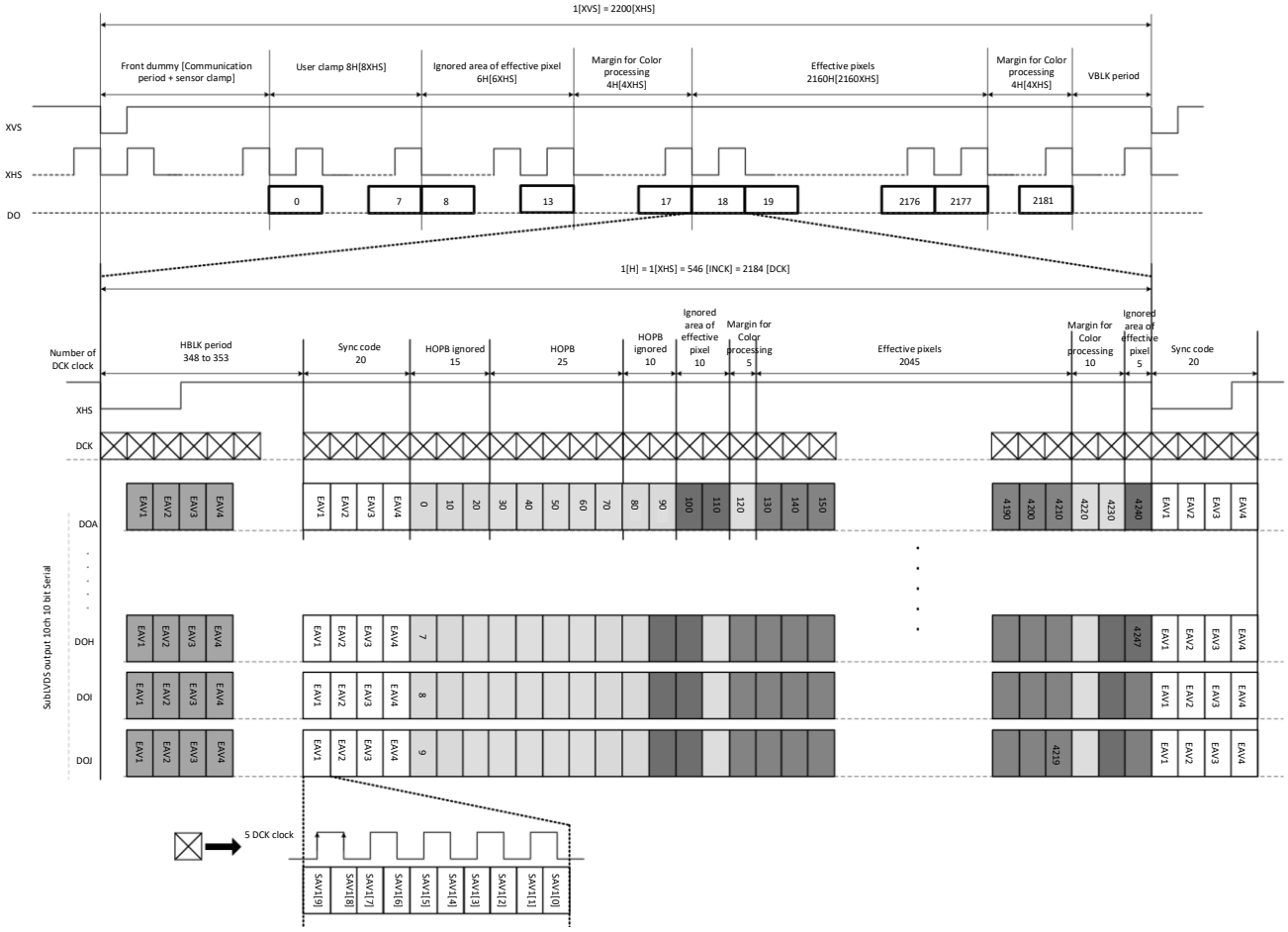

Figure 2.9. SubLVDS Image Sensor Receiver IP Core Input Bus Waveform

The horizontal and vertical timing of the received data are controlled by the XVS and XHS sync signals. The sync code is added before and after the pixel data. Table 2.10 lists the sync code details.

Table 2.10. Sync Code Details

LVDS Output Bit No.		Sync code			
12-bit Output	10-bit Output	1st Word	2nd Word	3rd Word	4th Word
11	9	1	0	0	1
10	8	1	0	0	0
91	7	1	0	0	V
82	6	1	0	0	H
73	5	1	0	0	P3
63	4	1	0	0	P2
53	3	1	0	0	P1
43	2	1	0	0	P0
3	1	1	0	0	0
2	0	1	0	0	0
1	—	1	0	0	0
0	—	1	0	0	0

		Protection Bits			
V	H	P3	P2	P1	P0
0	0	0	0	0	0
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	1	1	0

Notes:

1. 1: Blanking line; 0: Except blanking line
2. 1: End sync code; 2: Start sync code
3. Protection bits

2.8. Sample Configurations

Waveforms below show the output behavior with different *Word Count* and *Dropped Pixel Count* but having the same *Number of Rx Lanes* == 4, Data Type == RAW10 and the number of pixels sent by the sensor is 40 pixels.

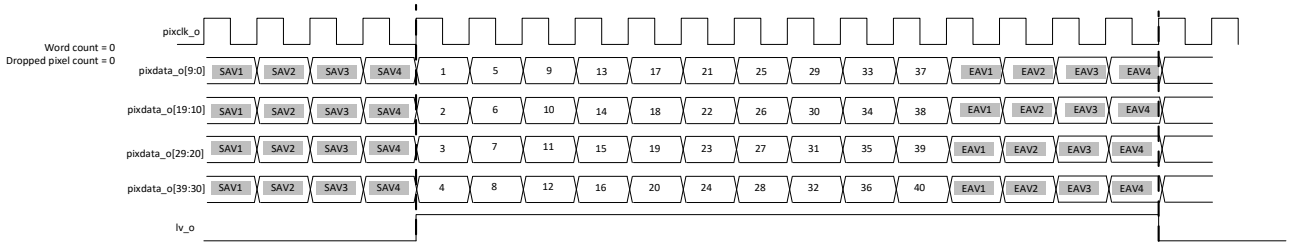

Figure 2.10. SubLVDS Image Sensor Receiver Output Concept Waveform when Word Count == 0 and Dropped Pixel Count ==0

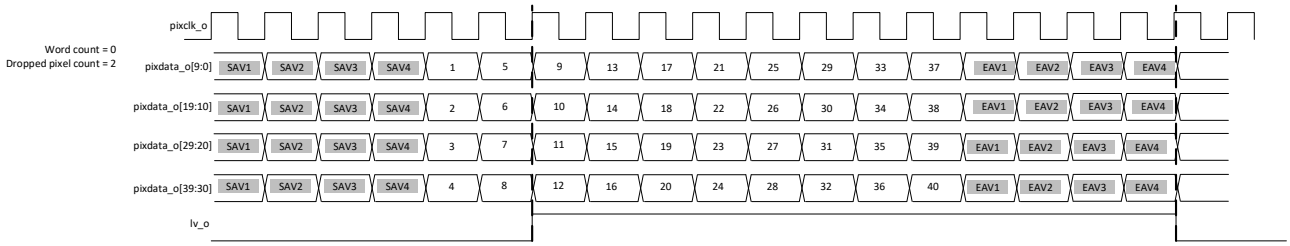

Figure 2.11. SubLVDS Image Sensor Receiver Output Concept Waveform when Word Count == 0 and Dropped Pixel Count ==2

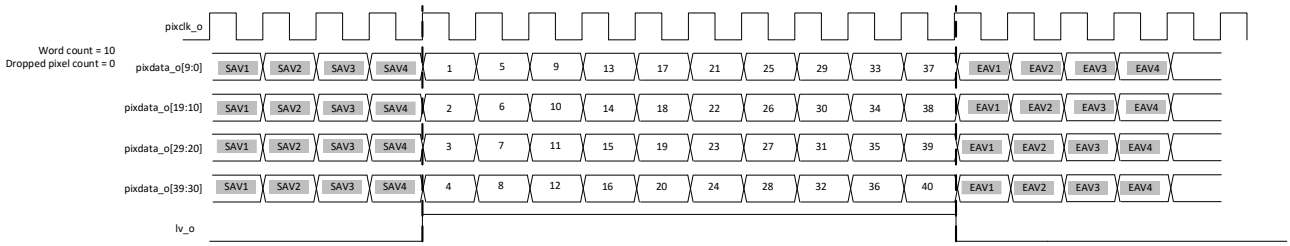

Figure 2.12. SubLVDS Image Sensor Receiver Output Concept Waveform when Word Count == 10 and Dropped Pixel Count ==0

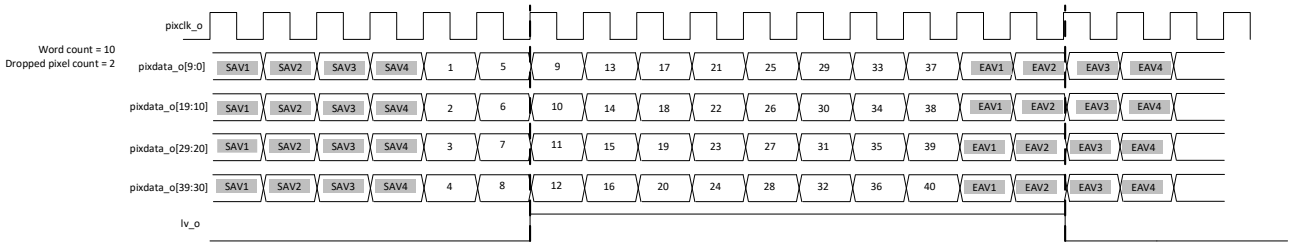

Figure 2.13. SubLVDS Image Sensor Receiver Output Concept Waveform when Word Count == 10 and Dropped Pixel Count ==2

3. IP Generation and Evaluation

This section provides information on how to generate the SubLVDS Image Sensor Receiver IP Core using the Lattice Radiant software and how to run simulation and synthesis. For more details on the Radiant software, refer to the Lattice Radiant Software User Guide.

3.1. Licensing the IP

An IP core-specific license string is required to enable the full use of the SubLVDS Image Sensor Receiver IP Core in a complete, top-level design. You can fully evaluate the IP core through functional simulation and implementation (synthesis, map, place and route) without an IP license string. This IP Core supports Lattice IP hardware evaluation capability, which makes it possible to create versions of the IP core, which operate in hardware for a limited time (approximately four hours) without requiring an IP license string. See the IP Evaluation section for further details. However, a license string is required to enable timing simulation and to generate bitstream file that does not include the hardware evaluation timeout limitation.

3.2. Generation and Synthesis

The Lattice Radiant software allows you to generate and customize modules and IPs and integrate them into the device architecture. The procedure for generating SubLVDS Image Sensor Receiver IP Core in Lattice Radiant software is described below.

To generate the SubLVDS Image Sensor Receiver IP Core:

1. Create a new Lattice Radiant software project or open an existing project.
2. In the **IP Catalog** tab, double-click on **SubLVDS_Image_Sensor_Receiver** under **IP, Audio_Video_Image_Processing** category. The **Module/IP Block Wizard** opens, as shown in Figure 3.1. Enter values in the **Component name** and the **Create in** fields and click **Next**.

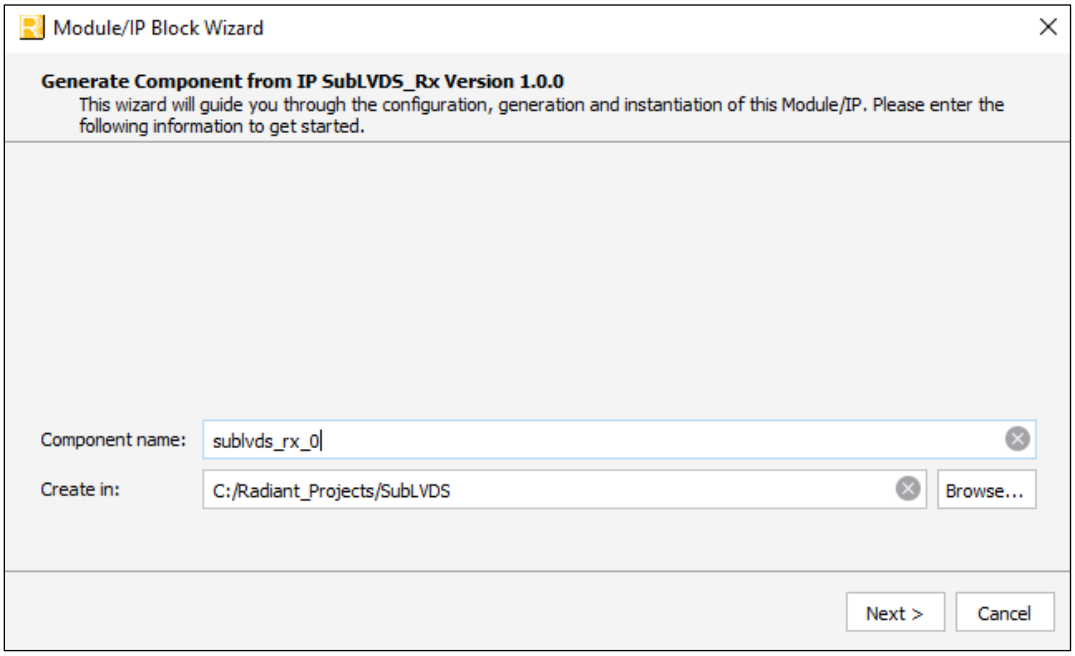

Figure 3.1. Module/IP Block Wizard

3. In the modules dialog box of the **Module/IP Block Wizard** window, customize the SubLVDS Image Sensor Receiver IP Core according to custom specifications, using drop-down menus and check boxes. As a sample configuration, see Figure 3.2. For configuration options, see the Attribute Summary section.

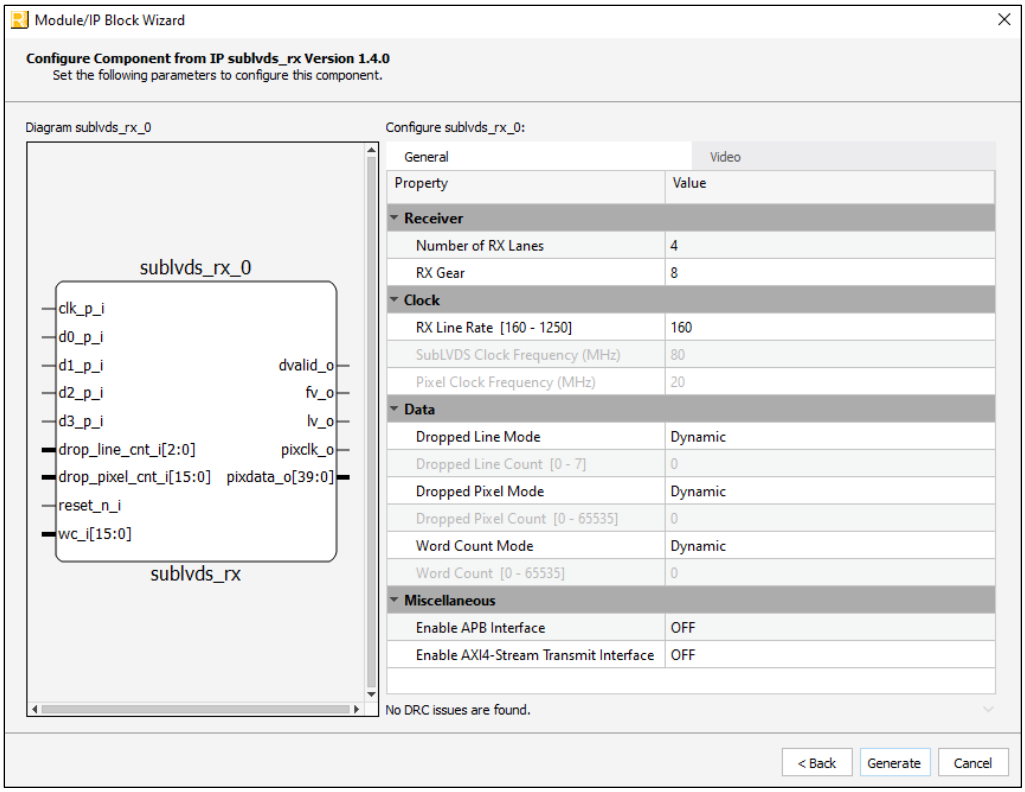

Figure 3.2. Configure Block of SubLVDS Image Sensor Receiver IP Core

4. Click **Generate**. The **Check Generated Result** dialog box opens, showing design block messages and results, as shown in Figure 3.3.

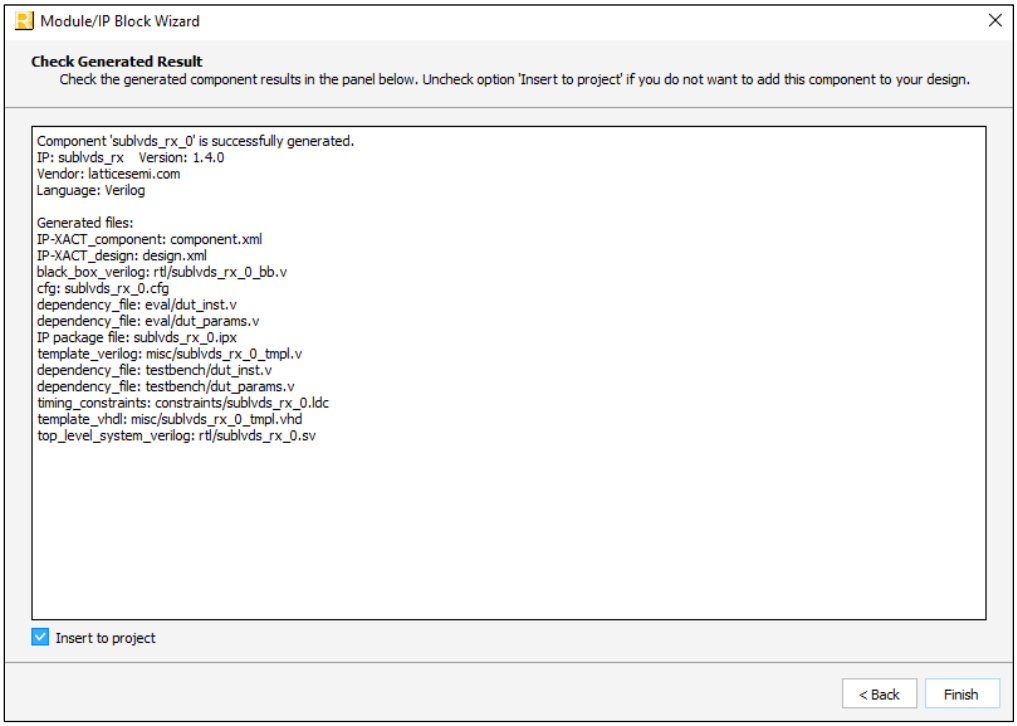

Figure 3.3. Check Generated Result

5. Click the **Finish** button. All the generated files are placed under the directory paths in the **Create in** and the **Component name** fields, as shown in Figure 3.1.

The generated SubLVDS Image Sensor Receiver IP Core package includes the black box (<Instance Name>_bb.v) and instance templates (<Instance Name>_tmpl.v/vhd) that can be used to instantiate the core in a top-level design. An example RTL top-level reference source file (<Instance Name>.v) that can be used as an instantiation template for the IP core is also provided. You may also use this top-level reference as the starting template for the top-level for their complete design. The generated files are listed in Table 3.1.

Table 3.1. Generated Files List

Attribute	Description
<Instance Name>.ipx	This file contains the information on the files associated to the generated IP.
<Instance Name>.cfg	This file contains the parameter values used in IP configuration.
component.xml	Contains the ipxact:component information of the IP.
design.xml	Documents the configuration parameters of the IP in IP-XACT 2014 format.
rtl/<Instance Name>.v	This file provides an example RTL top file that instantiates the IP core.
rtl/<Instance Name>_bb.v	This file provides the synthesis black box.
misc/<Instance Name>_tmpl.v misc /<Instance Name>_tmpl.vhd	These files provide instance templates for the IP core.

3.3. Running Functional Simulation

Running functional simulation can be performed after the IP is generated. The following steps can be performed.

1. Click the  button located on the **Toolbar** to initiate the **Simulation Wizard**, as shown in Figure 3.4.

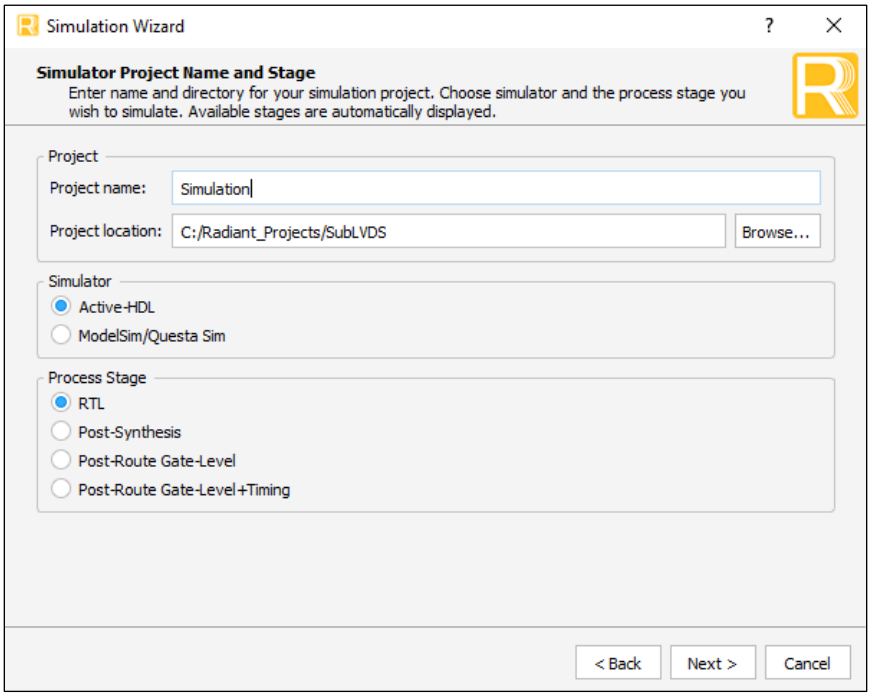

Figure 3.4. Simulation Wizard

2. Click **Next** to open the **Add and Reorder Source** window, as shown Figure 3.5.

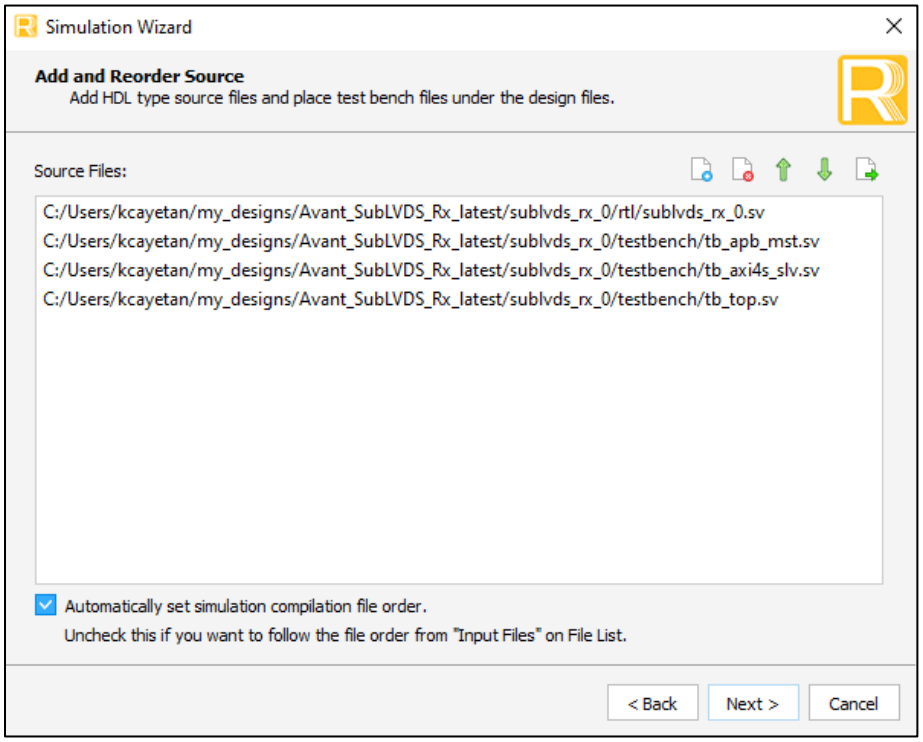

Figure 3.5. Adding and Reordering Source

Table 3.2. Testbench Files List

Testbench Files	Description
testbench/tb_top.sv	Top testbench to run loopback test of generated <Instance Name>.sv
testbench/tb_apb_mst.sv	Testbench to run test on APB Completer Interface.
testbench/tb_axi4s_slv.sv	Testbench to run test on AXI4-Stream Transmitter Interface.

3. Click **Next**. The Summary window is shown. Click **Finish** to run the simulation.

   Note: It is necessary to follow the procedure above until it is fully automated in the Lattice Radiant software suite. The results of the simulation in our example are provided in Figure 3.6.

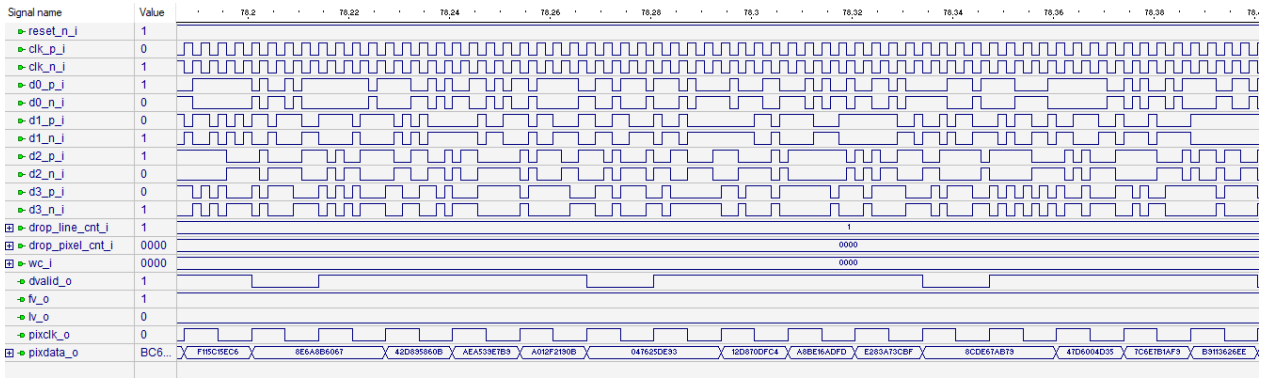

Figure 3.6. Simulation Waveform

3.4. Constraining the IP

You need to provide proper timing and physical design constraints to ensure that your design meets the desired performance goals on the FPGA. Add the content of the following IP constraint file to your design constraints: *<IP_Instance_Path>/<IP_Instance_Name>/eval/constraints.pdc.*

The constraint file has been verified during IP evaluation with the IP instantiated directly in the top-level module. You can modify the constraints in this file with thorough understanding of the effect of each constraint.

To use this constraint file, copy the content of *constraints.pdc* to the top-level design constraint for post-synthesis. Refer to Lattice Radiant Timing Constraints Methodology for details on how to constraint your design.

3.5. IP Evaluation

The SubLVDS Image Sensor Receiver IP Core supports Lattice IP evaluation capability when used with Lattice FPGA devices built on the Lattice Nexus™ platform. This makes it possible to create versions of the IP core that operate in hardware for a limited period of time (approximately four hours) without requiring the purchase of an IP license. It may also be used to evaluate the core in hardware in user-defined designs. The IP evaluation capability may be enabled/disabled in the Strategy dialog box. It is enabled by default. To change this setting, go to **Project** > **Active Strategy** > **Bitstream** > **IP Evaluation**.

4. Ordering Part Number

The Ordering Part Numbers (OPN) for this IP Core are the following:

Table 4.1 Ordering Part Numbers

Part Number	Device	License Type
LVDS-RX-CNX-US	CrossLink-NX	Single Machine Annual
LVDS-RX-CNX-UT	CrossLink-NX	Multi-site Perpetual
LVDS-RX-CTNX-US	Certus-NX	Single Machine Annual
LVDS-RX-CTNX-UT	Certus-NX	Multi-site Perpetual
LVDS-RX-CPNX-US	CertusPro-NX	Single Machine Annual
LVDS-RX-CPNX-UT	CertusPro-NX	Multi-site Perpetual
LVDS-RX-AVE-US	Avant-AT-E	Single Machine Annual
LVDS-RX-AVE-UT	Avant-AT-E	Multi-site Perpetual
LVDS-RX-AVG-US	Avant-AT-G	Single Machine Annual
LVDS-RX-AVG-UT	Avant-AT-G	Multi-site Perpetual
LVDS-RX-AVX-US	Avant-AT-X	Single Machine Annual
LVDS-RX-AVX-US	Avant-AT-X	Multi-site Perpetual
LVDS-RX-XO5-US	MachXO5-NX	Single Machine Annual
LVDS-RX-XO5-UT	MachXO5-NX	Multi-site Perpetual

Appendix A. Resource Utilization

Table A.1. Device and Tool Tested

	Value
Lattice Radiant Software Version	Radiant 2023.1
Device Used	LAV-AT-E70-3LFG1156C
Performance Grade	3
Synthesis Tool	Synplify Pro (R) Q-2020.03LR, Build 223R, March 1 2023

Note: Some bits are clipped to accommodate the current configuration with the selected device.

Table A.2. SubLVDS-RX Resource Utilization

Number of RX Gears	RX Gear	Line Rate	Synthesis Tool	Register	LUTs	F_{max}[1]
4	8	900 Mbps	Synplify Pro	293	640	clk_p_i = 450 MHz
						pixclk_o = 112.5 MHz
10	8	900 Mbps	Synplify Pro	633	1214	clk_p_i = 450 MHz
						pixclk_o = 112.5 MHz
16	8	900 Mbps	Synplify Pro	874	1681	clk_p_i = 450 MHz
						pixclk_o = 112.5 MHz
4	16	900 Mbps	Synplify Pro	756	1622	clk_p_i = 450 MHz
						pixclk_o = 56.25 MHz

Note:

1. The Fmax provided shows that the target frequency for a certain bitrate is attainable. While it is possible that the maximum frequency could be higher than what is shown, the IP is bounded to maintain the user's desired configuration.

References

- Lattice Radiant Software Web Page
- Lattice Avant-E FPGA Web Page
- Lattice Avant-G FPGA Web Page
- Lattice Avant-X FPGA Web Page
- MachXO5-NX FPGA Web Page
- CrossLink-NX FPGA Web Page
- CertusPro-NX FPGA Web Page
- Certus-NX FPGA Web Page
- Lattice Insights for Training Series and Learning Plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.8, December 2023

Section	Change Summary
All	• Updated title from SubLVDS Image Sensor Receiver IP Core – Lattice Radiant Software to *SubLVDS Image Sensor Receiver IP Core*. • Performed minor editorial fixes.
Disclaimers	Updated this section.
Inclusive Language	Added this section.
Introduction	Updated *LAV-AT-500E* to *LAV-AT-E70* and added devices *LAV-AT-G70* and *LAV-AT-X70* in Table 1.1. SubLVDS Image Sensor Receiver IP Core Quick Facts.
IP Generation and Evaluation	• Fixed broken link in the Licensing the IP section. • Updated the Constraining the IP section.
Ordering Part Number	Updated Table 4.1 with Avant-AT-E, Avant-AT-G, and Avant-AT-X part numbers.
Appendix A. Resource Utilization	• Updated device from *LAV-AT-500E-3LFG1156C* to *LAV-AT-E70-3LFG1156C* in Table A.2. SubLVDS-RX Resource Utilization. • Updated note below Table A.2. SubLVDS-RX Resource Utilization.
References	Added links to the Avant-G and Avant-X web pages.

Revision 1.7, September 2023

Section	Change Summary
All	• Changed all instances of *Master* to *Active*. • Changed all instances of *Slave* to *Passive*.

Introduction	• Table 1.1. SubLVDS Image Sensor Receiver IP Core Quick Facts:
	  • added *MachXO5-NX* to Supported FPGA Families;
	  • added *LFMXO5-25*, *LFMXO5-55T*, *LFMXO5-100T*, and *LIFCL-33* to Targeted Devices;
	  • added *APB Interface* and *AXI4-Stream Transmit Interface* to Supported User Interface;
	  • added *IP Core v1.4.x - Lattice Radiant Software 2023.1* to Lattice Implementation.
	• In the Features section:
	  • removed the *1 channel* feature;
	  • added *Supports APB Interface for register access and AXI4-Stream Transmit Interface*;
	  • removed *However, this IP Core does not support configuration through registers*.

Functional Description	• Updated Figure 2.1. SubLVDS Image Sensor Receiver IP Core Top Level Block Diagram;
	• Table 2.1. SubLVDS Image Sensor Receiver IP Core Signal Description:
	  • added *APB Completer Interface Ports* and *AXI4-Stream Transmitter Interface Ports*;
	  • added table notes 2 to 5.
	• Table 2.2. Attributes Table:
	  • added the attributes *Enable APB Interface* and *Enable AXI4-Stream Transmit Interface* under Miscellaneous;
	  • added the table note on inclusive language.
	• Added the attributes *Enable APB Interface* and *Enable AXI4-Stream Transmit Interface* under Miscellaneous in Table 2.3. Attributes Description.
	• Updated Figure 2.2. Clock Domain Crossing Block Diagram.
	• Changed the caption of Figure 2.3 to *SubLVDS Image Sensor Receiver IP Core Detailed Block Diagram (APB and AXI4-Stream Transmitter Interfaces not enabled)*.
	• Removed the previous Figure 2.4 *Deserializer of 1:8 Gearing Block Diagram,* Figure 2.5 *Deserializer of 1:16 Gearing Block Diagram*, and Figure 2.6 *SubLVDS Word Alignment Block Diagram*.
	• Added Figure 2.4. SubLVDS Image Sensor Receiver IP Core Detailed Block Diagram (APB Interface Enabled), Figure 2.5. SubLVDS Image Sensor Receiver IP Core Detailed Block

Section	Change Summary
	Diagram (AXI4-Stream Transmitter Interface Enabled), and Figure 2.6. SubLVDS Image Sensor Receiver IP Core Detailed Block Diagram (APB and AXI4-Stream Interfaces Enabled). • Added the Register Descriptions and AXI4-Stream Transmit Interface sections.

IP Generation and Evaluation	• Updated Figure 3.2. Configure Block of SubLVDS Image Sensor Receiver IP Core, Figure 3.3. Check Generated Result, and Figure 3.5. Adding and Reordering Source.
	• Added Table 3.2. Testbench Files List.
	• Added the Constraining the IP section.
	• IP Evaluation:
	  • changed the section name to *IP Evaluation*;
	  • updated the section content to reflect the section name change;
	  • updated the steps for changing the IP evaluation capability setting to *Project > Active Strategy > Bitstream > IP Evaluation*.

Ordering Part Number	Updated the OPNs for the SubLVDS Image Sensor Receiver IP Core.
References	Updated this section, added links to Lattice Radiant Software Web Page, Lattice Avant-E FPGA Web Page, MachXO5-NX FPGA Web Page, and Lattice Insights for Training Series and Learning Plans.
Appendix A. Resource Utilization	Updated Table A.2. SubLVDS-RX Resource Utilization.

Revision 1.6, March 2023

Section	Change Summary
Disclaimers	Updated this section.

Introduction	• In Table 1.1. SubLVDS Image Sensor Receiver IP Core Quick Facts:
	  • added LAV-AT-500E to the Targeted Devices;
	  • updated Lattice Implementation.
	• In Features, added *12*, *14* and *16* to the data lanes supported by the SubLVDS Image Sensor Receiver IP Core.

Functional Description	• Updated Figure 2.1. SubLVDS Image Sensor Receiver IP Core Top Level Block Diagram.
	• In Table 2.1. SubLVDS Image Sensor Receiver IP Core Signal Description:
	  • removed the complementary ports: d0_n_i, d1_n_i, d2_n_i, d3_n_i, d4_n_i, d5_n_i, d6_n_i, d7_n_i, d8_n_i, d9_n_i;
	  • added the following ports: d10_p_i, d11_p_i, d12_p_i, d13_p_i, d14_p_i, d15_p_i.
	• In Table 2.2. Attributes Table, added *12*, *14*, and *16* to the selectable values for the *Number of RX Lanes*.
	• Updated Figure 3.3. Check Generated Result.

IP Generation and Evaluation	• Updated • Figure 3.2. Configure Block of SubLVDS Image Sensor Receiver IP Core. • Updated Figure 3.3. Check Generated Result.
Ordering Part Number	Added the ordering part numbers for Lattice Avant.
Appendix A. Resource Utilization	• In Table A.1. Device and Tool Tested, updated the *Lattice Radiant Software Version*, *Device Used*, *Performance Grade* and *Synthesis Tool* for the LAV-AT-500E-3LFG1156C device. • In Table A.2. SubLVDS-RX Resource Utilization, updated the values for the *Number of RX Gears*, *RX Gear*, *Line Rate*, *Synthesis Tool*, *Register*, *LUTs*, and *Fmax*.

Revision 1.5, June 2021

Section	Change Summary

Introduction	• Updated Table 1.1. SubLVDS Image Sensor Receiver IP Core Quick Facts.
	  • Revised Supported FPGA Families
	  • Revised Targeted Devices
	  • Revised Lattice Implementation

Section	Change Summary
IP Generation and Evaluation	• In the Hardware Evaluation section, replaced specific device with *Lattice FPGA devices built on the Lattice Nexus platform*.
Ordering Part Number	Added part numbers.
References	Added reference to the CertusPro-NX web page.

Revision 1.4, December 2020

Section	Change Summary
Introduction	Updated Table 1.1. Modified Lattice Implementation details.
Functional Description	• Updated RX Line Rate selectable values in Table 2.2. Attributes Table. • Updated Line Rate information in Table 2.3. Attributes Description.
IP Generation and Evaluation	Updated Figure 3.2. Configure Block of SubLVDS Image Sensor Receiver IP Core.
References	Updated this section. Added references to product web pages.
All	Updated Lattice Radiant Software User Guide references.

Revision 1.3, June 2020

Section	Change Summary
All	Updated Lattice Radiant software user guide references to version 2.1 across the document.
Introduction	Added support for Certus-NX in Table 1.1.
Ordering Part Number	Updated this section.
Appendix A. Resource Utilization	Added this section.

Revision 1.2, April 2020

Section	Change Summary
Functional Description	Corrected maximum line rate in Table 2.2.

Revision 1.1, February 2020

Section	Change Summary
Introduction	• Updated Table 1.1 to add LIFCL-17 as targeted device. • Removed section 1.3.2. Data Ordering and Data Types
Functional Description	• Added pixclk_o port and note to Table 2.1. • Revised V_TOTAL values in Table 2.2. • Changed column heading to Description and updated descriptions of Dropped Pixel Count and Word Count attributes in Table 2.3. • Added Sample Configurations section.
IP Generation and Evaluation	Corrected interface item to *Check Generated Result*.
Appendix A.	Added table reference in introductory paragraph.

Revision 1.0, December 2019

Section	Change Summary
All	Initial release

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