EFB Module - Lattice Propel Builder

User Guide

FPGA-IPUG-02111-1.0

May 2020

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
CPU	Central Processing Unit
EAR	Extended Address Register
QSPI	Quad Serial Peripheral Interface
PLD	Programmable Logic Device
SPI	Serial Peripheral Interface

1. Introduction

The Lattice EFB Module for the MachXO3D™ FPGA device is a hard architectural block that is known as the Embedded Function Block (EFB). The EFB includes an I^2C, access to Configuration Blocks (CFG1), and User Flash Memory (UFM). All of these hard IP peripherals are addressable through the Advanced the Peripheral Bus (APB) interface of the Advanced Microcontroller Bus Architecture (AMBA) 3 protocol.

The design is implemented in Verilog HDL. It can be configured and generated using the Lattice Propel™ Builder software. It can be targeted to MachXO3D FPGA devices and implemented using the Lattice Diamond® software Place and Route tool integrated with the Synplify Pro® synthesis tool.

1.1. Features

The key features of the QSPI Monitor IP include:

- AMBA 3 APB Protocol v1.0 interface
- One I^2C block (I2C2)
- Support for the initialization of Configuration Block 1 (CFG1)
- Support for the initialization of User Flash Memory 2 (UFM2)

For more information on the EFB hardware, refer to Using Hardened Control Functions in MachXO3D Devices (FPGA-TN-02117).

1.2. Conventions

1.2.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.2.2. Signal Names

Signal names that end with:

- *_n* are active low (asserted when value is logic 0)
- *_i* are input signals
- *_o* are output signals
- *_io* are bi-directional input/output signals

1.2.3. Attribute Names

Attribute names in this document are formatted in title case and italicized (*Attribute Name*).

2. Functional Description

2.1. Overview

The EFB block described in this document focuses on three available functions: I^2C, CFG1, and UFM2. The I^2C block is accessed through the APB bus and its pins are routed directly outside the device for inter-chip communication. The CFG1 and UFM2 memory blocks can also be accessed through the APB and can be initialized based on your intended function. The equivalent I^2C discussed here refers to I2C2 (I^2C Secondary) in Using Hardened Control Functions in MachXO3 Devices Reference Guide (TN1294) and its equivalent programming registers.

2.2. Block Diagram

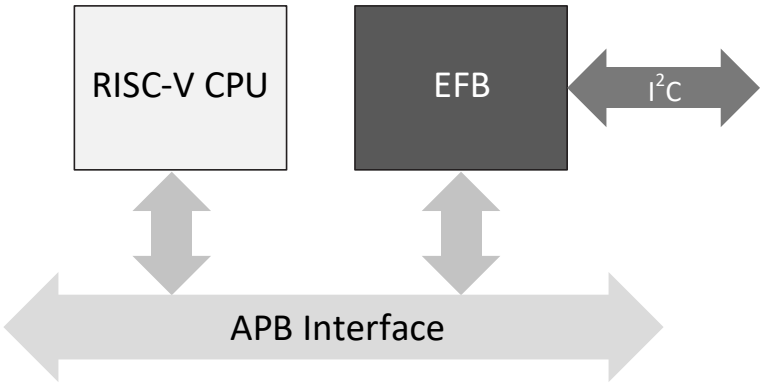

Figure 2.1. EFB Module Block Diagram

2.3. Signal Description

Table 2.1. QSPI Monitor Signal Description

Port	Direction	Width	Description
System			
clk_i	Input	1	Master clock input
reset_i	Input	1	Asynchronous reset active high
int_o	Output	1	Interrupt request
APB			
apb_psel_i	In	1	Select signal Indicates that the slave device is selected and a data transfer is required.
apb_paddr_i	In	32	Address signal
apb_pwdata_i	In	32	Write data signal
apb_pwrite_i	In	1	Direction signal Write = 1, Read = 0
apb_penable_i	In	1	Enable signal Indicates the second and subsequent cycles of an APB transfer.
apb_pready_o	Out	1	Ready signal Indicates transfer completion. Slave uses this signal to extend an APB transfer.
apb_prdata_o	Out	32	Read data signal
apb_pslverr_o	Out	1	Tied 0

Port	Direction	Width	Description
External I²C Protocol			
i2c2_scl	In/Out	1	Clock of I²C interface
i2c2_sda	In/Out	1	Data of I²C interface

2.4. Attribute Summary

The QSPI Monitor IP's configurable attributes are as shown in Table 2.2 and are described in Table 2.3.

Table 2.2. Attributes Table

Attribute	Selectable Values	Default	Dependency on Other Attributes
General			
Data-Width	8-32	32	—
Addr-Width	10-32	32	—
Enable Initialization (CFG1)	True, False	False	—
Initialization File (CFG1)	<file_path>	"none"	Enable Initialization (CFG1) = True
Enable Initialization (UFM2)	True, False	False	—
Initialization File (UFM2)	<file_path>	"none"	Enable Initialization (UFM2) = True

2.5. Register Description

The EFB Module follows the register mapping for the MachXO3 device EFB. For further information, refer to Using Hardened Control Functions in MachXO3 Devices Reference Guide (TN1294). I²C, CFG1, and UFM2,. There are certain offsets, however, that you should be mindful of in performing transactions on the APB bus, particularly on the address. There is a 2-bit shift to the left for the equivalent address in the APB interface compared with the ones in the document. Some examples:

Table 2.3. Register Description

Register Name	TN1294	APB Equivalent
I2C_2_CR	0x4A	0x128
I2C_2_CMDR	0x4B	0x12C
I2C_2_BR0	0x4C	0x130

In terms of data, the upper MSBs in configurations with data-widths larger than 8 are tied to 0 when writing. In the same way, writing only the lower 8-bits is significant. This is implemented to reduce the total number of logic required and improve the overall speed of the IP, in exchange for a small amount in the memory map.

References

- MachXO3D FPGA Web Page in latticesemi.com
- Lattice Propel 1.0 User Guide
- Lattice Diamond Software 3.11 User Guide
- Using Hardened Control Functions in MachXO3D Devices (FPGA-TN-02117)
- Using Hardened Control Functions in MachXO3 Devices Reference Guide (TN1294)

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.0, May 2020

Section	Change Summary
All	Initial release.

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