PLL Module - Lattice Radiant Software

User Guide

FPGA-IPUG-02063-1.3

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
FPGA	Field Programmable Gate Array
IP	Intellectual Property
LMMI	Lattice Memory Mapped Interface
APB	Advanced Peripheral Bus

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1. Introduction

The Phase Locked Loop (PLL) Module is capable of frequency synthesis and clock phase management including clock injection delay cancellation. It has the flexibility of input and feedback source selections, multiple output selections, VCO phase rotation, and independent phase shifting features. The multiple output clocks can be synchronized with the option to enable or be individually controlled dynamically by users.

1.1. Quick Facts

Table 1.1 presents a summary of the PLL Module.

Table 1.1. Quick Facts

IP Requirements	Supported FPGA Families	CrossLink™-NX, Certus™-NX
Resource Utilization	Targeted Devices	LIFCL-40, LIFCL-17, LFD2NX-40, LFD2NX-17
	Supported User Interfaces	LMMI (Lattice Memory Mapped Interface), APB
Design Tool Support	Lattice Implementation	Lattice Radiant® Software
	Synthesis	Lattice Synthesis Engine (LSE)
		Synopsys® Synplify Pro® for Lattice
	Simulation	For the list of supported simulators, see the Lattice Radiant Software User Guide.

1.2. Features

The key features of the PLL Module include:

- Multiple feedback inputs
- Multiple output clocks
- Output synchronization
- Lock detector – Phase and Frequency
- M (1 to 128), N (1 to 128) input and feedback dividers
- Fractional-N divider
- VCO phase shift – 8 VCO phases
- Divider phase shift
- Dynamic VCO and divider phase shift
- Output dividers (1 to 128)
- Output edge trim for clkop_o and clkos_o only
- Input bypass
- Power down mode
- Test mode
- Programmable bandwidth

1.3. Conventions

1.3.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.3.2. Signal Names

Signal names that end with:

- *_n* are active low
- *_i* are input signals
- *_o* are output signals

1.3.3. Attribute Names

Attribute names in this document are formatted in title case and italicized (*Attribute Name*).

2. Functional Description

2.1. Overview

The PLL Module is capable of clock synthesis and clock phase management including clock tree delay cancellation.

The PLL Module performs frequency synthesis, multiplication, division, and clock injection delay removal. For clock synthesis application where removal of clock injection delay is not a requirement, the GPLL block has an internal feedback path that is used to complete the feedback loop. Applications that require the removal of the clock injection delay take the feedback clock form the output of the relevant clock tree.

A top-level block diagram of the Global Phase Locked Loop Module is shown in Figure 2.1.

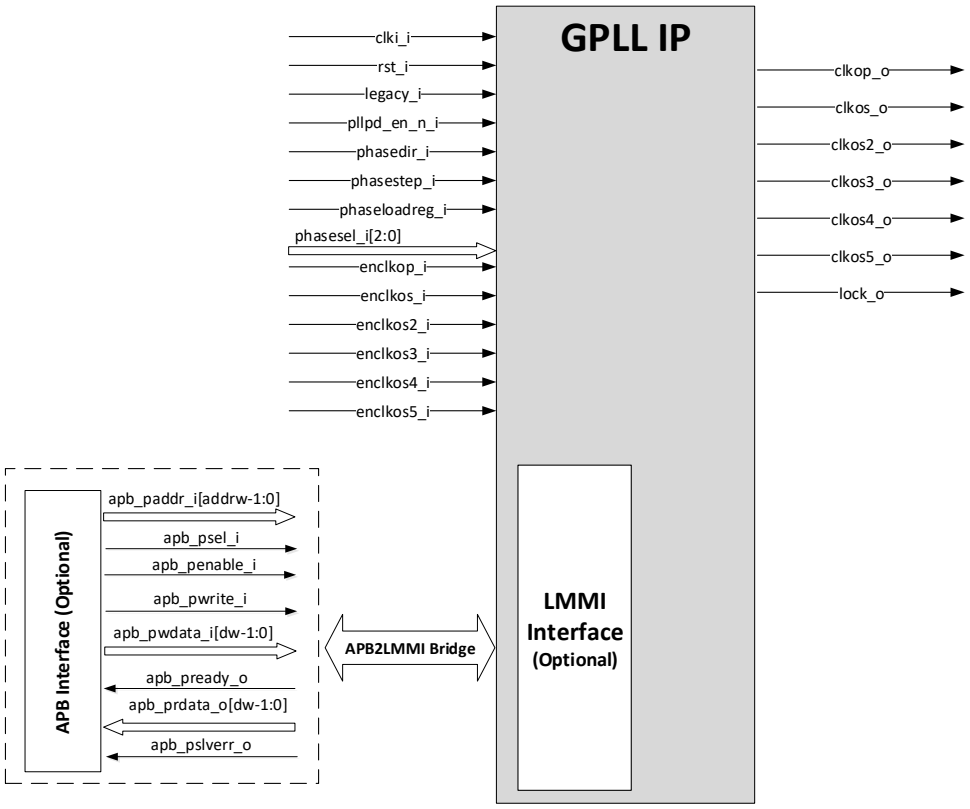

Figure 2.1. GPLL Top Level Block Diagram

This PLL Module has the flexibility of multiple feedback clock source selections. It has main logic features as 6 independent output clocks, output phase shifting through VCO phases, synchronous outputs, and divider phase shifts. The effective feedback divider value cannot exceed 80.

2.2. Signal Description

Table 2.1. PLL Module Signal Description

Port Name	I/O	Width	Description
Clock and Reset			
clki_i	In	1	System clock.
rst_i	In	1	PLL reset signal enabled by user from the user interface via *PLL Reset Options: Provide PLL Reset*
clkop_o	Out	1	Primary output clock, always enabled
clkos_o	Out	1	Secondary output clock, enabled by user from the user interface via *CLKOS: Enable*
clkos2_o	Out	1	Secondary output clock, enabled by user from the user interface via *CLKOS2: Enable*
clkos3_o	Out	1	Secondary output clock, enabled by user from the user interface via *CLKOS3: Enable*
clkos4_o	Out	1	Secondary output clock, enabled by user from the user interface via *CLKOS4: Enable*
clkos5_o	Out	1	Secondary output clock, enabled by user from the user interface via *CLKOS5: Enable*
usr_fbclk_i	In	1	User Feedback Clock input. Available if selected by user from the user interface via *Enable User Feedback Clock*.
User Interface			
legacy_i	In	1	PLL Legacy mode signal enabled by user from the user interface via *Power Mode Settings: Enable Legacy Mode*
pllpd_en_n_i	In	1	Power Down mode signal enabled by user from the user interface via *Power Mode Settings: Enable Power Down Mode*
phasedir_i	In	1	Dynamic Phase direction signal enabled by user from the user interface via *Optional Port Selections: Dynamic Phase Ports*
phasestep_i	In	1	Dynamic Phase step signal enabled by user from the user interface via *Optional Port Selections: Dynamic Phase Ports*
phaseloadreg_i	In	1	Dynamic Phase load signal enabled by user from the user interface via *Optional Port Selections: Dynamic Phase Ports" attribute*
phasesel_i	In	3	Dynamic Phase select signal enabled by user from the user interface via *Optional Port Selections: Dynamic Phase Ports* 3'b000: CLKOS 3'b001: CLKOS2 3'b010: CLKOS3 3'b011: CLKOS4 3'b100: CLKOS5 3'b101: CLKOP
enclkop_i	In	1	CLKOP Enable signal, enabled by user from the user interface via *Optional Port Selections: Clock Enable Ports* to populate displayed ports for CLKOP
enclkos_i	In	1	CLKOS Enable signal, enabled by user from the user interface via *Optional Port Selections: Clock Enable Ports* to populate displayed ports for CLKOS
enclkos2_i	In	1	CLKOS2 Enable signal, enabled by user from the user interface via *Optional Port Selections: Clock Enable Ports* to populate displayed ports for CLKOS2
enclkos3_i	In	1	CLKOS3 Enable signal, enabled by user from the user interface via *Optional Port Selections: Clock Enable Ports* to populate displayed ports for CLKOS3
enclkos4_i	In	1	CLKOS4 Enable signal, enabled by user from the user interface via *Optional Port Selections: Clock Enable Ports* to populate displayed ports for CLKOS4
enclkos5_i	In	1	CLKOS5 Enable signal, enabled by user from the user interface via *Optional Port Selections: Clock Enable Ports* to populate displayed ports for CLKOS5

Port Name	I/O	Width	Description
lock_o	Out	1	PLL lock signal enabled by user from the user interface via *Lock Settings: Provide PLL Lock Signal*
LMMI Interface[1]			
lmmi_clk_i	In	1	LMMI Clock
lmmi_resetn_i	In	1	Reset (active low) Resets the LMM interface and sets registers to their default values. Does not reset the internals of the Hard IP block.
lmmi_request_i	In	1	Start transaction
lmmi_wr_rdn_i	In	1	Write = HIGH, Read = LOW
lmmi_offset_i	In	7	Offset (0-31 bits) – register offset within the slave, starting at offset 0. Bit width is hard IP dependent.
lmmi_wdata_i	In	8	Write data (0-16 bits) Bit width is hard IP dependent.
lmmi_rdata_o	Out	8	Read data (0-16 bits) Bit width is hard IP dependent.
lmmi_rdata_valid_o	Out	1	Read transaction is complete and lmmi_rdata_o[] contains valid data.
lmmi_ready_o	Out	1	Slave is ready to start a new transaction. Slave can insert wait states by holding this signal low. This signal is optional in hardware and mandatory in RTL soft wrappers. Hardware slaves may omit this signal if they do not need wait states. For zero-wait-state slaves, the soft wrapper ties this signal high.
APB Interface[1]			
apb_pclk_i	In	1	APB clock
apb_preset_n_i	In	1	APB reset (active low)
apb_paddr_i	In	7	APB Address signal
apb_psel_i	In	1	APB Select signal
apb_penable_i	In	1	APB Enable signal
apb_pwrite_i	In	1	APB Direction signal
apb_pwdata_i	In	8	APB Write Data signal
apb_pready_o	Out	1	APB Ready signal
apb_prdata_o	Out	8	APB Read Data signal
apb_pslverr_o	Out	1	APB Slave Error signal

Notes:

1. Only one of the three interfaces is available as selected by Interface attribute.
2. The bit width of some signals is set by the attribute. Refer to Table 2.2 for the description of these attributes.

2.3. Attribute Summary

The configurable attributes of the PLL Module are shown in Table 2.2. The attributes can be configured through the IP Catalog's Module/IP wizard of the Lattice Radiant Software.

Table 2.2. Attributes Table

Attribute	Selectable Values	Default	Description
General			
Configuration Mode	Frequency, Divider	Frequency	Select the configuration mode. Frequency – set the desired input and output frequency. Divider – set the desired input frequency and desired divider settings.
Enable Fractional-N Divider	Checked, Unchecked	Unchecked	Enable/Disable the Fractional Feedback Clock Divider.
Enable User Feedback Clock	Checked, Unchecked	Unchecked	When enabled, feedback clock will be from user input.
VCO Frequency	Calculated	N/A	Display only.
Select Monitor Clock Frequency	3.2 MHz, 1.0 MHz	3.2 MHz	Select the frequency for reference clock monitoring logic.
Enable PMU Wait for Lock	Checked, Unchecked	Checked	When enabled, synchronize with PMU to wait for PLL lock.
Enable Internal Path Switching	Checked, Unchecked	Unchecked	Enable/Disable the internal path switching during POR/Sleep/Standby modes.
Reference Clock			
CLKI: Frequency (MHz)	10 – 800	100	Set the Reference Clock frequency. (applicable for Frequency mode only)
CLKI: Divider Desired Value	1 to 128	1	Set the Reference Clock divider. (applicable for Divider mode only)
Phase Detector Frequency (MHz)	Calculated	N/A	Display only.
CLKI: Divider Actual Value	Calculated	N/A	Display only.
Feedback			
CLKFB: Feedback Mode	CLKOP, CLKOS, CLKOS2, CLKOS3, CLKOS4, CLKOS5, INTCLKOP, INTCLKOS, INT_CLKOS2, INTCLKOS3, INTCLKOS4, INTCLKOS5	CLKOP	Select the feedback clock from the enabled PLL clock outputs (internal or external).
CLKFB: FBK Divider Desired Value	1 to 128	1	Set the Feedback Clock divider. (applicable for Divider mode only)
CLKFB: FBK Divider Actual Value	Calculated	N/A	Display only.
CLKFB: FBK Divider Desired Value (Fractional)	0 to 4095	0	Set the Feedback Clock fractional divider. (applicable if Fractional-N Divider is enabled)
CLKFB: FBK Divider Actual Value (Fractional)	Calculated	N/A	Display only.
CLKFB: FBK Divider Actual Value (Float)	Calculated	N/A	Display only (Integer+Fractional).

Attribute	Selectable Values	Default	Description
Clock Output			
CLKO*: Enable	Checked, Unchecked	Unchecked	Enable/Disable PLL Clock Output
CLKO*: Bypass	Checked, Unchecked	Unchecked	Bypass the actual divider output and output the reference clock instead.
CLKO*: Frequency Desired Value (MHz)	6.25 – 800 MHz	100	Set the Output Clock frequency. (applicable for Frequency mode only)
CLKO*: Tolerance (%)	0, 0.1, 0.2, 0.5, 1, 2, 5, 10	0.0	Set the acceptable tolerance for actual vs desired output frequency.
CLKO*: Divider Desired Value	1 to 128	8	Set the Output Clock frequency. (applicable for Divider mode only)
CLKO*: Divider Actual Value	Calculated	N/A	Display Only.
CLKO*: Frequency Actual Value (MHz)	Calculated	N/A	Display Only.
CLKO*: Static Phase Shift (Degrees)	0, 45, 90, 135, 180, 225, 270, 315	0	Set the desired clock output phase.
CLKO*: ERROR (PPM)	Calculated	0	Display Only. Difference between desired and actual frequencies.
CLKO*: Enable Trim for CLKO*	Checked, Unchecked	Unchecked	Enable/Disable Trim for clock output.
CLKO*: Duty Trim Options Mode	Rising, Falling	Falling	Select Trim mode.
CLKO*: Duty Trim Options Delay Multiplier	0, 1, 2, 4	0	Select Trim Delay Multiplier.
Optional Ports			
Reference Clock I/O Pin			
Set I/O Pin for PLL Reference Clock	Checked, Unchecked	Unchecked	Enable/Disable I/O Pin option for reference clock.
I/O Standard for Reference Clock	Legal Configuration Table for LIFCL	LVDS	Select type of I/O pin.
Dynamic Phase Control Ports			
Enable Dynamic Phase Ports	Checked, Unchecked	Unchecked	Enable/Disable dynamic phase control ports.
Clock Enable Ports			
CLKOP/CLKOS[n] Enable Port	Checked, Unchecked	Unchecked	Set to provide clock enable port.
PLL Reset			
Provide PLL Reset	Checked, Unchecked	Unchecked	Set to provide PLL reset port.
PLL Lock			
Provide PLL Lock Signal	Checked, Unchecked	Unchecked	Set to provide PLL lock port.
PLL Lock is Sticky	Checked, Unchecked	Unchecked	Set the behavior of PLL lock signal.
Register Interface			
Select Register Interface	None, APB, LMMI	None	Select type of register interface.
Power Mode Settings			
Enable Legacy Mode	Checked, Unchecked	Unchecked	Set to provide legacy port.
Enable Power Down Mode	Checked, Unchecked	Unchecked	Set to provide power down port.

3. IP Generation and Evaluation

This section provides information on how to generate the PLL Module using the Lattice Radiant Software and how to run simulation and synthesis. For more details on the Lattice Radiant Software, refer to the the Lattice Radiant Software User Guide.

3.1. Licensing the IP

No license is required for this IP module.

3.2. Generating and Synthesizing the IP

Lattice Radiant Software allows you to generate and customize modules and IPs and integrate them into the device architecture.

To generate PLL Module:

1. Create a new Lattice Radiant Software project or open an existing project.
2. In the **IP Catalog** tab, double-click on **PLL** under **Module, Architecture_Modules** category. The **Module/IP Block Wizard** opens as shown in Figure 3.1. Enter values in the **Instance name** and the **Create in** fields and click **Next**.

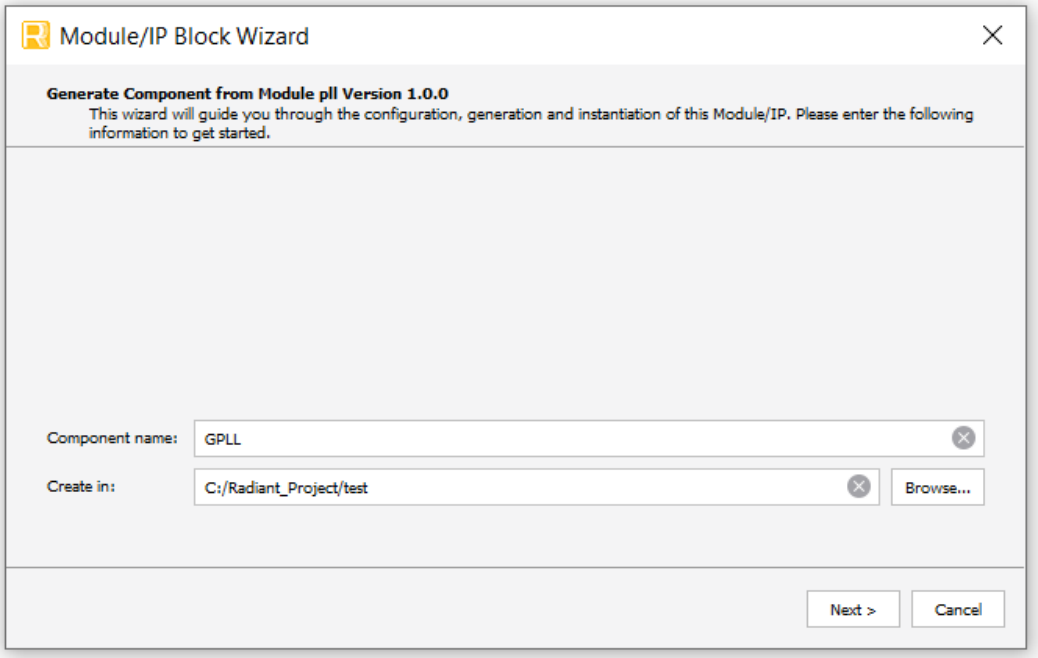

Figure 3.1. Configure Module/IP Block Wizard

3. In the module's dialog box of the **Module/IP Block Wizard** window, customize the selected PLL Module using drop-down menus and check boxes. As a sample configuration, see Figure 3.2. For configuration options, see the Attributes section.

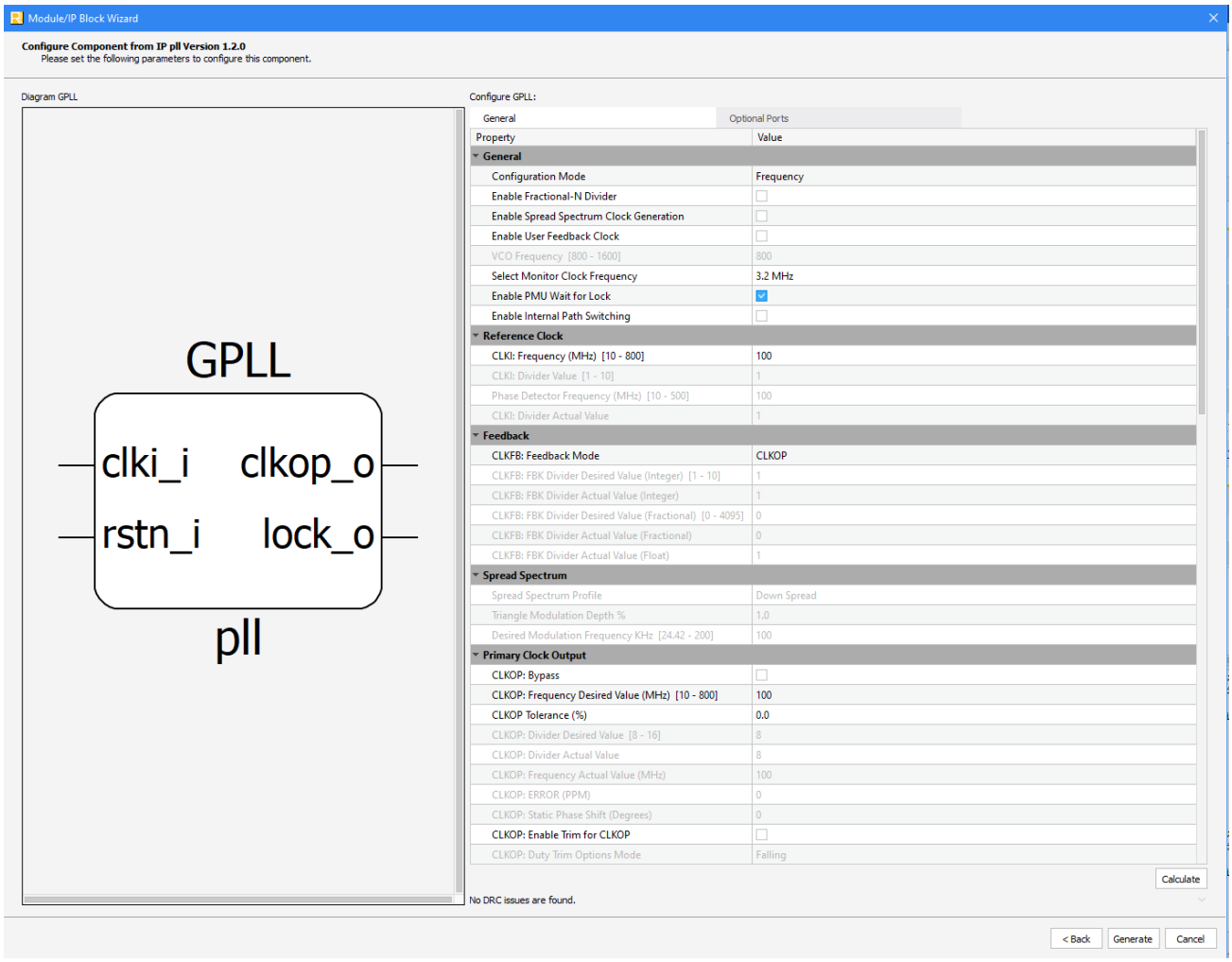

Figure 3.2. Configure User Interface of PLL Module

4. Click **Generate**. The **Check Generating Result** dialog box opens, showing design block messages and results as shown in Figure 3.3.

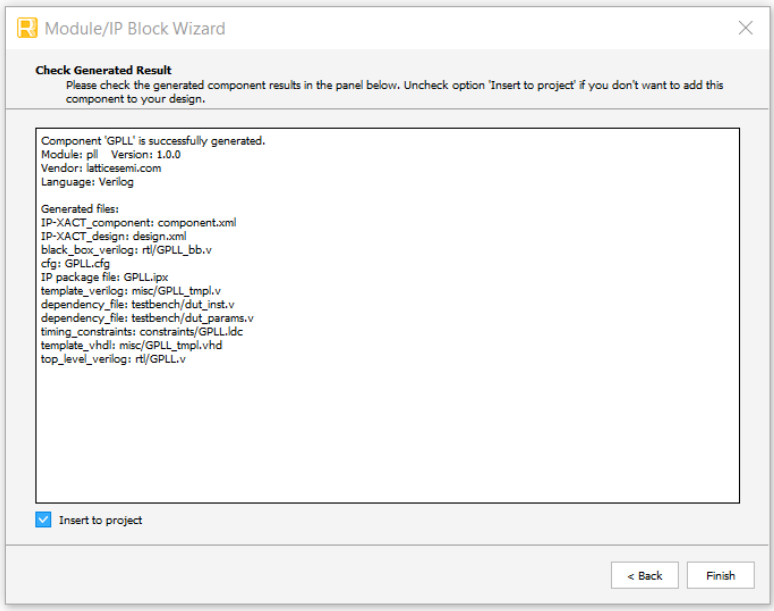

Figure 3.3. Check Generating Result

5. Click **Finish**. All the generated files are placed under the directory paths in the **Create in** and the **Instance name** fields shown in Figure 3.1.

The generated PLL Module package includes the black box (<Instance Name>_bb.v) and instance templates (<Instance Name>_tmpl.v/vhd) that can be used to instantiate the module in a top-level design. An example RTL top-level reference source file (<Instance Name>.v) that can be used as an instantiation template for the module is also provided. You may also use this top-level reference as the starting template for the top-level for their complete design. The generated files are listed in Table 3.1.

Table 3.1. Generated File List

Attribute	Description
<Instance Name>.ipx	This file contains the information on the files associated to the generated IP.
<Instance Name>.cfg	This file contains the attribute values used in IP configuration.
component.xml	Contains the ipxact:component information of the IP.
design.xml	Documents the configuration attributes of the IP in IP-XACT 2014 format.
rtl/<Instance Name>.v	This file provides an example RTL top file that instantiates the module.
rtl/<Instance Name>_bb.v	This file provides the synthesis black box.
misc/<Instance Name>_tmpl.v misc /<Instance Name>_tmpl.vhd	These files provide instance templates for the module.

3.3. Running the Functional Simulation

Running functional simulation can be performed after the IP is generated and the testbench is added. For this module, a customer testbench is provided.

To add the generated testbench:

1. Go to **File List** tab, right click **Input Files**.
2. Click Add > Existing File.
3. A window appears. Open the instance folder **testbench**, then double-click **tb_top.v**.
4. Right-click the **tb_top.v** under **Input files** folder.
5. Choose **Include for** > **Simulation**.

To run the simulation:

1. Click  button located on the **Toolbar** to initiate **Simulation Wizard**, as shown in Figure 3.4.

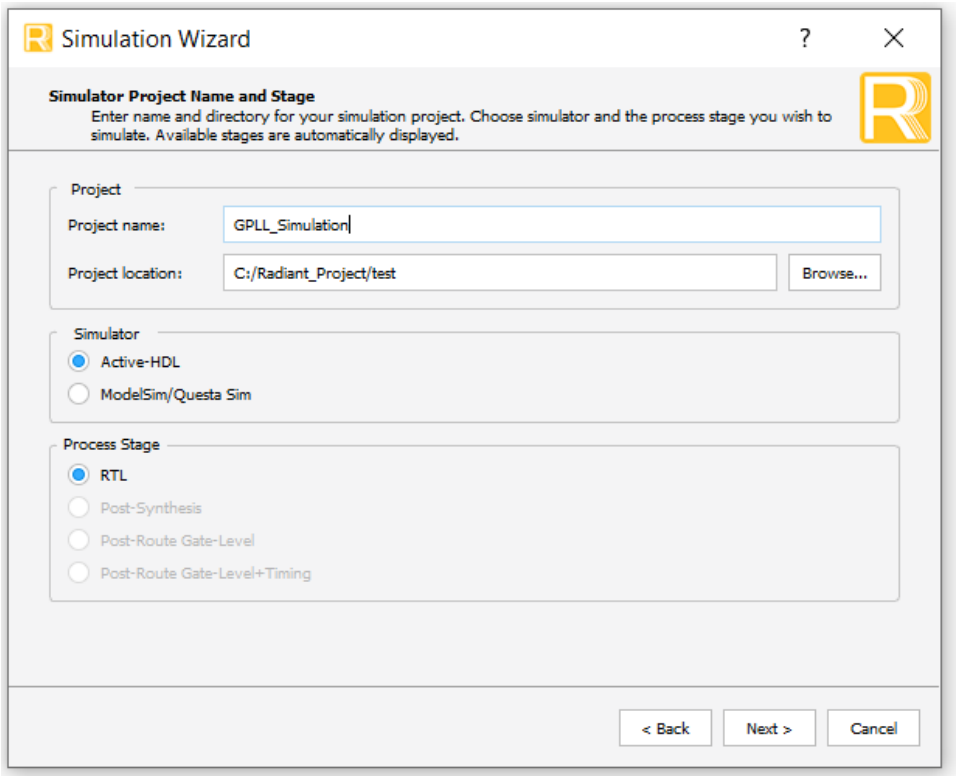

Figure 3.4. Simulation Wizard

2. Click **Next** to open the **Add and Reorder Source** window as shown in Figure 3.5.

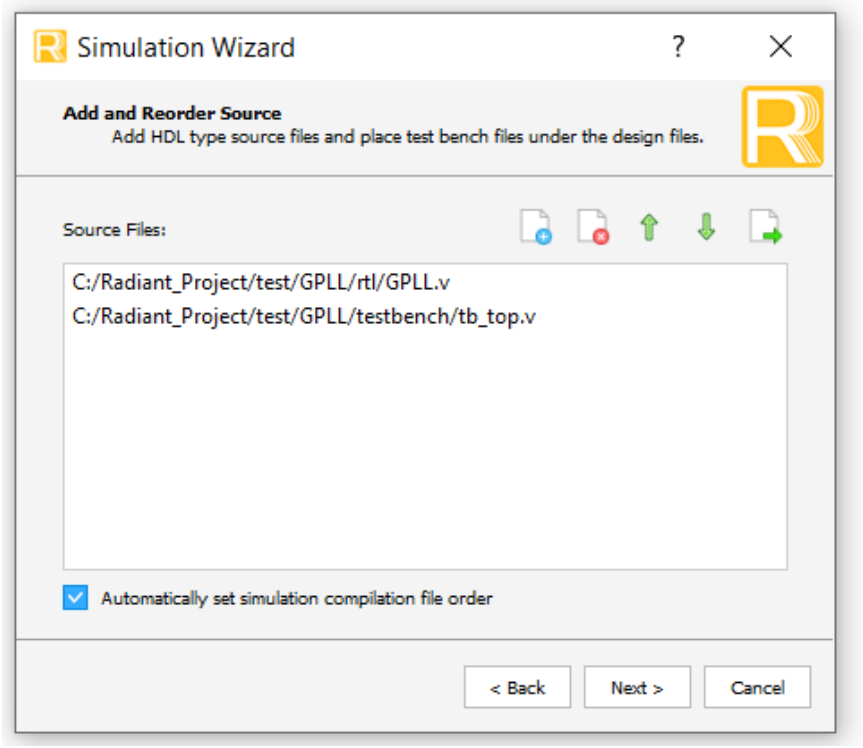

Figure 3.5. Adding and Reordering Source

Note: It is necessary to follow the procedure above until it is fully automated in the Lattice Radiant Software Suite. The results of the simulation in our example is shown in Figure 3.6.

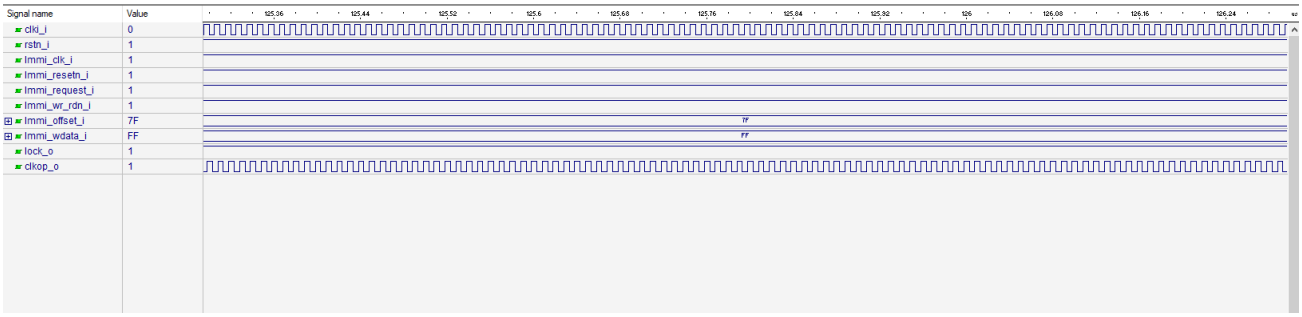

Figure 3.6. Simulation Waveform

3.4. Hardware Evaluation

There is no restriction on the hardware evaluation of this module.

References

For complete information on Lattice Radiant Project-Based Environment, Design Flow, Implementation Flow and Tasks, as well as on the Simulation Flow, see the Lattice Radiant Software User Guide.

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Document Revision 1.3, Lattice Radiant SW version 2.1, March 2021

Section	Change Summary
Acronyms in This Document	Removed SSC.
Introduction	• Updated Table 1.1. Quick Facts. Added LFD2NX-17 as supported device. Removed Lattice Radiant version. • Removed Spread Spectrum Clock Generation from Features section.
Functional Description	Removed Enable Spread Spectrum Clock Generation item and Spread Spectrum group from Table 2.2. Attributes Table.
All	Updated references to Lattice Radiant Software User Guide.

Document Revision 1.2, Lattice Radiant SW version 2.1, June 2020

Section	Change Summary
Introduction	• Updated Table 1.1 to add Certus-NX and LFD2NX-40 as targeted device. • Updated Lattice Implementation to Lattice Radiant 2.1. • Added items to Features section.
Functional Description	• Added ports to Table 2.1. PLL Module Signal Description. • General update to Table 2.2. Attributes Table.
All	• Updated references to Lattice Radiant Software User Guide. • Removed reference to Lattice Radiant Software 2.0 tutorials.

Document Revision 1.1, Lattice Radiant SW version 2.0, February 2020

Section	Change Summary
Introduction	Updated Table 1.1 to add LIFCL-17 as targeted device and minimal device needed.
Appendix	Removed this section.

Document Revision 1.0, Lattice Radiant SW version 2.0, December 2019

Section	Change Summary
All	• Updated document status from Preliminary to final. • Removed features not implemented in this release.
Appendix	Added this section.

Document Revision 0.80, Lattice Radiant SW version 2.0, October 2019

Section	Change Summary
All	Preliminary release

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