Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
DDR3	Double Data Rate 3
SDRAM	Synchronous Dynamic Random-Access Memory

1. Introduction

This guide describes how to run a DDR3 demo using the Certus™-NX Versa Evaluation Board.

The Certus-NX Versa Evaluation Board features the Certus-NX FPGA in the 256-ball caBGA package, which is built on the Lattice Nexus™ FPGA platform using low power 28 nm FDSOI technology. The board can expand the usability of the Certus-NX FPGA with DDR3, soft D-PHY, 1 Gbps Ethernet and 1× PCIe (Gen2) channel. Board resources such as jumpers, LED indicators, push buttons, and switches are available for user-defined applications.

This demo design demonstrates the functionality of the Lattice DDR3 SDRAM Controller IP operating at a core speed of 400 MHz and 800 Mbps. The Certus-NX Versa Evaluation Board has an onboard 16-bit DDR3 SDRAM and the demo performs the following:

- Generates 16-bit test data
- Writes to the onboard DDR3 SDRAM
- Reads the DDR3 SDRAM and compares the data with the original expected data
- Allows you to control certain parameters through DIP switches to modify demo test patterns
- Allows you to initiate resets to the DDR3 SDRAM Controller and user logic
- Allows you to observe critical signals through Reveal Analyzer

1.1. Learning Objectives

After completing the steps in this guide, you will be able to perform the following:

- Set up the Certus-NX Versa Evaluation Board and become familiar with its main features
- Install all applicable development tools and DDR3 demos
- Run the DDR3 Demo, which allows you to manipulate test patterns and observe the results through onboard LEDs
- Learn about Lattice DDR3 solutions through the DDR3 demo
- Modify and rebuild the DDR3 Demo
- Become familiar with the software development tools and major design flow steps employed in this kit
- Use other existing documentation in conjunction with this guide

This document assumes that you have already installed the Lattice Radiant™ design software. This document covers some of the basic of function of Lattice Radiant. If you would like to learn more about Lattice Radiant, refer to the Lattice Radiant Help system.

2. Hardware and Software Requirements

2.1. Hardware Requirements

To run the demo, a single computer running Windows 10 Operating System with an available USB-A port is required.

- Certus-NX Versa Evaluation Board
- USB Cable
- 12 V Power Adapter

2.2. Software Requirements

The following are the software required to obtain the expected results for the procedures described in this guide:

- Lattice Radiant version 3.1 or later
- Lattice Radiant Programmer version 3.1 or later
- DDR3 Certus-NX Versa Evaluation Board Demo
- Minimum system requirements as described in the Lattice Radiant Installation Guide

Note: All the files and dependencies for the DDR3 Certus-NX Versa Evaluation Board Demo are available in the .zip folder.

3. DDR3 Demo Design Overview

The DDR3 Demo Design consists of two major parts: the DDR3 SDRAM Controller IP core and the User Logic block. The DDR3 SDRAM Controller IP core interfaces directly with the onboard external DDR3 SDRAM to perform control, write, and read operations. The User Logic block generates test data to be written to the SDRAM and compares the data read from the external DDR3 SDRAM to the expected result, flagging an error if a data mismatch is detected. The demo parameters can be modified using onboard DIP switches, whereas the status of the demo is indicated through the onboard LEDs.

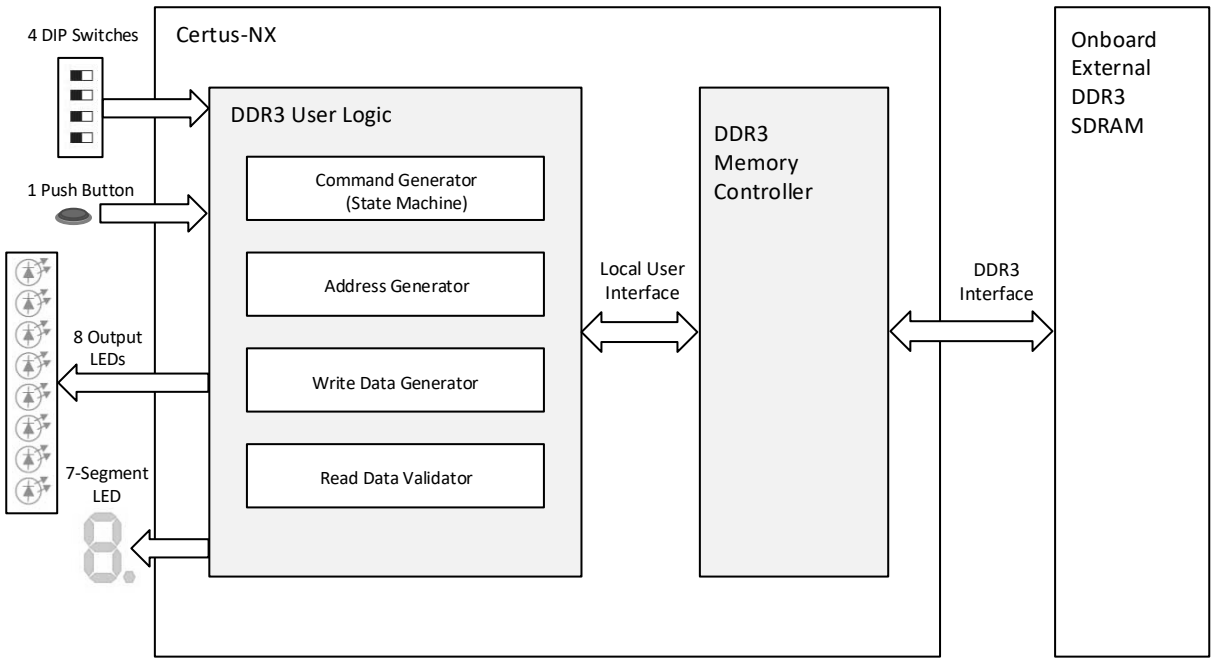

Figure 3.1. DDR3 Demo Design Block Diagram

3.1. DDR3 SDRAM Controller Core

The IP core used to generate the DDR3 Memory Controller is the DDR3 SDRAM Controller IP core, version 1.4.2. The core has been configured to a frequency of 400MHz, since Certus-NX supports the DDR3 burst chop feature for 4:1 gearing only, which translates to a maximum frequency of 400MHz. The core is also configured to a data width of 16 bits because the DDR3 memory module installed on the Certus-NX Versa Evaluation Board is 16 bits wide.

3.2. DDR3 User Logic

The user logic implemented in the DDR3 Demo Design provides the following functions:

- Command Generation State Machine
- Programs mode registers
- Controls DDR3 write and read operations
- Address Generation
- Write Data Generation
- Read Data Validation
- Control and Observation

3.2.1. Command Generation State Machine

The state machine controls the demo using the control input that you enter through the four DIP switch inputs. Once the device is programmed or a reset signal is applied to the user logic by pressing SW3, the state machine programs all DDR3 mode registers (MR0 – MR3) based on the user test configuration (DIP switch setting) – refer to Table 3.3 for details on the configuration settings. The state machine then generates a write command sequence which may be repeated up to 32 times using either the command burst feature or multiple single write commands. After the write command sequence, the read command sequence is initiated and can be repeated up to 32 times similar to the write command sequence. The state machine ensures that both the write and read command sequences are always the same even when the user test configuration is changed at any time during the command sequence. This allows the DDR3 demo to be dynamically reconfigurable.

3.2.2. Address Generation

The address generation block provides the start address for the current write/read command generated by the state machine. When burst command mode is enabled the address generation block automatically calculates the next address according to the demo control input.

3.2.3. Write Data Generation

The demo uses either PRBS or sequential data patterns. When PRBS is selected, a 128-bit PRBS pattern generator is connected to the local write data bus to generate a 16-bit DDR3 data pattern. For 16-bit DDR3 data, the lower 64 bits of the 128-bit PRBS are allocated to the local data bus. For the sequential data pattern, the demo design uses only a 32-bit sequential data pattern generator to provide 16-bit DDR3 data. This 32-bit data pattern is allocated to each 32-bit wide local data bus slot. For example, a 16-bit DDR3 bus requires a 64-bit local data bus which has two identically sequenced 32-bit patterns allocated on two 32-bit slots. The write data generation is enabled and driven by the *datain_rdy* signal assertions.

3.2.4. Read Data Validation

The read data validator checks the read data from the DDR3 memory module to determine if a mismatch has occurred. This is done by comparing the read data to the expected data. The expected data pattern is generated exactly the same as the data sequences from the Write Data Generation block. The expected data generation is enabled and driven by the *read_data_valid* signal assertions. The read data captured by *read_data_valid* is then compared with the expected data generated by the Read Data Validation block. If a mismatch as occurred, the demo design with assert the error detection signal, *err_det*.

3.2.5. Control and Observation

The control and observation block includes the demo control input and result display functions. The demo control input uses four DIP switches and one out of the five available push buttons on the Certus-NX Versa Evaluation Board. The demo result is displayed through eight LEDs on the board. A 7-segment LED display is also provided for a quick assessment of the demo's operation. When the write and read operation is running and there is no data mismatch, the segments of the display blink in a clockwise pattern. If an error is encountered, all 7 segments blink simultaneously.

3.3. Port Assignments and Descriptions

Table 3.1 lists all the signals used by the DDR3 SDRAM Controller IP core in the demo design to control and interface with the onboard DDR3 SDRAM.

Table 3.1. DDR3 Interface

Port Name	Active	Direction	Description
em_ddr_data [DATA_WIDTH – 1 : 0]	N/A	In/Out	Memory bi-directional data bus
em_ddr_reset_n	Low	Output	Asynchronous reset signal from the controller to the memory. Asserted by the controller for the duration of power on reset or SW3
em_ddr_dqs [DQS_WIDTH – 1 : 0]	N/A	In/Out	Memory bi-directional data strobe
em_ddr_dm [DATA_WIDTH / 8 – 1 : 0]	High	Output	Memory write data mask
em_ddr_clk [CLKO_WIDTH – 1 : 0]	N/A	Output	400 MHz memory clock generated by the controller
em_ddr_cke [CKE_WIDTH – 1 : 0]	High	Output	Memory clock enable generated by the controller
em_ddr_ras_n	Low	Output	Memory row address strobe
em_ddr_cas_n	Low	Output	Memory column address strobe
em_ddr_we_n	Low	Output	Memory write enable
em_ddr_cs_n	Low	Output	Memory chip select
em_ddr_odt	High	Output	Memory on-die termination
em_ddr_addr	N/A	Output	Memory address bus - multiplexed row and column address for the memory
em_ddr_ba	N/A	Output	Memory bank address

Table 3.2 lists all the interfaces which are available to you to either dynamically configure the parameters of the design or observe the running status of the demo.

Table 3.2. DDR3 Demo User Interface

Port Name	Active	Direction	Description
clk_in	N/A	Input	Reference clock connected to a dedicated PLL clock input of the Certus-NX FPGA
reset_n	Low	Input	Asynchronous reset connected to the SW3 button. This resets the entire demo system including the IP core and DDR3 memory.
rvl_clk	N/A	Input	Clock used to capture data utilizing Reveal Analyzer. Clock is connected to a dedicated PLL clock input of the Certus-NX FPGA
dip_sw [3 : 0]	N/A	Input	User test configuration input. See the Control and Observation Port Description section of this document for further information
oled [7 : 0]	N/A	Output	Demo result LED indicator output. See the Control and Observation Port Description section of this document for further information
seg [7 : 0]	N/A	Output	7-Segment LED display. The segments of the display (D36) blink in a clockwise pattern as long as no data mismatch has occurred. Once a data mismatch occurs, all the LED segments blink together. To restart transactions, the *reset_n* signal must be toggled

3.3.1. Control and Observation Port Descriptions

The Control and Observation Ports include the user interface ports as described in Table 3.2, which lists all the interfaces which are available to you to either dynamically configure the parameters of the design or observe the running status of the demo.

This section describes in detail the two main control ports: DIP switch and LED. Table 3.3 covers the functionality of each DIP switch on SW10 and how design parameters can be modified by changing the position of the switches. The recommended default setting for the DIP switch is for all switches to be in the OFF position.

Seven of the eight available LEDs are used to indicate the demo progress and results. The reference designator column corresponds to the diode label printed on the Certus-NX Versa Evaluation Board. Each LED indicates a particular status or condition of the DDR3 demo design.

Table 3.3. DIP Switch Definitions

Port Name	DIP Switch Reference #	Function	DIP Switch Setting	Description
dip_sw[3]	4	Data Mode	OFF	The test data consists of 128-bit pseudo random patterns
			ON	The test data consists of 32-bit sequential patterns
dip_sw[2]	3	Maximum Command Size	OFF	Use the maximum command burst size. The DDR3 core performs a 32 command burst when command burst is enabled and generates 32 consecutive single commands when command burst is disabled
			ON	Use the user-specified command burst size. Both the command burst and single command repetition modes use the burst size value (UsrCmdBrstCnt) defined in the ddr3_params.v file. The allowed values are 2, 4, 8, 16, or 32 with the default value set to 2
dip_sw[1]	2	Command Burst Mode	OFF	Enable command burst mode
			ON	Disable command burst mode. Demo works in single command mode where manual single command repetitions are performed instead of using command burst mode
dip_sw[0]	1	Burst Length (On The Fly)	OFF	Set burst length to BL8
			ON	Set burst length to BC4

Table 3.4. LED Definitions

Port Name	Reference Designator	Function	Status	Description
oled[0]	D18	Heartbeat Indicator	Blink	Board is alive and core is receiving the clock input
			OFF	Unstable clock condition where core is unable to receive the clock signal
oled[1]	D19	INIT done Indicator	ON	The core and memory initialization have completed
			OFF	Initialization hasn't occurred/completed
oled[2]	D20	Write Leveling Indicator	ON	Write leveling has failed during initialization sequence
			OFF	Write leveling sequence was successful
oled[3]	D21	Read Training Indicator	ON	Read training has failed during initialization sequence
			OFF	Read training sequence was successful
oled[4]	D22	Not used	OFF	N/A
oled[5]	D23	Write Indicator	ON	Core's write operation is properly working by detecting the *datain_rdy* signal assertions
			OFF	Core is not ready to receive write data from the user
oled[6]	D24	Read Indicator	ON	Core's read operation is properly working by detecting the *read_data_valid* signal assertions
			OFF	Invalid data on the read data bus
oled[7]	D25	Error Indicator	Blink	A data mismatch has occurred. The *reset_n* signal must be toggled to clear this indicator
			OFF	No error detected

3.4. Demo Package Directory Structure

Within the certus_nx_versa_ddr3_demo folder, there are several subfolders. The bitstream folder contains the demo bitstream for the Certus-NX Versa Evaluation Board. The ddr3_core subfolder contains the generated DDR3 SDRAM Controller IP. The ddr3_impl subfolder is the implementation folder for the Certus-NX Versa Evaluation Board, and the source folder contains all the source files other than the IP core.

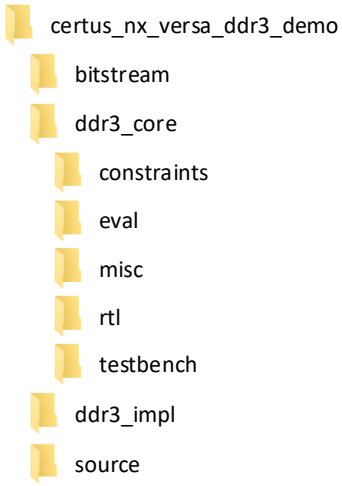

Figure 3.2. DDR3 Demo Package Directory Structure

4. Running the DDR3 Demo

4.1. Hardware Setup

This section covers the steps in programming the demo onto the Certus-NX Versa Evaluation Board.

To program the demo:

1. Connect the 12 V power adapter to J35. The power LEDs D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, D16, and D17 should glow. These LEDs are located in the lower right corner of the board near the power adapter.
2. Connect the USB cable to the computer and to J2. The LED D26, located near the USB-B Mini slot on the board, should glow.
3. At this point, the board is prepared to receive a bit stream from the Lattice Radiant Programmer.

4.2. Programming the Demo .bit File to the Certus-NX Versa Evaluation Board

To program the demo .bit file to the board:

1. Start the Lattice Radiant Programmer 3.1 software.
2. In the **Getting Started** dialog box, select **Open an existing programmer project** and navigate to the extracted demo .zip project location *certus_nx_versa_ddr3_demo/certus_nx_versa_ddr3_demo.xcf*. Click **OK**.

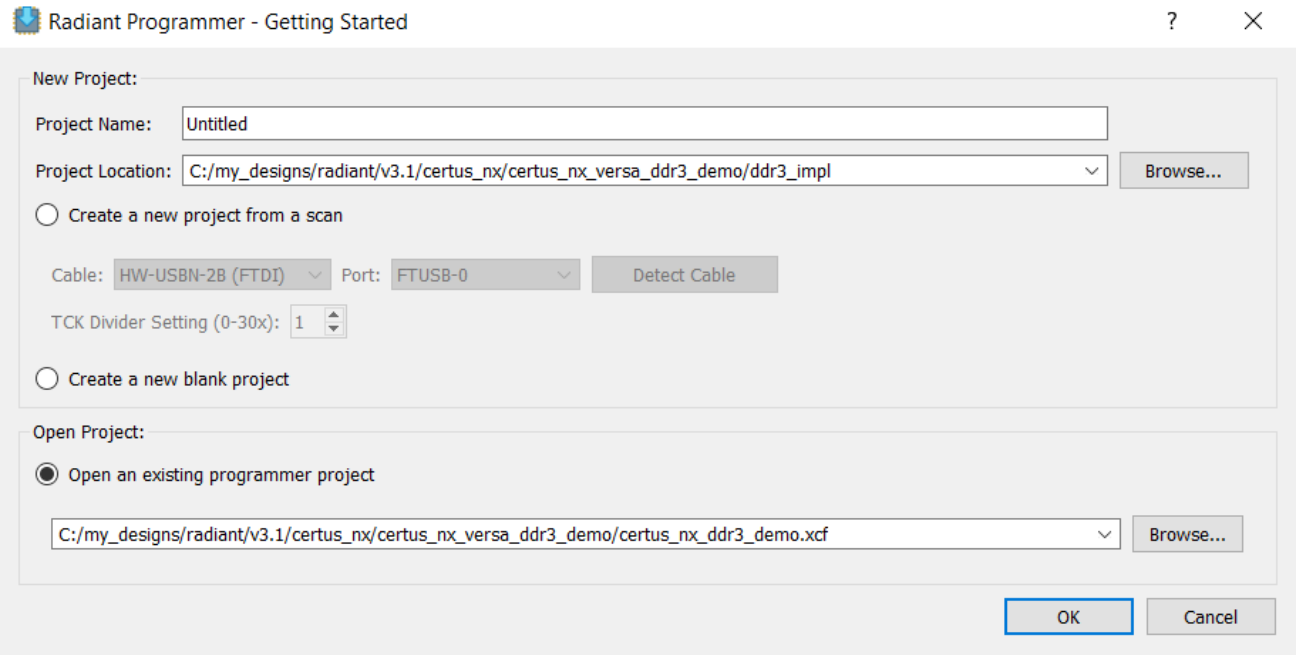

Figure 4.1. Lattice Radiant Programmer Project

3. The Lattice Radiant Programmer main interface opens.

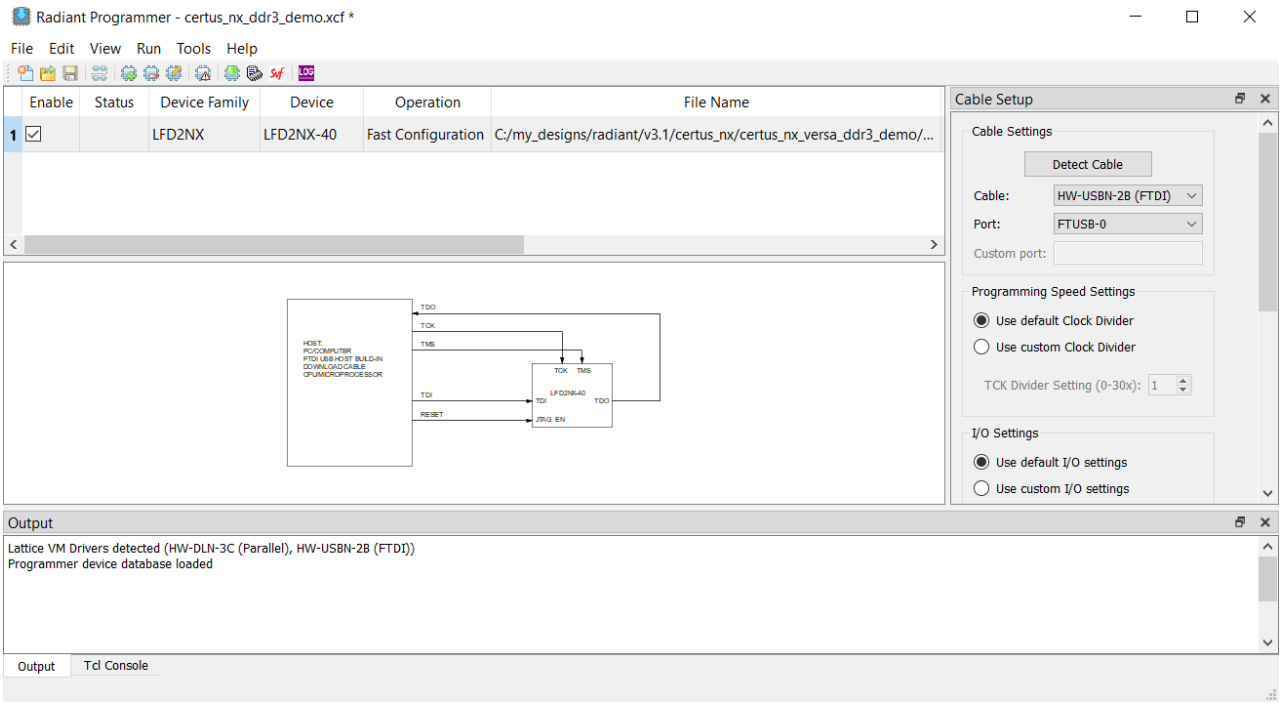

Figure 4.2. Lattice Radiant Main Interface

4. Click the **Detect Cable** button. Click **OK**.
5. Select **Run > Scan Device** from the toolbar. Click **No**.
6. Under **File Name** select the **Browse** button and navigate to the provided bitstream *certus_nx_versa_ddr3_demo/bitstream/certus_nx_versa_ddr3_demo.bit*. Click **Open**.
7. Click the **Programming** button highlighted in Figure 4.3 to start programming.

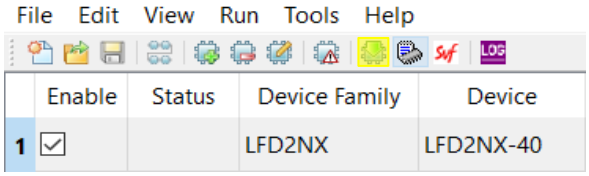

Figure 4.3. Programming Button

8. When programming is successfully completed, the output console shows the status as **Operation Successful**.
9. Refer to Table 4.1 to verify whether the LEDs are blinking as expected. If the LED D25 blinks and all segments of the 7-segment display blink together, press the *reset_n* (SW3) button to clear the error counter and reset the design.

Table 4.1. Expected LED Status from Successful Demo

Name	Expected Status
D36 (7-Segment Display)	Rotating clockwise
D25	OFF
D24	ON
D23	ON
D22	OFF
D20	OFF
D21	OFF
D19	ON
D18	Blinking

4.3. Running Reveal Analyzer

This document assumes that you already have an understanding of Reveal Tools. If you would like to learn more about Reveal for Lattice Radiant software, refer to the Reveal User Guide.

The provided Reveal Inserter instance allows you to observe the status of the DDR3 initialization sequence.

To run reveal analyzer, the steps listed in the Programming the Demo .bit File to the Certus-NX Versa Evaluation Board section must be completed before performing the following:

1. Start the Lattice Radiant 3.1 software.
2. Select **Tools > Reveal Analyzer/Controller** from the toolbar.
3. In the **Reveal Analyzer Startup Wizard** dialog box, select **Create a new file** and change the name from 'untitled' to 'ddr3_rvl.' Click the **Detect** and **Scan** buttons. Click **OK**.

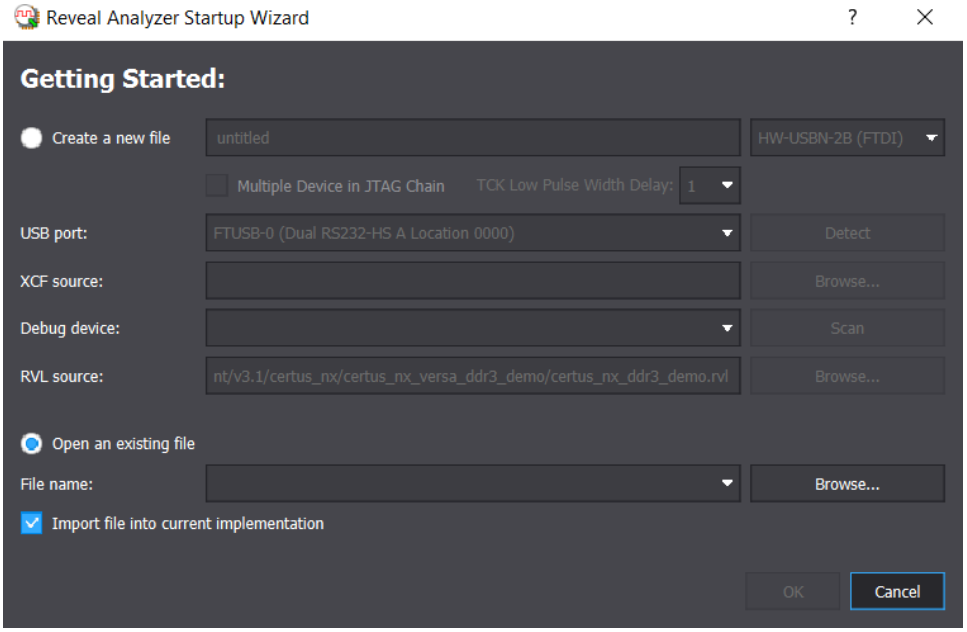

Figure 4.4. Reveal Analyzer Project

4. In the **Reveal Analyzer/Controller** dialog box, uncheck the expressions under **Trigger Expressions** that you do not wish to trigger on. Refer to Table 4.2. for descriptions on each of the triggers and suggested use.

Table 4.2. Reveal Analyzer Trigger Definitions

Name	Description
reset_n THEN init_start	Captures the start of the initialization sequence after reset is applied to the user logic (which is responsible for initiating the initialization sequence) Useful in ensuring the initialization sequence is starting
init_done	Captures the end of the initialization sequence Useful in capturing/reading the wl_err and rt_err signals which would indicate a failure during the initialization sequence
reset_n THEN err_det	Captures the assertion of the err_det signal after reset is applied to the DDR3 SDRAM and Controller Useful in verifying that a data mismatch has occurred during the demo
err_det	Captures the assertion of the err_det signal Useful in capturing data mismatch when toggling demo parameters through the DIP switches

5. Click on the Run button highlighted in Figure 4.5 to run the analyzer and assert the reset signal to capture the waveforms.

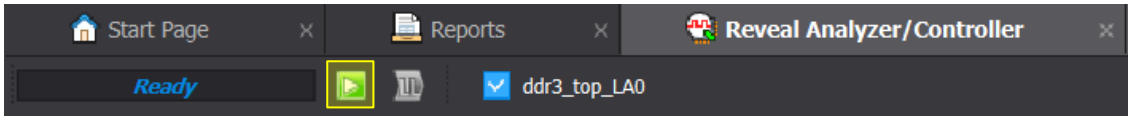

Figure 4.5. Run Button

6. Figure 4.6 shows the expected waveforms upon assertion of *init_done* and refer to Table 4.3 for a brief description of the displayed waveform signals.

Figure 4.6. Expected Waveform from Successful Demo

Table 4.3. Reveal Analyzer Waveform Signal Definitions

Name	Description
reset_n	Active-low reset signal tied to SW3
init_start	Initialization start request Asserted after power-on reset or before sending the first user command to the memory controller. Deasserts when *init_done* pulse occurs
init_done	Initialization done output Asserted for one clock period
wl_err	Write leveling error
rt_err	Read training error
u_ddr3_ulogic/err_det	Data mismatch error
u_ddr3_ulogic/U_data_gen_chk/dqs_ok	Data mismatch has occurred in the corresponding dqs group when set low
u_ddr3_ulogic/U_data_gen_chk/byte_ok	Data mismatch has occurred in the corresponding byte of data when set high

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.0, February 2022

Section	Change Summary
All	Initial release.

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